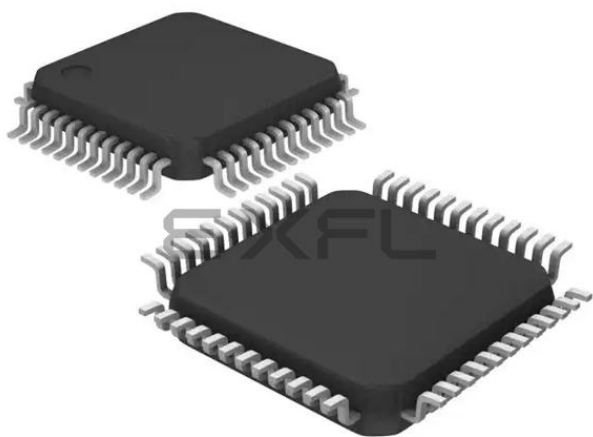




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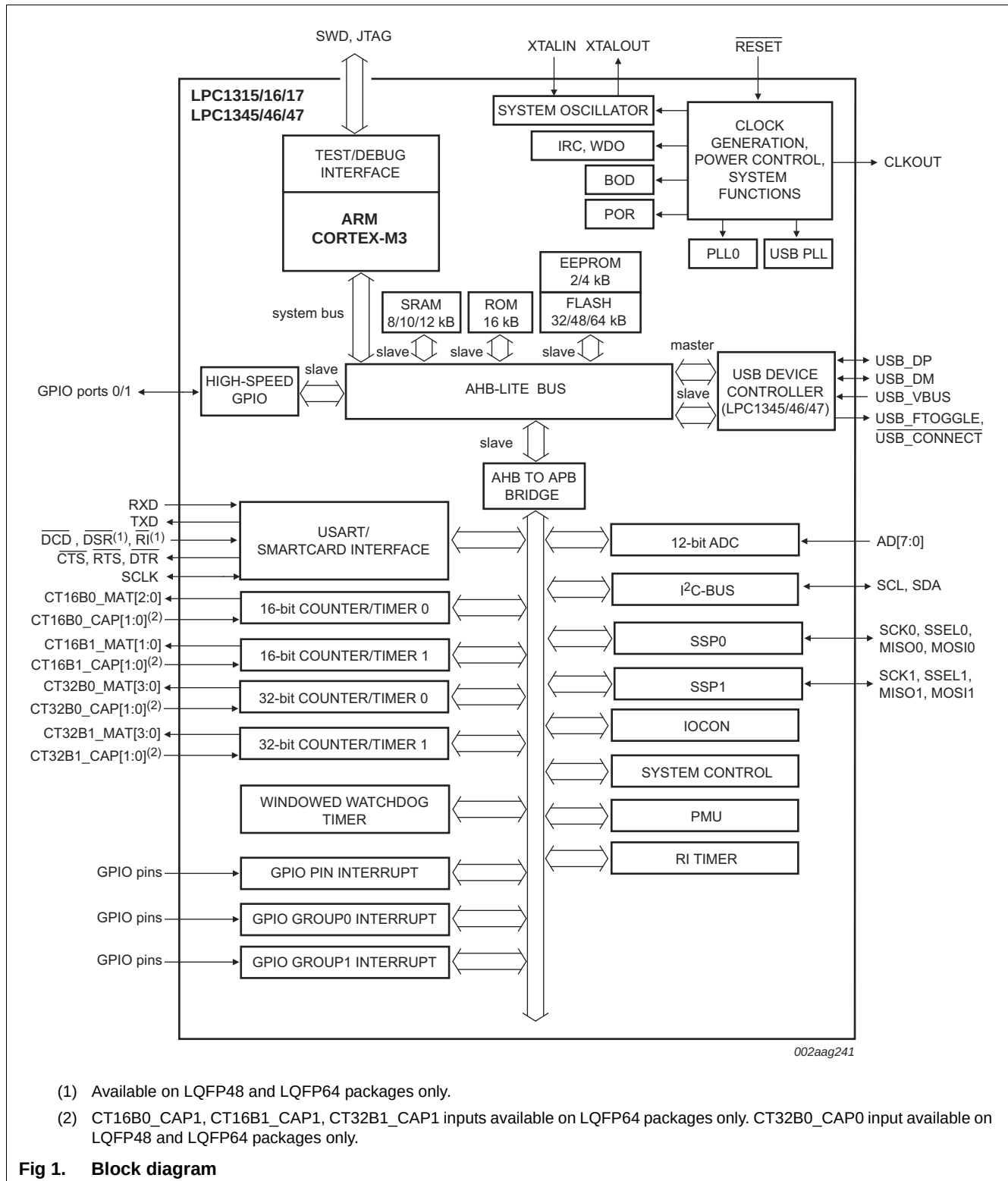
Details

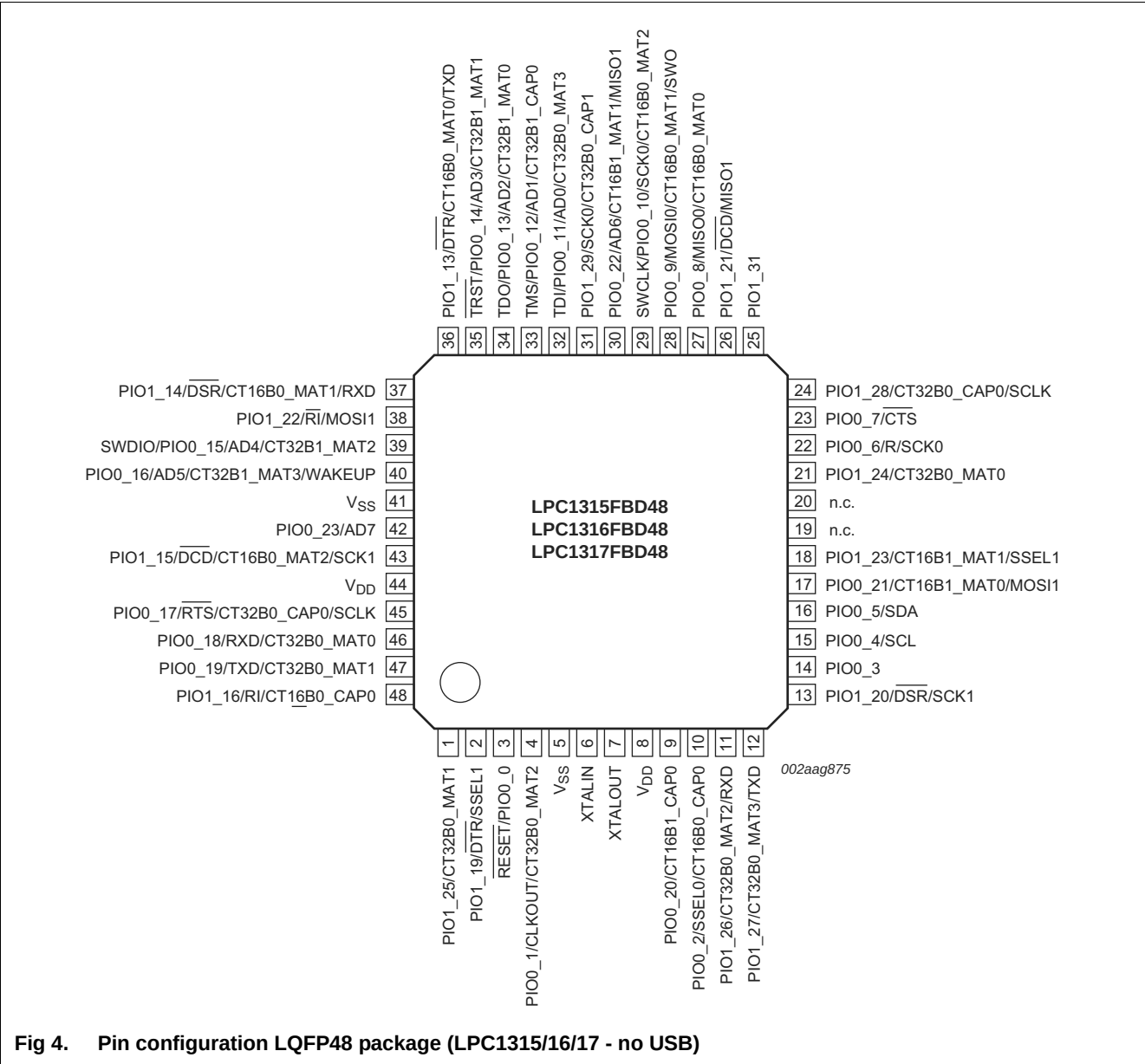
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	I ² C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	40
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1317fbd48-551

4.1 Ordering options**Table 2. Ordering options**

Type number	Flash [kB]	SRAM [kB]			EEPROM [kB]	USB device	SSP	I2C/ FM+	ADC channels	GPIO pins
		SRAM0	USB SRAM	SRAM1						
LPC1345FHN33	32	8	2	-	2	yes	2	1	8	26
LPC1345FBD48	32	8	2	-	2	yes	2	1	8	40
LPC1346FHN33	48	8	2	-	4	yes	2	1	8	26
LPC1346FBD48	48	8	2	-	4	yes	2	1	8	40
LPC1347FHN33	64	8	2	2	4	yes	2	1	8	26
LPC1347FBD48	64	8	2	2	4	yes	2	1	8	40
LPC1347FBD64	64	8	2	2	4	yes	2	1	8	51
LPC1315FHN33	32	8	-	-	2	no	2	1	8	28
LPC1315FBD48	32	8	-	-	2	no	2	1	8	40
LPC1316FHN33	48	8	-	-	4	no	2	1	8	28
LPC1316FBD48	48	8	-	-	4	no	2	1	8	40
LPC1317FHN33	64	8	-	2	4	no	2	1	8	28
LPC1317FBD48	64	8	-	2	4	no	2	1	8	40
LPC1317FBD64	64	8	-	2	4	no	2	1	8	51

5. Block diagram





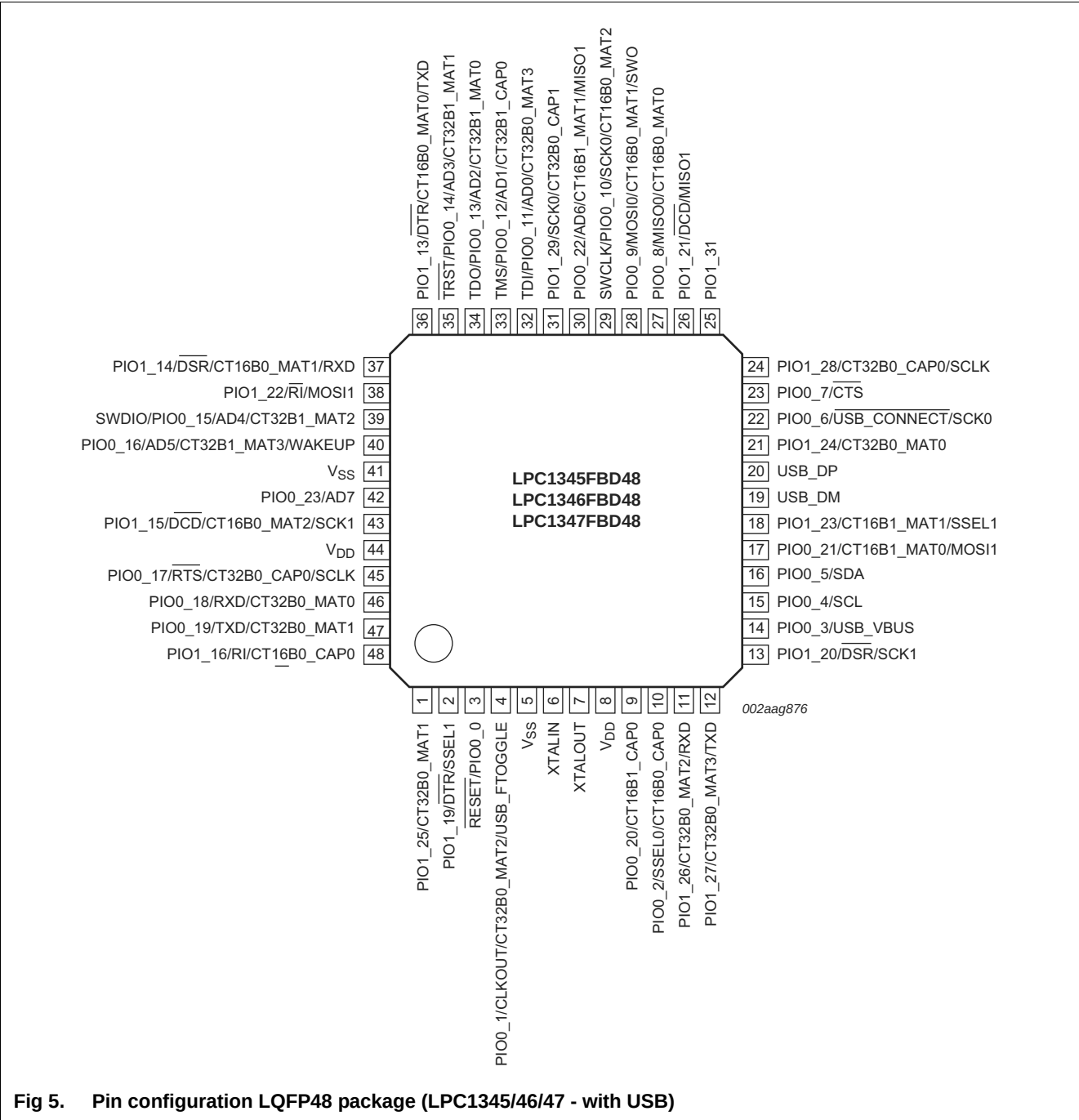


Fig 5. Pin configuration LQFP48 package (LPC1345/46/47 - with USB)

Table 4. Pin description (LPC1345/46/47 - with USB)

Symbol	LQFP64	LQFP48	HVQFN33	Reset state ^[1]	Type	Description
PIO0_9/MOSI0/ CT16B0_MAT1/ SWO	37	28	18	^[3]	I; PU	PIO0_9 — General purpose digital input/output pin.
					I/O	MOSI0 — Master Out Slave In for SSP0.
					O	CT16B0_MAT1 — Match output 1 for 16-bit timer 0.
					O	SWO — Serial wire trace output.
SWCLK/PIO0_10/SCK0/ CT16B0_MAT2	38	29	19	^[3]	I; PU	SWCLK — Serial wire clock and test clock TCK for JTAG interface.
					I/O	PIO0_10 — General purpose digital input/output pin.
					O	SCK0 — Serial clock for SSP0.
					O	CT16B0_MAT2 — Match output 2 for 16-bit timer 0.
TDI/PIO0_11/AD0/ CT32B0_MAT3	42	32	21	^[6]	I; PU	TDI — Test Data In for JTAG interface.
					I/O	PIO0_11 — General purpose digital input/output pin.
					I	AD0 — A/D converter, input 0.
					O	CT32B0_MAT3 — Match output 3 for 32-bit timer 0.
TMS/PIO0_12/AD1/ CT32B1_CAP0	44	33	22	^[6]	I; PU	TMS — Test Mode Select for JTAG interface.
					I/O	PIO_12 — General purpose digital input/output pin.
					I	AD1 — A/D converter, input 1.
					I	CT32B1_CAP0 — Capture input 0 for 32-bit timer 1.
TDO/PIO0_13/AD2/ CT32B1_MAT0	45	34	23	^[6]	I; PU	TDO — Test Data Out for JTAG interface.
					I/O	PIO0_13 — General purpose digital input/output pin.
					I	AD2 — A/D converter, input 2.
					O	CT32B1_MAT0 — Match output 0 for 32-bit timer 1.
TRST/PIO0_14/AD3/ CT32B1_MAT1	46	35	24	^[6]	I; PU	TRST — Test Reset for JTAG interface.
					I/O	PIO0_14 — General purpose digital input/output pin.
					I	AD3 — A/D converter, input 3.
					O	CT32B1_MAT1 — Match output 1 for 32-bit timer 1.
SWDIO/PIO0_15/AD4/ CT32B1_MAT2	52	39	25	^[6]	I; PU	SWDIO — Serial wire debug input/output.
					I/O	PIO0_15 — General purpose digital input/output pin.
					I	AD4 — A/D converter, input 4.
					O	CT32B1_MAT2 — Match output 2 for 32-bit timer 1.
PIO0_16/AD5/ CT32B1_MAT3/WAKEUP	53	40	26	^[7]	I; PU	PIO0_16 — General purpose digital input/output pin.
					I	AD5 — A/D converter, input 5.
					O	CT32B1_MAT3 — Match output 3 for 32-bit timer 1.
					I	WAKEUP — Deep power-down mode wake-up pin with 20 ns glitch filter. This pin must be pulled HIGH externally to enter Deep power-down mode and pulled LOW to exit Deep power-down mode. A LOW-going pulse as short as 50 ns wakes up the part.

Table 4. Pin description (LPC1345/46/47 - with USB)

Symbol	LQFP64	LQFP48	HVQFN33		Reset state ^[1]	Type	Description
PIO0_17/ <u>RTS</u> / CT32B0_CAP0/SCLK	60	45	30	[3]	I; PU	I/O	PIO0_17 — General purpose digital input/output pin.
					-	O	RTS — Request To Send output for USART.
					-	I	CT32B0_CAP0 — Capture input 0 for 32-bit timer 0.
					-	I/O	SCLK — Serial clock input/output for USART in synchronous mode.
PIO0_18/RXD/ CT32B0_MAT0	61	46	31	[3]	I; PU	I/O	PIO0_18 — General purpose digital input/output pin.
					-	I	RXD — Receiver input for USART. Used in UART ISP mode.
					-	O	CT32B0_MAT0 — Match output 0 for 32-bit timer 0.
PIO0_19/TXD/ CT32B0_MAT1	62	47	32	[3]	I; PU	I/O	PIO0_19 — General purpose digital input/output pin.
					-	O	TXD — Transmitter output for USART. Used in UART ISP mode.
					-	O	CT32B0_MAT1 — Match output 1 for 32-bit timer 0.
PIO0_20/CT16B1_CAP0	11	9	7	[3]	I; PU	I/O	PIO0_20 — General purpose digital input/output pin.
					-	I	CT16B1_CAP0 — Capture input 0 for 16-bit timer 1.
PIO0_21/CT16B1_MAT0/ MOSI1	22	17	12	[3]	I; PU	I/O	PIO0_21 — General purpose digital input/output pin.
					-	O	CT16B1_MAT0 — Match output 0 for 16-bit timer 1.
					-	I/O	MOSI1 — Master Out Slave In for SSP1.
PIO0_22/AD6/ CT16B1_MAT1/MISO1	40	30	20	[6]	I; PU	I/O	PIO0_22 — General purpose digital input/output pin.
					-	I	AD6 — A/D converter, input 6.
					-	O	CT16B1_MAT1 — Match output 1 for 16-bit timer 1.
					-	I/O	MISO1 — Master In Slave Out for SSP1.
PIO0_23/AD7	56	42	27	[6]	I; PU	I/O	PIO0_23 — General purpose digital input/output pin.
					-	I	AD7 — A/D converter, input 7.
PIO1_0/CT32B1_MAT0	1	-	-	[3]	I; PU	I/O	PIO1_0 — General purpose digital input/output pin.
					-	O	CT32B1_MAT0 — Match output 0 for 32-bit timer 1.
PIO1_1/CT32B1_MAT1	17	-	-	[3]	I; PU	I/O	PIO1_1 — General purpose digital input/output pin.
					-	O	CT32B1_MAT1 — Match output 1 for 32-bit timer 1.
PIO1_2/CT32B1_MAT2	34	-	-	[3]	I; PU	I/O	PIO1_2 — General purpose digital input/output pin.
					-	O	CT32B1_MAT2 — Match output 2 for 32-bit timer 1.
PIO1_3/CT32B1_MAT3	50	-	-	[3]	I; PU	I/O	PIO1_3 — General purpose digital input/output pin.
					-	O	CT32B1_MAT3 — Match output 3 for 32-bit timer 1.
PIO1_4/CT32B1_CAP0	16	-	-	[3]	I; PU	I/O	PIO1_4 — General purpose digital input/output pin.
					-	I	CT32B1_CAP0 — Capture input 0 for 32-bit timer 1.
PIO1_5/CT32B1_CAP1	32	-	-	[3]	I; PU	I/O	PIO1_5 — General purpose digital input/output pin.
					-	I	CT32B1_CAP1 — Capture input 1 for 32-bit timer 1.
PIO1_7	6	-	-	[3]	I; PU	I/O	PIO1_7 — General purpose digital input/output pin.
PIO1_8	39	-	-	[3]	I; PU	I/O	PIO1_8 — General purpose digital input/output pin.

Table 4. Pin description (LPC1345/46/47 - with USB)

Symbol	LQFP64	LQFP48	HVQFN33	Reset state ^[1]	Type	Description
VREFP	64	-	-	-	-	ADC positive reference voltage: This should be nominally the same voltage as V_{DDA} but should be isolated to minimize noise and error. Level on this pin is used as a reference for ADC. This pin should be tied to 3.3 V if the ADC is not used.
V _{SSA}	55	-	-	-	-	analog ground: 0 V reference. This should nominally be the same voltage as V_{SS} , but should be isolated to minimize noise and error.
V _{DD}	10; 33; 58	8; 44	6; 29	-	-	Supply voltage to the internal regulator and the external rail. On LQFP48 and HVQFN33 packages, this pin is also connected to the 3.3 V ADC supply and reference voltage.
V _{SS}	7; 54	5; 41	33	-	-	Ground.

- [1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled; IA = inactive, no pull-up/down enabled; F = floating; floating pins, if not used, should be tied to ground or power to minimize power consumption.
- [2] See [Figure 33](#) for the reset pad configuration. RESET functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode.
- [3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see [Figure 32](#)).
- [4] I²C-bus pins compliant with the I²C-bus specification for I²C standard mode, I²C Fast-mode, and I²C Fast-mode Plus.
- [5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see [Figure 32](#)); includes high-current output driver.
- [6] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled and the pin is not 5 V tolerant (see [Figure 32](#)); includes programmable digital input glitch filter.
- [7] WAKEUP pin. 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled and the pin is not 5 V tolerant (see [Figure 32](#)); includes digital input glitch filter.
- [8] Pad provides USB functions. It is designed in accordance with the USB specification, revision 2.0 (Full-speed and Low-speed mode only). This pad is not 5 V tolerant.
- [9] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.¹⁵

The USART includes full modem control, support for synchronous mode, and a smart card interface. The RS-485/9-bit mode allows both software address detection and automatic address detection using 9-bit mode.

The USART uses a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

7.10.1 Features

- Maximum USART data bit rate of 3.125 Mbit/s.
- 16-byte receive and transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Fractional divider for baud rate control, auto baud capabilities and FIFO control mechanism that enables software flow control implementation.
- Support for RS-485/9-bit mode.
- Support for modem control.
- Support for synchronous mode.
- Includes smart card interface (ISO 7816-3).

7.11 SSP serial I/O controller

The SSP controllers are capable of operation on a SSP, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full duplex transfers, with frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

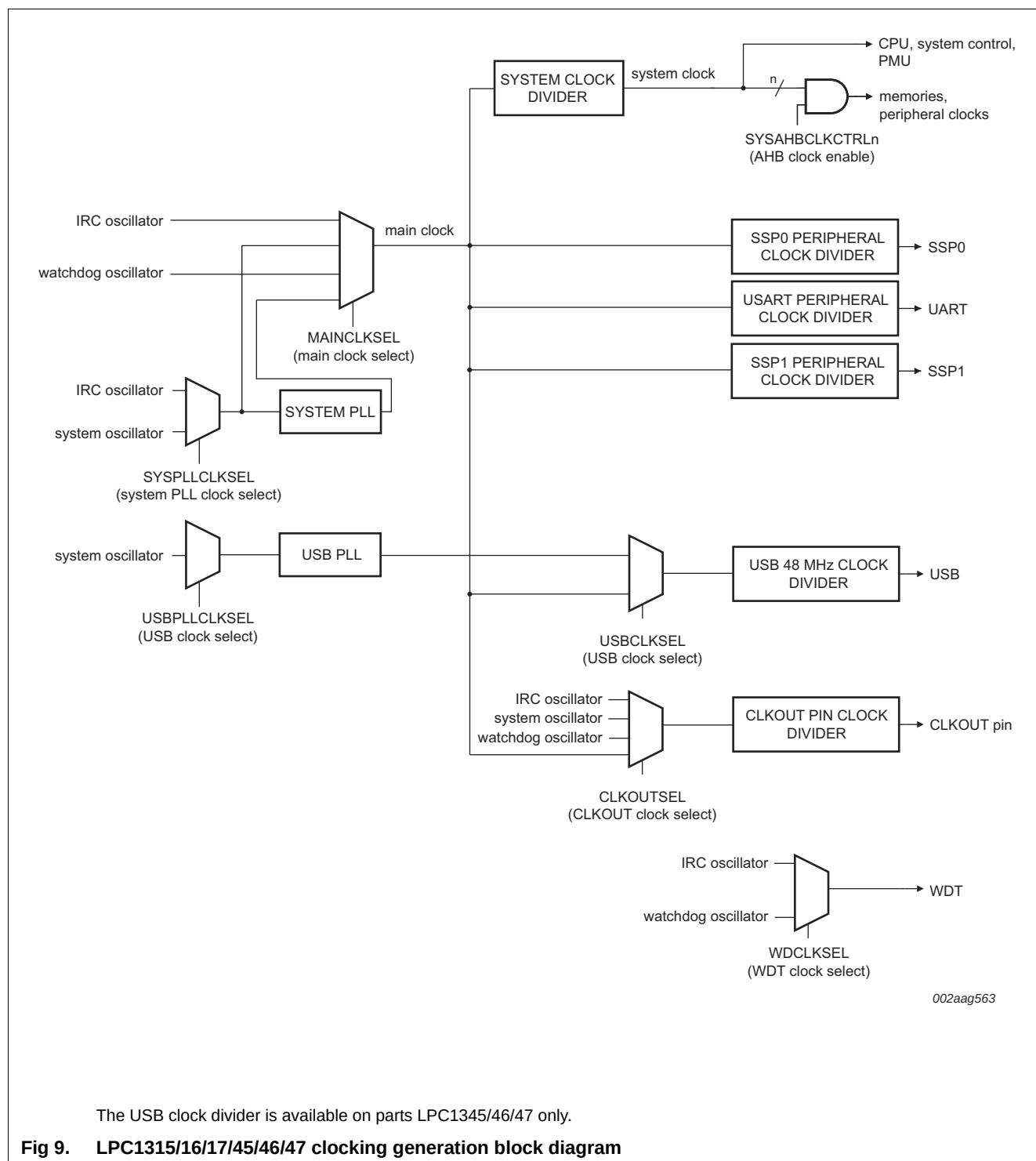
7.11.1 Features

- Maximum SSP speed of 25 Mbit/s (master) or 4.17 Mbit/s (slave) (in SSP mode)
- Compatible with Motorola SPI, 4-wire Texas Instruments SSI, and National Semiconductor Microwire buses
- Synchronous serial communication
- Master or slave operation
- 8-frame FIFOs for both transmit and receive
- 4-bit to 16-bit frame

7.12 I²C-bus serial I/O controller

The LPC1315/16/17/45/46/47 contain one I²C-bus controller.

The I²C-bus is bidirectional for inter-IC control using only two wires: a Serial Clock line (SCL) and a Serial Data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or



7.18.1.1 Internal RC oscillator

The IRC may be used as the clock source for the WDT, and/or as the clock that drives the system PLL and subsequently the CPU. The nominal IRC frequency is 12 MHz. The IRC is trimmed to 1 % accuracy over the entire voltage and temperature range.

controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, a register is provided for shutting down the clocks to individual on-chip peripherals, allowing fine tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider which provides even better power control.

7.18.5.1 Power profiles

The power consumption in Active and Sleep modes can be optimized for the application through simple calls to the power profile. The power configuration routine configures the LPC1315/16/17/45/46/47 for one of the following power modes:

- Default mode corresponding to power configuration after reset.
- CPU performance mode corresponding to optimized processing capability.
- Efficiency mode corresponding to optimized balance of current consumption and CPU performance.
- Low-current mode corresponding to lowest power consumption.

In addition, the power profile includes routines to select the optimal PLL settings for a given system clock and PLL input clock.

Remark: When using the USB, configure the LPC1345/46/47 in Default mode.

7.18.5.2 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence but re-enabling the clock to the ARM core.

In Sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

7.18.5.3 Deep-sleep mode

In Deep-sleep mode, the LPC1315/16/17/45/46/47 is in Sleep-mode and all peripheral clocks and all clock sources are off with the exception of the IRC. The IRC output is disabled unless the IRC is selected as input to the watchdog timer. In addition all analog blocks are shut down and the flash is in stand-by mode. In Deep-sleep mode, the user has the option to keep the watchdog oscillator and the BOD circuit running for self-timed wake-up and BOD protection.

The LPC1315/16/17/45/46/47 can wake up from Deep-sleep mode via reset, selected GPIO pins, a watchdog timer interrupt, or an interrupt generating USB port activity.

Deep-sleep mode saves power and allows for short wake-up times.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).^[1]

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DD}	supply voltage (core and external rail)		2.0	3.6	V
V _I	input voltage	5 V tolerant I/O pins; only valid when the V _{DD} supply voltage is present	^[2] -0.5	+5.5	V
I _{DD}	supply current	per supply pin	-	100	mA
I _{SS}	ground current	per ground pin	-	100	mA
I _{latch}	I/O latch-up current	-(0.5V _{DD}) < V _I < (1.5V _{DD}); T _j < 125 °C	-	100	mA
T _{stg}	storage temperature	non-operating	^[3] -65	+150	°C
T _{j(max)}	maximum junction temperature		-	150	°C
P _{tot(pack)}	total power dissipation (per package)	based on package heat transfer, not device power consumption	-	1.5	W
V _{ESD}	electrostatic discharge voltage	human body model; all pins	^[4] -5000	+5000	V

[1] The following applies to the limiting values:

- a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.
- b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Including voltage on outputs in 3-state mode.

[3] The maximum non-operating storage temperature is different than the temperature for required shelf life which should be determined based on required shelf lifetime. Please refer to the JEDEC spec (J-STD-033B.1) for further details.

[4] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

Table 6. Static characteristics ...continued
 $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
I _{OH}	HIGH-level output current	2.5 V ≤ V _{DD} ≤ 3.6 V; V _{OH} = V _{DD} − 0.4 V	−4	-	-	mA
		2.0 V ≤ V _{DD} < 2.5 V; V _{OH} = V _{DD} − 0.4 V	−3	-	-	mA
I _{OL}	LOW-level output current	2.5 V ≤ V _{DD} ≤ 3.6 V; V _{OL} = 0.4 V	4	-	-	mA
		2.0 V ≤ V _{DD} < 2.5 V; V _{OL} = 0.4 V	3	-	-	mA
I _{OHS}	HIGH-level short-circuit output current	V _{OH} = 0 V	^[15] -	-	−45	mA
I _{OLS}	LOW-level short-circuit output current	V _{OL} = V _{DD}	^[15] -	-	50	mA
I _{pd}	pull-down current	V _I = 5 V	10	50	150	μA
I _{pu}	pull-up current	V _I = 0 V; 2.0 V < V _{DD} ≤ 3.6 V	−15	−50	−85	μA
		V _{DD} = 2.0 V	−10	−50	−85	μA
		V _{DD} < V _I < 5 V	0	0	0	μA
High-drive output pin (PIO0_7)						
I _{IL}	LOW-level input current	V _I = 0 V; on-chip pull-up resistor disabled	-	0.5	10	nA
I _{IH}	HIGH-level input current	V _I = V _{DD} ; on-chip pull-down resistor disabled	-	0.5	10	nA
I _{OZ}	OFF-state output current	V _O = 0 V; V _O = V _{DD} ; on-chip pull-up/down resistors disabled	-	0.5	10	nA
V _I	input voltage	pin configured to provide a digital function	^{[12][13][14]} 0	-	5.0	V
V _O	output voltage	output active	0	-	V _{DD}	V
V _{IH}	HIGH-level input voltage		0.7V _{DD}	-	-	V
V _{IL}	LOW-level input voltage		-	-	0.3V _{DD}	V
V _{hys}	hysteresis voltage		0.4	-	-	V
V _{OH}	HIGH-level output voltage	2.5 V ≤ V _{DD} ≤ 3.6 V; I _{OH} = −20 mA	V _{DD} − 0.4	-	-	V
		2.0 V ≤ V _{DD} < 2.5 V; I _{OH} = −12 mA	V _{DD} − 0.4	-	-	V
V _{OL}	LOW-level output voltage	2.5 V ≤ V _{DD} ≤ 3.6 V; I _{OL} = 4 mA	-	-	0.4	V
		2.0 V ≤ V _{DD} < 2.5 V; I _{OL} = 3 mA	-	-	0.4	V
I _{OH}	HIGH-level output current	2.5 V ≤ V _{DD} ≤ 3.6 V; V _{OH} = V _{DD} − 0.4 V	20	-	-	mA
		2.0 V ≤ V _{DD} < 2.5 V; V _{OH} = V _{DD} − 0.4 V;	12	-	-	mA
I _{OL}	LOW-level output current	2.5 V ≤ V _{DD} ≤ 3.6 V; V _{OL} = 0.4 V	4	-	-	mA
		2.0 V ≤ V _{DD} < 2.5 V; V _{OL} = 0.4 V	3	-	-	mA
I _{OLS}	LOW-level short-circuit output current	V _{OL} = V _{DD}	^[15] -	-	50	mA
I _{pd}	pull-down current	V _I = 5 V	10	50	150	μA

10.6 SSP interface

Table 16. Dynamic characteristics: SSP pins in SPI mode

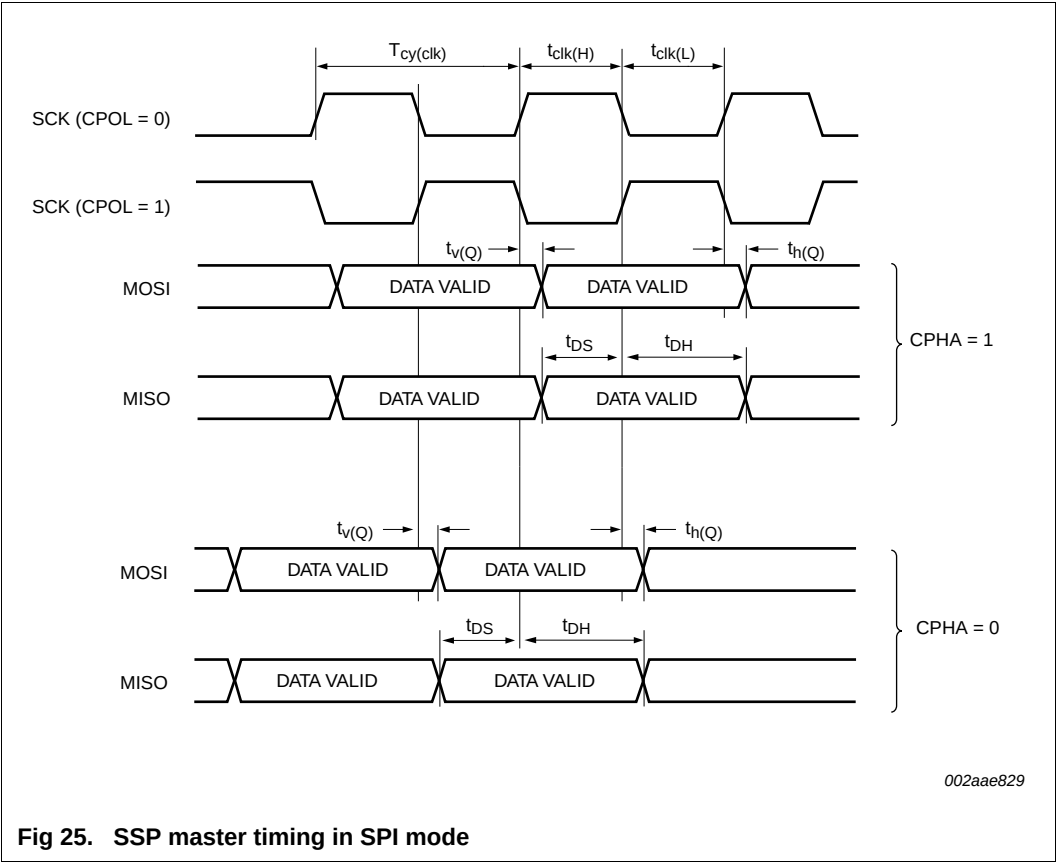
Symbol	Parameter	Conditions	Min	Max	Unit
SSP master					
$T_{cy(clk)}$	clock cycle time	full-duplex mode ^[1]	40	-	ns
		when only transmitting ^[1]	27.8	-	ns
t_{DS}	data set-up time	in SPI mode; $2.4\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ ^[2]	15	-	ns
		$2.0\text{ V} \leq V_{DD} < 2.4\text{ V}$ ^[2]	20	-	ns
t_{DH}	data hold time	in SPI mode ^[2]	0	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode ^[2]	-	10	ns
$t_{h(Q)}$	data output hold time	in SPI mode ^[2]	0	-	ns
SSP slave					
$T_{cy(PCLK)}$	PCLK cycle time		13.9	-	ns
t_{DS}	data set-up time	in SPI mode ^{[3][4]}	0	-	ns
t_{DH}	data hold time	in SPI mode ^{[3][4]}	$3 \times T_{cy(PCLK)} + 4$	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode ^{[3][4]}	-	$3 \times T_{cy(PCLK)} + 11$	ns
$t_{h(Q)}$	data output hold time	in SPI mode ^{[3][4]}	-	$2 \times T_{cy(PCLK)} + 5$	ns

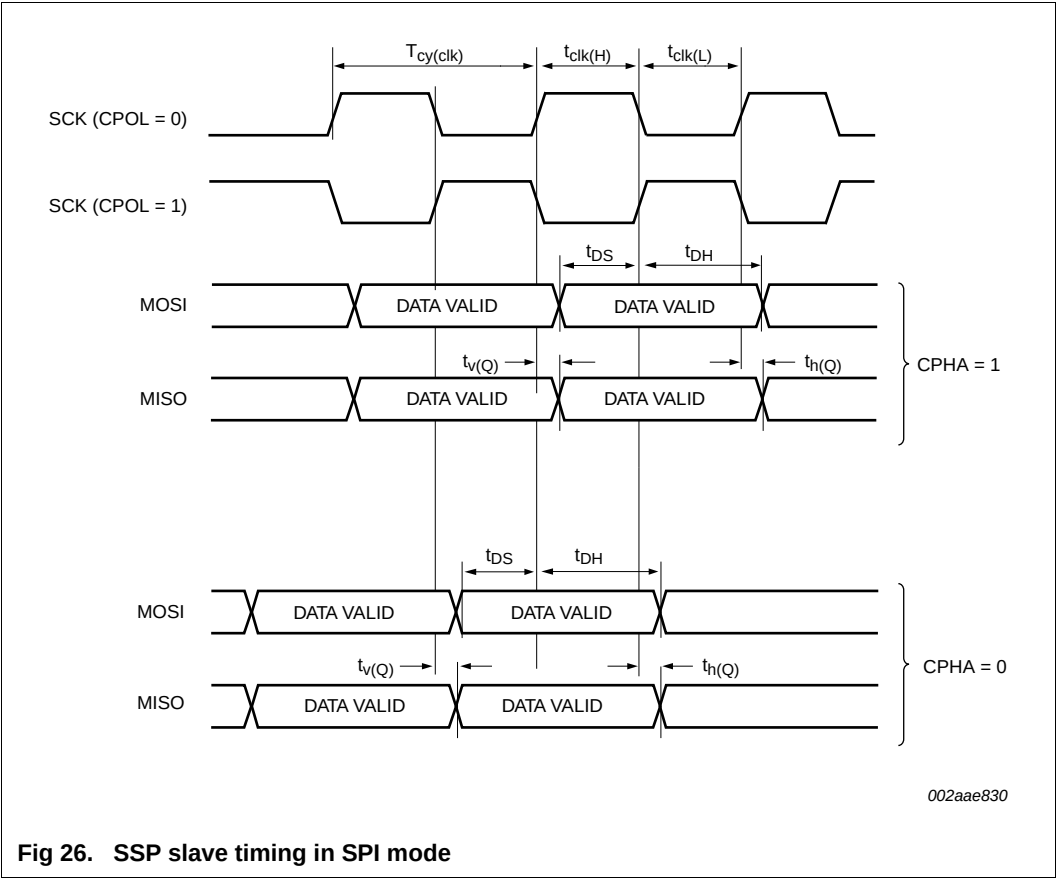
[1] $T_{cy(clk)} = (SSPCLKDIV \times (1 + SCR) \times CPDVSRR) / f_{main}$. The clock cycle time derived from the SPI bit rate $T_{cy(clk)}$ is a function of the main clock frequency f_{main} , the SSP peripheral clock divider (SSPCLKDIV), the SSP SCR parameter (specified in the SSP0CR0 register), and the SSP CPDVSRR parameter (specified in the SSP clock prescale register).

[2] $T_{amb} = -40\text{ °C}$ to 85 °C .

[3] $T_{cy(clk)} = 12 \times T_{cy(PCLK)}$.

[4] $T_{amb} = 25\text{ °C}$; $V_{DD} = 3.3\text{ V}$.





12. Application information

12.1 Suggested USB interface solutions

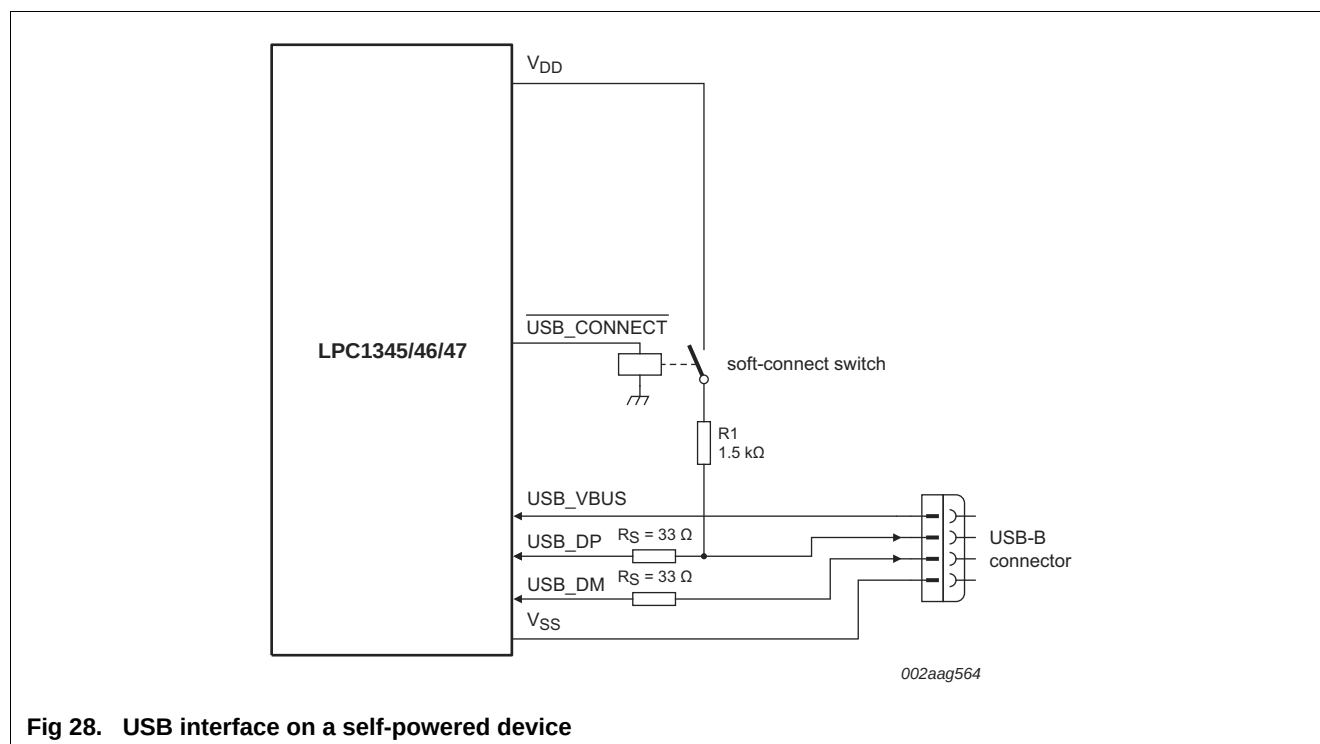


Fig 28. USB interface on a self-powered device

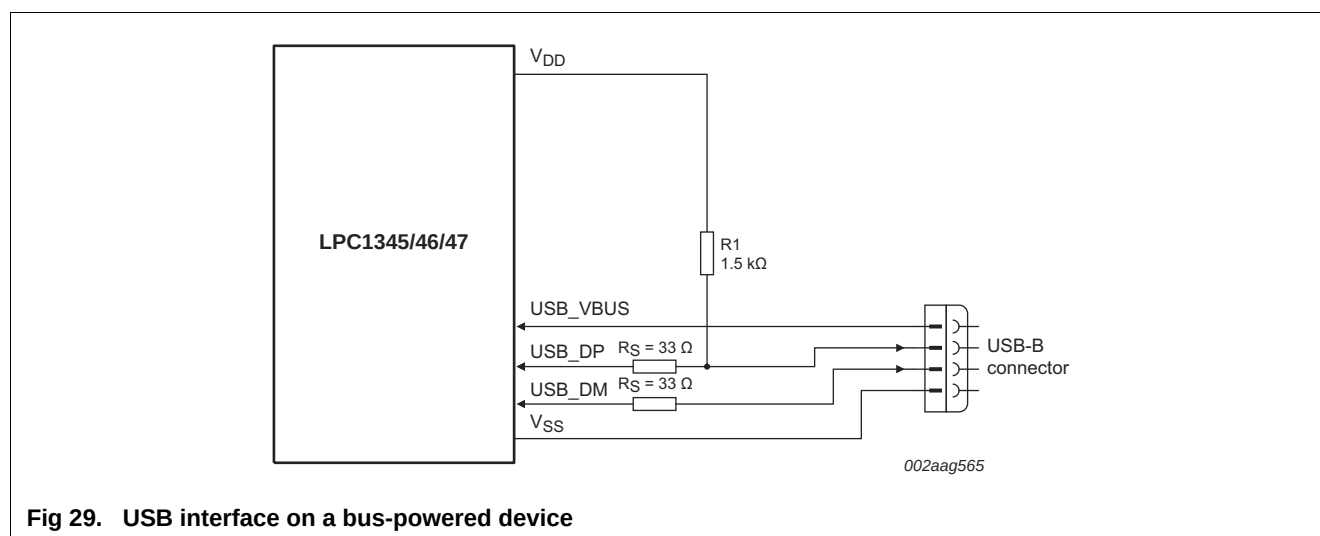
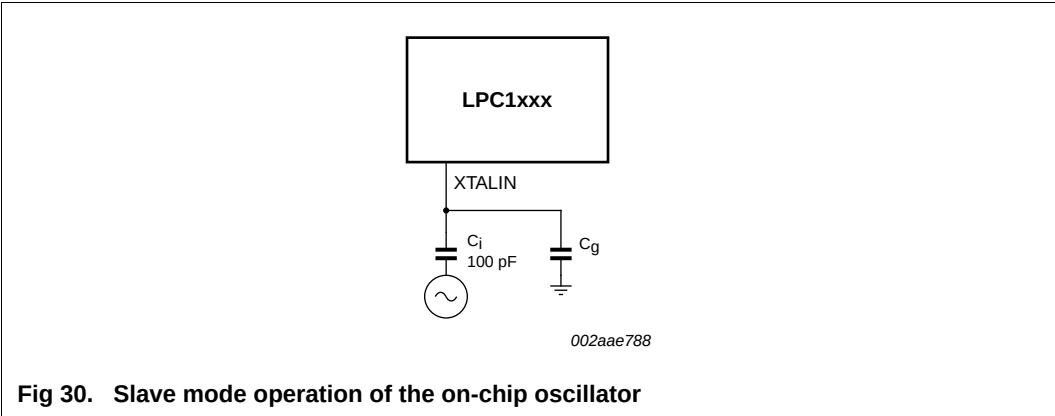


Fig 29. USB interface on a bus-powered device

12.2 XTAL input

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with $C_i = 100$ pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV(RMS) is needed.



In slave mode the input clock signal should be coupled by means of a capacitor of 100 pF (Figure 30), with an amplitude between 200 mV(RMS) and 1000 mV(RMS). This corresponds to a square wave signal with a signal swing of between 280 mV and 1.4 V. The XTALOUT pin in this configuration can be left unconnected.

External components and models used in oscillation mode are shown in Figure 31 and in Table 18 and Table 19. Since the feedback resistance is integrated on chip, only a crystal and the capacitances C_{X1} and C_{X2} need to be connected externally in case of fundamental mode oscillation (the fundamental frequency is represented by L , C_L and R_S). Capacitance C_P in Figure 31 represents the parallel package capacitance and should not be larger than 7 pF. Parameters F_{OSC} , C_L , R_S and C_P are supplied by the crystal manufacturer.

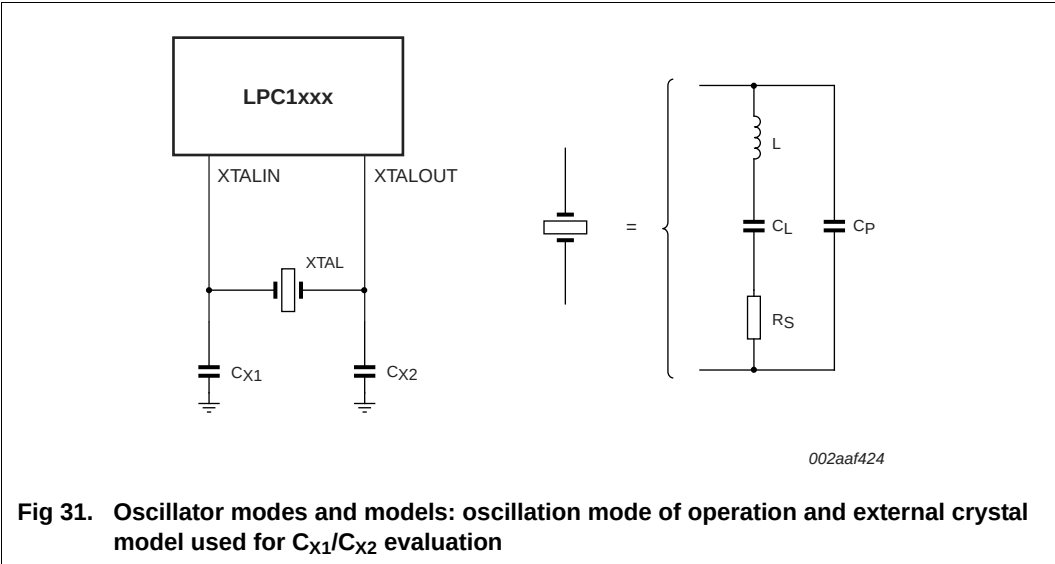


Table 18. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) low frequency mode			
Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1} , C_{X2}
1 MHz - 5 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 300 Ω	39 pF, 39 pF
	30 pF	< 300 Ω	57 pF, 57 pF

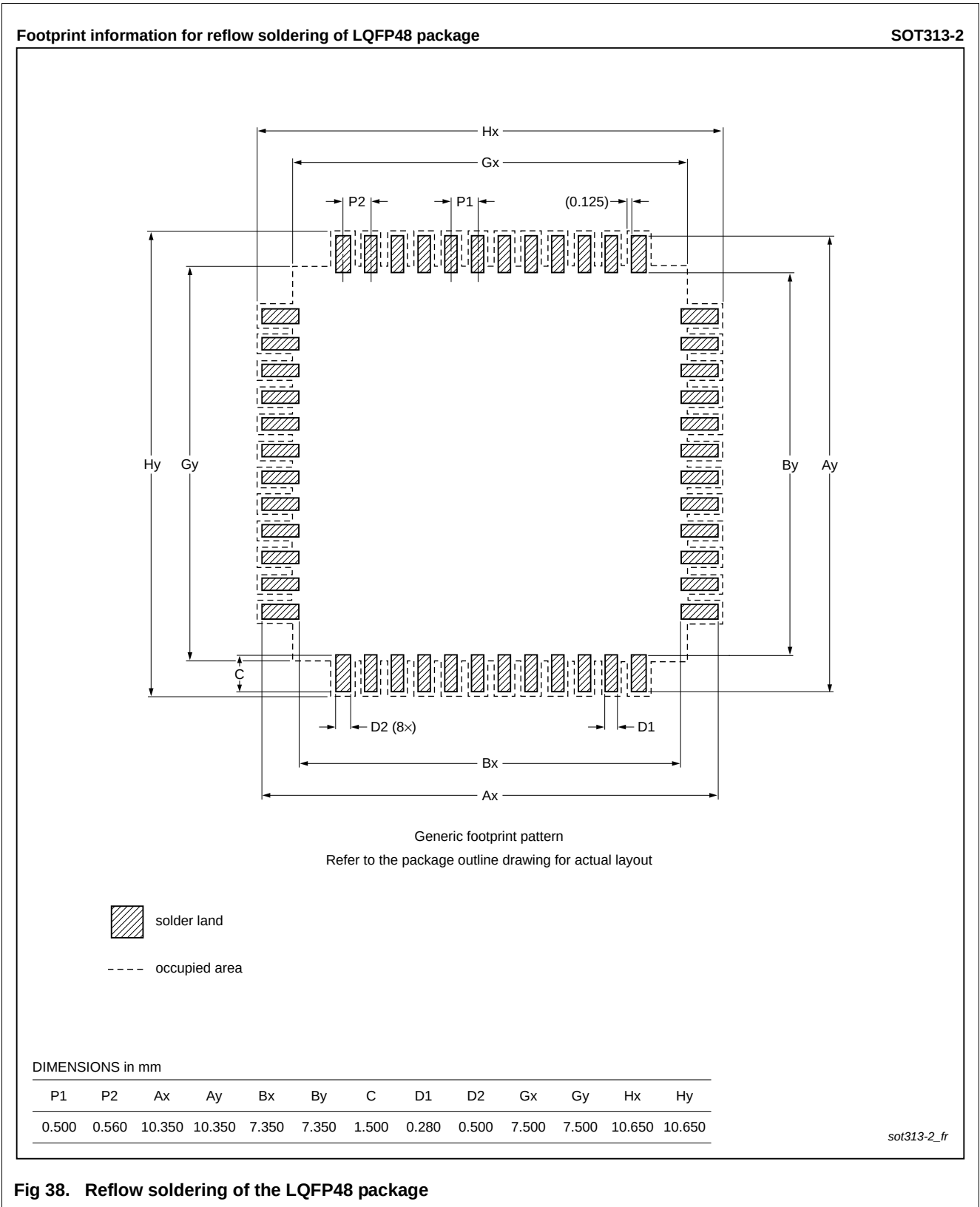
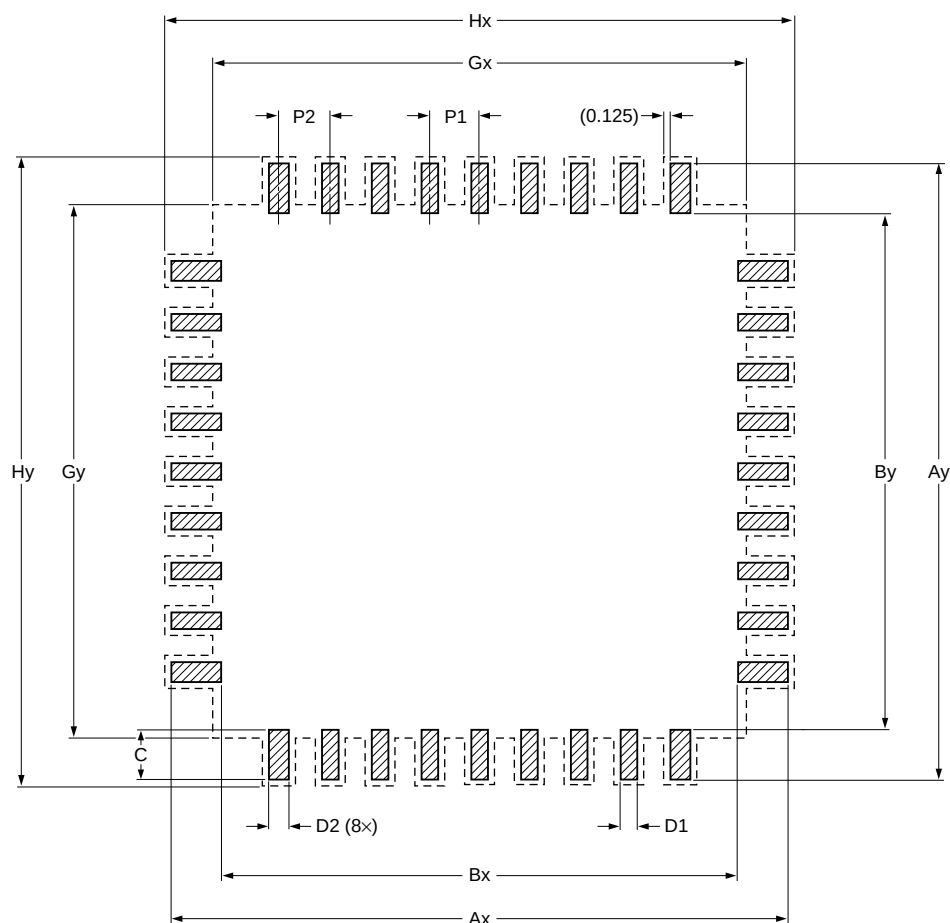


Fig 38. Reflow soldering of the LQFP48 package

Footprint information for reflow soldering of LQFP64 package

SOT314-2



Generic footprint pattern

Refer to the package outline drawing for actual layout



solder land

--- occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	13.300	13.300	10.300	10.300	1.500	0.280	0.400	10.500	10.500	13.550	13.550

sot314-2 fr

Fig 39. Reflow soldering of the LQFP64 package

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