Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

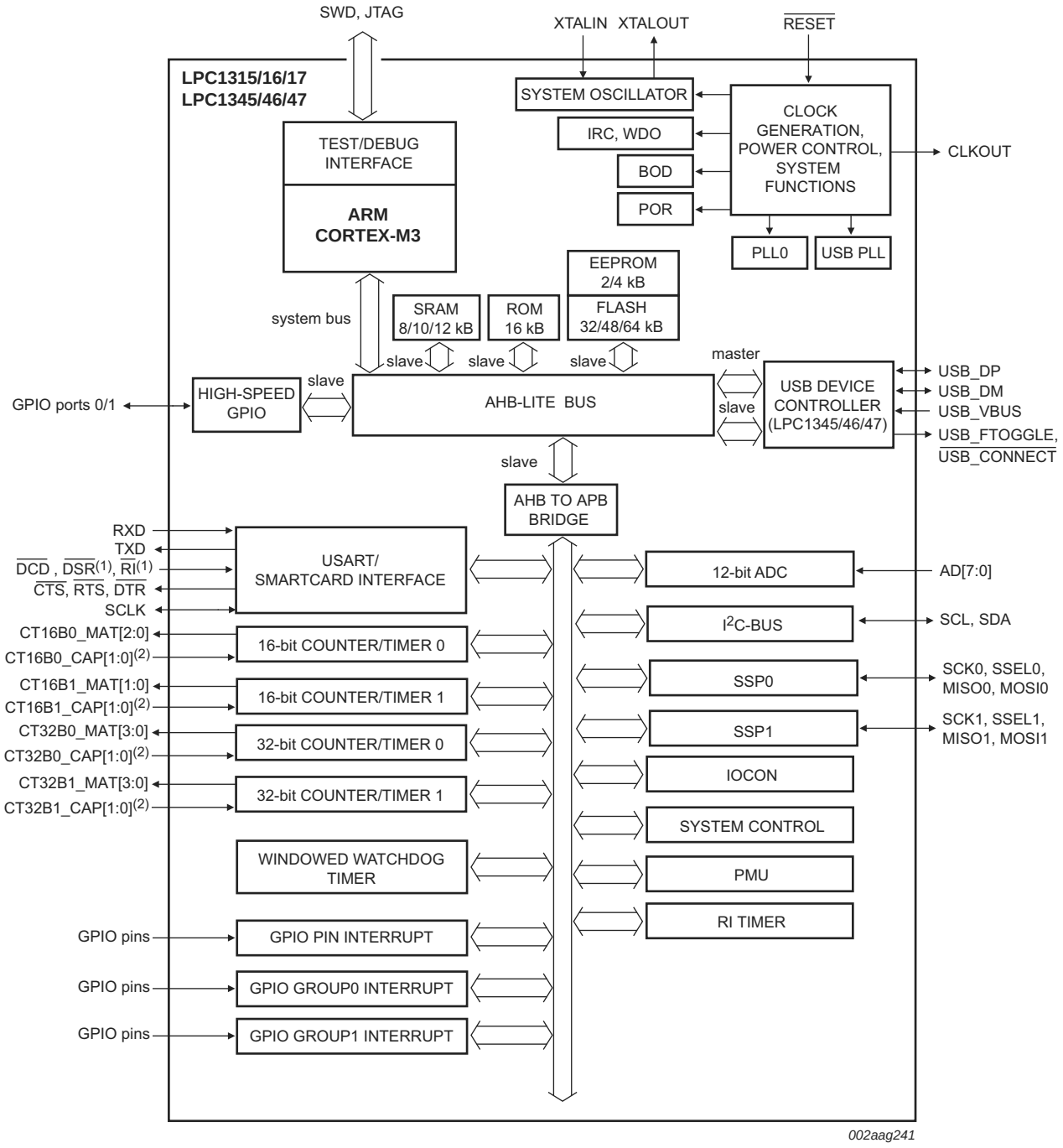
Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	I²C, Microwire, SPI, SSI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	51
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1347fbd64-551

4.1 Ordering options

Table 2. Ordering options

Type number	Flash [kB]	SRAM [kB]			EEPROM [kB]	USB device	SSP	I2C/ FM+	ADC channels	GPIO pins
		SRAM0	USB SRAM	SRAM1						
LPC1345FHN33	32	8	2	-	2	yes	2	1	8	26
LPC1345FBD48	32	8	2	-	2	yes	2	1	8	40
LPC1346FHN33	48	8	2	-	4	yes	2	1	8	26
LPC1346FBD48	48	8	2	-	4	yes	2	1	8	40
LPC1347FHN33	64	8	2	2	4	yes	2	1	8	26
LPC1347FBD48	64	8	2	2	4	yes	2	1	8	40
LPC1347FBD64	64	8	2	2	4	yes	2	1	8	51
LPC1315FHN33	32	8	-	-	2	no	2	1	8	28
LPC1315FBD48	32	8	-	-	2	no	2	1	8	40
LPC1316FHN33	48	8	-	-	4	no	2	1	8	28
LPC1316FBD48	48	8	-	-	4	no	2	1	8	40
LPC1317FHN33	64	8	-	2	4	no	2	1	8	28
LPC1317FBD48	64	8	-	2	4	no	2	1	8	40
LPC1317FBD64	64	8	-	2	4	no	2	1	8	51

5. Block diagram



(1) Available on LQFP48 and LQFP64 packages only.

(2) CT16B0_CAP1, CT16B1_CAP1, CT32B1_CAP1 inputs available on LQFP64 packages only. CT32B0_CAP0 input available on LQFP48 and LQFP64 packages only.

Fig 1. Block diagram

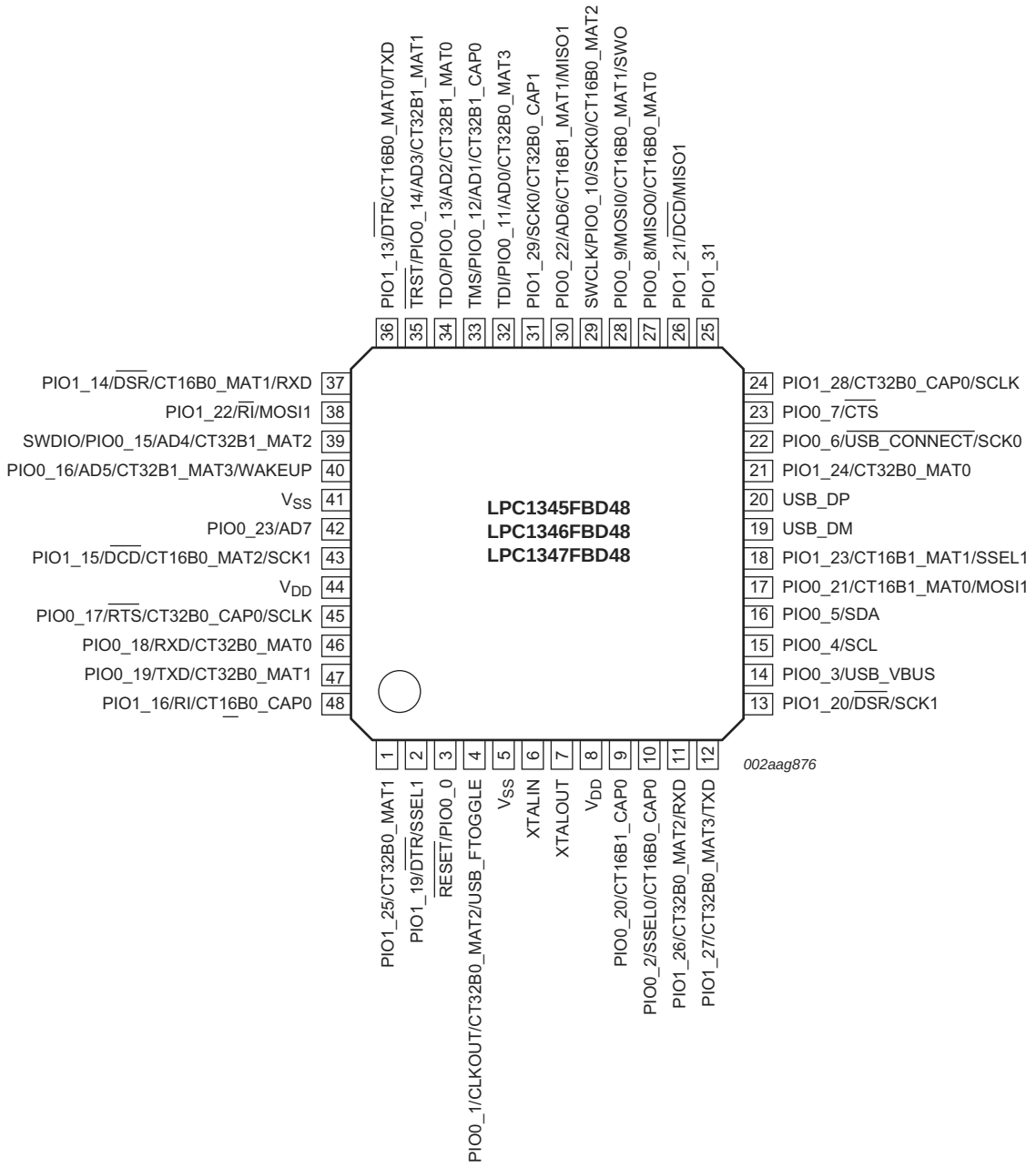


Fig 5. Pin configuration LQFP48 package (LPC1345/46/47 - with USB)

Table 3. Pin description (LPC1315/16/17 - no USB)

Symbol	LQFP64	LQFP48	HVQFN33	Reset state[1]	Type	Description
VREFP	64	-	-	-	-	ADC positive reference voltage: This should be nominally the same voltage as V_{DDA} but should be isolated to minimize noise and error. Level on this pin is used as a reference for ADC. This pin should be tied to 3.3 V if the ADC is not used.
V_{SSA}	55	-	-	-	-	Analog ground: 0 V reference. This should nominally be the same voltage as V_{SS}Product data sheet but should be isolated to minimize noise and error.
V_{DD}	10; 33; 58	8; 44	6; 29	-	-	Supply voltage to the internal regulator and the external rail. On LQFP48 and HVQFN33 packages, this pin is also connected to the 3.3 V ADC supply and reference voltage.
V_{SS}	7; 54	5; 41	33	-	-	Ground.

[1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled; IA = inactive, no pull-up/down enabled; F = floating; floating pins, if not used, should be tied to ground or power to minimize power consumption.

[2] See Figure 33 for the reset pad configuration. $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode.

[3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 32).

[4] I^2C-bus pins compliant with the I^2C-bus specification for I^2C standard mode, I^2C Fast-mode, and I^2C Fast-mode Plus.

[5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 32); includes high-current output driver.

[6] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled and the pin is not 5 V tolerant (see Figure 32); includes programmable digital input glitch filter.

[7] WAKEUP pin. 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled and the pin is not 5 V tolerant (see Figure 32); includes digital input glitch filter.

[8] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.

7.8.1 Features

- GPIO pins can be configured as input or output by software.
- All GPIO pins default to inputs with interrupt disabled at reset.
- Pin registers allow pins to be sensed and set individually.
- Up to eight GPIO pins can be selected from all GPIO pins to create an edge- or level-sensitive GPIO interrupt request.
- Port interrupts can be triggered by any pin or pins in each port.

7.9 USB interface

Remark: The USB interface is available on parts LPC1345/46/47 only.

The Universal Serial Bus (USB) is a 4-wire bus that supports communication between a host and one or more (up to 127) peripherals. The host controller allocates the USB bandwidth to attached devices through a token-based protocol. The bus supports hot-plugging and dynamic configuration of the devices. All transactions are initiated by the host controller.

The LPC1345/46/47 USB interface consists of a full-speed device controller with on-chip PHY (PHYsical layer) for device functions.

Remark: Configure the LPC1345/46/47 in default power mode with the power profiles before using the USB (see Section 7.18.5.1). Do not use the USB with the part in performance, efficiency, or low-power mode.

7.9.1 Full-speed USB device controller

The device controller enables 12 Mbit/s data exchange with a USB Host controller. It consists of a register interface, serial interface engine, and endpoint buffer memory. The serial interface engine decodes the USB data stream and writes data to the appropriate endpoint buffer. The status of a completed USB transfer or error condition is indicated via status registers. An interrupt is also generated if enabled.

7.9.1.1 Features

- Dedicated USB PLL available.
- Fully compliant with *USB 2.0 specification (full speed)*.
- Supports 10 physical (5 logical) endpoints including one control endpoint.
- Single and double buffering supported.
- Each non-control endpoint supports bulk, interrupt, or isochronous endpoint types.
- Supports wake-up from Deep-sleep mode and Power-down mode on USB activity and remote wake-up.
- Supports SoftConnect.
- Supports Link Power Management (LPM).

7.10 USART

The LPC1315/16/17/45/46/47 contains one USART.

Upon power-up, any chip reset, or wake-up from Deep power-down mode, the LPC1315/16/17/45/46/47 use the IRC as the clock source. Software may later switch to one of the other available clock sources.

7.18.1.2 System oscillator

The system oscillator can be used as the clock source for the CPU, with or without using the PLL. On the LPC1315/16/17/45/46/47, the system oscillator must be used to provide the clock source to USB.

The system oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

7.18.1.3 Watchdog oscillator

The watchdog oscillator can be used as a clock source that directly drives the CPU, the watchdog timer, or the CLKOUT pin. The watchdog oscillator nominal frequency is programmable between 9.4 kHz and 2.3 MHz. The frequency spread over processing and temperature is ±40 % (see also Table 13).

7.18.2 System PLL and USB PLL

The LPC1315/16/17/45/46/47 contain a system PLL and a dedicated PLL for generating the 48 MHz USB clock. The system and USB PLLs are identical.

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. The PLL output frequency must be lower than 100 MHz. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is 100 μs.

7.18.3 Clock output

The LPC1315/16/17/45/46/47 features a clock output function that routes the IRC oscillator, the system oscillator, the watchdog oscillator, or the main clock to an output pin.

7.18.4 Wake-up process

The LPC1315/16/17/45/46/47 begin operation at power-up and when awakened from Deep power-down mode by using the 12 MHz IRC oscillator as the clock source. This allows chip operation to resume quickly. If the main oscillator or the PLL is needed by the application, software will need to enable these features and wait for them to stabilize before they are used as a clock source.

7.18.5 Power control

The LPC1315/16/17/45/46/47 support a variety of power control features. There are four special modes of processor power reduction: Sleep mode, Deep-sleep mode, Power-down mode, and Deep power-down mode. The CPU clock rate may also be

The $\overline{\text{RESET}}$ pin selects between the JTAG boundary scan ($\overline{\text{RESET}}$ = LOW) and the ARM SWD debug ($\overline{\text{RESET}}$ = HIGH). The ARM SWD debug port is disabled while the LPC1315/16/17/45/46/47 is in reset.

Remark: Boundary scan operations should not be started until 250 μs after POR, and the test TAP should be reset after the boundary scan. Boundary scan is not affected by Code Read Protection.

Remark: The JTAG interface cannot be used for debug purposes.

Table 6. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

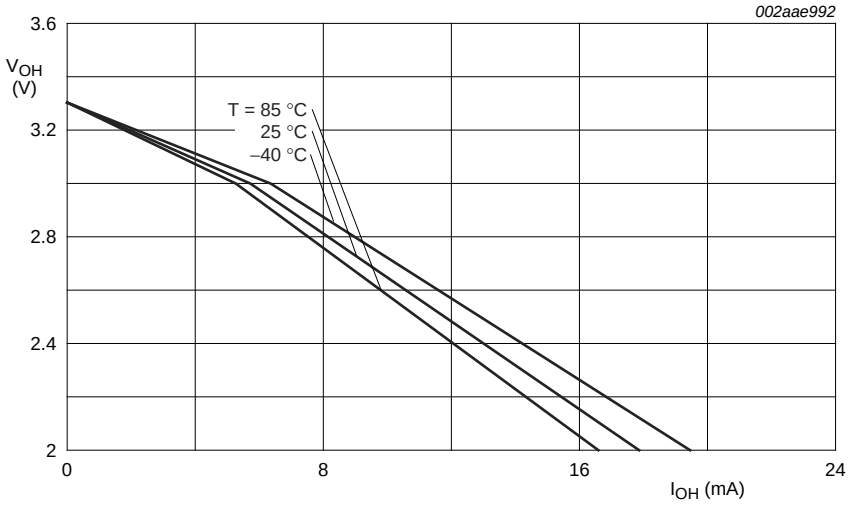
Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{OH}	HIGH-level output current	2.5 V≤ V_{DD} ≤ 3.6 V; V_{OH} = V_{DD} − 0.4 V		−4	-	-	mA
		2.0 V ≤ V_{DD} < 2.5 V; V_{OH} = V_{DD} − 0.4 V		−3	-	-	mA
I_{OL}	LOW-level output current	2.5 V ≤ V_{DD} ≤ 3.6 V; V_{OL} = 0.4 V		4	-	-	mA
		2.0 V ≤ V_{DD} < 2.5 V; V_{OL} = 0.4 V		3	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[15]	-	-	−45	mA
I_{OLS}	LOW-level short-circuit output current	V_{OL} = V_{DD}	[15]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V		10	50	150	μA
I_{pu}	pull-up current	V_I = 0 V; 2.0 V < V_{DD} ≤ 3.6 V		−15	−50	−85	μA
		V_{DD} = 2.0 V		−10	−50	−85	μA
		V_{DD} < V_I < 5 V		0	0	0	μA
High-drive output pin (PIO0_7)							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10	nA
I_{IH}	HIGH-level input current	V_I = V_{DD}; on-chip pull-down resistor disabled		-	0.5	10	nA
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = V_{DD}; on-chip pull-up/down resistors disabled		-	0.5	10	nA
V_I	input voltage	pin configured to provide a digital function	[12][13] [14]	0	-	5.0	V
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.3V_{DD}	V
V_{hys}	hysteresis voltage			0.4	-	-	V
V_{OH}	HIGH-level output voltage	2.5 V ≤ V_{DD} ≤ 3.6 V; I_{OH} = −20 mA		V_{DD} − 0.4	-	-	V
		2.0 V ≤ V_{DD} < 2.5 V; I_{OH} = −12 mA		V_{DD} − 0.4	-	-	V
V_{OL}	LOW-level output voltage	2.5 V ≤ V_{DD} ≤ 3.6 V; I_{OL} = 4 mA		-	-	0.4	V
		2.0 V ≤ V_{DD} < 2.5 V; I_{OL} = 3 mA		-	-	0.4	V
I_{OH}	HIGH-level output current	2.5 V ≤ V_{DD} ≤ 3.6 V; V_{OH} = V_{DD} − 0.4 V		20	-	-	mA
		2.0 V ≤ V_{DD} < 2.5 V; V_{OH} = V_{DD} − 0.4 V;		12	-	-	mA
I_{OL}	LOW-level output current	2.5 V ≤ V_{DD} ≤ 3.6 V; V_{OL} = 0.4 V		4	-	-	mA
		2.0 V ≤ V_{DD} < 2.5 V; V_{OL} = 0.4 V		3	-	-	mA
I_{OLS}	LOW-level short-circuit output current	V_{OL} = V_{DD}	[15]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V		10	50	150	μA

Table 6. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{pu}	pull-up current	V_I = 0 V		−15	−50	−85	μA
		2.0 V < V_{DD} ≤ 3.6 V					
		V_{DD} = 2.0 V		−10	−50	−85	μA
		V_{DD} < V_I < 5 V		0	0	0	μA
I^2C-bus pins (PIO0_4 and PIO0_5)							
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.3V_{DD}	V
V_{hys}	hysteresis voltage			-	0.05V_{DD}	-	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as standard mode pins		3.5	-	-	mA
		2.5 V ≤ V_{DD} ≤ 3.6 V					
		2.0 V ≤ V_{DD} < 2.5 V		3.0	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as Fast-mode Plus pins		20	-	-	mA
		2.5 V ≤ V_{DD} ≤ 3.6 V					
		2.0 V ≤ V_{DD} < 2.5 V		16	-	-	
I_{LI}	input leakage current	V_I = V_{DD}	[16]	-	2	4	μA
		V_I = 5 V		-	10	22	μA
Oscillator pins							
$V_{i(xtal)}$	crystal input voltage			−0.5	1.8	1.95	V
$V_{o(xtal)}$	crystal output voltage			−0.5	1.8	1.95	V
USB pins							
I_{OZ}	OFF-state output current	0 V < V_I < 3.3 V	[2]	-	-	±10	μA
V_{BUS}	bus supply voltage		[2]	-	-	5.25	V
V_{DI}	differential input sensitivity voltage	|(D+) − (D−)|	[2]	0.2	-	-	V
V_{CM}	differential common mode voltage range	includes V_{DI} range	[2]	0.8	-	2.5	V
$V_{th(rs)se}$	single-ended receiver switching threshold voltage		[2]	0.8	-	2.0	V
V_{OL}	LOW-level output voltage	for low-/full-speed; R_L of 1.5 kΩ to 3.6 V	[2]	-	-	0.18	V
V_{OH}	HIGH-level output voltage	driven; for low-/full-speed; R_L of 15 kΩ to GND	[2]	2.8	-	3.5	V
C_{trans}	transceiver capacitance	pin to GND	[2]	-	-	20	pF
Z_{DRV}	driver output impedance for driver which is not high-speed capable	with 33 Ω series resistor; steady state drive	[17][2]	36	-	44.1	Ω

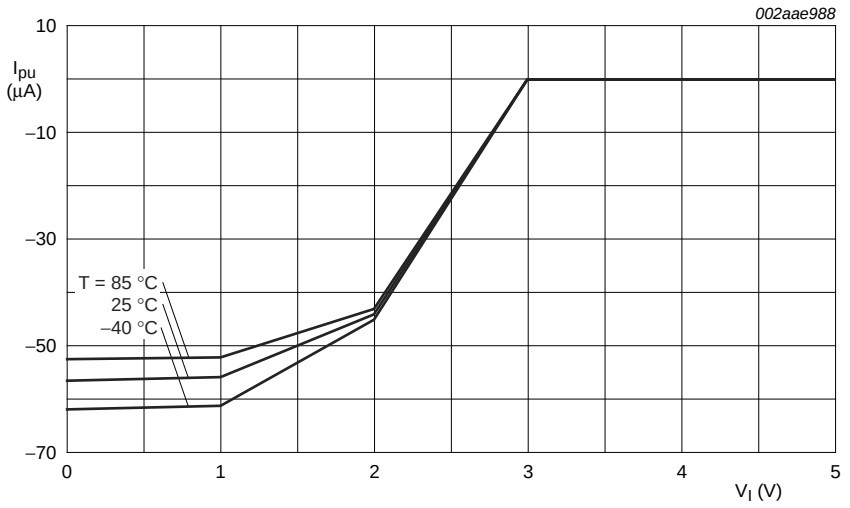
[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] For USB operation 3.0 V ≤ V_{DD} ≤ 3.6 V. Guaranteed by design.



Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 19. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}



Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 20. Typical pull-up current I_{pu} versus input voltage V_I

10. Dynamic characteristics

10.1 Flash/EEPROM memory

Table 9. Flash characteristics

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
N_{endu}	endurance		[1]	10000	100000	-	cycles
t_{ret}	retention time	powered		10	-	-	years
		unpowered		20	-	-	years
t_{er}	erase time	sector or multiple consecutive sectors		95	100	105	ms
t_{prog}	programming time		[2]	0.95	1	1.05	ms

[1] Number of program/erase cycles.

[2] Programming times are given for writing 256 bytes from RAM to the flash. Data must be written to the flash in blocks of 256 bytes.

Table 10. EEPROM characteristics

T_{amb} = −40 °C to +85 °C; V_{DD} = 2.7 V to 3.6 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{clk}	clock frequency		200	375	400	kHz
N_{endu}	endurance		100000	1000000	-	cycles
t_{ret}	retention time	powered	100	200	-	years
		unpowered	150	300	-	years
t_{er}	erase time	64 bytes	-	1.8	-	ms
t_{prog}	programming time	64 bytes	-	1.1	-	ms

10.2 External clock

Table 11. Dynamic characteristic: external clock

T_{amb} = −40 °C to +85 °C; V_{DD} over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
f_{osc}	oscillator frequency		1	-	25	MHz
$T_{cy(clk)}$	clock cycle time		40	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

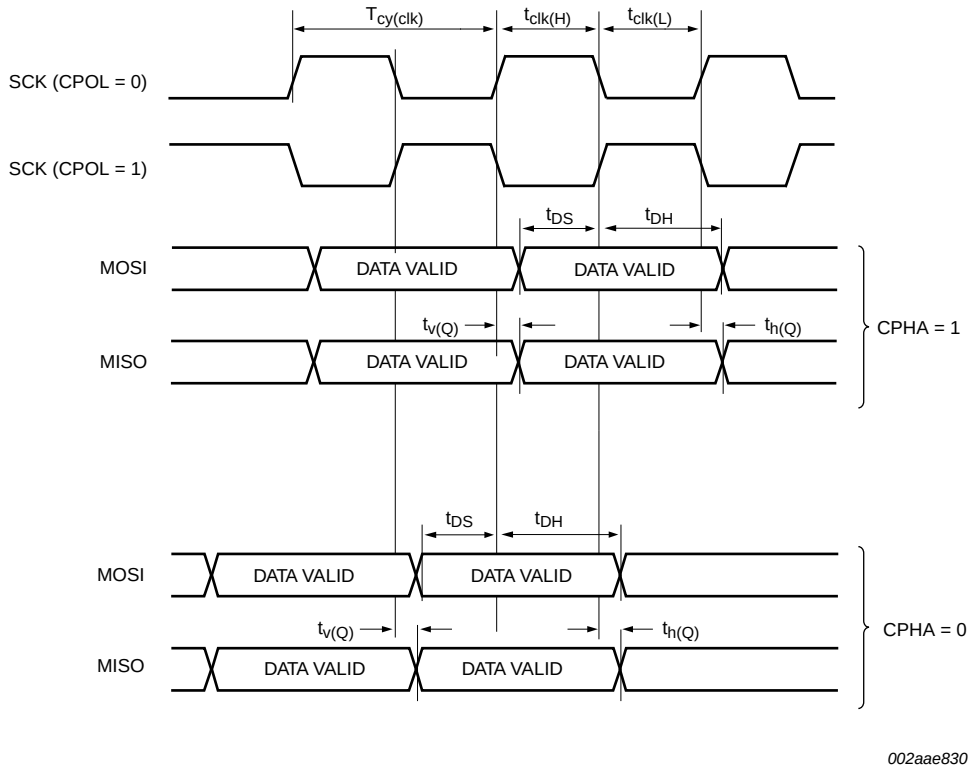


Fig 26. SSP slave timing in SPI mode

12. Application information

12.1 Suggested USB interface solutions

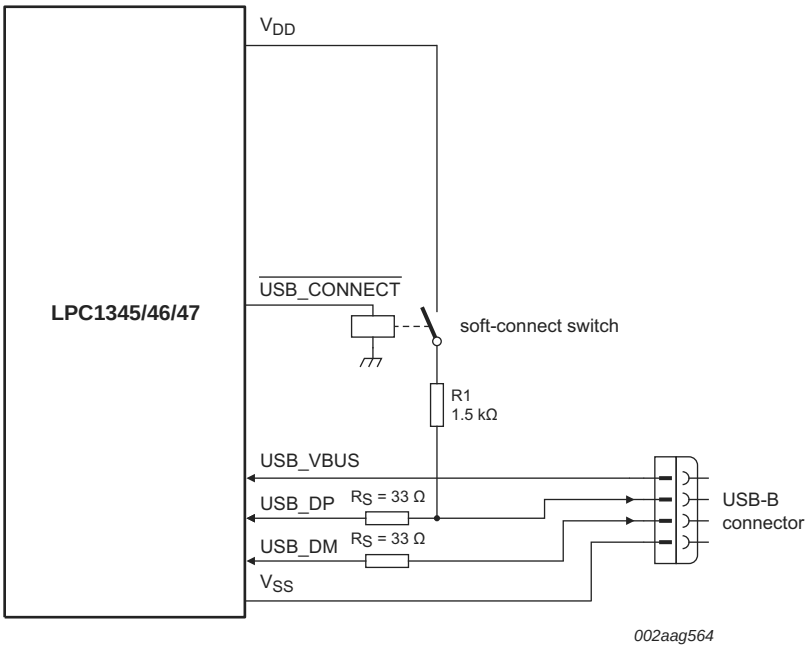


Fig 28. USB interface on a self-powered device

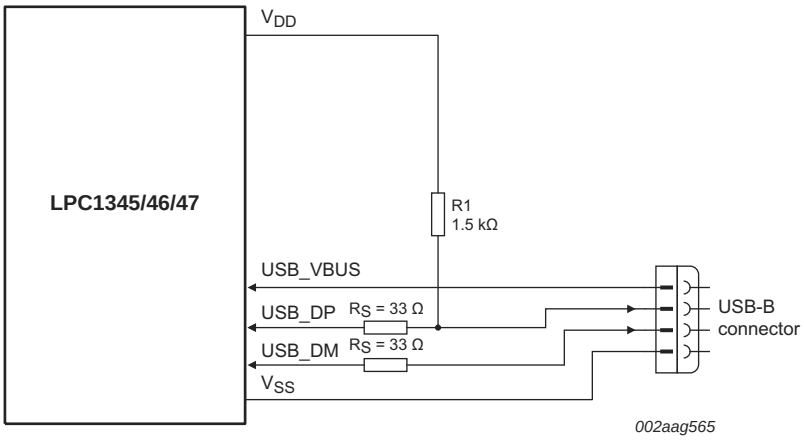


Fig 29. USB interface on a bus-powered device

12.2 XTAL input

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with C_i = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV(RMS) is needed.

Table 18. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) low frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
5 MHz - 10 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 200 Ω	39 pF, 39 pF
	30 pF	< 100 Ω	57 pF, 57 pF
10 MHz - 15 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 60 Ω	39 pF, 39 pF
15 MHz - 20 MHz	10 pF	< 80 Ω	18 pF, 18 pF

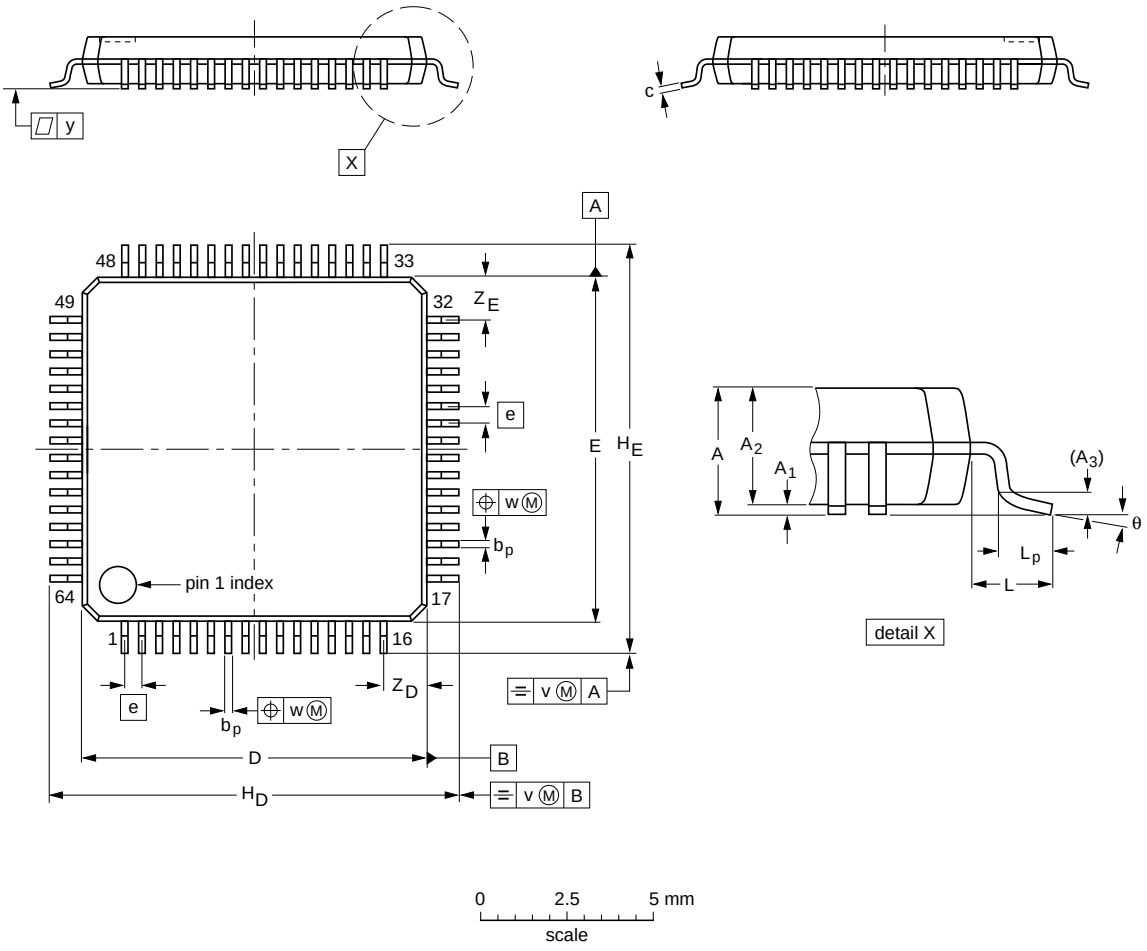
Table 19. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) high frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
15 MHz - 20 MHz	10 pF	< 180 Ω	18 pF, 18 pF
	20 pF	< 100 Ω	39 pF, 39 pF
20 MHz - 25 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 80 Ω	39 pF, 39 pF

12.3 XTAL Printed-Circuit Board (PCB) layout guidelines

The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{x1}, C_{x2}, and C_{x3} in case of third overtone crystal usage have a common ground plane. The external components must also be connected to the ground plain. Loops must be made as small as possible in order to keep the noise coupled in via the PCB as small as possible. Also parasitics should stay as small as possible. Values of C_{x1} and C_{x2} should be chosen smaller accordingly to the increase in parasitics of the PCB layout.

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm **SOT314-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1	0.75 0.45	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT314-2	136E10	MS-026				~~00-01-19~~ 03-02-25

Fig 36. Package outline LQFP64 (SOT314-2)

14. Soldering

Footprint information for reflow soldering of HVQFN33 package

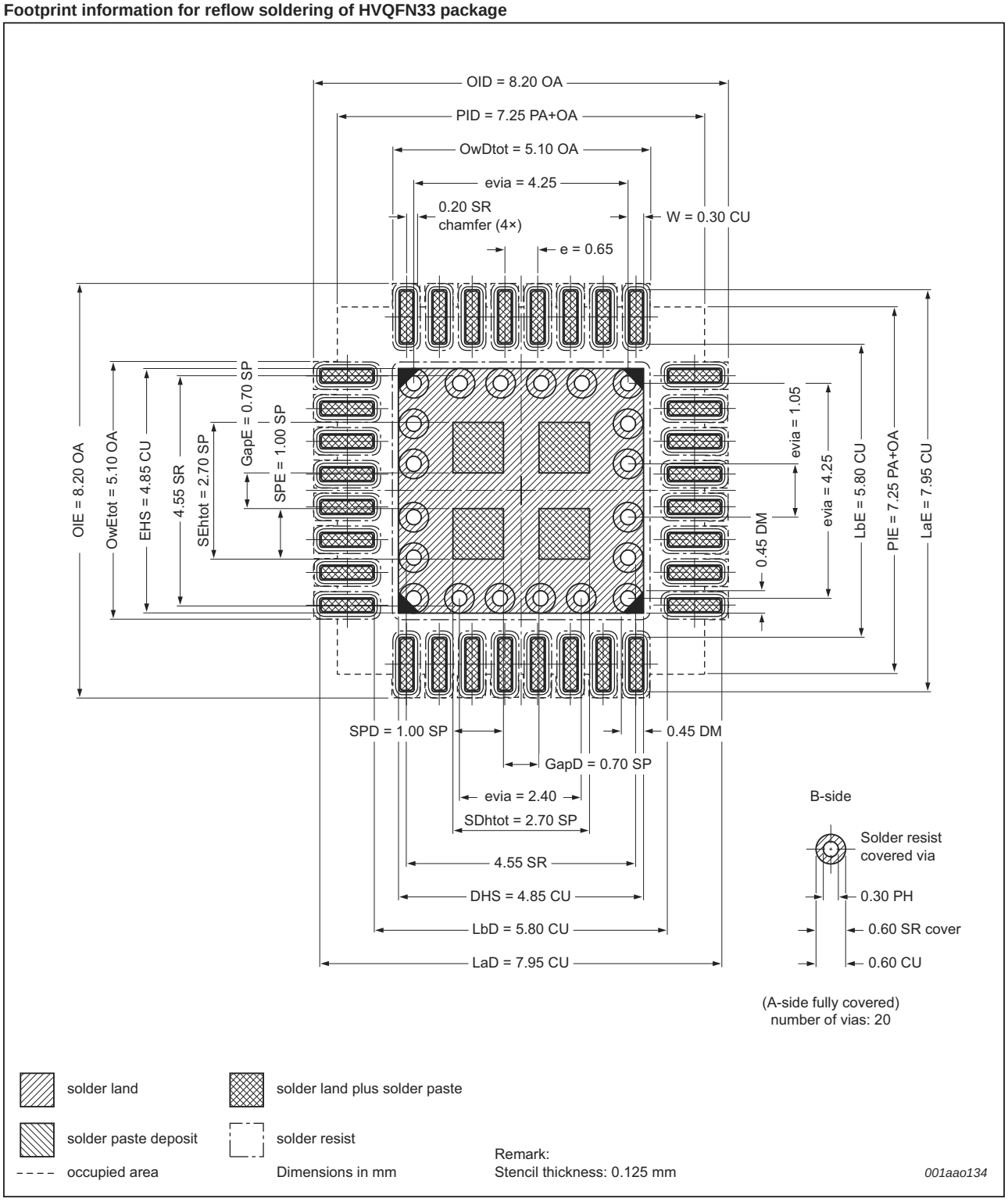
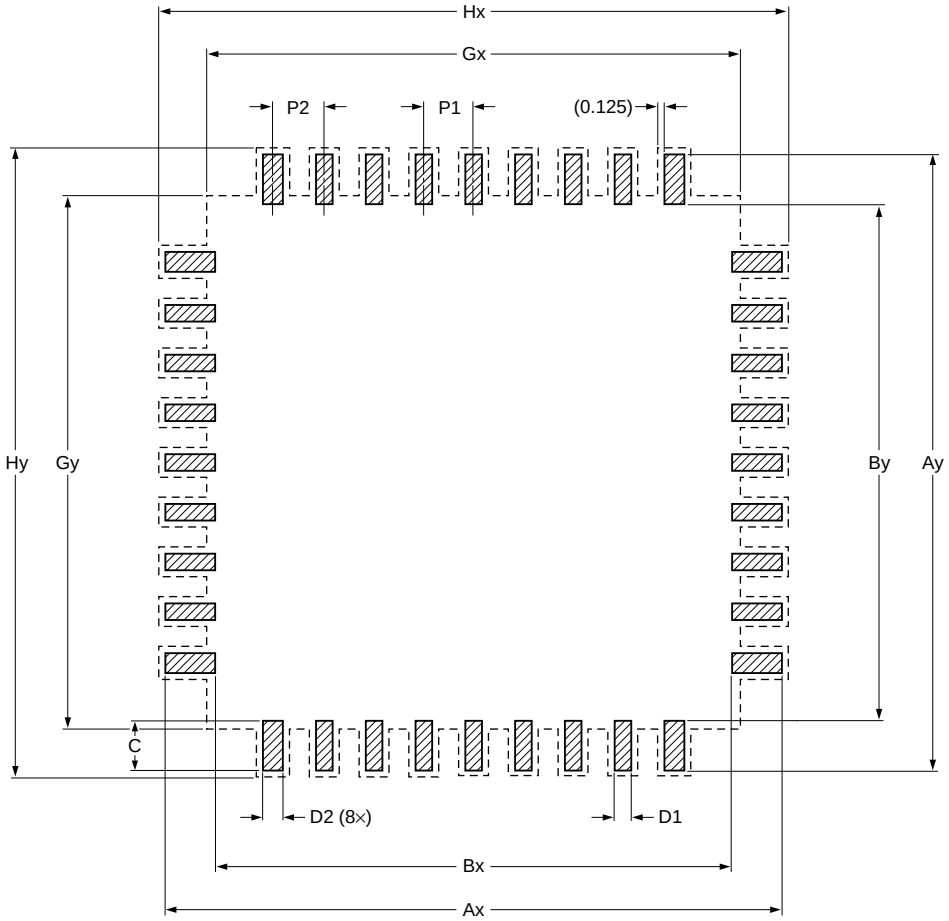


Fig 37. Reflow soldering of the HVQFN33 package

Footprint information for reflow soldering of LQFP64 package **SOT314-2**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	13.300	13.300	10.300	10.300	1.500	0.280	0.400	10.500	10.500	13.550	13.550

sot314-2_fr

Fig 39. Reflow soldering of the LQFP64 package

16. Revision history

Table 21. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC1315_16_17_45_46_47 v.3	20120920	Product data sheet	-	LPC1315_16_17_45_46_47 v.2
	• Reflow soldering drawing corrected for the HVQFN33 package. See Figure 37. • BOD interrupt trigger level 0 removed. See Table 7. • Pin configuration diagrams updated: Orientation of index sector relative to part marking corrected in Figure 4 to Figure 7.			
LPC1315_16_17_45_46_47 v.2	20120718	Product data sheet	-	LPC1315_16_17_45_46_47 v.1
Modifications:	• Data sheet status changed to Product data sheet. • Parameters V_{OL}, V_{OH}, I_{OL}, I_{OH} updated for voltage range 2.0 V ≤ V_{DD} < 2.5 V in Table 6. • Condition “The peak current is limited to 25 times the corresponding maximum current.” removed from parameters I_{DD} and I_{SS} in Table 5. • Typical operating frequencies of the watchdog oscillator corrected in Table 13 and Section 7.18.1.3.			
LPC1315_16_17_45_46_47 v.1	20120229	Preliminary data sheet	-	-

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

17.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

17.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

17.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

I²C-bus — logo is a trademark of NXP B.V.

18. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**