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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM9®
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	Audio Codec, EBI/EMI, IrDA, Memory Card, SmartCard, SSP, UART/USART, USB
Peripherals	AC'97, DMA, LCD, POR, PWM, WDT
Number of I/O	64
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	324-LFBGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/socle/lh7a404n0f000b1a

Table 1. LH7A404 Functional Pin List (Cont'd)

CABGA	SIGNAL	DESCRIPTION	RESET STATE	STANDBY STATE	OUTPUT DRIVE	I/O	NOTES
C14	SCKE3	Clock Enable 3 for Synchronous Memory	Depends on MEDCHG	LOW	12 mA	I/O	4
D14	SCLK	Synchronous Memory Clock	LOW	No Change	24 mA	I/O	2, 4
A13	nBLE0	Byte Lane Enable 0	HIGH	HIGH	12 mA	I/O	4
U9	nBLE1	Byte Lane Enable 1	HIGH	HIGH	12 mA	O	
Y7	nBLE2	Byte Lane Enable 2	HIGH	HIGH	12 mA	O	
C13	nBLE3	Byte Lane Enable 3	HIGH	HIGH	8 mA	O	
C15	nCAS	Synchronous Memory Column Address Strobe	HIGH	HIGH	12 mA	I/O	4
A15	nRAS	Synchronous Memory Row Address Strobe	HIGH	HIGH	12 mA	I/O	4
D13	DQM0	Data Mask for Synchronous Memories	HIGH	No Change	12 mA	O	
E13	DQM1						
B12	DQM2						
A12	DQM3						
M2	PA0/ LCDVD16	• GPIO Port A0 • LCD Data pin 16	PA0: Input	No Change	8 mA	I/O	
L4	PA1/ LCDVD17	• GPIO Port A1 • LCD Data pin 17	PA1: Input	No Change	8 mA	I/O	
M3	PA2	GPIO Port A[6:2]	PAx: Input	No Change	8 mA	I/O	
M4	PA3						
M1	PA4						
N3	PA5						
N2	PA6						
N1	PA7	• GPIO Port A7 • Boot Width Selection (See Table 5)	PA7: Input	No Change	8 mA	I/O	6
N4	PB0/ UARTRX1	• GPIO Port B0 • UART1 Receive Data Input	PB0: Input	No Change	8 mA	I/O	
P3	PB1/ UARTTX3	• GPIO Port B1 • UART3 Transmit Data Out	PB1: Input	No Change	8 mA	I/O	
P2	PB2/ UARTRX3	• GPIO Port B2 • UART3 Receive Data In	PB2: Input	No Change	8 mA	I/O	
P1	PB3/ UARTCTS3	• GPIO Port B3 • UART3 Clear to Send	PB3: Input	No Change	8 mA	I/O	
R3	PB4/ UARTDCD3	• GPIO Port B4 • UART3 Data Carrier Detect	PB4: Input	No Change	8 mA	I/O	
N5	PB5/ UARTDSR3	• GPIO Port B5 • UART3 Data Set Ready	PB5: Input	No Change	8 mA	I/O	
R2	PB6/ SWID/ SMBD	• GPIO Port B6 • Single Wire Data • Smart Battery Data	PB6: Input	No Change	8 mA	I/O	
R1	PB7/ SMBCLK	• GPIO Port B7 • Smart Battery Clock	PB7: Input	No Change	8 mA	I/O	
P4	PC0/ UARTTX1	• GPIO Port C0 • UART1 Transmit Data Output	PC0: LOW	No Change	12 mA	I/O	
T1	PC1	GPIO Port C[5:1]	PCx: LOW	No Change	12 mA	I/O	
T2	PC2						
T3	PC3						
R4	PC4						
U1	PC5						
U2	PC6	GPIO Port C6	PC6: LOW	No Change	12 mA	I/O	6

Table 1. LH7A404 Functional Pin List (Cont'd)

CABGA	SIGNAL	DESCRIPTION	RESET STATE	STANDBY STATE	OUTPUT DRIVE	I/O	NOTES
V1	PC7	GPIO Port C7	PC7: LOW	No Change	12 mA	I/O	
Y11	PD0/LCDVD8	• GPIO Port D[7:0] • LCD Video Data Interface	PDx: LOW	LOW if 8-bit LCD enabled; else No Change	12 mA	I/O	
U10	PD1/LCDVD9						
W12	PD2/LCDVD10						
V11	PD3/LCDVD11						
W11	PD4/LCDVD12						
U11	PD5/LCDVD13						
V12	PD6/LCDVD14						
Y12	PD7/LCDVD15						
Y9	PE0/LCDVD4	• GPIO Port E[3:0] • LCD Video Data Interface	PEx: Input	LOW if 8-bit LCD enabled; else No Change	12 mA	I/O	
W10	PE1/LCDVD5						
V10	PE2/LCDVD6						
T9	PE3/LCDVD7						
D4	PE4/ SCCLKIN	• GPIO Port E4 • Smart Card Push-Pull Mode Clock Input	PE4: Input	No Change	12 mA	I/O	
C3	PE5/ SCCLKEN	• GPIO Port E5 • Smart Card Push-Pull Mode External Clock Buffer Enable	PE5: Input	No Change	12 mA	I/O	
B2	PE6/ SCIN	• GPIO Port E6 • Smart Card Push-Pull Mode Data Input	PE6: Input	No Change	12 mA	I/O	
A1	PE7/ SCDATEN	• GPIO Port E7 • Smart Card Push-Pull Mode Data Out External Buffer Enable	PE7: Input	No Change	12 mA	I/O	
A9	PF0/ INT0	• GPIO Port F0 • Interrupt 0	PF0: Input	No Change	8 mA	I/O	3
D9	PF1/ INT1	• GPIO Port F1 • Interrupt 1	PF1: Input	No Change	8 mA	I/O	3
A8	PF2/ INT2	• GPIO Port F2 • Interrupt 2	PF2: Input	No Change	8 mA	I/O	3
C8	PF3/ INT3	• GPIO Port F3 • Interrupt 3	PF3: Input	No Change	8 mA	I/O	3
B8	PF4/ INT4	• GPIO Port F4 • Interrupt 4	PF4: Input	No Change	8 mA	I/O	3
D8	PF5/ INT5/ SCDETECT	• GPIO Port F5 • Interrupt 5 • Smart Card Interface Card Detect Signal	PF5: Input	No Change	8 mA	I/O	3
A7	PF6/ INT6/ PCRDY1	• GPIO Port F6 • Interrupt 6 • Ready for Card 1 for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode	PF6: Input	No Change	8 mA	I/O	3
E8	PF7/ INT7/ PCRDY2	• GPIO Port F7 • Interrupt 7 • Ready for Card 2 for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode	PF7: Input	No Change	8 mA	I/O	3
Y2	PG0/ nPCOE	• GPIO Port G0 • Output Enable for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode	LOW	No Change	8 mA	I/O	
W4	PG1/ nPCWE	• GPIO Port G1 • Write Enable for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode	LOW	No Change	8 mA	I/O	

Table 1. LH7A404 Functional Pin List (Cont'd)

CABGA	SIGNAL	DESCRIPTION	RESET STATE	STANDBY STATE	OUTPUT DRIVE	I/O	NOTES
U7	PH7/ nPCSTATRE	• GPIO Port H7 • Status Read Enable for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode	PHx: Input	No Change	8 mA	I/O	
T4	LCDFP/ LCDSPS	• LCD Frame Pulse • ALI Reset Row Driver Counter	LOW	LOW if not in ALI mode	12 mA	O	
V2	LCDLP/ LCDHRLP	• LCD Linepulse • ALI Latch Pulse	LOW	LOW if not in ALI mode	12 mA	O	
U3	LCDCLS	ALI Clock for Row Drivers	Input	No Change	12 mA	O	
V3	LCDSPL	ALI Start Pulse Left for reverse scanning	LOW	No Change	12 mA	O	
U4	LCDUBL	ALI Up, Down signal for reverse scanning	Input	No Change	12 mA	O	
W1	LCDSPR	ALI Start Pulse Right for normal scanning	Input	No Change	12 mA	O	
V4	LCDLBR	ALI Output for reverse scanning	HIGH	No Change	12 mA	O	
W2	LCDMOD	ALI MOD Signal used by the row driver	LOW	No Change	12 mA	O	
V5	LCDPS	ALI Power Save	HIGH	No Change	12 mA	O	
Y1	LCDVDDEN	ALI Power Sequence Control	LOW	No Change	12 mA	O	
W3	LCDREV	ALI Reverse	HIGH	No Change	12 mA	O	
U8	LCDCLKIN	External Clock Input for LCD controller	Input	No Change		I	
V8	LCDVD0	LCD Video Data Interface	LOW	LOW	12 mA	O	
T8	LCDVD1						
W9	LCDVD2						
Y8	LCDVD3						
V9	LCDENAB/ LCDM	• LCD TFT Data Enable • LCD STN AC Bias	LOW	LOW	12 mA	O	
Y10	LCDDCLK	LCD Pixel Clock	LOW	LOW	12 mA	O	
U17	USBDCP	USB Device Full Speed Pull-up Resistor Control	Input	Input	12 mA	I	
U20	USBDP	USB Device Data Positive (Differential Pair)	Input	Input	12 mA	I/O	
U19	USBDN	USB Device Data Negative (Differential Pair)	Input	Input	12 mA	I/O	
W19	USBHDP0	USB Data Host Positive 0 (Differential Pair)	Input	HIGH	12 mA	I/O	
W20	USBHDN0	USB Data Host Negative 0 (Differential Pair)	Input	LOW	12 mA	I/O	
V19	USBHDP1	USB Data Host Positive 1 (Differential Pair)	Input	Input	12 mA	I/O	
V20	USBHDN1	USB Data Host Negative 1 (Differential Pair)	Input	Input	12 mA	I/O	
T17	USBHPWR	USB Host Power	LOW	Input	12 mA	O	
V17	USBHOVRCURR	USB Host Overcurrent	Input	Input	12 mA	I	
D11	nPWME0	DC-DC Converter 0 PWM 0 Enable	Input	Input	8 mA	I/O	5
A10	nPWME1	DC-DC Converter 1 PWM 1 Enable	Input	Input	8 mA	I/O	5
C11	PWM0	DC-DC Converter 0 Output (Pulse Width Modulated)	Input	Input	8 mA	I/O	4
C10	PWM1	DC-DC Converter 1 Output (Pulse Width Modulated)	Input	Input	8 mA	I/O	4
B9	PWM2	PWM Output 2	Input	No Change	8 mA	O	
D10	PWM3	PWM Output 3	Input	No Change		O	
C9	PWMSYNC	PWM Synchronizing Input for PWM2	Input	No Change	8 mA	I	
C7	ACBITCLK	• Audio Codec (AC97) Clock • Audio Codec (ACI) Clock	Input	No Change	8 mA	I/O	
B7	ACOUT	• Audio Codec (AC97) Output • Audio Codec (ACI) Output	LOW	LOW	8 mA	O	
A6	ACSYNC	• Audio Codec (AC97) Synchronization • Audio Codec (ACI) Synchronization	LOW	LOW	8 mA	O	

Table 4. CABGA Numerical Pin List

CABGA	SIGNAL	SLEW RATE	OUTPUT DRIVE
A1	PE7/SCDATEN	95 mV/ns	12 mA
A2	DACK1	95 mV/ns	12 mA
A3	DREQ0		
A4	MMCDATA2	110 mV/ns	8 mA
A5	MMCCLK	110 mV/ns	8 mA
A6	ACSYNC	110 mV/ns	8 mA
A7	PF6/INT6/PCRDY1	110 mV/ns	8 mA
A8	PF2/INT2	110 mV/ns	8 mA
A9	PF0/INT0	110 mV/ns	8 mA
A10	nPWME1	95 mV/ns	12 mA
A11	SCCLK	95 mV/ns	12 mA
A12	DQM3	110 mV/ns	8 mA
A13	nBLE0	95 mV/ns	12 mA
A14	SCKE0	95 mV/ns	12 mA
A15	nRAS	95 mV/ns	12 mA
A16	A25	95 mV/ns	12 mA
A17	D30	95 mV/ns	12 mA
A18	D29	95 mV/ns	12 mA
A19	nSCS1	95 mV/ns	12 mA
A20	D25	95 mV/ns	12 mA
B1	TDO	100 mV/ns	4 mA
B2	PE6/SCIN	95 mV/ns	12 mA
B3	DREQ1		
B4	MMCDATA3	110 mV/ns	8 mA
B5	MMCDATA1	110 mV/ns	8 mA
B6	ACIN	110 mV/ns	8 mA
B7	ACOUT	110 mV/ns	8 mA
B8	PF4/INT4	110 mV/ns	8 mA
B9	PWM2	110 mV/ns	8 mA
B10	SCVCCEN	95 mV/ns	12 mA
B11	nSCRESET	95 mV/ns	12 mA
B12	DQM2	95 mV/ns	12 mA
B13	SCKE1_2	95 mV/ns	12 mA
B14	A27	95 mV/ns	12 mA
B15	D31	95 mV/ns	12 mA
B16	nSWE	95 mV/ns	12 mA
B17	D28	95 mV/ns	12 mA
B18	D26	95 mV/ns	12 mA
B19	A24	95 mV/ns	12 mA
B20	D23	95 mV/ns	12 mA
C1	nEXTPWR		
C2	TCK		
C3	PE5/SCCLKEN	95 mV/ns	12 mA
C4	DEOT0	95 mV/ns	12 mA
C5	nRESETOUT		

Table 4. CABGA Numerical Pin List (Cont'd)

CABGA	SIGNAL	SLEW RATE	OUTPUT DRIVE
C6	MMCDATA	110 mV/ns	8 mA
C7	ACBITCLK	110 mV/ns	8 mA
C8	PF3/INT3	110 mV/ns	8 mA
C9	PWMSYNC		
C10	PWM1	110 mV/ns	8 mA
C11	PWM0	110 mV/ns	8 mA
C12	nOE	95 mV/ns	12 mA
C13	nBLE3	110 mV/ns	8 mA
C14	SCKE3	95 mV/ns	12 mA
C15	nCAS	95 mV/ns	12 mA
C16	D27	95 mV/ns	12 mA
C17	nSCS0	95 mV/ns	12 mA
C18	D24	95 mV/ns	12 mA
C19	A22	95 mV/ns	12 mA
C20	D21	95 mV/ns	12 mA
D1	nBATCHG		
D2	nPOR		
D3	TDI		
D4	PE4/SCCLKIN	95 mV/ns	12 mA
D5	DACK0	95 mV/ns	12 mA
D6	CTCLKIN		
D7	MMCCMD	110 mV/ns	8 mA
D8	PF5/INT5/SCDETECT	110 mV/ns	8 mA
D9	PF1/INT1	110 mV/ns	8 mA
D10	PWM3	110 mV/ns	8 mA
D11	nPWME0	110 mV/ns	8 mA
D12	nWE	95 mV/ns	12 mA
D13	DQM0	95 mV/ns	12 mA
D14	SCLK	190 mV/ns	24 mA
D15	A26	95 mV/ns	12 mA
D16	nSCS2	95 mV/ns	12 mA
D17	A23	95 mV/ns	12 mA
D18	D22	95 mV/ns	12 mA
D19	A20	95 mV/ns	12 mA
D20	D19	95 mV/ns	12 mA
E1	nURESET		
E2	BATOK		
E3	TMS		
E4	MEDCHG		
E5	DEOT1	95 mV/ns	12 mA
E6	VSSC		
E7	VDDC		
E8	PF7/INT7/PCRDY2	110 mV/ns	8 mA
E9	VDDC		
E10	VDD		

Power Modes

The LH7A404 has three operational states: Run, Halt, and Standby. During Run all clocks are hardware enabled and the processor is clocked. In the Halt mode the device is functioning, but the processor clock is halted while it waits for an event such as a key press. Standby equates to the computer being switched 'off', i.e. no display (LCD disabled) and the main oscillator is shut down.

Reset Modes

Three external signals can generate resets to the LH7A404: nPOR (power on reset), nPWRFL (power failure) and nURESET (user reset). If any of these are active, a system reset is internally generated. An nPOR reset performs a full system reset. The nPWRFL and nURESET resets perform a full system reset except for the SDRAM refresh control, SDRAM Global Configuration, SDRAM Device Configuration, and the RTC peripheral registers. The SDRAM controller issues a self-refresh command to external SDRAM before the system enters an nPWRFL and nURESET reset. This allows the system to maintain its Real Time Clock and SDRAM contents. Upon release of Reset, the chip enters Standby mode. Once in the Run mode the PWRSR register can be interrogated to determine the nature of the reset and the trigger source, after which software can then take appropriate actions.

Data Paths

The data paths in the LH7A404 are:

- The AMBA AHB bus
- The AMBA APB bus
- The External Bus Interface
- The LCD AHB bus
- The DMA busses.

AMBA AHB BUS

The Advanced Microprocessor Bus Architecture AHB (AMBA AHB) is a high speed 32-bit-wide data bus. The AMBA AHB is for high-performance, high-clock-frequency system modules.

LH7A404 peripherals and memory with high bandwidth requirements are connected to the ARM922T processor and other bus masters using a multi-master AHB bus. These peripherals include the external memory interfaces, on-chip SRAM, LCD Controller (bus master), DMA Controller (bus master), and USB Host (bus master). Remaining peripherals reside on the lower bandwidth Advanced Peripheral Bus (APB), which is accessed from the AHB via the APB Bridge. The APB Bridge is the only master on the APB, and its operation is transparent to the user as it converts AHB accesses into slower APB accesses automatically.

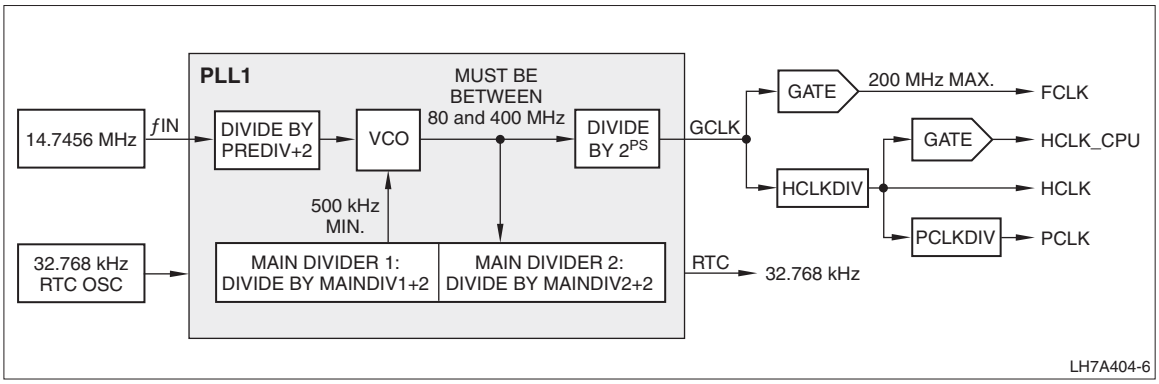


Figure 3. Clock and State Controller Block Diagram

AMBA APB BUS

The AMBA APB provides a lower-bandwidth bus for peripherals accessed less frequently. This reduces the loading on the AHB, allowing it to run faster to maximize system performance, while the APB can operate at a lower clock rate to conserve power. The APB Bridge is the only master on the APB. All AHB masters can access APB peripherals via the ABP Bridge. The APB clock frequency can be selected by software to divide the clock speed of the AHB bus by 2, 4, or 8.

EXTERNAL BUS INTERFACE (EBI)

The External Bus Interface (EBI) provides a 32-bit-wide, high speed gateway to external memory devices. The supported memory devices include:

- Asynchronous RAM/ROM/Flash
- Synchronous DRAM/Flash
- PCMCIA interfaces
- CompactFlash interfaces.

The EBI can be controlled by either the Asynchronous Memory Controller or Synchronous Memory Controller. There is an arbiter on the EBI input, with priority given to the Synchronous Memory Controller interface.

LCD BUS

The LCD controller has its own local memory bus that connects it to the system's embedded memory and external SDRAM. The function of this local data bus is to allow the LCD controller to perform its video refresh function without congesting the main AHB bus. This leads to better system performance and lower power consumption. There is an arbiter on both the embedded memory and the synchronous memory controller. In both cases the LCD bus is given priority.

DMA BUSES

The LH7A404 has a DMA system that connects the higher speed/higher data volume APB peripherals (MMC, USB Device and AC97) to the AHB bus. This enables the efficient transfer of data between these peripherals and external memory without the intervention of the ARM922T core.

USB HOST CONTROLLER DMA BUS

The USB Host Controller has its own DMA controller. It acts as another bus master on the AHB bus. It does not interact with the non-USB DMA controller except in bus arbitration.

Memory Map

The LH7A404 system has a 32-bit-wide address bus, allowing addressing up to 4GB of memory. This memory space is subdivided into a number of memory banks, shown in Figure 4. Four of these banks (each 256MB) are allocated to the Synchronous Memory Controller. Eight banks (each 256MB) are allocated to the Asynchronous Memory Controller. Two of these eight banks are designed for PCMCIA systems. Part of the remaining memory space is allocated to the embedded SRAM, and to the control registers of the AHB and APB. The rest of the memory space is not used.

The LH7A404 can boot from both internal and external devices. The selection is determined by the value of five pins at power-on reset as shown in Table 5. If booting is from an external device (with INTBOOT = 0), refer to Table 6. When booting from external synchronous memory, bank 4 (nSCS3) is mapped into memory location zero. When booting from external asynchronous memory, memory bank 0 (nSCS0) is mapped into memory location zero.

Figure 4 shows the memory map of the LH7A404 system for the two boot modes.

Once the LH7A404 has booted, the boot code can configure the ARM922T MMU to remap the low memory space to a location in RAM. This allows the user to set the interrupt vector table.

External Bus Interface

The ARM922T, LCD controller, and DMA engine have access to an external memory system. The LCD controller has access to an internal frame buffer in embedded SRAM and an extension buffer in Synchronous Memory for large displays. The processor and DMA engine share the main system bus, providing access to all external memory devices and the embedded SRAM frame buffer.

An arbitration unit ensures that control over the External Bus Interface (EBI) is only granted when an existing access has been completed. See Figure 4.

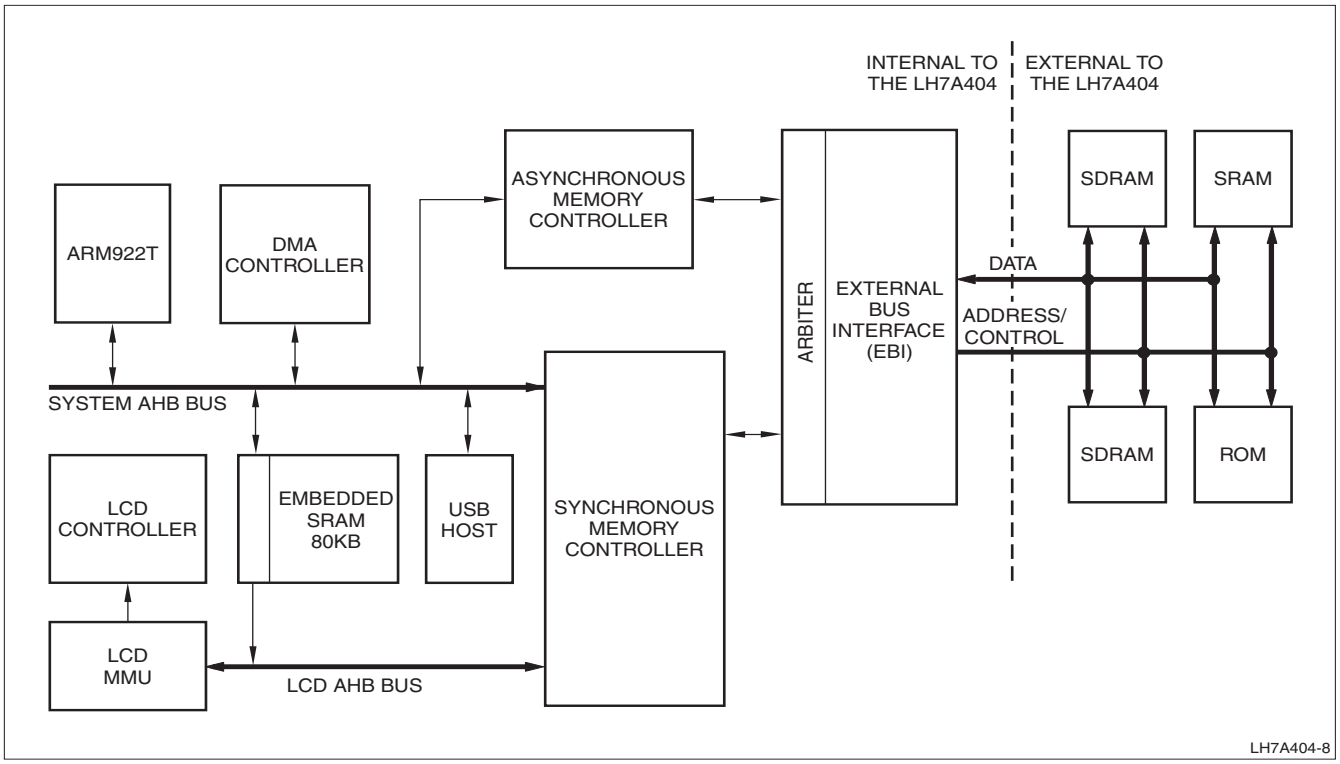


Figure 4. External Bus Interface Block Diagram

Embedded SRAM

The LH7A404 incorporates 80KB of embedded SRAM. This embedded memory is used for storing code, data, or LCD frame data and is contiguous with external SDRAM. The 80KB is large enough to store a QVGA frame (320 × 240) at 8 bits per pixel, equivalent to 70KB of information.

Locating the frame buffer on chip reduces the overall power consumed by LH7A404 applications. Normally, the system performs external accesses to acquire this data. The LCD controller automatically uses an overflow frame buffer in SDRAM if a larger screen size is required. This overflow buffer can be located on any 4KB page boundary in SDRAM, allowing software to set the MMU (in the LCD controller) page tables so the two memory areas appear contiguous, allowing byte, half-word, and word accesses.

Static Memory Controller (SMC)

The asynchronous Static Memory Controller (SMC) provides an interface between the AMBA AHB system bus and external (off-chip) memory devices.

The SMC simultaneously supports up to eight independently configurable memory banks. Each memory bank can support:

- SRAM
- ROM
- Flash EPROM
- Burst ROM memory.

Each memory bank may use devices with either 8-, 16-, or 32-bit external memory data paths. The memory controller can be configured to support either little-endian or big-endian operation.

The memory banks can be configured to support:

- Non-burst read and write accesses only to high-speed CMOS static RAM
- Non-burst write accesses, nonburst read accesses and asynchronous page mode read accesses to fast-boot block flash memory.

The SMC has six main functions:

- Memory bank select
- Access sequencing
- Wait state generation
- Byte lane write control
- External bus interface
- CompactFlash or PCMCIA interfacing.

SDRAM (Synchronous) Memory Controller

The SDRAM (Synchronous) Memory Controller provides a high speed memory interface to a wide variety of synchronous memory devices, including Synchronous DRAM, Synchronous Flash and Synchronous ROMs.

The key features of the controller are:

- LCD DMA port for high bandwidth
- Up to four Synchronous Memory banks can be independently set up
- Includes special configuration bits for Synchronous ROM operation
- Includes ability to program Synchronous Flash devices using write and erase commands
- On booting from Synchronous ROM, (and optionally with Synchronous Flash), a configuration sequence is performed before releasing the processor from reset
- Data is transferred between the controller and the Synchronous DRAM in four-word bursts. Longer transfers within the same page are concatenated, forming a seamless burst
- Programmable for 16- or 32-bit data bus size
- Two reset domains enable Synchronous DRAM contents to be preserved over a ‘soft’ reset
- Power saving Synchronous Memory SCKE and external clock modes provided.

Secure Digital/MultiMediaCard (MMC)

The SD Memory Card is a flash-based memory card that meets the security, capacity, performance, and environment requirements inherent in electronic devices. The SD Memory Card host supports MultiMediaCard (MMC) operation as well, and is compatible with MMC Cards.

The SD/MMC controller can be used as an MMC card controller or as an SD Card controller, and supports the full SD/MMC bus protocol as defined in the MMC system specification 2.11 provided by the MMC Association and the SD Memory Card Spec v1.0 from the SD Association.

SD/MMC INTERFACE DESCRIPTION

The SD/MMC controller uses the three-wire signal bus (clock, command, and data) to input and output data to and from the MMC, and to configure and acquire status information from the card. The SD controller differs in that it has four data lines instead of one.

The SD/MMC bus lines can be divided into three groups:

- Power supply: VSS1, VSS2, and VDD
- Data transfer group: MMCCMD, MMCDATA0, MMCDATA1, MMCDATA2, MMCDATA3 (for MMC, do not use MMCDATA1, MMCDATA2, MMCDATA3)
- Clock: MMCCLK

MMC CONTROLLER

The MMC controller implements MMC-specific functions, serves as the bus master for the MMC Bus and implements the standard interface to the MMC (card initialization, CRC generation and validation, command/response transactions, etc.).

Smart Card Interface (SCI)

The SCI (ISO7816) connects to an external Smart Card reader. The SCI can autonomously control data transfer to and from the Smart Card. Transmit and receive data FIFOs are provided to reduce the required interaction between the CPU core and the peripheral.

SCI FEATURES

- Supports asynchronous T0 and T1 transmission protocols
- Supports clock rate conversion factor F = 372, with bit rate adjustment factors of D = 1, 2, or 4
- Eight-character-deep buffered Tx and Rx paths
- Direct interrupts for Tx and Rx FIFO level monitoring
- Interrupt status register
- Hardware-initiated card deactivation sequence on detection of card removal
- Software-initiated card deactivation sequence on transaction complete
- Limited support for synchronous smart cards via registered input/output.

PROGRAMMABLE PARAMETERS

- Smart Card clock frequency
- Communication baud rate
- Protocol convention
- Card activation/deactivation time
- Maximum time for first character of Answer to Reset (ATR) reception checking
- Maximum ATR character stream duration checking
- Maximum time of receipt of first character of data stream checking
- Maximum time allowed between characters checking
- Character guard time
- Block guard time
- Transmit/receive character retry.

Direct Memory Access Controller (DMA)

The DMA Controller can be used to interface streams from 20 internal peripherals to the system memory using 10 fully-independent programmable channels which consist of five M2P (transmit) channels and five P2M (receive) channels.

The following peripherals may be allocated to the 10 channels:

- USB Device
- USB Host
- SD/MMC
- AC97
- UART1
- UART2
- UART3

Each of the above peripherals contain one Tx and one Rx channel, except the AC97, which contains three Tx and Rx channels. These peripherals also have their own bi-directional DMA bus, capable of simultaneously transferring data in both directions. All memory transfers take place via the main system AHB bus.

The DMA Controller can also be used to interface streams from memory-to-memory (M2M) or memory-to-external peripheral (M2P) using two dedicated M2M channels. External handshake signals are available to support memory-to-/from-external peripheral (M2P/P2M) transfers. A software trigger is available for M2M transfers only.

The DMA Controller features:

- Two dedicated channels for M2M and external M2P/P2M
- Ten fully independent, programmable DMA controller internal M2P/P2M channels (5 Tx and 5 Rx)
- Channels assignable to one of a number of different peripherals
- Independent source and destination address registers. Source and destination can be programmed to auto-increment or not auto-increment for M2M channels
- Two buffer descriptors per M2P and M2M channel to avoid potential data under/over-flow due to software introduced latency. A buffer refers to the area in system memory that is characterized by a buffer descriptor, i.e., a start address and the length of the buffer in bytes
- No AMBA wrapping bursts for DMA channels; only incrementing bursts are supported
- Buffer size independent of the peripheral's packet size for the internal M2P channels. Transfers can automatically switch between buffers
- Maskable interrupt generation
- Internal arbitration between DMA channels, plus support for an AHB bus arbiter
- DMA data transfer sizes, byte, word and quad-word data transfers are supported using a 16-byte data. Maximum data transfer size per M2M channel is programmable
- Per-channel clock gating reducing power in channels that have not been enabled by software. See the 'Clock and State Controller' section.

A set of control and status registers are available to the system processor for setting up DMA operations and monitoring their status. System interrupts are generated when any/all of the DMA channels wish to inform the processor to update the buffer descriptor. The DMA controller can service 10 out of 20 possible peripherals using the ten DMA channels, each with its own peripheral DMA bus capable of simultaneously transferring data in both directions.

The SD/MMC, UART[3:1], USB Device, and USB Host peripherals can each use two DMA channels, one for transmit and one for receive. The AC97 peripheral can use six DMA channels (three transmit and three receive) to allow different sample frequency data queues to be handled with low software overhead.

The DMA controller includes an M2M transfer feature allowing block moves of data from one memory address space to another with minimum of program effort and time. An M2M software trigger capability is provided. The DMA controller can also fill a block of memory with data from a single location.

The DMA controller's M2M channels can also be used in M2P/P2M mode. A set of external handshake signals, DREQ, DACK and TC/DEOT are provided for each of two M2M channels.

DREQ (input) can be programmed edge or level active, and active HIGH or LOW. The peripheral may hold DREQ active for the duration of the block transfers or may assert/deassert on each transfer.

DACK (output) can be programmed active HIGH or LOW. DACK will assert and return to de-asserted with each Read or Write, the timing coinciding with nOE or nWE from the EBI.

TC/DEOT is a bidirectional signal with programmable direction and active polarity. When configured as an Output, the DMA will assert Terminal Count (TC) on the final transfer to coincide with the DACK, typically when the byte count has expired. When configured as an Input, the peripheral must assert DEOT concurrent with DREQ for the final transfer in the block.

Transfer is terminated when DEOT is asserted by the external peripheral or when the byte count expires, whichever occurs first. Status bits indicate if the actual byte count is equal to the programmed limit, and if the count was terminated by peripheral asserting DEOT. Terminating the transfer causes a DMA interrupt on that channel and rollover to the 'other' buffer if so configured.

USB Device

The features of the USB are:

- Compliant with USB 2.0 Full Speed specification
- Provides a high-level interface that removes the USB protocol details from firmware
- Compatible with both OpenHCI and Intel UHCI standards
- Supports full-speed (12 Mbit/s) functions
- Supports Suspend and Resume signalling.

USB Host Controller

The features of the USB Host Controller are:

- Open Host Controller Interface Specification (OpenHCI) Rev. 1.0 Compliant
- Universal Serial Bus Specification 2.0 Full Speed compatible
- Supports Low Speed and High Speed USB devices
- Root Hub has two Downstream Ports
- DMA functionality.

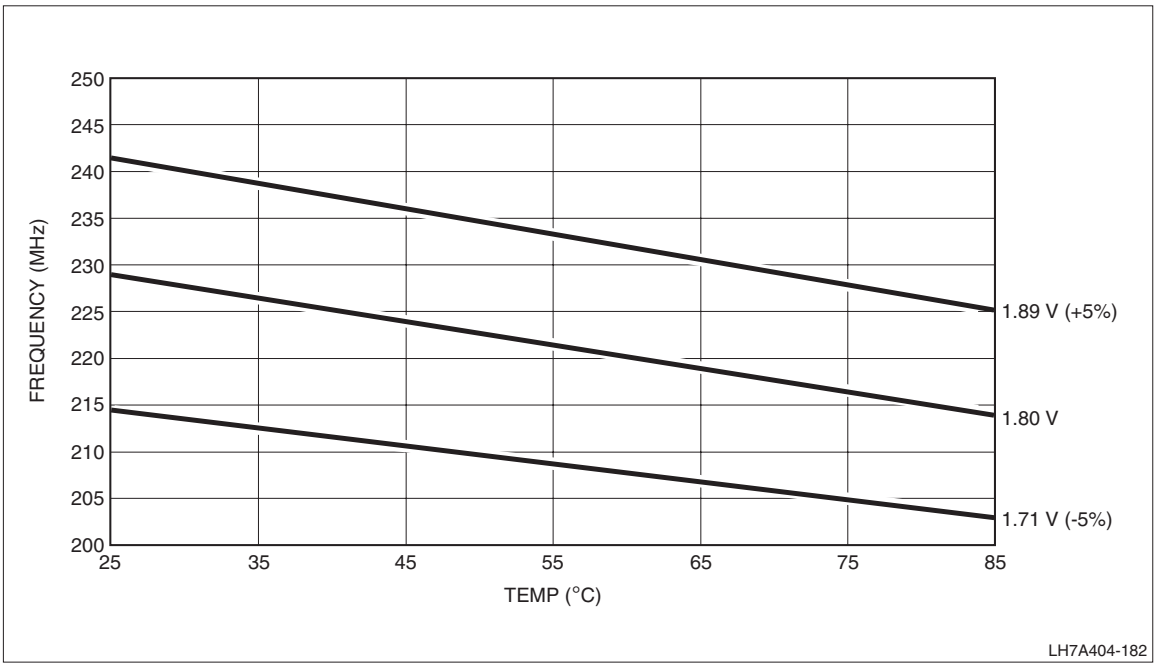


Figure 5. Temperature/Voltage/Speed Chart

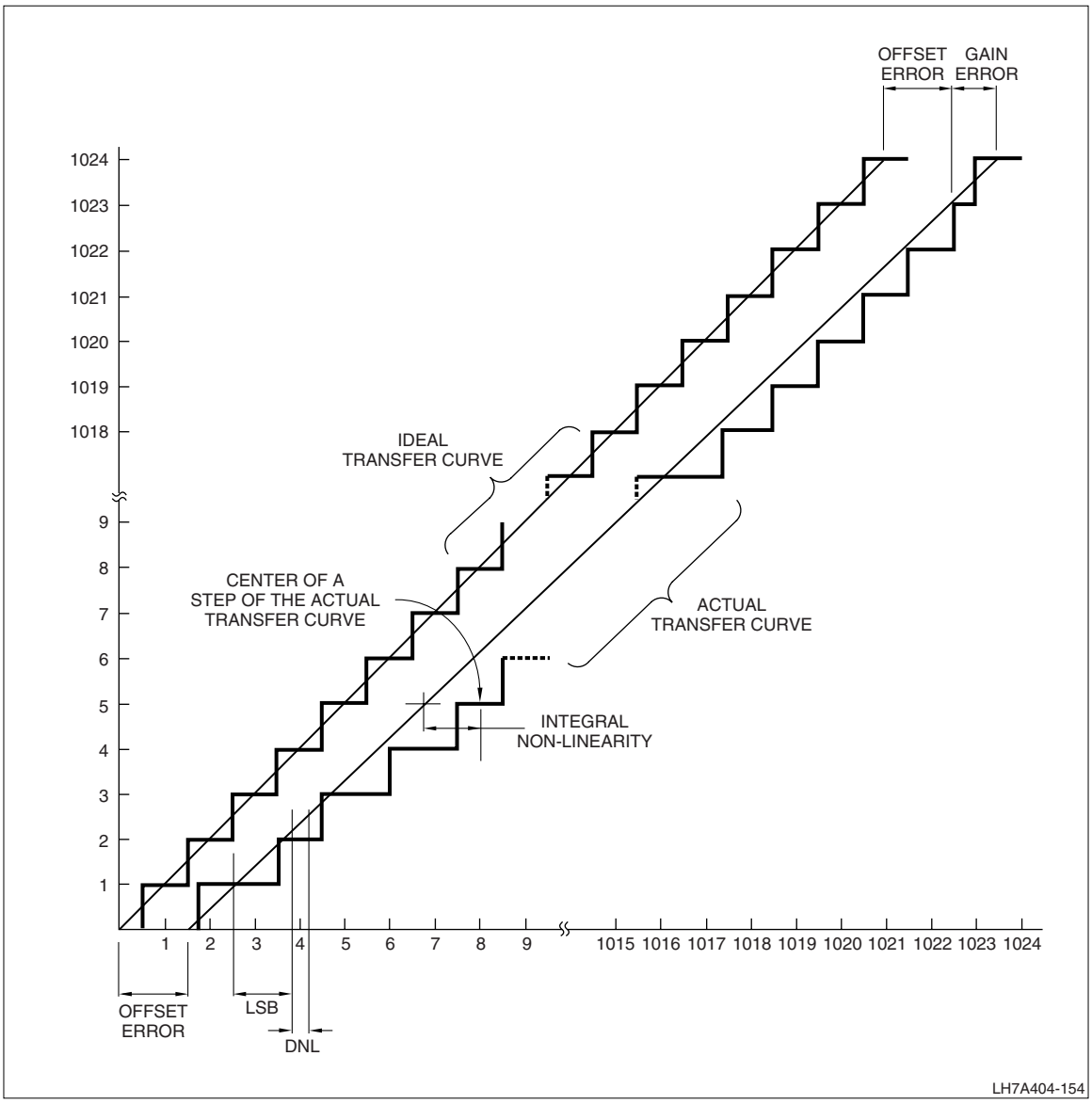


Figure 6. ADC Transfer Characteristics

AC Test Conditions

PARAMETER	RATING	UNIT
DC I/O Supply Voltage (VDD)	3.0 to 3.6	V
DC Core Supply Voltage (VDDC)	1.7 to 1.9	V
Input Pulse Levels	VSS to 3	V
Input Rise and Fall Times	2	ns
Input and Output Timing Reference Levels	VDD/2	V

CURRENT CONSUMPTION BY OPERATING MODE

Current consumption can depend on a number of parameters. To make these data more usable, the values presented in Table 9 were derived under the conditions described here.

Maximum Specified Value

The values specified in the MAXIMUM column were determined using these operating characteristics:

- All IP blocks either operating or enabled at maximum frequency and size configuration
- Core operating at maximum power configuration
- All voltages at maximum specified values
- Nominal specified ambient temperature.

Typical

The values in the TYPICAL column were determined using a 'typical' application under 'typical' environmental conditions and the following operating characteristics:

- LINUX operating system running from SDRAM
- UART and AC97 peripherals operating; all other peripherals as needed by the OS
- LCD enabled with 320 × 240 × 16-bit color, 60 Hz refresh rate, data in SDRAM
- I/O loads at nominal
- Cache enabled
- FCLK = 200 MHz; HCLK = 100 MHz; PCLK = 50 MHz
- All voltages at typical values
- Nominal case temperature.

Table 9. Current Consumption by Mode

SYMBOL	PARAMETER	TYP.	MAX.	UNITS
RUN MODE				
ICORE	Current drawn by core	132	180	mA
IIO	Current drawn by I/O	15	58	mA
HALT MODE (ALL PERIPHERALS DISABLED)				
ICORE	Current drawn by core	40	44	mA
IIO	Current drawn by I/O	1	1	mA
STANDBY MODE (TYPICAL CONDITIONS ONLY)				
ICORE	Current drawn by core	66		μA
IIO	Current drawn by I/O	4		μA

PERIPHERAL CURRENT CONSUMPTION

In addition to the modal current consumption, Table 10 shows the typical current consumption for each of the on-board peripheral blocks. The values were determined with the peripheral clock running at maximum frequency, typical conditions, and no I/O loads. This current is supplied by the 1.8 V power supply.

Table 10. Peripheral Current Consumption

PERIPHERAL	TYPICAL	UNITS
AC97	1.3	mA
UART (each)	1.0	mA
RTC	0.005	mA
Timers (each)	0.1	mA
LCD (+I/O)	5.4 (1.0)	mA
MMC	0.6	mA
SCI	23	mA
PWM (each)	<0.1	mA
BMI-SWI	1.0	mA
BMI-SBus	1.0	mA
SDRAM (+I/O)	1.5 (14.8)	mA
USB Device (+PLL)	5.6 (3.3)	mA
ACI	0.8	mA
USB Host	TBD	TBD
ADC/TSC	TBD	TBD
VIC	TBD	TBD
KMI	TBD	TBD
PWM (each)	TBD	TBD

SSP Waveforms

The Synchronous Serial Port (SSP) supports three data frame formats:

- Texas Instruments SSI
- Motorola SPI
- National Semiconductor MICROWIRE

Each frame format is between 4 and 16 bits in length, depending upon the programmed data size. Each data frame is transmitted beginning with the Most Significant Bit (MSB) i.e. 'big endian'. For all three formats, the SSP serial clock is held LOW (inactive) while the SSP is idle. The SSP serial clock transitions only during active transmission of data. The SSPFRM signal marks the beginning and end of a frame. The SSPEN signal controls an off-chip line driver's output enable pin.

Figure 14 and Figure 15 show Texas Instruments synchronous serial frame format, Figure 16 through Figure 23 show the Motorola SPI format, and Figure 24 and Figure 25 show National Semiconductor's MICROWIRE data frame format.

For Texas Instruments SSI format, the SSPFRM pin is pulsed prior to each frame's transmission for one serial clock period beginning at its rising edge. For this frame format, both the SSP and the external slave device drive their output data on the rising edge of the clock and latch data from the other device on the falling edge. See Figure 14 and Figure 15.

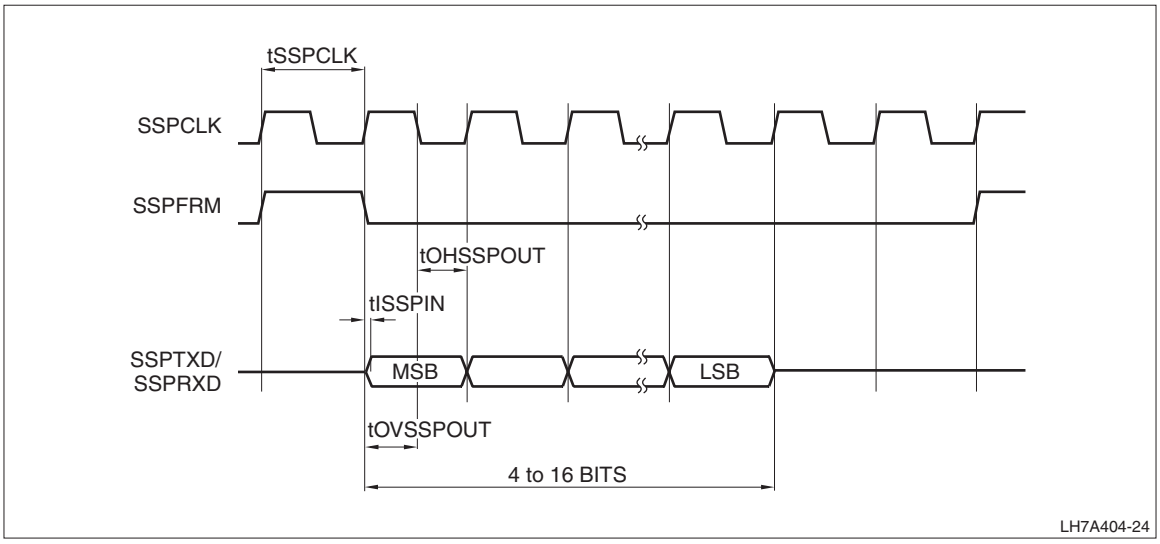


Figure 14. Texas Instruments Synchronous Serial Frame Format (Single Transfer)

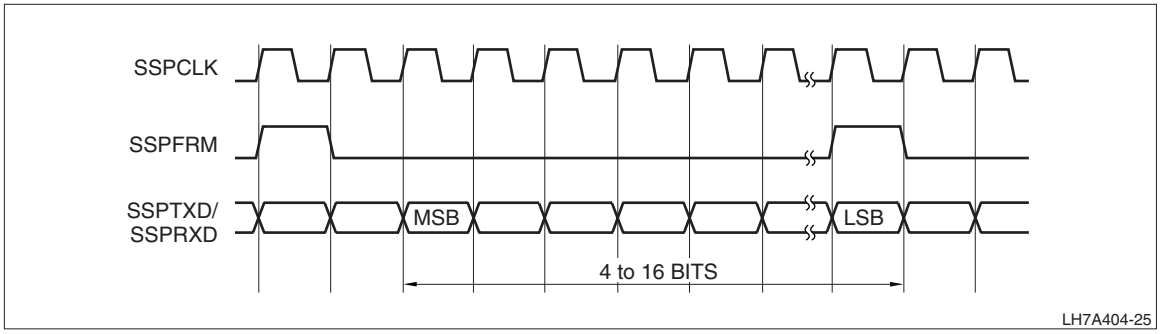


Figure 15. Texas Instruments Synchronous Serial Frame Format (Continuous Transfer)

For Motorola SPI, the serial frame pin (SSPFRM) is active LOW. The SPO and SPH bits in SSP Control Register 0 determine SSPCLK and SSPFRM operation in single and continuous modes. See Figures 16 through 23.

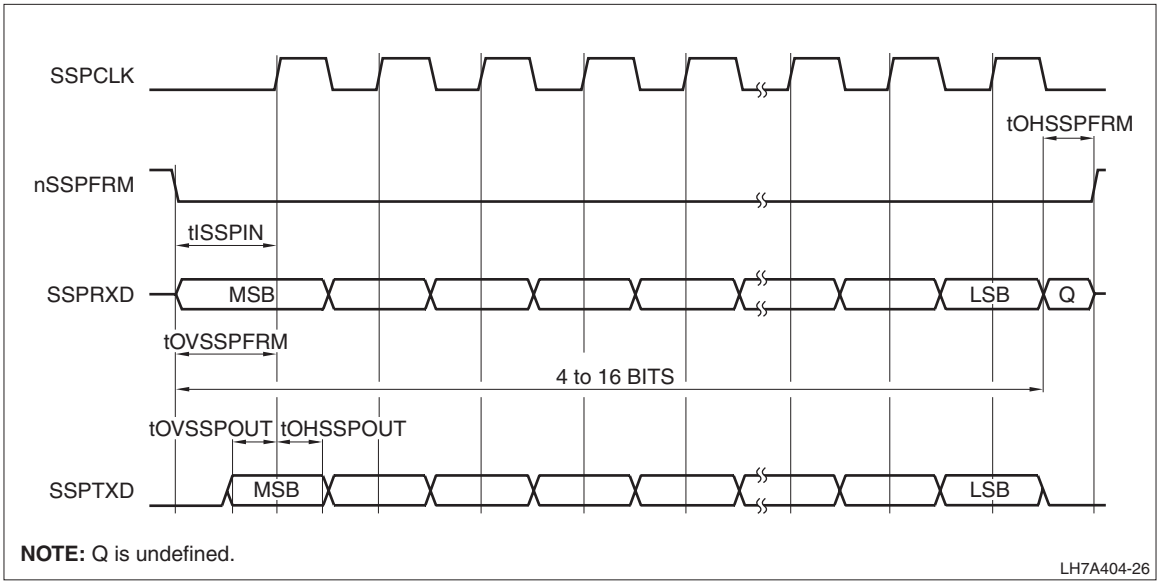


Figure 16. Motorola SPI Frame Format (Single Transfer) with SPO = 0 and SPH = 0

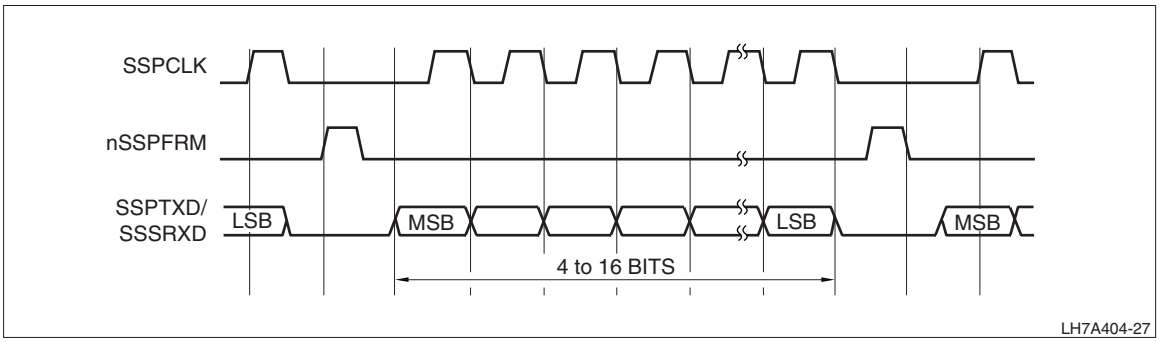


Figure 17. Motorola SPI Frame Format (Continuous Transfer) with SPO = 0 and SPH = 0

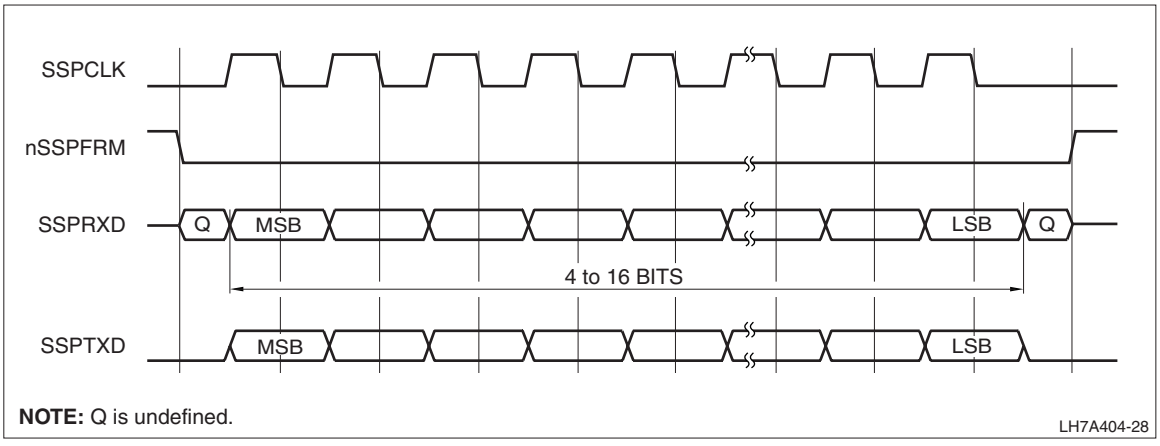


Figure 18. Motorola SPI Frame Format (Single Transfer) with SPO = 0 and SPH = 1

Clock and State Controller (CSC) Waveforms

Figure 33 shows the behavior of the LH7A404 when coming out of Reset or Power-On. Figure 34 shows external reset timing, and Table 12 gives the timing parameters.

Table 12. Reset AC Timing

PARAMETER	DESCRIPTION	MIN.	MAX.	UNIT
tOSC32 (32 kHz)	Oscillator stabilization time after Power Up (VDDC = VDDCMIN)		550	ms
tOSC14 (14 MHz)	Oscillator stabilization time after Power Up (VDDC = VDDCMIN)		2.5	ms
tPORH	nPOR Hold Time after tOSC32	0		ms
tPLLL	Phase locked loop lockup time		250	µs
tURESET/tPWRFL	nURESET/nPWRFL Pulse Width (once sampled LOW)	2		System Clock Cycles

NOTE: *VDDC = VDDCmin

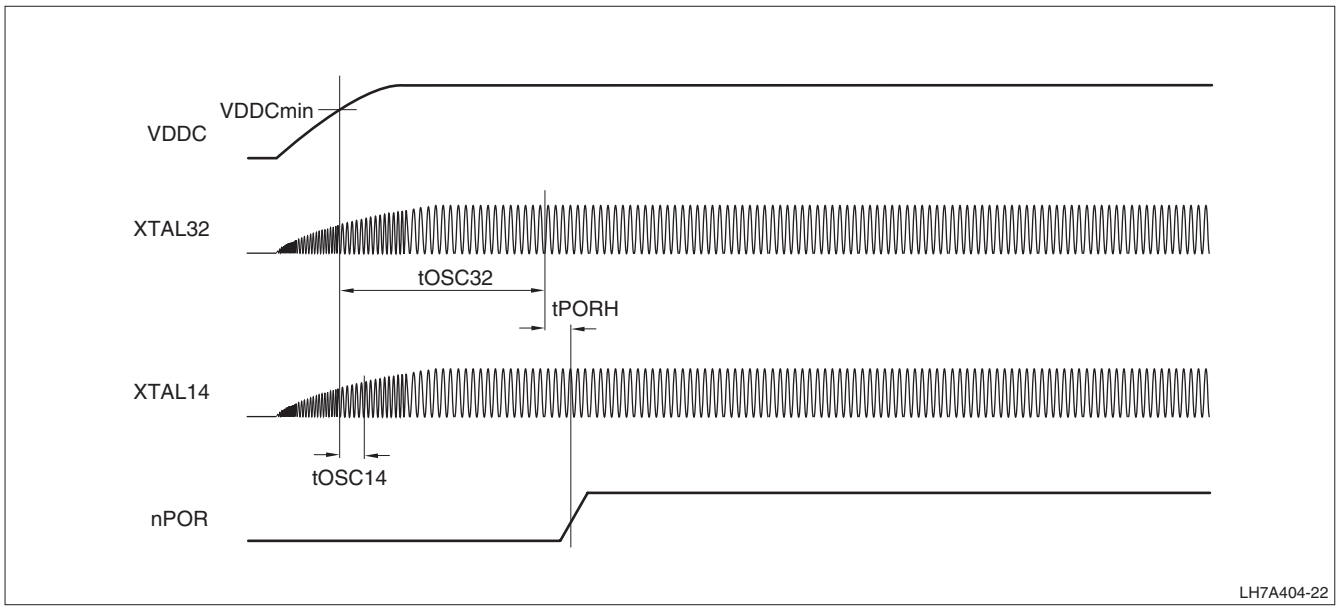


Figure 33. PLL Start-up

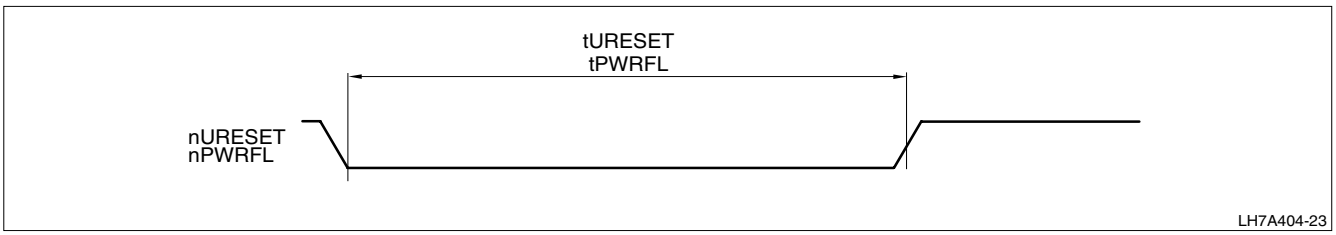
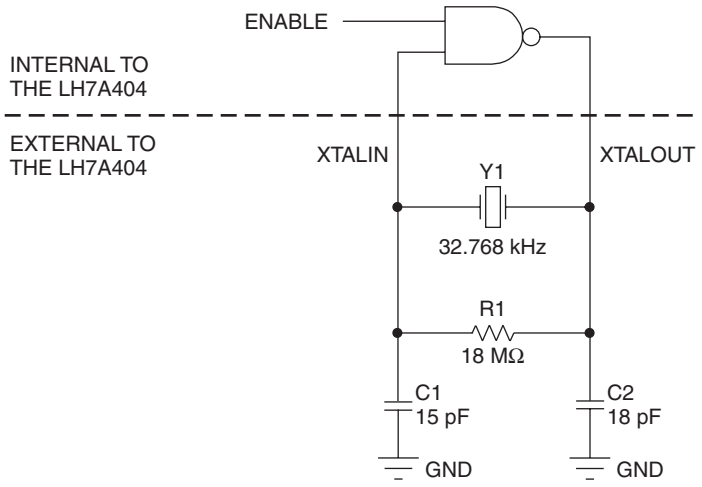


Figure 34. External Reset

Recommended Oscillator Circuit Design

Figure 35 and Figure 36 show the recommended oscillator design for both the 32.768 kHz and 14.7456 MHz clocks.



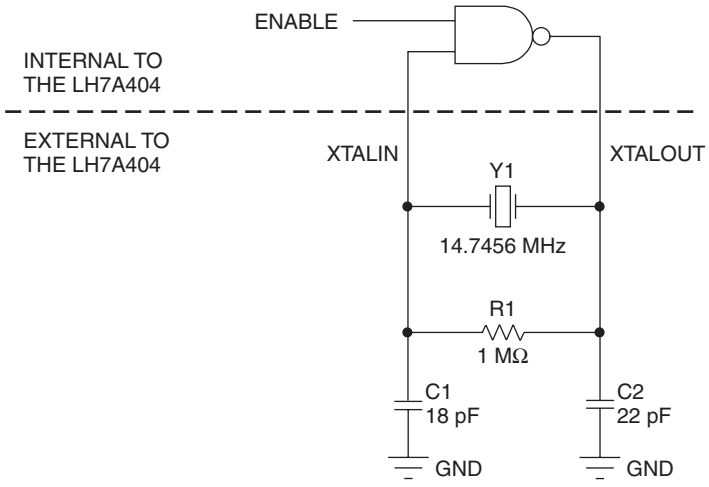
NOTES:
1. Y1 is a parallel-resonant type crystal. (See table)
2. The nominal values for C1 and C2 shown are for a crystal specified at 12.5 pF load capacitance (CL).
3. The values for C1 and C2 are dependent upon the cystal's specified load capacitance and PCB stray capacitance.
4. R1 must be in the circuit.
5. Ground connections should be short and return to the ground plane which is connected to the processor's core ground pins.
6. Tolerance for R1, C1, C2 is ≤ 5%.

RECOMMENDED CRYSTAL SPECIFICATIONS

PARAMETER	DESCRIPTION
32.768 kHz Crystal	Parallel Mode
Tolerance	±30 ppm
Aging	±3 ppm
Load Capacitance	12.5 pF
ESR (MAX.)	50 kΩ
Drive Level	1.0 µW (MAX.)
Recommended Part	MTRON SX1555 or equivalent

LH7A404-168

Figure 35. 32.768 kHz External Oscillator Components and Schematic



NOTES:
1. Y1 is a parallel-resonant type crystal. (See table)
2. The nominal values for C1 and C2 shown are for a crystal specified at 18 pF load capacitance (CL).
3. The values for C1 and C2 are dependent upon the cystal's specified load capacitance and PCB stray capacitance.
4. R1 must be in the circuit.
5. Ground connections should be short and return to the ground plane which is connected to the processor's core ground pins.
6. Tolerance for R1, C1, C2 is ≤ 5%.

RECOMMENDED CRYSTAL SPECIFICATIONS

PARAMETER	DESCRIPTION
14.7456 MHz Crystal	(AT-Cut) Parallel Mode
Tolerance	±50 ppm
Stability	±100 ppm
Aging	±5 ppm
Load Capacitance	18 pF
ESR (MAX.)	40 Ω
Drive Level	100 µW (MAX.)
Recommended Part	MTRON SX2050 or equivalent

LH7A404-167

Figure 36. 14.7456 MHz External Oscillator Components and Schematic

Table 13. Record of Revisions

DATE	PAGE NO.	PARAGRAPH OR ILLUSTRATION	SUMMARY OF CHANGES
4/1/04	1	Text	Clarified Industrial and Commercial temperature ranges; removed MMC/SD as a boot device.
	1, 30, 31	Text	Removed 1.8 VDC I/O capability (VDD).
	4	Table 1	Changed “BOOTWIDTH” to “WIDTH” for consistency.
	13	Table 3	Extensively revised to make more usable.
	14-16	Pin List	Minor corrections to Slew Rate and Output Drive on some cells.
	21	Table 5	Revised Boot Mode table to show various device possibilities.
		Table 6	External Boot Modes table Added.
	34	Table 7	Changed ‘MAXIMUM’ test conditions from maximum temperature to nominal temperature.
	36	Table 9	Changed Synchronous Memory Interface tISD to 2.5 ns.
	37	Table 9	Changed MMC timing reference to ‘MMC Clock Periods’; minor changes to several timing values; changed ADC resolution value.
	54	Text	Altered low pass filter description.
	Various	1.8 VDC Tolerance	Changed 1.8 VDC supply voltage to ±5%.
	Various	Text	Minor text editing for clarity.
6/10/04	4-12	Table 1	Minor editorial corrections.
	30	Power Sequencing	Paragraph added explaining sequencing of power supplies.
	53	Text	Added ground connection to drawing and removed the “Caution” box.
9/1/04	29	Note to Table	Clarified Note 1.
	55	Figure 37, Table 12	Temperature/Voltage/Speed chart and Table added.
1/14/05	ALL	Text	Rolled revision to Version 1.0.
	Various	Text	Cleaned up formatting.
	1	“5 V Tolerant” bullet	Added sub-bullet limiting voltage on the oscillator pins.
	31	DC Specifications	Added “Typ.” column and corrected values for IACTIVE, IHALT, ISTANDBY.
	31	Power Sequencing	Added text to allow power up sequencing longer than 100 µs if supplies remain within 1.5 V.
	36	Table 11	Changed Asynchronous Memory timing to match SRAM datasheet parameter naming conventions. Corrected Asynchronous Memory values for tOHCA, tOHRA, tOHSDW, tOHSC, and tOHD; added value for tOHA. Corrected PCMCIA D[31:0] timing values tISD and tIHD.
	38 - 41	Figure 8 - Figure 11	Revised drawings to match SRAM datasheet parameter naming conventions.

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