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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM9®
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	Audio Codec, EBI/EMI, IrDA, Memory Card, SmartCard, SSP, UART/USART, USB
Peripherals	AC'97, DMA, LCD, POR, PWM, WDT
Number of I/O	64
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	324-LFBGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/socle/lh7a404n0f000b2

Table 1. LH7A404 Functional Pin List

CABGA	SIGNAL	DESCRIPTION	RESET STATE	STANDBY STATE	OUTPUT DRIVE	I/O	NOTES
E10	VDD	I/O Ring Power					
E11							
H10							
H11							
K5							
K8							
K13							
K16							
L5							
L8							
L13							
L16							
N10							
N11							
T10							
T11							
U18							
J9	VSS	I/O Ring Ground					
J10							
J11							
J12							
K9							
K10							
K11							
K12							
L9							
L10							
L11							
L12							
M9							
M10							
M11							
M12							
T18							
E7	VDDC	Core Power					
E9							
E14							
G5							
G16							
P5							
P16							
T7							
T12							
T14							

Table 1. LH7A404 Functional Pin List (Cont'd)

CABGA	SIGNAL	DESCRIPTION	RESET STATE	STANDBY STATE	OUTPUT DRIVE	I/O	NOTES
E6	VSSC	Core Ground					
E15							
F5							
F16							
J16							
M5							
R5							
R16							
T6							
T15							
Y17	VDDA	Analog Power for PLL1 and PLL2					
W17							
V16	VSSA	Analog Ground for PLL1 and PLL2					
U15							
W16	VDDAD	Analog Power for A/D, Touch Screen Controller					
V13	VSSAD	Analog Ground for A/D, Touch Screen Controller					
D2	nPOR	Power on Reset	Input	Input		I	3
E1	nURESET	User Reset	Input	Input		I	3
F3	WAKEUP	Wake Up	Input	Input		I	3
F4	nPWRFL	Power Fail Signal	Input	Input		I	3
C1	nEXTPWR	External Power	Input	Input		I	3
C5	nRESETOUT	Reset Output to external devices. This pin carries the same state as the internal SoC reset signal.			12 mA		
Y18	XTALIN	14.7456 MHz Crystal Oscillator pins. To drive the device from an external clock source, XTALIN can be used while XTALOUT is left unconnected.					
Y19	XTALOUT						
T19	XTAL32IN	32.768 kHz Real Time Clock, Crystal Oscillator pins. To drive the device from an external clock source, XTAL32IN can be used while XTAL32OUT is left unconnected.					
T20	XTAL32OUT						
L2	PGMCLK	Programmable Clock (14.7456 MHz MAX.)	LOW	LOW	8 mA	O	
T16	CLKEN	External Oscillator Enable Output	LOW	LOW	8 mA	I/O	4
Y13	WIDTH0	Boot Width Pins. Used with the MEDCHG and INTBOOT bits for internal Boot ROM. On power up, the values on these pins are latched to determine the width and type of Boot device. Boot width can be 8-, 16-, or 32-bit. These pins have a weak internal pull-up resistor	Input with pull-up	Input with pull-up		I	3
W13	WIDTH1						
E4	MEDCHG	Media Change bit; used at power on with INTBOOT and WIDTHx pins to determine boot device.	Input	No Change		I	3
Y20	INTBOOT	When LOW, boot device is selected according to the MEDCHG bit. When HIGH, the lower 64KB addresses are mapped to the internal Boot ROM.	Input	No Change		I	

Table 1. LH7A404 Functional Pin List (Cont'd)

CABGA	SIGNAL	DESCRIPTION	RESET STATE	STANDBY STATE	OUTPUT DRIVE	I/O	NOTES
V1	PC7	GPIO Port C7	PC7: LOW	No Change	12 mA	I/O	
Y11	PD0/LCDVD8	• GPIO Port D[7:0] • LCD Video Data Interface	PDx: LOW	LOW if 8-bit LCD enabled; else No Change	12 mA	I/O	
U10	PD1/LCDVD9						
W12	PD2/LCDVD10						
V11	PD3/LCDVD11						
W11	PD4/LCDVD12						
U11	PD5/LCDVD13						
V12	PD6/LCDVD14						
Y12	PD7/LCDVD15						
Y9	PE0/LCDVD4	• GPIO Port E[3:0] • LCD Video Data Interface	PEx: Input	LOW if 8-bit LCD enabled; else No Change	12 mA	I/O	
W10	PE1/LCDVD5						
V10	PE2/LCDVD6						
T9	PE3/LCDVD7						
D4	PE4/ SCCLKIN	• GPIO Port E4 • Smart Card Push-Pull Mode Clock Input	PE4: Input	No Change	12 mA	I/O	
C3	PE5/ SCCLKEN	• GPIO Port E5 • Smart Card Push-Pull Mode External Clock Buffer Enable	PE5: Input	No Change	12 mA	I/O	
B2	PE6/ SCIN	• GPIO Port E6 • Smart Card Push-Pull Mode Data Input	PE6: Input	No Change	12 mA	I/O	
A1	PE7/ SCDATEN	• GPIO Port E7 • Smart Card Push-Pull Mode Data Out External Buffer Enable	PE7: Input	No Change	12 mA	I/O	
A9	PF0/ INT0	• GPIO Port F0 • Interrupt 0	PF0: Input	No Change	8 mA	I/O	3
D9	PF1/ INT1	• GPIO Port F1 • Interrupt 1	PF1: Input	No Change	8 mA	I/O	3
A8	PF2/ INT2	• GPIO Port F2 • Interrupt 2	PF2: Input	No Change	8 mA	I/O	3
C8	PF3/ INT3	• GPIO Port F3 • Interrupt 3	PF3: Input	No Change	8 mA	I/O	3
B8	PF4/ INT4	• GPIO Port F4 • Interrupt 4	PF4: Input	No Change	8 mA	I/O	3
D8	PF5/ INT5/ SCDETECT	• GPIO Port F5 • Interrupt 5 • Smart Card Interface Card Detect Signal	PF5: Input	No Change	8 mA	I/O	3
A7	PF6/ INT6/ PCRDY1	• GPIO Port F6 • Interrupt 6 • Ready for Card 1 for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode	PF6: Input	No Change	8 mA	I/O	3
E8	PF7/ INT7/ PCRDY2	• GPIO Port F7 • Interrupt 7 • Ready for Card 2 for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode	PF7: Input	No Change	8 mA	I/O	3
Y2	PG0/ nPCOE	• GPIO Port G0 • Output Enable for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode	LOW	No Change	8 mA	I/O	
W4	PG1/ nPCWE	• GPIO Port G1 • Write Enable for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode	LOW	No Change	8 mA	I/O	

Table 1. LH7A404 Functional Pin List (Cont'd)

CABGA	SIGNAL	DESCRIPTION	RESET STATE	STANDBY STATE	OUTPUT DRIVE	I/O	NOTES
U7	PH7/ nPCSTATRE	• GPIO Port H7 • Status Read Enable for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode	PHx: Input	No Change	8 mA	I/O	
T4	LCDFP/ LCDSPS	• LCD Frame Pulse • ALI Reset Row Driver Counter	LOW	LOW if not in ALI mode	12 mA	O	
V2	LCDLP/ LCDHRLP	• LCD Linepulse • ALI Latch Pulse	LOW	LOW if not in ALI mode	12 mA	O	
U3	LCDCLS	ALI Clock for Row Drivers	Input	No Change	12 mA	O	
V3	LCDSPL	ALI Start Pulse Left for reverse scanning	LOW	No Change	12 mA	O	
U4	LCDUBL	ALI Up, Down signal for reverse scanning	Input	No Change	12 mA	O	
W1	LCDSPR	ALI Start Pulse Right for normal scanning	Input	No Change	12 mA	O	
V4	LCDLBR	ALI Output for reverse scanning	HIGH	No Change	12 mA	O	
W2	LCDMOD	ALI MOD Signal used by the row driver	LOW	No Change	12 mA	O	
V5	LCDPS	ALI Power Save	HIGH	No Change	12 mA	O	
Y1	LCDVDDEN	ALI Power Sequence Control	LOW	No Change	12 mA	O	
W3	LCDREV	ALI Reverse	HIGH	No Change	12 mA	O	
U8	LCDCLKIN	External Clock Input for LCD controller	Input	No Change		I	
V8	LCDVD0	LCD Video Data Interface	LOW	LOW	12 mA	O	
T8	LCDVD1						
W9	LCDVD2						
Y8	LCDVD3						
V9	LCDENAB/ LCDM	• LCD TFT Data Enable • LCD STN AC Bias	LOW	LOW	12 mA	O	
Y10	LCDDCLK	LCD Pixel Clock	LOW	LOW	12 mA	O	
U17	USBDCP	USB Device Full Speed Pull-up Resistor Control	Input	Input	12 mA	I	
U20	USBDP	USB Device Data Positive (Differential Pair)	Input	Input	12 mA	I/O	
U19	USBDN	USB Device Data Negative (Differential Pair)	Input	Input	12 mA	I/O	
W19	USBHDP0	USB Data Host Positive 0 (Differential Pair)	Input	HIGH	12 mA	I/O	
W20	USBHDN0	USB Data Host Negative 0 (Differential Pair)	Input	LOW	12 mA	I/O	
V19	USBHDP1	USB Data Host Positive 1 (Differential Pair)	Input	Input	12 mA	I/O	
V20	USBHDN1	USB Data Host Negative 1 (Differential Pair)	Input	Input	12 mA	I/O	
T17	USBHPWR	USB Host Power	LOW	Input	12 mA	O	
V17	USBHOVRCURR	USB Host Overcurrent	Input	Input	12 mA	I	
D11	nPWME0	DC-DC Converter 0 PWM 0 Enable	Input	Input	8 mA	I/O	5
A10	nPWME1	DC-DC Converter 1 PWM 1 Enable	Input	Input	8 mA	I/O	5
C11	PWM0	DC-DC Converter 0 Output (Pulse Width Modulated)	Input	Input	8 mA	I/O	4
C10	PWM1	DC-DC Converter 1 Output (Pulse Width Modulated)	Input	Input	8 mA	I/O	4
B9	PWM2	PWM Output 2	Input	No Change	8 mA	O	
D10	PWM3	PWM Output 3	Input	No Change		O	
C9	PWMSYNC	PWM Synchronizing Input for PWM2	Input	No Change	8 mA	I	
C7	ACBITCLK	• Audio Codec (AC97) Clock • Audio Codec (ACI) Clock	Input	No Change	8 mA	I/O	
B7	ACOUT	• Audio Codec (AC97) Output • Audio Codec (ACI) Output	LOW	LOW	8 mA	O	
A6	ACSYNC	• Audio Codec (AC97) Synchronization • Audio Codec (ACI) Synchronization	LOW	LOW	8 mA	O	

Table 4. CABGA Numerical Pin List (Cont'd)

CABGA	SIGNAL	SLEW RATE	OUTPUT DRIVE
E11	VDD		
E12	SCIO	95 mV/ns	12 mA
E13	DQM1	95 mV/ns	12 mA
E14	VDDC		
E15	VSSC		
E16	nSCS3	95 mV/ns	12 mA
E17	A21	95 mV/ns	12 mA
E18	D20	95 mV/ns	12 mA
E19	D18	95 mV/ns	12 mA
E20	D17	95 mV/ns	12 mA
F1	UARTDCD2	110 mV/ns	8 mA
F2	UARTCTS2	110 mV/ns	8 mA
F3	WAKEUP		
F4	nPWRFL		
F5	VSSC		
F16	VSSC		
F17	A19	95 mV/ns	12 mA
F18	A17/SBANK1	95 mV/ns	12 mA
F19	D16	95 mV/ns	12 mA
F20	A14/SA12	95 mV/ns	12 mA
G1	UARTIRRX1	110 mV/ns	8 mA
G2	UARTDSR2	110 mV/ns	8 mA
G3	UARTIRTX1	110 mV/ns	8 mA
G4	UARTRX2	110 mV/ns	8 mA
G5	VDDC		
G16	VDDC		
G17	A18	95 mV/ns	12 mA
G18	A15/SA13	95 mV/ns	12 mA
G19	D14	95 mV/ns	12 mA
G20	D13	95 mV/ns	12 mA
H1	KMIDAT	95 mV/ns	12 mA
H2	UARTTX2	110 mV/ns	8 mA
H3	KMICLK	95 mV/ns	12 mA
H4	COL1	100 mV/ns	8 mA
H5	COL2	100 mV/ns	8 mA
H10	VDD		
H11	VDD		
H16	A16/SBANK0	95 mV/ns	12 mA
H17	D15	95 mV/ns	12 mA
H18	A13/SA11	95 mV/ns	12 mA
H19	D12	95 mV/ns	12 mA
H20	A11/SA9	95 mV/ns	12 mA
J1	COL3	100 mV/ns	8 mA
J2	COL0	100 mV/ns	8 mA
J3	COL4	100 mV/ns	8 mA

Table 4. CABGA Numerical Pin List (Cont'd)

CABGA	SIGNAL	SLEW RATE	OUTPUT DRIVE
J4	COL5	100 mV/ns	8 mA
J5	COL6	100 mV/ns	8 mA
J9	VSS		
J10	VSS		
J11	VSS		
J12	VSS		
J16	VSSC		
J17	A12/SA10	95 mV/ns	12 mA
J18	D11	95 mV/ns	12 mA
J19	D9	95 mV/ns	12 mA
J20	A10/SA8	95 mV/ns	12 mA
K1	TBUZ	110 mV/ns	8 mA
K2	COL7	100 mV/ns	8 mA
K3	SSPCLK	110 mV/ns	8 mA
K4	SSPFRM	110 mV/ns	8 mA
K5	VDD		
K8	VDD		
K9	VSS		
K10	VSS		
K11	VSS		
K12	VSS		
K13	VDD		
K16	VDD		
K17	D10	95 mV/ns	12 mA
K18	A7/SA5	95 mV/ns	12 mA
K19	A9/SA7	95 mV/ns	12 mA
K20	A8/SA6	95 mV/ns	12 mA
L1	SSPRX	110 mV/ns	8 mA
L2	PGMCLK	110 mV/ns	8 mA
L3	SSPTX	110 mV/ns	8 mA
L4	PA1/LCDVD17	110 mV/ns	8 mA
L5	VDD		
L8	VDD		
L9	VSS		
L10	VSS		
L11	VSS		
L12	VSS		
L13	VDD		
L16	VDD		
L17	D7	95 mV/ns	12 mA
L18	D6	95 mV/ns	12 mA
L19	D8	95 mV/ns	12 mA
L20	A5/SA3	95 mV/ns	12 mA
M1	PA4	110 mV/ns	8 mA
M2	PA0/LCDVD16	110 mV/ns	8 mA

Power Modes

The LH7A404 has three operational states: Run, Halt, and Standby. During Run all clocks are hardware enabled and the processor is clocked. In the Halt mode the device is functioning, but the processor clock is halted while it waits for an event such as a key press. Standby equates to the computer being switched 'off', i.e. no display (LCD disabled) and the main oscillator is shut down.

Reset Modes

Three external signals can generate resets to the LH7A404: nPOR (power on reset), nPWRFL (power failure) and nURESET (user reset). If any of these are active, a system reset is internally generated. An nPOR reset performs a full system reset. The nPWRFL and nURESET resets perform a full system reset except for the SDRAM refresh control, SDRAM Global Configuration, SDRAM Device Configuration, and the RTC peripheral registers. The SDRAM controller issues a self-refresh command to external SDRAM before the system enters an nPWRFL and nURESET reset. This allows the system to maintain its Real Time Clock and SDRAM contents. Upon release of Reset, the chip enters Standby mode. Once in the Run mode the PWRSR register can be interrogated to determine the nature of the reset and the trigger source, after which software can then take appropriate actions.

Data Paths

The data paths in the LH7A404 are:

- The AMBA AHB bus
- The AMBA APB bus
- The External Bus Interface
- The LCD AHB bus
- The DMA busses.

AMBA AHB BUS

The Advanced Microprocessor Bus Architecture AHB (AMBA AHB) is a high speed 32-bit-wide data bus. The AMBA AHB is for high-performance, high-clock-frequency system modules.

LH7A404 peripherals and memory with high bandwidth requirements are connected to the ARM922T processor and other bus masters using a multi-master AHB bus. These peripherals include the external memory interfaces, on-chip SRAM, LCD Controller (bus master), DMA Controller (bus master), and USB Host (bus master). Remaining peripherals reside on the lower bandwidth Advanced Peripheral Bus (APB), which is accessed from the AHB via the APB Bridge. The APB Bridge is the only master on the APB, and its operation is transparent to the user as it converts AHB accesses into slower APB accesses automatically.

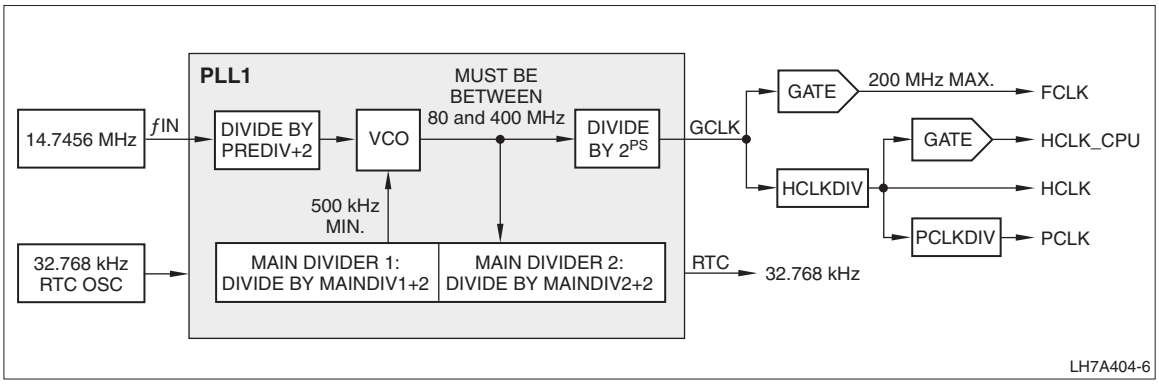


Figure 3. Clock and State Controller Block Diagram

SD/MMC INTERFACE DESCRIPTION

The SD/MMC controller uses the three-wire signal bus (clock, command, and data) to input and output data to and from the MMC, and to configure and acquire status information from the card. The SD controller differs in that it has four data lines instead of one.

The SD/MMC bus lines can be divided into three groups:

- Power supply: VSS1, VSS2, and VDD
- Data transfer group: MMCCMD, MMCDATA0, MMCDATA1, MMCDATA2, MMCDATA3 (for MMC, do not use MMCDATA1, MMCDATA2, MMCDATA3)
- Clock: MMCCLK

MMC CONTROLLER

The MMC controller implements MMC-specific functions, serves as the bus master for the MMC Bus and implements the standard interface to the MMC (card initialization, CRC generation and validation, command/response transactions, etc.).

Smart Card Interface (SCI)

The SCI (ISO7816) connects to an external Smart Card reader. The SCI can autonomously control data transfer to and from the Smart Card. Transmit and receive data FIFOs are provided to reduce the required interaction between the CPU core and the peripheral.

SCI FEATURES

- Supports asynchronous T0 and T1 transmission protocols
- Supports clock rate conversion factor F = 372, with bit rate adjustment factors of D = 1, 2, or 4
- Eight-character-deep buffered Tx and Rx paths
- Direct interrupts for Tx and Rx FIFO level monitoring
- Interrupt status register
- Hardware-initiated card deactivation sequence on detection of card removal
- Software-initiated card deactivation sequence on transaction complete
- Limited support for synchronous smart cards via registered input/output.

PROGRAMMABLE PARAMETERS

- Smart Card clock frequency
- Communication baud rate
- Protocol convention
- Card activation/deactivation time
- Maximum time for first character of Answer to Reset (ATR) reception checking
- Maximum ATR character stream duration checking
- Maximum time of receipt of first character of data stream checking
- Maximum time allowed between characters checking
- Character guard time
- Block guard time
- Transmit/receive character retry.

Direct Memory Access Controller (DMA)

The DMA Controller can be used to interface streams from 20 internal peripherals to the system memory using 10 fully-independent programmable channels which consist of five M2P (transmit) channels and five P2M (receive) channels.

The following peripherals may be allocated to the 10 channels:

- USB Device
- USB Host
- SD/MMC
- AC97
- UART1
- UART2
- UART3

Each of the above peripherals contain one Tx and one Rx channel, except the AC97, which contains three Tx and Rx channels. These peripherals also have their own bi-directional DMA bus, capable of simultaneously transferring data in both directions. All memory transfers take place via the main system AHB bus.

The DMA Controller can also be used to interface streams from memory-to-memory (M2M) or memory-to-external peripheral (M2P) using two dedicated M2M channels. External handshake signals are available to support memory-to-/from-external peripheral (M2P/P2M) transfers. A software trigger is available for M2M transfers only.

The DMA Controller features:

- Two dedicated channels for M2M and external M2P/P2M
- Ten fully independent, programmable DMA controller internal M2P/P2M channels (5 Tx and 5 Rx)
- Channels assignable to one of a number of different peripherals
- Independent source and destination address registers. Source and destination can be programmed to auto-increment or not auto-increment for M2M channels
- Two buffer descriptors per M2P and M2M channel to avoid potential data under/over-flow due to software introduced latency. A buffer refers to the area in system memory that is characterized by a buffer descriptor, i.e., a start address and the length of the buffer in bytes
- No AMBA wrapping bursts for DMA channels; only incrementing bursts are supported
- Buffer size independent of the peripheral's packet size for the internal M2P channels. Transfers can automatically switch between buffers
- Maskable interrupt generation
- Internal arbitration between DMA channels, plus support for an AHB bus arbiter
- DMA data transfer sizes, byte, word and quad-word data transfers are supported using a 16-byte data. Maximum data transfer size per M2M channel is programmable
- Per-channel clock gating reducing power in channels that have not been enabled by software. See the 'Clock and State Controller' section.

A set of control and status registers are available to the system processor for setting up DMA operations and monitoring their status. System interrupts are generated when any/all of the DMA channels wish to inform the processor to update the buffer descriptor. The DMA controller can service 10 out of 20 possible peripherals using the ten DMA channels, each with its own peripheral DMA bus capable of simultaneously transferring data in both directions.

The SD/MMC, UART[3:1], USB Device, and USB Host peripherals can each use two DMA channels, one for transmit and one for receive. The AC97 peripheral can use six DMA channels (three transmit and three receive) to allow different sample frequency data queues to be handled with low software overhead.

The DMA controller includes an M2M transfer feature allowing block moves of data from one memory address space to another with minimum of program effort and time. An M2M software trigger capability is provided. The DMA controller can also fill a block of memory with data from a single location.

The DMA controller's M2M channels can also be used in M2P/P2M mode. A set of external handshake signals, DREQ, DACK and TC/DEOT are provided for each of two M2M channels.

DREQ (input) can be programmed edge or level active, and active HIGH or LOW. The peripheral may hold DREQ active for the duration of the block transfers or may assert/deassert on each transfer.

DACK (output) can be programmed active HIGH or LOW. DACK will assert and return to de-asserted with each Read or Write, the timing coinciding with nOE or nWE from the EBI.

TC/DEOT is a bidirectional signal with programmable direction and active polarity. When configured as an Output, the DMA will assert Terminal Count (TC) on the final transfer to coincide with the DACK, typically when the byte count has expired. When configured as an Input, the peripheral must assert DEOT concurrent with DREQ for the final transfer in the block.

Transfer is terminated when DEOT is asserted by the external peripheral or when the byte count expires, whichever occurs first. Status bits indicate if the actual byte count is equal to the programmed limit, and if the count was terminated by peripheral asserting DEOT. Terminating the transfer causes a DMA interrupt on that channel and rollover to the 'other' buffer if so configured.

USB Device

The features of the USB are:

- Compliant with USB 2.0 Full Speed specification
- Provides a high-level interface that removes the USB protocol details from firmware
- Compatible with both OpenHCI and Intel UHCI standards
- Supports full-speed (12 Mbit/s) functions
- Supports Suspend and Resume signalling.

USB Host Controller

The features of the USB Host Controller are:

- Open Host Controller Interface Specification (OpenHCI) Rev. 1.0 Compliant
- Universal Serial Bus Specification 2.0 Full Speed compatible
- Supports Low Speed and High Speed USB devices
- Root Hub has two Downstream Ports
- DMA functionality.

Color LCD Controller

The LH7A404's LCD Controller is programmable to support up to 1,024 × 768, 16-bit color LCD panels. It interfaces directly to STN, color STN, TFT, AD-TFT, and HR-TFT panels. Unlike other LCD controllers, the LH7A404's LCD Controller saves an external timing ASIC by incorporating the timing conversion logic for thin LCD modules such as AD-TFT and HR-TFT.

The Color LCD Controller features support for:

- Up to 1,024 × 768 Resolution
- 16-bit Video Bus
- 16 bits-per-pixel (bpp) 5:5:5:1 or 5:6:5 direct color or on-chip color palette for 1, 2, 4, and 8 bpp resolution
- STN, Color STN, AD-TFT, HR-TFT, TFT panels
  - Single and Dual Scan STN panels
  - Up to 15 Gray Shades (mono STN)
  - Up to 3375 colors (color STN)
  - Up to 64 k-Colors
  - An on-chip SRAM frame buffer conserves bus bandwidth and saves active power.

AC97 Codec Controller

The AC97 Codec controller includes a 5-pin serial interface to an external audio codec. The AC97 link is a bi-directional, fixed rate, serial Pulse Code Modulated (PCM) digital stream, dividing each audio frame into 12 outgoing and 12 incoming data streams (slots), each with 20-bit resolution per sample.

The AC97 controller contains logic that controls the AC97 link to the audio codec and an interface to the AMBA APB.

Its main features include:

- Serial-to-parallel conversion for data received from the external codec
- Parallel-to-serial conversion for data transmitted to the external codec
- Reception/transmission of control and status information via the AMBA APB interface
- Support for up to 4 simultaneous codec sampling rates with its 4 transmit and 4 receive channels. The transmit and receive paths are buffered with internal FIFO memories, allowing data to be stored independently in both transmit and receive modes. Three of the outgoing FIFOs can be written via either the APB interface or with DMA channels 1-3.

Audio Codec Interface (ACI)

The ACI provides:

- A digital serial interface to an off-chip 8-bit codec
- All the necessary clocks and timing pulses to perform serialization or de-serialization of the data stream to, or from the codec device.

The interface supports full duplex operation and the transmit and receive paths are buffered with internal FIFO memories allowing up to 16 bytes to be stored independently in both transmit and receive modes.

The ACI includes a programmable frequency divider that generates a common transmit and receive bit clock output from the on-chip ACI clock input (ACBITCLK). Transmit data values are output synchronous with the rising edge of the bit clock output. Receive data values are sampled on the falling edge of the bit clock output. The start of a data frame is indicated by a synchronization output signal that is coincident with the bit clock.

Pulse Width Modulator (PWM)

The Pulse Width Modulator features:

- Configurable dual output
- Separate input clocks for each PWM output
- 16-bit resolution
- Programmable synchronous mode support allows external input to start PWM
- Programmable pulse width (duty cycle), interval (frequency), and polarity
  - Static programming: when the PWM is stopped
  - Dynamic programming: when the PWM is running
  - Updates duty cycle, frequency, and polarity at end of a PWM cycle

The PWM is a configurable dual-output, dual-clock-input AMBA slave module, and connects to the APB.

Synchronous Serial Port (SSP)

The SSP is a master-only interface for synchronous serial communication with peripheral devices that have either Motorola SPI, National Semiconductor MICROWIRE, or Texas Instruments Synchronous Serial Interfaces.

The SSP performs serial-to-parallel conversion on data received from a peripheral. The transmit and receive paths are buffered with internal FIFO memories allowing up to eight 16-bit values to be stored independently in both transmit and receive modes. Serial data is transmitted on SSPTXD and received on SSPRXD.

The LH7A404 SSP includes a programmable bit rate clock divider and prescaler to generate the serial output clock SCLK from the input clock SSPCLK. Bit rates are supported to 2 MHz and beyond, subject to choice of frequency for SSPCLK; the maximum bit rate will usually be determined by peripheral device's capability.

- Battery voltage sense in addition to normal direct voltage inputs
- A 9-channel multiplexer for routing user-selected inputs to A/D
- A 16 × 16 FIFO for 10-bit digital output of A/D
- A pen-down sensor to generate interrupts to the host
- Low-power circuitry and power control modes to minimize on-chip power dissipation
- Conversion automation for flexibility while minimizing CPU management and interrupt overhead
- A brownout detector with separate interrupt

Battery Monitor Interface (BMI)

The BMI is a serial communication interface specified for two types of battery monitors/gas gauges. The first type employs a single wire interface. The second interface employs a two-wire multi-master bus, implementing the Smart Battery System Specification. If both interfaces are enabled at the same time, the Single Wire Interface has priority.

SINGLE WIRE INTERFACE

The Single Wire Interface performs:

- Serial-to-parallel conversion on data received from the peripheral device
- Parallel-to-serial conversion on data transmitted to the peripheral device
- Data packet coding/decoding on data transfers (incorporating Start/Data/Stop data packets)

The Single Wire interface uses a command-based protocol in which the host initiates a data transfer by sending a WriteData/Command word to the battery monitor.

SMART BATTERY INTERFACE

The Smart Battery Interface performs:

- Serial-to-parallel conversion on data received from the peripheral device
- Parallel-to-serial conversion of data transmitted to the peripheral device.

The Smart Battery Interface uses a two-wire multi-master bus (the SMBus), allowing multiple bus masters to be connected to it. A master device initiates a bus transfer and provides the clock signals. A slave device can receive data provided by the master or it can provide data to the master. Since more than one device may attempt to take control of the bus as a master, SMBus provides an arbitration mechanism by relying on the wired-AND connection of all SMBus interfaces to the SMBus.

DC-to-DC Converter

The features of the DC-DC Converter interface are:

- Dual-drive PWM outputs with independent closed loop feedback
- Software programmable configuration of one of 8 output frequencies (each being a fixed division of the input clock).
- Software programmable configuration of duty cycle from 0 to 15/16, in intervals of 1/16.
- Hardware-configured output polarity (for positive or negative voltage generation) during power-on reset via the polarity select inputs
- Dynamically switched PWM outputs to one of a pair of preprogrammed frequency/duty cycle combinations via external pins.

Watchdog Timer (WDT)

The Watchdog Timer provides hardware protection against malfunctions. It is a programmable timer that is reset by software at regular intervals. Failure to reset the timer will cause an FIQ interrupt. Failure to service the FIQ interrupt generates a system reset.

Features of the WDT:

- Timing derived from the system clock
- 16 programmable time-out periods: 2^{16} through 2^{31} clock cycles
- Generates a system reset (resets LH7A404) or a FIQ interrupt whenever a time-out period is reached
- Software enable, lockout, and counter-reset mechanisms add security against inadvertent writes
- Protection mechanism guards against interrupt-service-failure:
  - The first WDT time-out triggers FIQ and asserts nWDFIQ status flag
  - If FIQ service routine fails to clear nWDFIQ, then the next WDT time-out triggers a system reset.

General Purpose I/O (GPIO)

The GPIO has eight ports, each with a data register and a data direction register. It also has added registers including Keyboard Scan, PINMUX, GPIO Interrupt Enable, INTYPE1/2, GPIOFEOI and PGHCON.

The data direction register determines whether a port is configured as an input or an output while the data register is used to read the value of the GPIO pins.

The GPIO Interrupt Enable, INTYPE[2:1], and the GPIOFEOI registers control edge-triggered Interrupts on Port F. The PINMUX register controls which signals are from Port D and Port E when they are set as outputs, while the PGHCON controls the operations of Port G and Port H.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

PARAMETER	MINIMUM	MAXIMUM
DC Core Supply Voltage (VDDC)	- 0.3 V	2.4 V
DC I/O Supply Voltage (VDD)	- 0.3 V	4.6 V
DC Analog Supply Voltage (VDDA)	- 0.3 V	2.4 V
DC Analog Supply Voltage (VDDAD)	- 0.3 V	4.6 V
Storage Temperature	-55°C	125°C

NOTE: These stress ratings are only for transient conditions. Operation at or beyond absolute maximum rating conditions may affect reliability and cause permanent damage to the device.

Recommended Operating Conditions

PARAMETER	MINIMUM	TYPICAL	MAXIMUM	NOTES
DC Core Supply Voltage (VDDC)	1.7 V	1.8 V	1.9 V	1
DC I/O Supply Voltage (VDD)	3.0 V	3.3 V	3.6 V	
DC Analog Supply Voltage (VDDA)	1.7 V	1.8 V	1.9 V	
DC A/D and TSC Supply Voltage (VDDAD)	3.0 V	3.3 V	3.6 V	
Clock Frequency (Commercial)	10 MHz		200 MHz	2, 3
Clock Frequency (Industrial)	10 MHz		195 MHz	2, 3
External Clock Input (XTALIN)	14 MHz	14.7456 MHz	20 MHz	4
Operating Temperature (Commercial)	0°C	25°C	70°C	
Operating Temperature (Industrial)	-40°C	25°C	+85°C	

NOTES:
1. Core Voltage should never exceed I/O Voltage after initial power up.
2. VDDC = 1.7 V to 1.9 V.
3. VDD = 3.0 V to 3.6 V.
4. Many peripherals operate improperly at clock speeds other than 14.7456 MHz. Some (such as USB) function only at 14.7456 MHz.

Table 7. Clock Frequency vs. Voltages (VDD) vs. Temperature

PARAMETER		1.7 V	1.8 V	1.9 V
25°C	Clock Frequency (FCLK)	213 MHz	227 MHz	253 MHz
	Clock Period (FCLK)	4.69 ns	4.41 ns	3.95 ns
70°C	Clock Frequency (FCLK)	205 MHz	220 MHz	232 MHz
	Clock Period (FCLK)	4.88 ns	4.46 ns	2.36 ns
85°C	Clock Frequency (FCLK)	200 MHz	212 MHz	236 MHz
	Clock Period (FCLK)	5.00 ns	4.72 ns	4.24 ns

NOTE: Table 7 is representative of a typical wafer process.
Guaranteed values are in the Recommended Operating Conditions table.

Table 11. AC Signal Characteristics

SIGNAL	TYPE	LOAD	SYMBOL	MIN.	MAX.	DESCRIPTION
ASYNCHRONOUS MEMORY INTERFACE SIGNALS (+ wait states × C)[1]						
A[27:0]	Output	50 pF	tRC	4C ns		Read Cycle Time
	Output	50 pF	tWC	4C ns		Write Cycle Time
	Output	50 pF	tAW	2C – 10 ns		Address Valid to Write Edge
	NA		None	1C ns	1C ns	Wait State Width
D[31:0]	Output	50 pF	tDW	1C – 9 ns		Data Valid to Write Edge
			tDH	1C + 3 ns		Data Hold after Write Edge
	Input		tAA	3C – 20 ns		Address Valid to Data Valid
			tOH	0 ns		Data Output Hold
nCS[3:0]/CS[7:6]	Output	30 pF	tCO	3C – 20 ns		Chip Select Valid to Data Valid (Read)
			tCW		1C – 10 ns	Chip Select Valid to Write edge
			tAS (Write)	1C ns		Address Valid to Chip Select Valid (Address setup time)
			tAS (Read)	0		Address Valid to Chip Select Valid (Address setup time)
nWE[3:0]	Output	30 pF	tWP	1C – 10 ns		Write Pulse Width
			tWHZ	0 ns		Write Edge to High Z on SRAM
nOE	Output	30 pF	tOE		2C – 20 ns	Output Enable Valid to Data Valid
			tOHZ	0 ns		Output Enable invalid to High Z on SRAM
SYNCHRONOUS MEMORY INTERFACE SIGNALS						
SA[13:0]	Output	50 pF	tOVA		7.5 ns	Address Valid
			tOHA	1.5 ns		Address Hold
A[17:16]/SB[1:0]	Output	50 pF	tOVB		7.5 ns	Bank Select Valid
D[31:0]	Output	50 pF	tOVD	2 ns	7.5 ns	Data Valid
	Input		tISD	2.5 ns		Data Setup
			tIHD	1.5 ns		Data Hold
nCAS	Output	30 pF	tOVCA	2 ns	7.5 ns	CAS Valid
			tOHCA	2 ns		CAS Hold
nRAS	Output	30 pF	tOVRA	2 ns	7.5 ns	RAS Valid
			tOHRA	2 ns		RAS Hold
nSWE	Output	30 pF	tOVSDW	2 ns	7.5 ns	Write Enable Valid
			tOHSDW	2 ns		Write Enable Hold
SCKE[1:0]	Output	30 pF	tOVC0	2 ns	7.5 ns	Clock Enable Valid
DQM[3:0]	Output	30 pF	tOVDQ	2 ns	7.5 ns	Data Mask Valid
nSCS[3:0]	Output	30 pF	tOVSC	2 ns	7.5 ns	Synchronous Chip Select Valid
			tOHSC	2 ns		Synchronous Chip Select Hold
PCMCIA INTERFACE SIGNALS (+ wait states × C)[1]						
nPCREG	Output	30 pF	tOVDREG		1C + 5 ns	nREG Valid
			tOHDREG	4C – 5 ns		nREG Hold
D[31:0]	Output	50 pF	tOVD		1C + 5 ns	Data Valid
			tOHD	4C – 12 ns		Data Hold
	Input		tISD		1C - 10 ns	Data Setup Time
			tIHD	4C – 5 ns		Data Hold Time
nPCCE1	Output	30 pF	tOVCE1		1C + 5 ns	Chip Enable 1 Valid
			tOHCE1	4C – 5 ns		Chip Enable 1 Hold
nPCCE2	Output	30 pF	tOVCE2		1C + 5 ns	Chip Enable 2 Valid
			tOHCE2	4C – 5 ns		Chip Enable 2 Hold

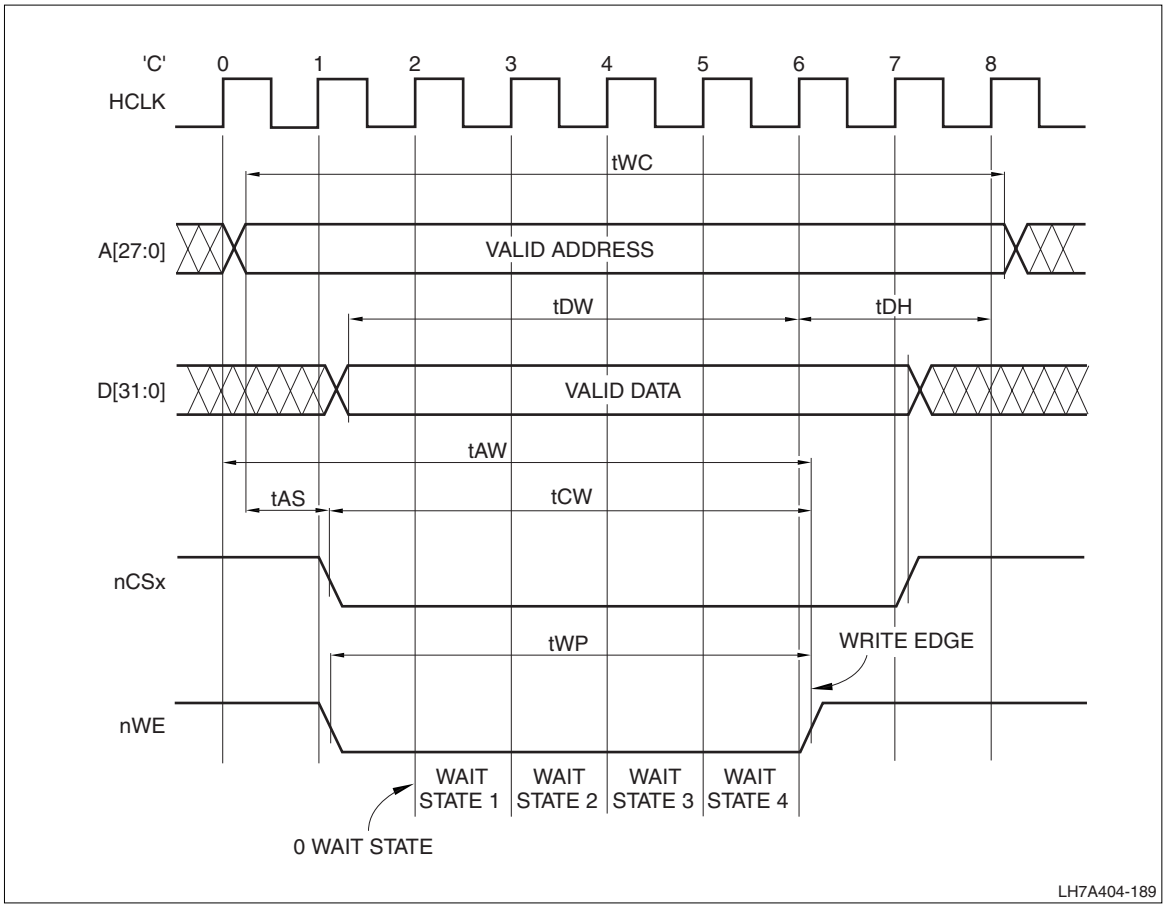


Figure 9. External Asynchronous Memory Write, Four Wait States (BCRx:WST1 = 0b100)

SSP Waveforms

The Synchronous Serial Port (SSP) supports three data frame formats:

- Texas Instruments SSI
- Motorola SPI
- National Semiconductor MICROWIRE

Each frame format is between 4 and 16 bits in length, depending upon the programmed data size. Each data frame is transmitted beginning with the Most Significant Bit (MSB) i.e. 'big endian'. For all three formats, the SSP serial clock is held LOW (inactive) while the SSP is idle. The SSP serial clock transitions only during active transmission of data. The SSPFRM signal marks the beginning and end of a frame. The SSPEN signal controls an off-chip line driver's output enable pin.

Figure 14 and Figure 15 show Texas Instruments synchronous serial frame format, Figure 16 through Figure 23 show the Motorola SPI format, and Figure 24 and Figure 25 show National Semiconductor's MICROWIRE data frame format.

For Texas Instruments SSI format, the SSPFRM pin is pulsed prior to each frame's transmission for one serial clock period beginning at its rising edge. For this frame format, both the SSP and the external slave device drive their output data on the rising edge of the clock and latch data from the other device on the falling edge. See Figure 14 and Figure 15.

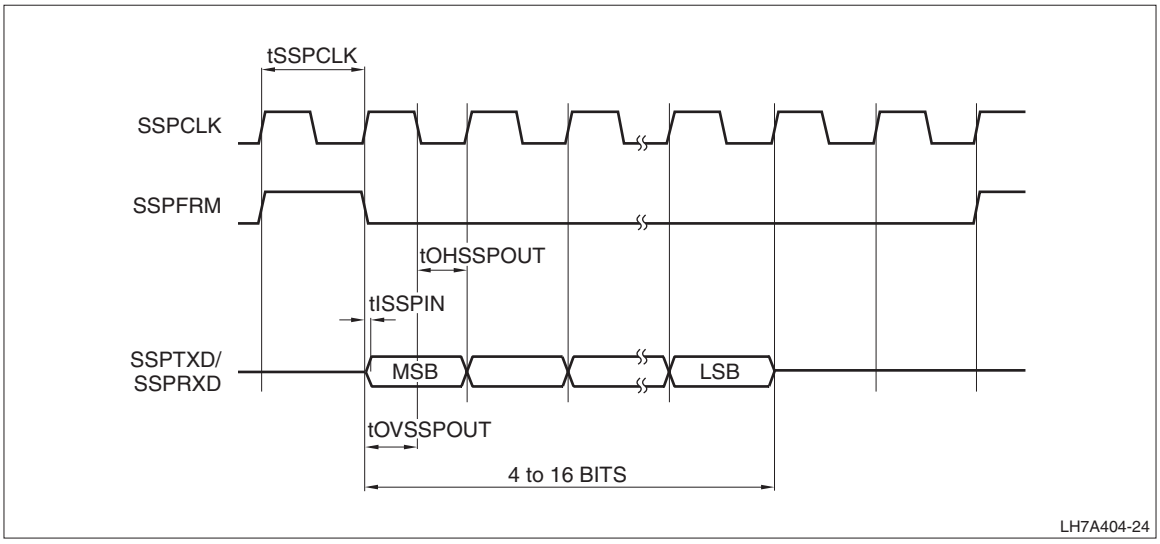


Figure 14. Texas Instruments Synchronous Serial Frame Format (Single Transfer)

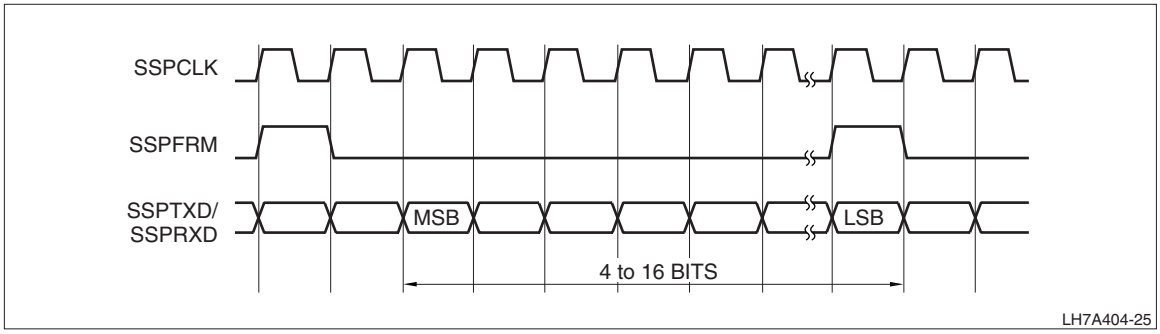
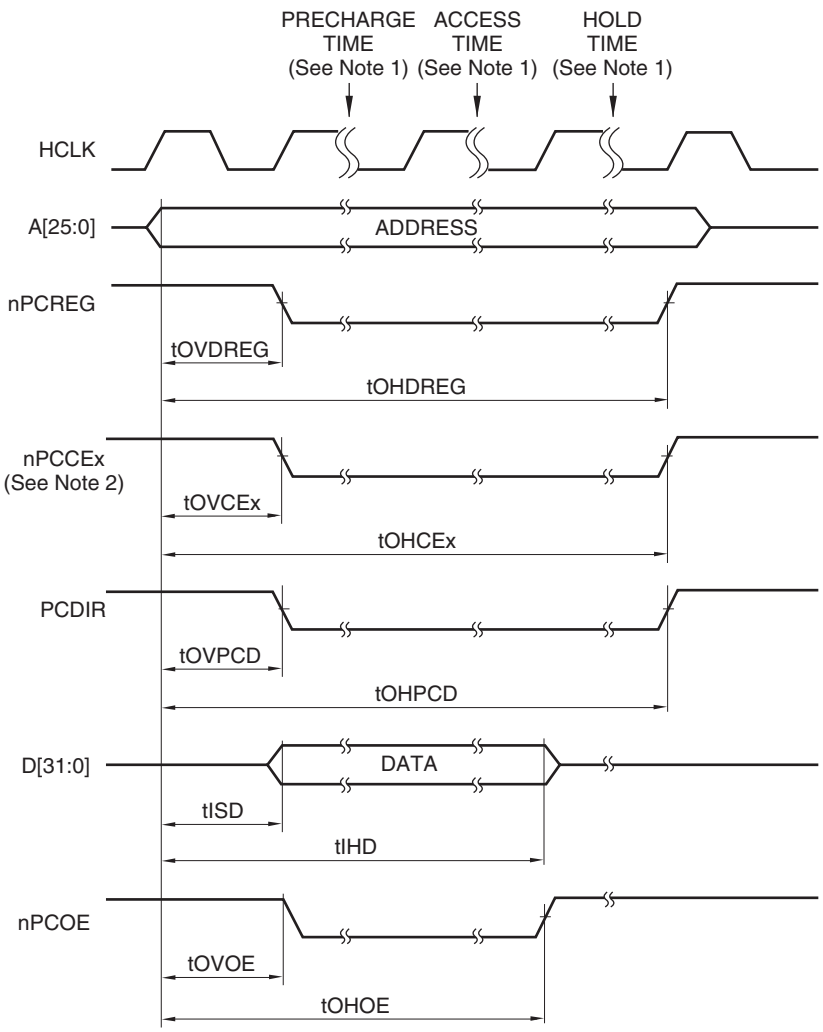


Figure 15. Texas Instruments Synchronous Serial Frame Format (Continuous Transfer)

PC Card (PCMCIA) Waveforms

Figure 26 shows the waveforms for PCMCIA Read transactions and Figure 27 shows the waveforms and timing for Write transactions.



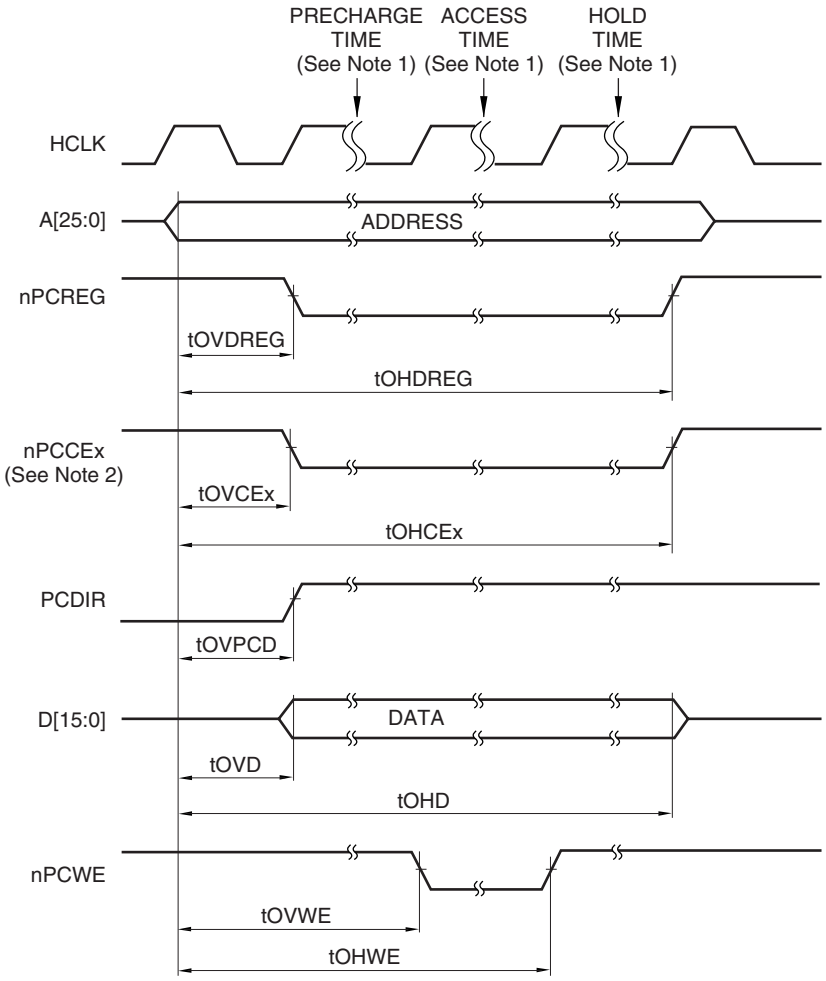
NOTES:

1. Precharge time, access time, and hold time are programmable wait-state times.
2.

nPCCE1	nPCCE2	TRANSFER TYPE
0	0	Common Memory
0	1	Attribute Memory
1	0	I/O
1	1	None

LH7A404-15

Figure 26. PCMCIA Read Transfer



NOTES:

1. Precharge time, access time, and hold time are programmable wait-state times.
2.

nPCCE1	nPCCE2	TRANSFER TYPE
0	0	Common Memory
0	1	Attribute Memory
1	0	I/O
1	1	None

LH7A404-16

Figure 27. PCMCIA Write Transfer

Clock and State Controller (CSC) Waveforms

Figure 33 shows the behavior of the LH7A404 when coming out of Reset or Power-On. Figure 34 shows external reset timing, and Table 12 gives the timing parameters.

Table 12. Reset AC Timing

PARAMETER	DESCRIPTION	MIN.	MAX.	UNIT
tOSC32 (32 kHz)	Oscillator stabilization time after Power Up (VDDC = VDDCMIN)		550	ms
tOSC14 (14 MHz)	Oscillator stabilization time after Power Up (VDDC = VDDCMIN)		2.5	ms
tPORH	nPOR Hold Time after tOSC32	0		ms
tPLLL	Phase locked loop lockup time		250	µs
tURESET/tPWRFL	nURESET/nPWRFL Pulse Width (once sampled LOW)	2		System Clock Cycles

NOTE: *VDDC = VDDCmin

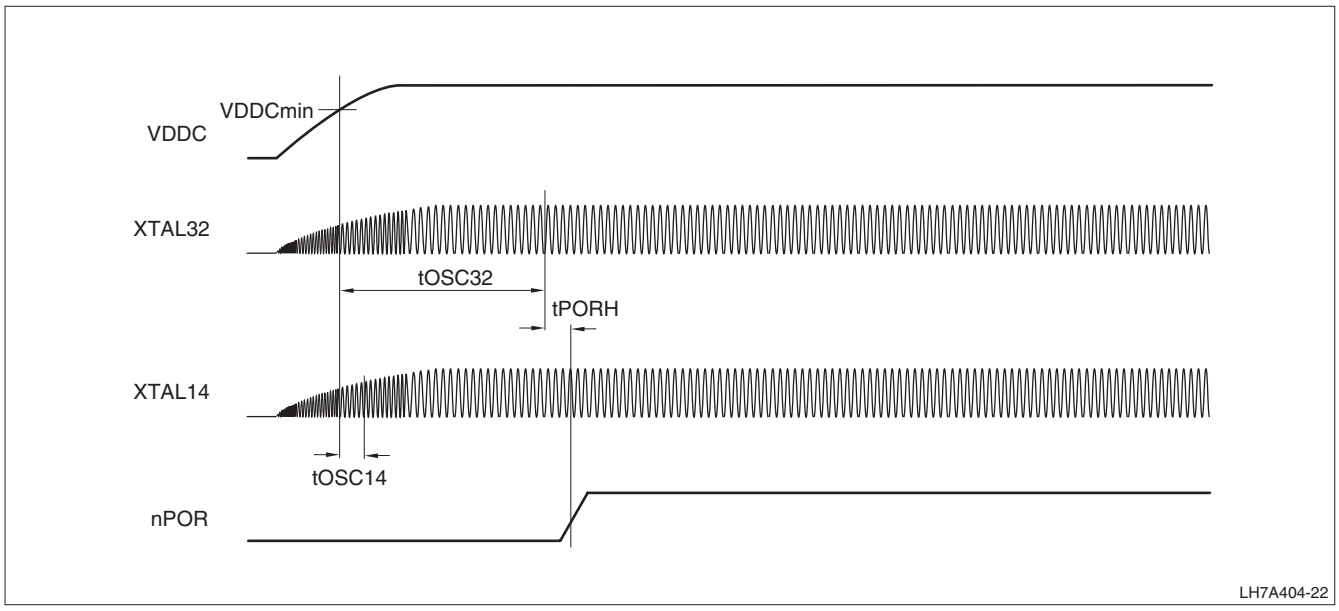


Figure 33. PLL Start-up

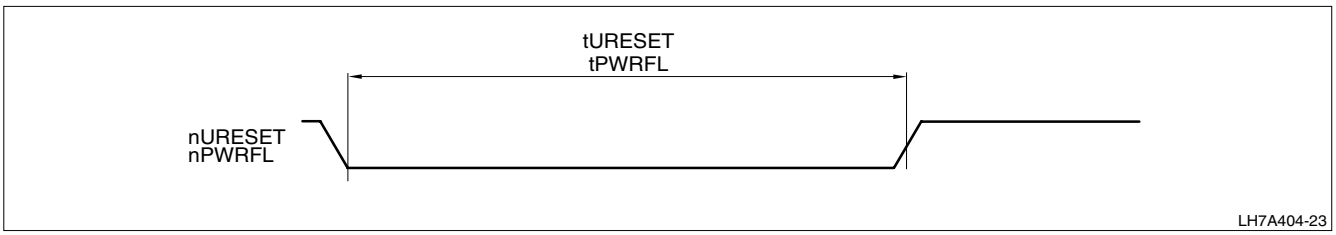
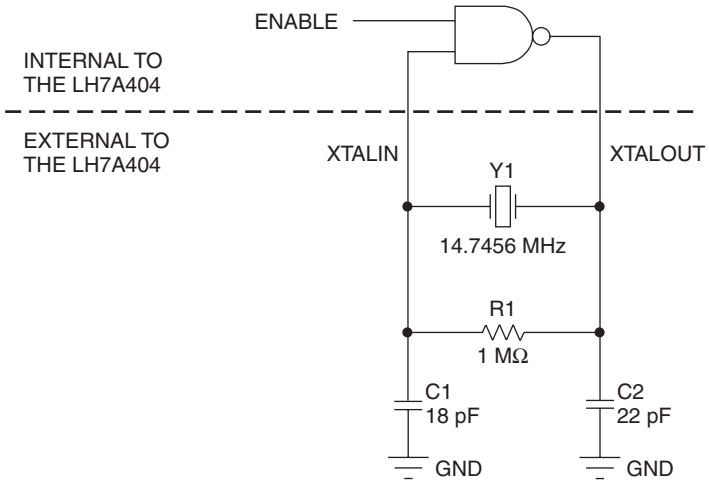


Figure 34. External Reset



NOTES:
1. Y1 is a parallel-resonant type crystal. (See table)
2. The nominal values for C1 and C2 shown are for a crystal specified at 18 pF load capacitance (CL).
3. The values for C1 and C2 are dependent upon the cystal's specified load capacitance and PCB stray capacitance.
4. R1 must be in the circuit.
5. Ground connections should be short and return to the ground plane which is connected to the processor's core ground pins.
6. Tolerance for R1, C1, C2 is ≤ 5%.

RECOMMENDED CRYSTAL SPECIFICATIONS

PARAMETER	DESCRIPTION
14.7456 MHz Crystal	(AT-Cut) Parallel Mode
Tolerance	±50 ppm
Stability	±100 ppm
Aging	±5 ppm
Load Capacitance	18 pF
ESR (MAX.)	40 Ω
Drive Level	100 µW (MAX.)
Recommended Part	MTRON SX2050 or equivalent

LH7A404-167

Figure 36. 14.7456 MHz External Oscillator Components and Schematic

CONTENT REVISIONS

This document contains the following changes to content, causing it to differ from previous versions.

Table 13. Record of Revisions

DATE	PAGE NO.	PARAGRAPH OR ILLUSTRATION	SUMMARY OF CHANGES
9/16/03	3-20	Tables 1, 4, 5	Added CABGA pinout, CABGA numerical pin listing, PBGA numerical pin list.
	52	Figure 30	Added ACI timing diagram.
	54-56	Figure 33, 34	Added oscillator example circuits and text.
	57	Figure 36	Added CABGA package diagram.
11/15/03	1	Text	Corrected minor text errors; added separate Commercial and Industrial temperature specification.
	2	Figure 1	Corrected name of ALI.
	3-12	Table 1	Added “Notes” column and notes 4, 5, and 6.
	12-18	Tables 3-14	Added tables to define pins by peripheral device.
	26, 27, 30, 38	Text	Minor corrections made to wording in text.
	33	“Recommended Operating Conditions”	Broke out “Commercial” and “Industrial” speed ranges.
	39	Table 20	Corrected nWE signal name; added tOHWECS; added ACI timing; changed note to number 1.
	41	Figure 8	Added text; corrected nWE signal name; added tOHWECS.
	53	Figure 30, 31	Added ACI timing.
2/10/04	1	Standby current; misc. text	Corrected value for Standby current; corrected copyright notice; reference to PBGA package removed.
	4, 6-12	Table 1	Minor wording revisions.
	13	Table 3	Corrected LCDVDx pin numbers.
	15	Table 7	Minor text revisions.
	16	Table 10	Minor text revision.
	23, 24, 26-32	Text	Minor text revisions.
	33	“Recommended Operating Conditions”	Removed unused “Note”.
	34	DC Specifications	Added IIN with pullup resistors; corrected values for Active and Standby current.
	35	Table 17	Corrected values for DNL Max. and Offset Error; removed “MAX.” values for Standby and Stop Current.
	37	Table 18	Corrected value for ICORE.
	39-40	Table 20	Corrected the following values: SRAM tOHD; PCMCIA tOVx and tOHD; MMC tOVx and tOHx; AC97 tOVx, tOHx, and tISAC97; SSP tOVx, tOHx, and removed tISSPFRM. Changed reference on MMC and AC97 to their respective domain clocks instead of absolute values.
	41, 45, 46, 53, 57	Text	Minor text revisions.
	45-46	Figures 13 and 15	Removed tISSPFRM from timing diagrams.

Table 13. Record of Revisions

DATE	PAGE NO.	PARAGRAPH OR ILLUSTRATION	SUMMARY OF CHANGES
4/1/04	1	Text	Clarified Industrial and Commercial temperature ranges; removed MMC/SD as a boot device.
	1, 30, 31	Text	Removed 1.8 VDC I/O capability (VDD).
	4	Table 1	Changed “BOOTWIDTH” to “WIDTH” for consistency.
	13	Table 3	Extensively revised to make more usable.
	14-16	Pin List	Minor corrections to Slew Rate and Output Drive on some cells.
	21	Table 5	Revised Boot Mode table to show various device possibilities.
		Table 6	External Boot Modes table Added.
	34	Table 7	Changed ‘MAXIMUM’ test conditions from maximum temperature to nominal temperature.
	36	Table 9	Changed Synchronous Memory Interface tISD to 2.5 ns.
	37	Table 9	Changed MMC timing reference to ‘MMC Clock Periods’; minor changes to several timing values; changed ADC resolution value.
	54	Text	Altered low pass filter description.
	Various	1.8 VDC Tolerance	Changed 1.8 VDC supply voltage to ±5%.
	Various	Text	Minor text editing for clarity.
6/10/04	4-12	Table 1	Minor editorial corrections.
	30	Power Sequencing	Paragraph added explaining sequencing of power supplies.
	53	Text	Added ground connection to drawing and removed the “Caution” box.
9/1/04	29	Note to Table	Clarified Note 1.
	55	Figure 37, Table 12	Temperature/Voltage/Speed chart and Table added.
1/14/05	ALL	Text	Rolled revision to Version 1.0.
	Various	Text	Cleaned up formatting.
	1	“5 V Tolerant” bullet	Added sub-bullet limiting voltage on the oscillator pins.
	31	DC Specifications	Added “Typ.” column and corrected values for IACTIVE, IHALT, ISTANDBY.
	31	Power Sequencing	Added text to allow power up sequencing longer than 100 µs if supplies remain within 1.5 V.
	36	Table 11	Changed Asynchronous Memory timing to match SRAM datasheet parameter naming conventions. Corrected Asynchronous Memory values for tOHCA, tOHRA, tOHSDW, tOHSC, and tOHD; added value for tOHA. Corrected PCMCIA D[31:0] timing values tISD and tIHD.
	38 - 41	Figure 8 - Figure 11	Revised drawings to match SRAM datasheet parameter naming conventions.