3. Package and Pinout

3.1 AVR32AP7001

Figure 3-1. 208 QFP Pinout.

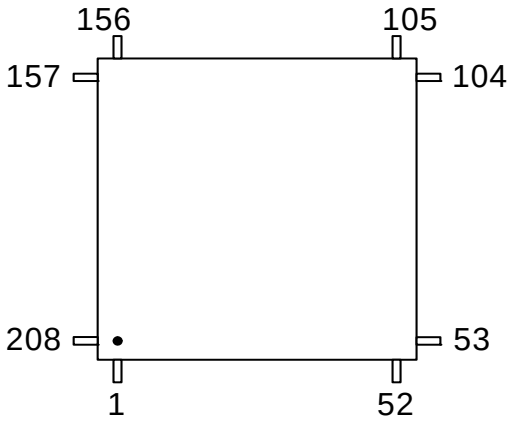

Table 3-1. QFP-208 Package Pinout

1	GND		53	GND		105	GND		157	GND
2	PE17		54	PA23		106	PX13		158	PB10
3	PE18		55	PA24		107	PX14		159	PB11
4	PX47		56	XIN1		108	PX15		160	PB12
5	PX48		57	XOUT1		109	PX16		161	PB13
6	PX49		58	AVDDUSB		110	PX17		162	PB14
7	PX50		59	AGNDUSB		111	PX34		163	PB15
8	PX51		60	VDDIO		112	PX35		164	PB16
9	VDDIO		61	FSDM		113	PX36		165	PB17
10	PX32		62	FSDP		114	PX37		166	PB18
11	PX33		63	GND		115	PX38		167	PB19
12	PX00		64	GND		116	PX18		168	PB20
13	PX01		65	HSDM		117	PX19		169	PB21
14	PX02		66	HSDP		118	PX20		170	PB22
15	PX03		67	VDDCORE		119	PX21		171	PB23
16	PX04		68	GND		120	PX22		172	VDDCORE
17	PX05		69	GND		121	PX23		173	GND
18	VDDCORE		70	VBG		122	PX24		174	GND
19	GND		71	VDDIO		123	PX25		175	PA06
20	TDO		72	PA25		124	PX26		176	PA07
21	TCK		73	PA26		125	VDDIO		177	VDDIO

8.4 Clock Connections

8.4.1 Timer/Counters

Each Timer/Counter channel can independently select an internal or external clock source for its counter:

Table 8-4. Timer/Counter clock connections

Timer/Counter	Source	Name	Connection
0	Internal	TIMER_CLOCK1	clk_osc32
		TIMER_CLOCK2	clk_pbb / 4
		TIMER_CLOCK3	clk_pbb / 8
		TIMER_CLOCK4	clk_pbb / 16
		TIMER_CLOCK5	clk_pbb / 32
	External	XC0	See Section 8.7
		XC1	
		XC2	
1	Internal	TIMER_CLOCK1	clk_osc32
		TIMER_CLOCK2	clk_pbb / 4
		TIMER_CLOCK3	clk_pbb / 8
		TIMER_CLOCK4	clk_pbb / 16
		TIMER_CLOCK5	clk_pbb / 32
	External	XC0	See Section 8.7
		XC1	
		XC2	

8.4.2 USARTs

Each USART can be connected to an internally divided clock:

Table 8-5. USART clock connections

USART	Source	Name	Connection
0	Internal	CLK_DIV	clk_pba / 8
1			
2			
3			

Table 8-9. PIO Controller A Multiplexing

76	PA29	PWM - PWM[1]	TC1 - B2
77	PA30	PM - GCLK[0]	TC1 - CLK1
78	PA31	PM - GCLK[1]	TC1 - CLK2

8.7.2 PIO Controller B Multiplexing

Table 8-10. PIO Controller B Multiplexing

QFP208	I/O Line	Peripheral A	Peripheral B
144	PB00	ISI - DATA[0]	SPI1 - MISO
145	PB01	ISI - DATA[1]	SPI1 - MOSI
146	PB02	ISI - DATA[2]	SPI1 - NPCS[0]
147	PB03	ISI - DATA[3]	SPI1 - NPCS[1]
148	PB04	ISI - DATA[4]	SPI1 - NPCS[2]
149	PB05	ISI - DATA[5]	SPI1 - SCK
150	PB06	ISI - DATA[6]	MCI - CMD[1]
151	PB07	ISI - DATA[7]	MCI - DATA[4]
152	PB08	ISI - HSYNC	MCI - DATA[5]
153	PB09	ISI - VSYNC	MCI - DATA[6]
158	PB10	ISI - PCLK	MCI - DATA[7]
159	PB11	PSIF - CLOCK[1]	ISI - DATA[8]
160	PB12	PSIF - DATA[1]	ISI - DATA[9]
161	PB13	SSC2 - TX_DATA	ISI - DATA[10]
162	PB14	SSC2 - RX_DATA	ISI - DATA[11]
163	PB15	SSC2 - TX_CLOCK	USART3 - CTS
164	PB16	SSC2 - TX_FRAME_SYNC	USART3 - RTS
165	PB17	SSC2 - RX_FRAME_SYNC	USART3 - TXD
166	PB18	SSC2 - RX_CLOCK	USART3 - RXD
167	PB19	PM - GCLK[2]	USART3 - CLK
168	PB20	ABDAC - DATA[1]	AC97C - SDO
169	PB21	ABDAC - DATA[0]	AC97C - SYNC
170	PB22	ABDAC - DATAN[1]	AC97C - SCLK
171	PB23	ABDAC - DATAN[0]	AC97C - SDI
33	PB24	NMI_N	DMACA - DMARQ[0]
34	PB25	EXTINT0	DMACA - DMARQ[1]
80	PB26	EXTINT1	USART2 - RXD
81	PB27	EXTINT2	USART2 - TXD
82	PB28	EXTINT3	USART2 - CLK
100	PB29	PM - GCLK[3]	USART2 - CTS
101	PB30	PM - GCLK[4]	USART2 - RTS

Table 8-12. IO Pins without multiplexing (Continued)

PX32	EBI - ADDR[16]
PX33	EBI - ADDR[17]
PX34	EBI - ADDR[18]
PX35	EBI - ADDR[19]
PX36	EBI - ADDR[20]
PX37	EBI - ADDR[21]
PX38	EBI - ADDR[22]
PX39	EBI - NCS[0]
PX40	EBI - NCS[1]
PX41	EBI - NCS[3]
PX42	EBI - NRD
PX43	EBI - NWE0
PX44	EBI - NWE1
PX45	EBI - NWE3
PX46	EBI - SDCK
PX47	EBI - SDCKE
PX48	EBI - RAS
PX49	EBI - CAS
PX50	EBI - SDWE
PX51	EBI - SDA10
PX52	EBI - NANDOE
PX53	EBI - NANDWE

8.8 Peripheral overview

8.8.1 External Bus Interface

- Optimized for Application Memory Space support
- Integrates Three External Memory Controllers:
  - Static Memory Controller
  - SDRAM Controller
  - ECC Controller
- Additional Logic for NAND Flash/SmartMedia™ and CompactFlash™ Support
  - SmartMedia support: 8-bit as well as 16-bit devices are supported
  - CompactFlash support: all modes (Attribute Memory, Common Memory, I/O, True IDE) are supported but the signals _IOIS16 (I/O and True IDE modes) and _ATA SEL (True IDE mode) are not handled.
- Optimized External Bus:
  - 16- or 32-bit Data Bus
  - Up to 26-bit Address Bus, Up to 64-Mbytes Addressable
  - Optimized pin multiplexing to reduce latencies on External Memories
- Up to 6 Chip Selects, Configurable Assignment:
  - Static Memory Controller on NCS0
  - SDRAM Controller or Static Memory Controller on NCS1
  - Static Memory Controller on NCS2
  - Static Memory Controller on NCS3, Optional NAND Flash/SmartMedia™ Support
  - Static Memory Controller on NCS4 - NCS5, Optional CompactFlash™ Support

8.8.2 Static Memory Controller

-

- Energy-saving Capabilities
  - Self-refresh, Power-down and Deep Power Modes Supported
  - Supports Mobile SDRAM Devices
- Error Detection
  - Refresh Error Interrupt
- SDRAM Power-up Initialization by Software
- CAS Latency of 1, 2, 3 Supported
- Auto Precharge Command Not Used

8.8.4 Error Corrected Code Controller

- Hardware Error Corrected Code (ECC) Generation
  - Detection and Correction by Software
- Supports NAND Flash and SmartMedia™ Devices with 8- or 16-bit Data Path.
- Supports NAND Flash/SmartMedia with Page Sizes of 528, 1056, 2112 and 4224 Bytes, Specified by Software

8.8.5 Serial Peripheral Interface

- Supports communication with serial external devices
  - Four chip selects with external decoder support allow communication with up to 15 peripherals
  - Serial memories, such as DataFlash™ and 3-wire EEPROMs
  - Serial peripherals, such as ADCs, DACs, CAN Controllers and Sensors
  - External co-processors
- Master or slave serial peripheral bus interface
  - 8- to 16-bit programmable data length per chip select
  - Programmable phase and polarity per chip select
  - Programmable transfer delays between consecutive transfers and between clock and data per chip select
  - Programmable delay between consecutive transfers
  - Selectable mode fault detection
- Very fast transfers supported
  - Transfers with baud rates up to MCK
  - The chip select line may be left active to speed up transfers on the same device

8.8.6 Two-wire Interface

- Compatibility with standard two-wire serial memory
- One, two or three bytes for slave address
- Sequential read/write operations

8.8.10 Audio Bitstream DAC

- Digital Stereo DAC
- Oversampled D/A conversion architecture
  - Oversampling ratio fixed 128x
  - FIR equalization filter
  - Digital interpolation filter: Comb4
  - 3rd Order Sigma-Delta D/A converters
- Digital bitstream outputs
- Parallel interface
- Connected to DMA Controller for background transfer without CPU intervention

8.8.11 Timer Counter

- Three 16-bit Timer Counter Channels
- Wide range of functions including:
  - Frequency Measurement
  - Event Counting
  - Interval Measurement
  - Pulse Generation
  - Delay Timing
  - Pulse Width Modulation
  - Up/down Capabilities
- Each channel is user-configurable and contains:
  - Three external clock inputs
  - Five internal clock inputs
  - Two multi-purpose input/output signals
- Two global registers that act on all three TC Channels

8.8.12 Pulse Width Modulation Controller

- 4 channels, one 16-bit counter per channel
- Common clock generator, providing Thirteen Different Clocks
  - A Modulo n counter providing eleven clocks
  - Two independent Linear Dividers working on modulo n counter outputs
- Independent channel programming
  - Independent Enable Disable Commands
  - Independent Clock
  - Independent Period and Duty Cycle, with Double Bufferization
  - Programmable selection of the output waveform polarity
  - Programmable center or left aligned output waveform

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