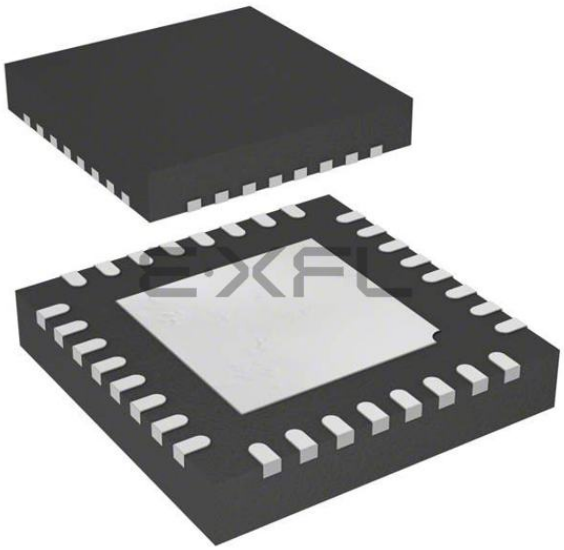

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	48MHz
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	LED, POR, PWM, WDT
Number of I/O	18
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VQFN Exposed Pad
Supplier Device Package	32-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89c5131a-putim

Signals

All the AT89C5131 signals are detailed by functionality on Table 1 through Table 12.

Table 1. Keypad Interface Signal Description

Signal Name	Type	Description	Alternate Function
KIN[7:0]	I	**Keypad Input Lines** Holding one of these pins high or low for 24 oscillator periods triggers a keypad interrupt if enabled. Held line is reported in the KBCON register.	P1[7:0]

Table 2. Programmable Counter Array Signal Description

Signal Name	Type	Description	Alternate Function
ECI	I	**External Clock Input**	P1.2
CEX[4:0]	I/O	Capture External Input Compare External Output	P1.3 P1.4 P1.5 P1.6 P1.7

Table 3. Serial I/O Signal Description

Signal Name	Type	Description	Alternate Function
RxD	I	**Serial Input** The serial input is P3.0 after reset, but it can also be configured to P4.0 by software.	P3.0
TxD	O	**Serial Output** The serial output is P3.1 after reset, but it can also be configured to P4.1 by software.	P3.1

Table 4. Timer 0, Timer 1 and Timer 2 Signal Description

Signal Name	Type	Description	Alternate Function
INT0	I	**Timer 0 Gate Input** $\overline{INT0}$ serves as external run control for timer 0, when selected by GATE0 bit in TCON register. **External Interrupt 0** $\overline{INT0}$ input set IE0 in the TCON register. If bit IT0 in this register is set, bits IE0 are set by a falling edge on $\overline{INT0}$. If bit IT0 is cleared, bits IE0 is set by a low level on $\overline{INT0}$.	P3.2
INT1	I	**Timer 1 Gate Input** $\overline{INT1}$ serves as external run control for Timer 1, when selected by GATE1 bit in TCON register. **External Interrupt 1** $\overline{INT1}$ input set IE1 in the TCON register. If bit IT1 in this register is set, bits IE1 are set by a falling edge on $\overline{INT1}$. If bit IT1 is cleared, bits IE1 is set by a low level on $\overline{INT1}$.	P3.3

Table 12. Power Signal Description (Continued)

Signal Name	Type	Description	Alternate Function
VREF	O	**USB pull-up Controlled Output** VREF is used to control the USB D+ 1.5 kΩ pull up. The Vref output is in high impedance when the bit DETACH is set in the USBCON register.	-

The Special Function Registers (SFRs) of the AT89C5131 fall into the following categories:

Table 14. C51 Core SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
ACC	E0h	Accumulator								
B	F0h	B Register								
PSW	D0h	Program Status Word								
SP	81h	Stack Pointer LSB of SPX								
DPL	82h	Data Pointer Low byte LSB of DPTR								
DPH	83h	Data Pointer High byte MSB of DPTR								

Table 15. I/O Port SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
P0	80h	Port 0								
P1	90h	Port 1								
P2	A0h	Port 2								
P3	B0h	Port 3								
P4	C0h	Port 4 (x2)								

Dual Data Pointer Register

The additional data pointer can be used to speed up code execution and reduce code size.

The dual DPTR structure is a way by which the chip will specify the address of an external data memory location. There are two 16-bit DPTR registers that address the external memory, and a single bit called DPS = AUXR1.0 (see Table 32) that allows the program code to switch between them (see Figure 10).

Figure 10. Use of Dual Pointer

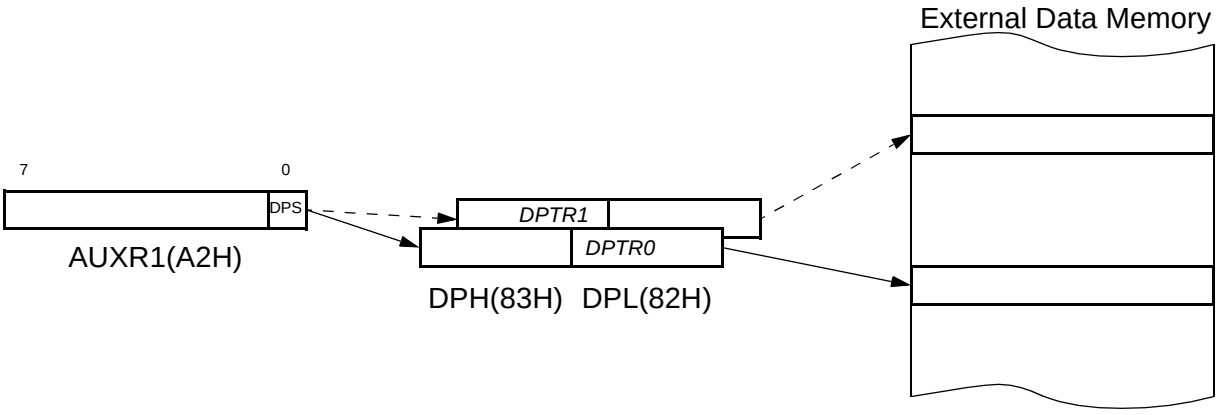


Table 32. AUXR1 Register

AUXR1- Auxiliary Register 1(0A2h)

7	6	5	4	3	2	1	0
-	-	ENBOOT	-	GF3	0	-	DPS

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	ENBOOT	**Enable Boot Flash** Cleared to disable boot ROM. Set to map the boot ROM between F800h - 0FFFFh.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	GF3	This bit is a general-purpose user flag.
2	0	Always cleared.
1	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
0	DPS	**Data Pointer Selection** Cleared to select DPTR0. Set to select DPTR1.

Reset Value = XX[BLJB]X X0X0b

Not bit addressable

a. Bit 2 stuck at 0; this allows to use INC AUXR1 to toggle DPS without changing GF3.

Flash Registers and Memory Map

The AT89C5131 Flash memory uses several registers:

- Hardware registers can only be accessed through the parallel programming modes which are handled by the parallel programmer.
- Software registers are in a special page of the Flash memory which can be accessed through the API or with the parallel programming modes. This page, called “Extra Flash Memory”, is not in the internal Flash program memory addressing space.

Hardware Registers

The only hardware registers of the AT89C5131 is called Hardware Security Byte (HSB).

Table 37. Hardware Security Byte (HSB)

7	6	5	4	3	2	1	0
X2	**BLJB**	**OSCON1**	**OSCON0**	**-**	**LB2**	**LB1**	**LB0**

Bit Number	Bit Mnemonic	Description
7	X2	**X2 Mode** Cleared to force X2 mode (6 clocks per instruction) Set to force X1 mode, Standard Mode (Default).
6	BLJB	**Bootloader Jump Bit** Set this bit to start the user’s application on next reset at address 0000h. Cleared this bit to start the bootloader at address F400h (default).
5-4	OSCON1-0	**Oscillator Control Bits** These two bits are used to control the oscillator in order to reduce consummation. **OSCON** **OSCON0** **Description** 1 1 The oscillator is configured to run from 0 to 32 MHz 1 0 The oscillator is configured to run from 0 to 16 MHz 0 1 The oscillator is configured to run from 0 to 8 MHz 0 0 This configuration shouldn’t be set
3	-	**Reserved**
2-0	LB2-0	**User Memory Lock Bits** See Table 38

Bootloader Jump Bit (BLJB)

One bit of the HSB, the BLJB bit, is used to force the boot address:

- When this bit is set the boot address is 0000h.
- When this bit is reset the boot address is F400h. By default, this bit is cleared and the ISP is enabled.

Flash Memory Lock Bits

The three lock bits provide different levels of protection for the on-chip code and data, when programmed as shown in Table 38.

Table 38. Program Lock bits

Program Lock Bits				
Security level	**LB0**	**LB1**	**LB2**	**Protection Description**
1	U	U	U	No program lock features enabled.
2	P	U	U	MOVC instruction executed from external program memory is disabled from fetching code bytes from any internal memory, $\overline{EA}$ is sampled and latched on reset, and further parallel programming of the Flash and of the EEPROM (boot and Xdata) is disabled. ISP and software programming with API are still allowed.
3	X	P	U	Same as 2, also verify through parallel programming interface is disabled and serial programming ISP is disabled.
4	X	X	P	Same as 3, also external execution is disabled.

Notes:
1. U: unprogrammed or “one” level.
2. P: programmed or “zero” level.
3. X: don’t care
4. WARNING: Security level 2 and 3 should only be programmed after Flash and code verification.

These security bits protect the code access through the parallel programming interface. They are set by default to level 4. The code access through the ISP is still possible and is controlled by the “software security bits” which are stored in the extra Flash memory accessed by the ISP firmware.

To load a new application with the parallel programmer, a chip erase must be done first. This will set the HSB in its inactive state and will erase the Flash memory. The part reference can always be read using Flash parallel programming modes.

Default Values

The default value of the HSB provides parts ready to be programmed with ISP:

- BLJB: Cleared to force ISP operation.
- X2: Set to force X1 mode (Standard Mode)
- OSCON1-0: Set to start with 32 MHz oscillator configuration value.
- LB2-0: Security level four to protect the code from a parallel access with maximum security.

Software Registers

Several registers are used, in factory and by parallel programmers, to make copies of hardware registers contents. These values are used by Atmel ISP (see Section “In-System Programming (ISP)”).

These registers are in the “Extra Flash Memory” part of the Flash memory. This block is also called ”XAF” or eXtra Array Flash. They are accessed in the following ways:

- Commands issued by the parallel memory programmer.
- Commands issued by the ISP software.
- Calls of API issued by the application software.

Several software registers are described in Table 39.

Table 39. Software Registers

Mnemonic	Description	Default value	
SBV	Software Boot Vector	FCh	–
HSB	Copy of the Hardware Security Byte	1011 1000b	–
BSB	Boot Status Byte	0FFh	–
SSB	Software Security Byte	FFh	–
–	Copy of the Manufacturer Code	58h	Atmel
–	Copy of the Device ID #1: Family Code	D7h	C51 X2, Electrically Erasable
–	Copy of the Device ID #2: Memories	F7h	AT89C5131 32 Kbyte
–	Size and Type	FBh	AT89C5131 16 Kbyte
–	Copy of the Device ID #3: Name	EFh	AT89C5131 32 Kbyte, revision 0
–	Revision	FFh	AT89C5131 16 Kbyte, revision 0

After programming the part by ISP, the BSB must be cleared (00h) in order to allow the application to boot at 0000h.

The content of the Software Security Byte (SSB) is described in Table 40 and Table 41.

To assure code protection from a parallel access, the HSB must also be at the required level.

Table 40. Software Security Byte (SSB)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	LB1	LB0

Bit Number	Bit Mnemonic	Description
7	-	Reserved Do not clear this bit.
6	-	Reserved Do not clear this bit.
5	-	Reserved Do not clear this bit.
4	-	Reserved Do not clear this bit.
3	-	Reserved Do not clear this bit.
2	-	Reserved Do not clear this bit.
1-0	LB1-0	User Memory Lock Bits See Table 41

Registers

Table 42. EECON (S:0D2h)
EECON Register

7	6	5	4	3	2	1	0
EEPL3	**EEPL2**	**EEPL1**	**EEPL0**	**-**	**-**	**EEE**	**EEBUSY**

Bit Number	Bit Mnemonic	Description
7-4	EEPL3-0	**Programming Launch command bits** Write 5Xh followed by AXh to EEPL to launch the programming.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
1	EEE	**Enable EEPROM Space bit** Set to map the EEPROM space during MOVX instructions (Write in the column latches) Clear to map the ERAM space during MOVX.
0	EEBUSY	**Programming Busy flag** Set by hardware when programming is in progress. Cleared by hardware when programming is done. Cannot be set or cleared by software.

Reset Value = XXXX XX00b
Not bit addressable

Table 52. PCA Module Modes (CCAPMn Registers)

ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMm	ECCFn	Module Function
0	0	0	0	0	0	0	No Operation
X	1	0	0	0	0	X	16-bit capture by a positive-edge trigger on CEXn
X	0	1	0	0	0	X	16-bit capture by a negative trigger on CEXn
X	1	1	0	0	0	X	16-bit capture by a transition on CEXn
1	0	0	1	0	0	X	16-bit Software Timer/Compare mode.
1	0	0	1	1	0	X	16-bit High Speed Output
1	0	0	0	0	1	0	8-bit PWM
1	0	0	1	X	0	X	Watchdog Timer (module 4 only)

There are two additional registers associated with each of the PCA modules. They are CCAPnH and CCAPnL and these are the registers that store the 16-bit count when a capture occurs or a compare should occur. When a module is used in the PWM mode these registers are used to control the duty cycle of the output (see Table 53 and Table 54)

Serial I/O Port

The serial I/O port in the AT89C5131 is compatible with the serial I/O port in the 80C52. It provides both synchronous and asynchronous communication modes. It operates as an Universal Asynchronous Receiver and Transmitter (UART) in three full-duplex modes (modes 1, 2 and 3). Asynchronous transmission and reception can occur simultaneously and at different baud rates.

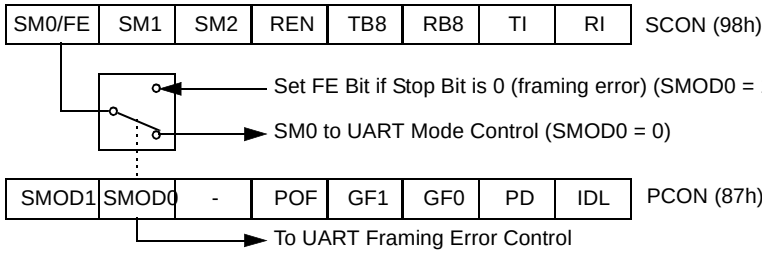
Serial I/O port includes the following enhancements:

- Framing error detection
- Automatic address recognition

Framing Error Detection

Framing bit error detection is provided for the three asynchronous modes (modes 1, 2 and 3). To enable the framing bit error detection feature, set SMOD0 bit in PCON register (see Figure 31).

Figure 31. Framing Error Block Diagram



When this feature is enabled, the receiver checks each incoming data frame for a valid stop bit. An invalid stop bit may result from noise on the serial lines or from simultaneous transmission by two CPUs. If a valid stop bit is not found, the Framing Error bit (FE) in SCON register (See Table 57) bit is set.
Software may examine FE bit after each reception to check for data errors. Once set, only software or a reset can clear FE bit. Subsequently received frames with valid stop bits cannot clear FE bit. When FE feature is enabled, RI rises on stop bit instead of the last data bit (See Figure 32 and Figure 33).

Figure 32. UART Timings in Mode 1

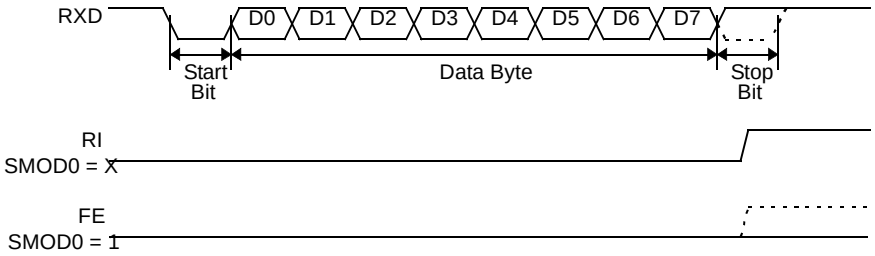
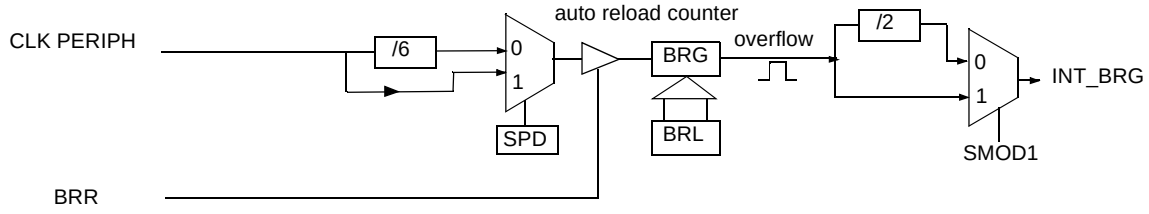


Figure 35. Internal Baud Rate



- The baud rate for UART is token by formula:

$$Baud\_Rate = \frac{2^{SMOD1} \times F_{CLK\ PERIPH}}{2 \times 2 \times 6^{(1-SPD)} \times 16 \times [256 - (BRL)]}$$

$$(BRL) = 256 - \frac{2^{SMOD1} \times F_{CLK\ PERIPH}}{2 \times 2 \times 6^{(1-SPD)} \times 16 \times Baud\_Rate}$$

Table 57. SCON Register – SCON Serial Control Register (98h)

7	6	5	4	3	2	1	0
FE/SM0	**SM1**	**SM2**	**REN**	**TB8**	**RB8**	**TI**	**RI**

Bit Number	Bit Mnemonic	Description
7	FE	**Framing Error bit (SMOD0 = 1)** Clear to reset the error state, not cleared by a valid stop bit. Set by hardware when an invalid stop bit is detected. SMOD0 must be set to enable access to the FE bit
	SM0	**Serial port Mode bit 0** Refer to SM1 for serial port mode selection. SMOD0 must be cleared to enable access to the SM0 bit
6	SM1	**Serial port Mode bit 1** SM0 SM1 Mode Description Baud Rate 0 0 0 Shift Register $F_{CPU\ PERIPH}/6$ 0 1 1 8-bit UART Variable 1 0 2 9-bit UART $F_{CPU\ PERIPH}/32$ or/16 1 1 3 9-bit UART Variable
5	SM2	**Serial port Mode 2 bit/Multiprocessor Communication Enable bit** Clear to disable multiprocessor communication feature. Set to enable multiprocessor communication feature in mode 2 and 3, and eventually mode 1. This bit should be cleared in mode 0.
4	REN	**Reception Enable bit** Clear to disable serial reception. Set to enable serial reception.
3	TB8	**Transmitter Bit 8/Ninth bit to Transmit in Modes 2 and 3** Clear to transmit a logic 0 in the 9th bit. Set to transmit a logic 1 in the 9th bit.
2	RB8	**Receiver Bit 8/Ninth bit received in modes 2 and 3** Cleared by hardware if 9th bit received is a logic 0. Set by hardware if 9th bit received is a logic 1. In mode 1, if SM2 = 0, RB8 is the received stop bit. In mode 0 RB8 is not used.
1	TI	**Transmit Interrupt flag** Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0 or at the beginning of the stop bit in the other modes.
0	RI	**Receive Interrupt flag** Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0, see Figure 32. and Figure 33. in the other modes.

Reset Value = 0000 0000b
Bit addressable

Power Reduction Mode

P1 inputs allow exit from idle and power down modes as detailed in section “Power-down Mode”.

Registers

Table 69. KBF Register

KBF - Keyboard Flag Register (9Eh)

7	6	5	4	3	2	1	0
KBF7	KBF6	KBF5	KBF4	KBF3	KBF2	KBF1	KBF0

Bit Number	Bit Mnemonic	Description
7	KBF7	**Keyboard line 7 flag** Set by hardware when the Port line 7 detects a programmed level. It generates a Keyboard interrupt request if the KBKBIE.7 bit in KBIE register is set. Must be cleared by software.
6	KBF6	**Keyboard line 6 flag** Set by hardware when the Port line 6 detects a programmed level. It generates a Keyboard interrupt request if the KBIE.6 bit in KBIE register is set. Must be cleared by software.
5	KBF5	**Keyboard line 5 flag** Set by hardware when the Port line 5 detects a programmed level. It generates a Keyboard interrupt request if the KBIE.5 bit in KBIE register is set. Must be cleared by software.
4	KBF4	**Keyboard line 4 flag** Set by hardware when the Port line 4 detects a programmed level. It generates a Keyboard interrupt request if the KBIE.4 bit in KBIE register is set. Must be cleared by software.
3	KBF3	**Keyboard line 3 flag** Set by hardware when the Port line 3 detects a programmed level. It generates a Keyboard interrupt request if the KBIE.3 bit in KBIE register is set. Must be cleared by software.
2	KBF2	**Keyboard line 2 flag** Set by hardware when the Port line 2 detects a programmed level. It generates a Keyboard interrupt request if the KBIE.2 bit in KBIE register is set. Must be cleared by software.
1	KBF1	**Keyboard line 1 flag** Set by hardware when the Port line 1 detects a programmed level. It generates a Keyboard interrupt request if the KBIE.1 bit in KBIE register is set. Must be cleared by software.
0	KBF0	**Keyboard line 0 flag** Set by hardware when the Port line 0 detects a programmed level. It generates a Keyboard interrupt request if the KBIE.0 bit in KBIE register is set. Must be cleared by software.

Reset Value = 0000 0000b

Bit Number	Bit Mnemonic	Description
2	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit
1	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
0	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.

Reset Value = 00X0 XXXXb
Not Bit addressable

Serial Peripheral Data Register (SPDAT)

The Serial Peripheral Data Register (Table 77) is a read/write buffer for the receive data register. A write to SPDAT places data directly into the shift register. No transmit buffer is available in this model.

A Read of the SPDAT returns the value located in the receive buffer and not the content of the shift register.

Table 77. SPDAT Register

SPDAT - Serial Peripheral Data Register (0C5H)

7	6	5	4	3	2	1	0
R7	**R6**	**R5**	**R4**	**R3**	**R2**	**R1**	**R0**

Reset Value = Indeterminate

R7:R0: Receive data bits

SPCON, SPSTA and SPDAT registers may be read and written at any time while there is no on-going exchange. However, special care should be taken when writing to them while a transmission is on-going:

- Do not change SPR2, SPR1 and SPR0
- Do not change CPHA and CPOL
- Do not change MSTR
- Clearing SPEN would immediately disable the peripheral
- Writing to the SPDAT will cause an overflow

Description

The CPU interfaces to the TWI logic via the following four 8-bit special function registers: the Synchronous Serial Control register (SSCON; Table 85 and Table 79), the Synchronous Serial Data register (SSDAT; Table 86), the Synchronous Serial Control and Status register (SSCS; Table 87) and the Synchronous Serial Address register (SSADR see Table 88 and Table 78).

SSCON is used to enable SSLC, to program the bit rate (see Table 79), to enable slave modes, to acknowledge or not a received data, to send a START or a STOP condition on the TWI bus, and to acknowledge a serial interrupt. A hardware reset disables SSLC.

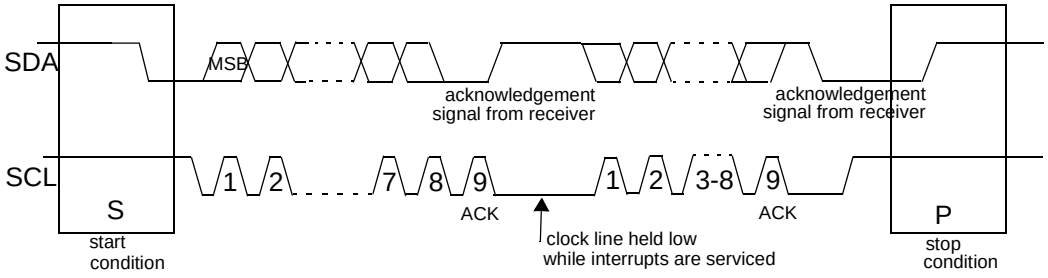
In write mode, SSCS is used to select the TWI interface and to select the bit rate source. In read mode, SSCS contains a status code which reflects the status of the TWI logic and the TWI bus. The three least significant bits are always zero. The five most significant bits contain the status code. There are 26 possible status codes. When SSCS contains F8h, no relevant state information is available and no serial interrupt is requested. A valid status code is available in SSCS one machine cycle after SI is set by hardware and is still present one machine cycle after SI has been reset by software. Table 80 to Table 83 give the status for the master modes and miscellaneous states.

SSDAT contains a byte of serial data to be transmitted or a byte which has just been received. It is addressable while it is not in process of shifting a byte. This occurs when TWI logic is in a defined state and the serial interrupt flag is set. Data in SSDAT remains stable as long as SI is set. While data is being shifted out, data on the bus is simultaneously shifted in; SSDAT always contains the last byte present on the bus.

SSADR may be loaded with the 7-bit slave address (7 most significant bits) to which SSLC will respond when programmed as a slave transmitter or receiver. The LSB is used to enable general call address (00h) recognition.

Figure 48 shows how a data transfer is accomplished on the TWI bus.

Figure 48. Complete Data Transfer on TWI Bus



The four operating modes are:

- Master Transmitter
- Master Receiver
- Slave Transmitter
- Slave Receiver

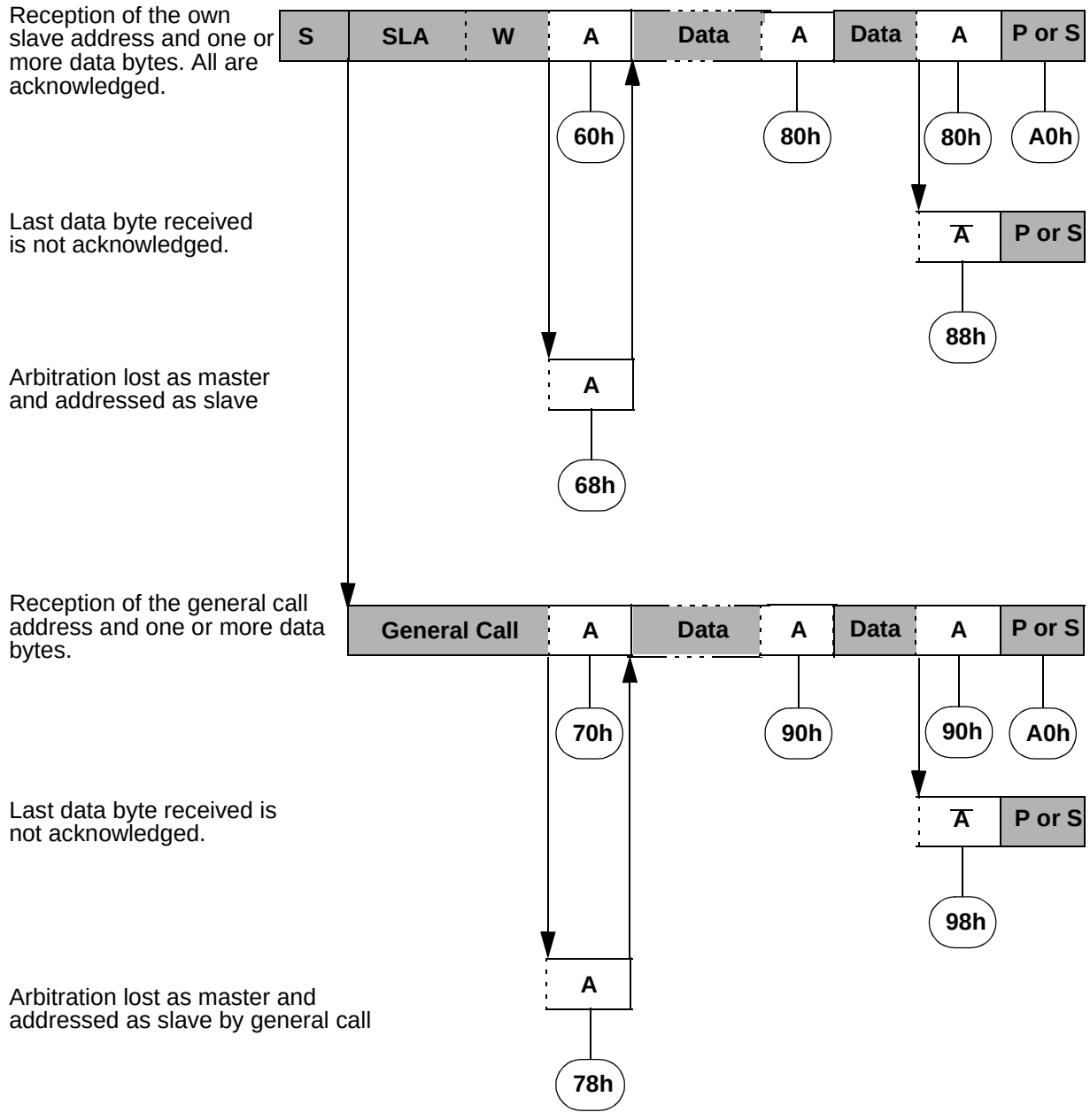
Data transfer in each mode of operation is shown in Figure 49 to Figure 52. These figures contain the following abbreviations:

S: START condition

R: Read bit (high level at SDA)

W: Write bit (low level at SDA)

Figure 51. Format and State in the Slave Receiver Mode



Serial Interface Engine (SIE)

The SIE performs the following functions:

- NRZI data encoding and decoding.
- Bit stuffing and un-stuffing.
- CRC generation and checking.
- Handshakes.
- TOKEN type identifying.
- Address checking.
- Clock generation (via DPLL).

Figure 54. SIE Block Diagram

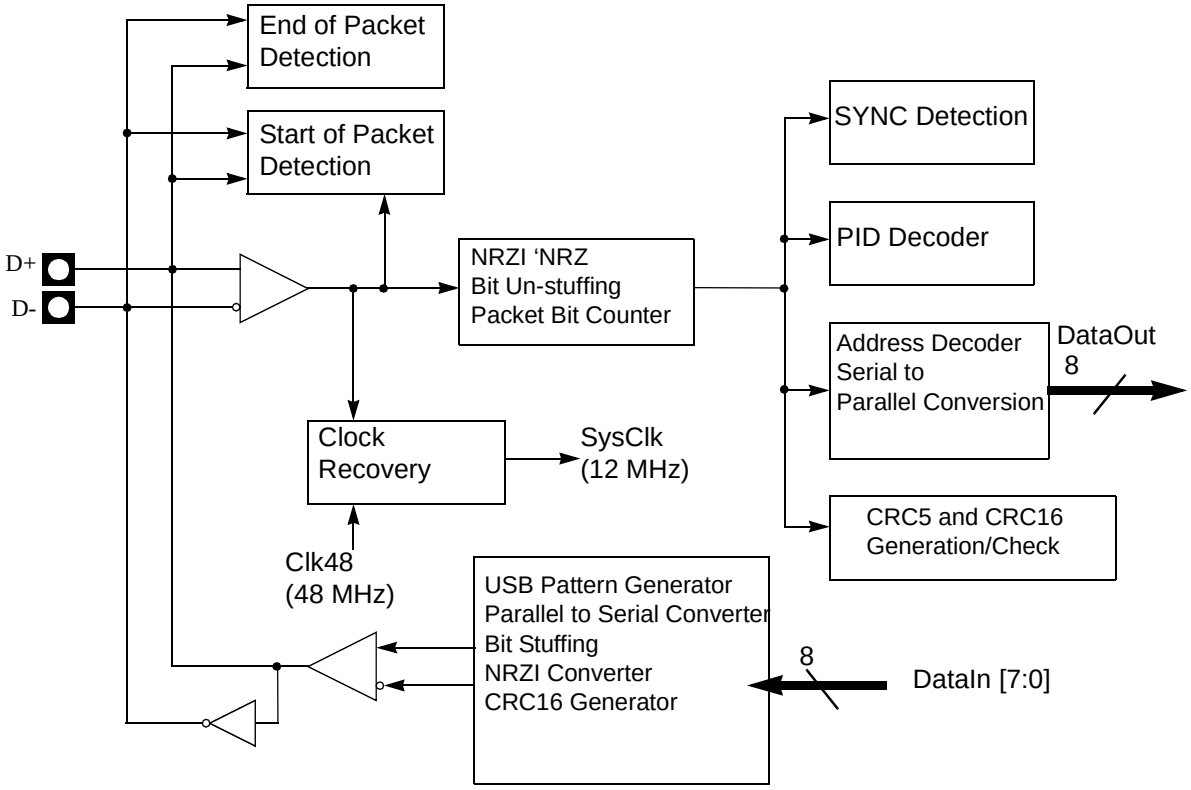
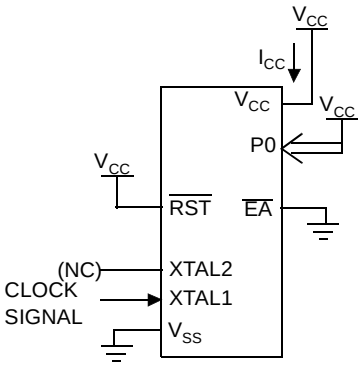
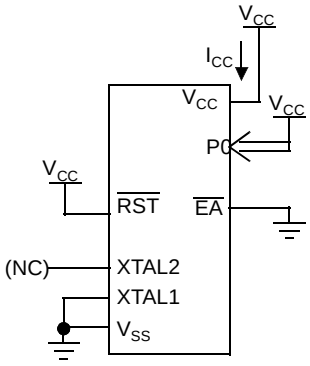


Figure 71. I_{CC} Test Condition, Idle Mode



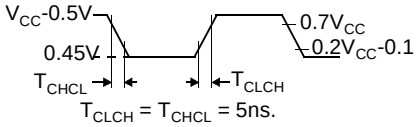
All other pins are disconnected.

Figure 72. I_{CC} Test Condition, Power-down Mode



All other pins are disconnected.

Figure 73. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes



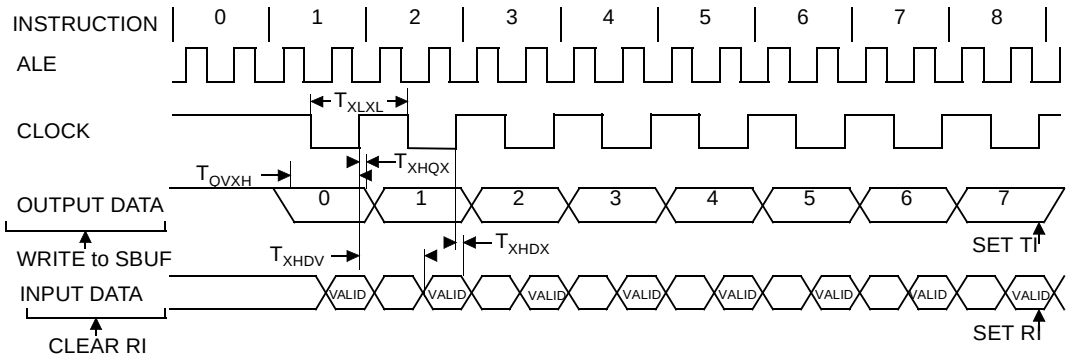
LED's

Table 111. LED Outputs DC Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{OL}	Output Low Current, P3.6 and P3.7 LED modes	1	2	4	mA	2 mA configuration
		2	4	8	mA	4 mA configuration
		5	10	20	mA	10 mA configuration

Note: 1. (T_A = -20°C to +50°C, V_{CC} - V_{OL} = 2 V ± 20%)

Shift Register Timing Waveform

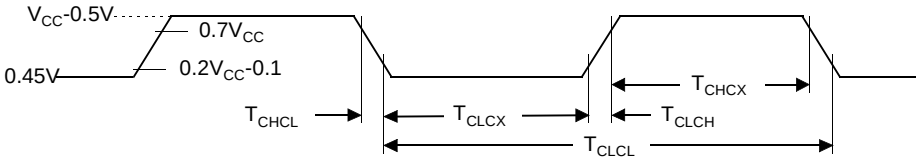


External Clock Drive Characteristics (XTAL1)

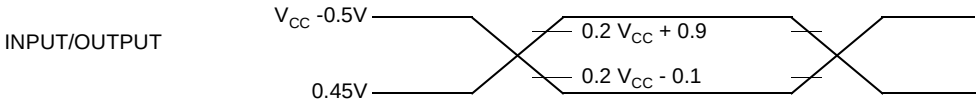
Table 121. AC Parameters

Symbol	Parameter	Min	Max	Units
T_{CLCL}	Oscillator Period	25		ns
T_{CHCX}	High Time	5		ns
T_{CLCX}	Low Time	5		ns
T_{CLCH}	Rise Time		5	ns
T_{CHCL}	Fall Time		5	ns
T_{CHCX}/T_{CLCX}	Cyclic ratio in X2 mode	40	60	%

External Clock Drive Waveforms

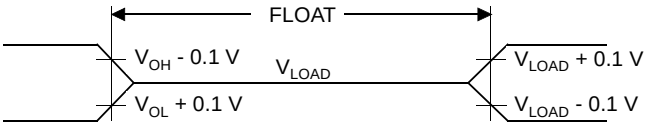


AC Testing Input/Output Waveforms



AC inputs during testing are driven at V_{CC} - 0.5 for a logic “1” and 0.45V for a logic “0”. Timing measurement are made at V_{IH} min for a logic “1” and V_{IL} max for a logic “0”.

Float Waveforms



For timing purposes as port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm 20$ mA.

Ordering Information

Table 125. Possible Order Entries

Part Number	Memory Size (Kbytes)	Supply Voltage	Temperature Range	Package	Packing
AT89C5130A-RDTUM	16	2.7 to 5.5V	Industrial	Green VQFP64(1)	Tray
AT89C5130A-PUTUM	16	2.7 to 5.5V	Industrial	Green QFN32(1)	Tray
AT89C5130A-S3SUM	16	2.7 to 5.5V	Industrial	Green PLCC52(1)	Stick
AT89C5131A-RDTIM	32	2.7 to 5.5V	Industrial	VQFP64	Tray
AT89C5131A-PUTIM	32	2.7 to 5.5V	Industrial	QFN32	Tray
AT89C5131A-S3SIM	32	2.7 to 5.5V	Industrial	PLCC52	Stick
AT89C5131A-RDTUM	32	2.7 to 5.5V	Industrial	Green VQFP64	Tray

Note: 1. “Green” product version. Green products are delivered in Dry Pack.

2. Optional Packing and Package options (please consult Atmel sales representative)
-Tape and Reel
-Dry Pack
-Die form