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Remarks 1. f_{XX}: Main system clock frequency (f_X or $f_X/2$)

2. f_X: Main system clock oscillation frequency

3. f_{XT}: Subsystem clock oscillation frequency

4. TI00: 16-bit timer/event counter input pin

5. TM0: 16-bit timer register

6. MCS: Bit 0 of oscillation mode select register (OSMS)

7. Values in parentheses apply to operation with f_X = 5.0 MHz or f_{XT} = 32.768 kHz.

(2) 16-bit timer mode control register (TMC0)

This register sets the 16-bit timer operating mode, the 16-bit timer register clear mode and output timing, and detects an overflow.

TMC0 is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears TMC0 to 00H.

Caution The 16-bit timer register starts operation at the moment TMC01 to TMC03 are set to values other than 0, 0, 0 (operation stop mode). Set TMC01 to TMC03 to 0, 0, 0 to stop the operation.

Figure 8-32. Square-Wave Output Operation Timing

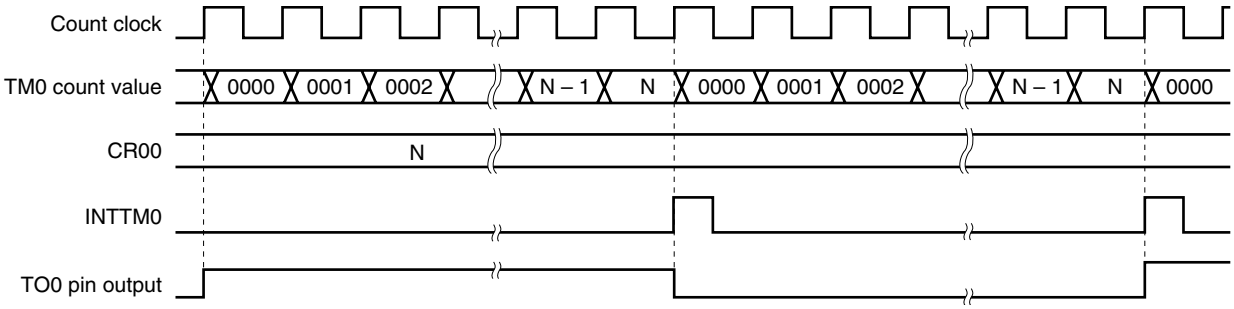


Table 8-8. 16-Bit Timer/Event Counter Square-Wave Output Ranges

Minimum Pulse Time		Maximum Pulse Time		Resolution	
MCS = 1	MCS = 0	MCS = 1	MCS = 0	MCS = 1	MCS = 0
2 × TI00 input cycle		2^{16} × TI00 input cycle		TI00 input edge cycle	
—	2 × 1/fx (400 ns)	—	2^{16} × 1/fx (13.1 ms)	—	1/fx (200 ns)
2 × 1/fx (400 ns)	2^2 × 1/fx (800 ns)	2^{16} × 1/fx (13.1 ms)	2^{17} × 1/fx (26.2 ms)	1/fx (200 ns)	2 × 1/fx (400 ns)
2^2 × 1/fx (800 ns)	2^3 × 1/fx (1.6 μs)	2^{17} × 1/fx (26.2 ms)	2^{18} × 1/fx (52.4 ms)	2 × 1/fx (400 ns)	2^2 × 1/fx (800 ns)
2^3 × 1/fx (1.6 μs)	2^4 × 1/fx (3.2 μs)	2^{18} × 1/fx (52.4 ms)	2^{19} × 1/fx (104.9 ms)	2^2 × 1/fx (800 ns)	2^3 × 1/fx (1.6 μs)
2 × watch timer output cycle		2^{16} × watch timer output cycle		Watch timer output edge cycle	

Remarks 1. fx: Main system clock oscillation frequency

2. MCS: Bit 0 of oscillation mode select register (OSMS)

3. Values in parentheses apply to operation with fx = 5.0 MHz

★ **(10) Timing at which A/D conversion result is undefined**

The A/D conversion value may be undefined if the timing of completion of A/D conversion and the timing of stopping the A/D conversion conflict with each other. Therefore, read the A/D conversion result during the A/D conversion operation. To read the conversion result after stopping the A/D conversion operation, be sure to stop the A/D conversion before the next conversion ends.

Figures 14-14 and 14-15 show the timing of reading the conversion result.

Figure 14-14. Timing of Reading Conversion Result (When Conversion Result is Undefined)

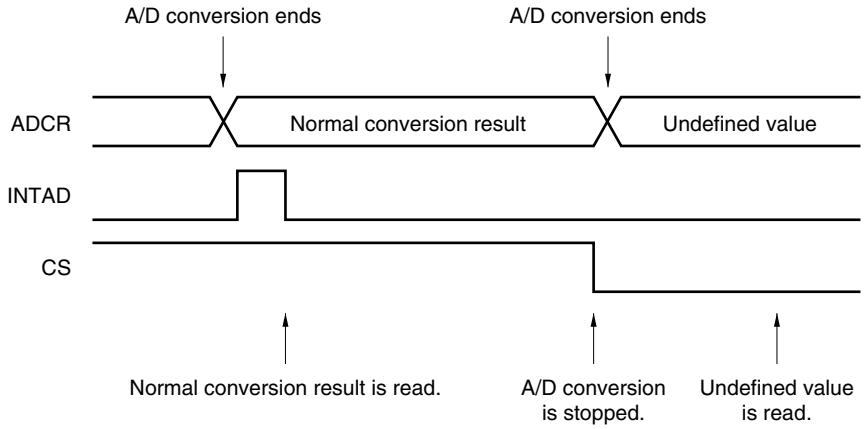
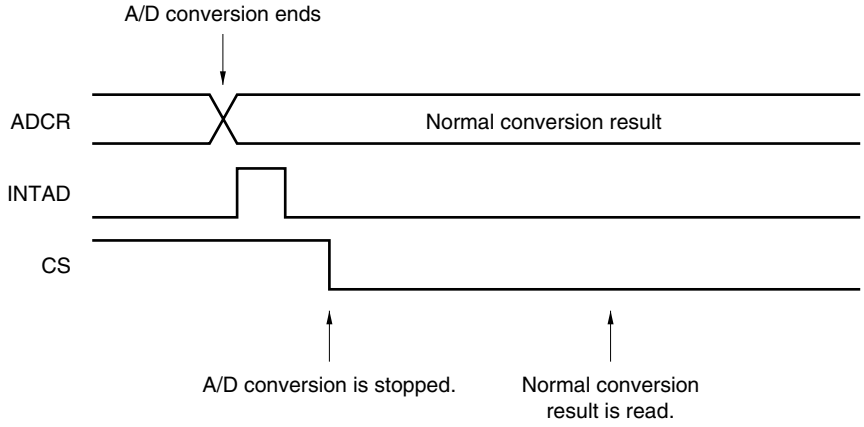


Figure 14-15. Timing of Reading Conversion Result (When Conversion Result is Normal)



★ **(11) Notes on board design**

Locate analog circuits as far away from digital circuits as possible on the board because the analog circuits may be affected by the noise of the digital circuits. In particular, do not cross an analog signal line with a digital signal line, or wire an analog signal line in the vicinity of a digital signal line. Otherwise, the A/D conversion characteristics may be affected by the noise of the digital line.

Connect AV_{SS} and V_{SS0} at one location on the board where the voltages are stable.

(b) Serial bus interface control register (SBIC)

SBIC is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears SBIC to 00H.

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After reset	R/W
SBIC	BSYE	ACKD	ACKE	ACKT	CMDD	RELD	CMDT	RELT	FF61H	00H	R/W

R/W		
R/W	RELT	When RELT = 1, the SO0 latch is set to 1. After the SO0 latch is set, RELT is automatically cleared to 0. It is also cleared to 0 when CSIE0 = 0.

R/W		
R/W	CMDT	When CMDT = 1, the SO0 latch is cleared to 0. After the SO0 latch is cleared, CMDT is automatically cleared to 0. It is also cleared to 0 when CSIE0 = 0.

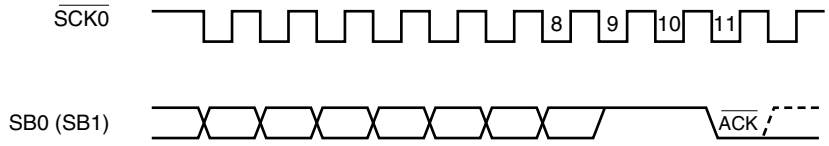
CSIE0: Bit 7 of serial operating mode register 0 (CSIM0)

(e) Acknowledge signal ($\overline{\text{ACK}}$)

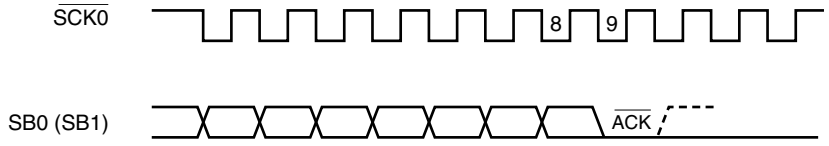
The acknowledge signal is used to check serial data reception between the transmitter and receiver.

Figure 16-18. Acknowledge Signal

[When output in synchronization with 11th $\overline{\text{SCK0}}$ clock]



[When output in synchronization with 9th $\overline{\text{SCK0}}$ clock]

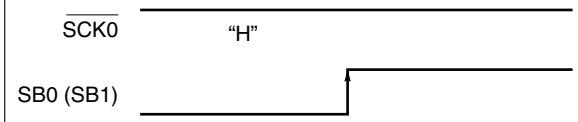
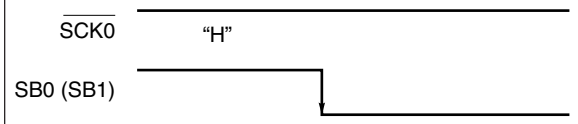
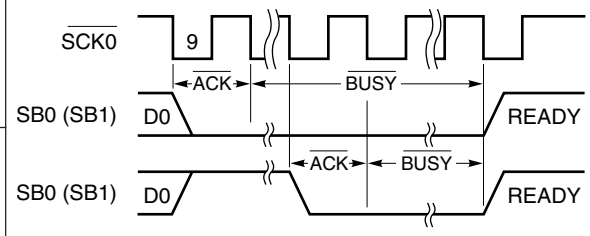


Remark The broken lines indicate the READY status.

The acknowledge signal is one-shot pulse generated at the falling edge of $\overline{\text{SCK0}}$ after 8-bit data transfer. It can be positioned anywhere and can be synchronized with any $\overline{\text{SCK0}}$ clock.

After 8-bit data transmission, the transmitter checks whether the receiver has returned the acknowledge signal. If the acknowledge signal is not returned for the preset period of time after data transmission, it can be judged that data reception has not been carried out correctly.

Table 16-3. Various Signals in SBI Mode (1/2)

Signal Name	Output Device	Definition	Timing Chart	Output Conditions	Effects on Flag	Meaning of Signal
Bus release signal (REL)	Master	SB0 (SB1) rising edge when $\overline{SCK0}$ = 1		• RELT set	• RELD set • CMDD clear	CMD signal is output to indicate that transmit data is an address.
Command signal (CMD)	Master	SB0 (SB1) falling edge when $\overline{SCK0}$ = 1		• CMDT set	• CMDD set	i) Transmit data is an address after REL signal output. ii) REL signal is not output and transmit data is an command.
Acknowledge signal ($\overline{ACK}$)	Master/ slave	Low-level signal output to SB0 (SB1) during one-clock period of $\overline{SCK0}$ after completion of serial reception	[Synchronous BUSY output]	①ACKE = 1 ②ACKT set	• ACKD set	Completion of reception
Busy signal ($\overline{BUSY}$)	Slave	[Synchronous BUSY signal] Low-level signal output to SB0 (SB1) following acknowledge signal		• BSYE = 1	—	Serial receive disabled because of processing
Ready signal (READY)	Slave	High-level signal output to SB0 (SB1) before serial transfer start and after completion of serial transfer		①BSYE = 0 ②Execution of instruction for data write to SIO0 (transfer start instruction)	—	Serial receive enabled

(4) Interrupt timing specification register (SINT)

This register sets the bus release interrupt and address mask functions and displays the $\overline{SCK0}$/SCL pin level status.

SINT is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{RESET}$ input clears SINT to 00H.

Figure 17-6. Format of Interrupt Timing Specification Register (1/2)

Symbol	7	<6>	<5>	<4>	<3>	<2>	1	0	Address	After reset	R/W
SINT	0	CLD	SIC	SVAM	CLC	WREL	WAT1	WAT0	FF63H	00H	R/W[Note 1]

R/W

WAT1	WAT0	Wait and interrupt control
0	0	Generates interrupt servicing request at rising edge of 8th $\overline{SCK0}$ clock cycle (keeping clock output in high impedance).
0	1	Setting prohibited
1	0	Used in I^2C bus mode (8-clock wait). Generates interrupt servicing request at rising edge of 8th SCK0 clock cycle. (In the case of master device, makes SCL output low to enter wait state after 8 clock pulses are output. In the case of slave device, makes SCL output low to request wait state after 8 clock pulses are input.)
1	1	Used in I^2C bus mode (9-clock wait). Generates interrupt servicing request at rising edge of 9th SCK0 clock cycle. (In the case of master device, makes SCL output low to enter wait state after 9 clock pulses are output. In the case of slave device, makes SCL output low to request wait state after 9 clock pulses are input.)

R/W

WREL	Wait sate release control
0	Wait state has been released.
1	Release wait state. Automatically cleared to 0 when the state is released (Used to cancel wait state by means of WAT0 and WAT1.)

R/W

CLC	Clock level control[Note 2]
0	Used in I^2C bus mode. Make output level of SCL pin low unless serial transfer is being performed.
1	Used in I^2C bus mode. Make SCL pin enter high-impedance state unless serial transfer is being performed (except for clock line which is kept high). Used to enable master device to generate start condition and stop condition signals.

Notes 1. Bit 6 (CLD) is a read-only bit.

2. When not using the I^2C mode, clear CLC to 0.

18.3 Control Registers of Serial Interface Channel 1

The following four registers are used to control serial interface channel 1.

- Timer clock select register 3 (TCL3)
- Serial operating mode register 1 (CSIM1)
- Automatic data transmit/receive control register (ADTC)
- Automatic data transmit/receive interval specification register (ADTI)

(1) Timer clock select register 3 (TCL3)

This register sets the serial clock of serial interface channel 1.

TCL3 is set with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets TCL3 to 88H.

Remark Besides setting the serial clock of serial interface channel 1, TCL3 sets the serial clock of serial interface channel 0.

When the internal clock is used as the serial clock in the 3-wire serial I/O mode, set BRGC as described below. BRGC setting is not required if an external serial clock is used.

(i) When the baud rate generator is not used:

Select the serial clock frequency using TPS0 to TPS3. Be sure then to set MDL0 to MDL3 to 1,1,1,1. The serial clock frequency becomes the same as the source clock frequency for the 5-bit counter.

(ii) When the baud rate generator is used:

Select the serial clock frequency using TPS0 to TPS3. Be sure then to set MDL0 to MDL3 to 1,1,1,1.

The serial clock frequency is calculated by the following formula:

$$\text{Serial clock frequency} = \frac{f_{XX}}{2^n \times (k + 16)} \text{ [Hz]}$$

Remarks 1. f_X: Main system clock oscillation frequency

2. f_{XX}: Main system clock frequency (f_X or $f_X/2$)

3. n: Value set in TPS0 to TPS3 ($1 \leq n \leq 11$)

4. k: Value set in MDL0 to MDL3 ($0 \leq k \leq 14$)

(5) Sampling clock select register (SCS)

This register is used to set the clock for sampling the valid edge input to INTP0. When remote controlled data reception is carried out using INTP0, digital noise is eliminated using the sampling clock.

SCS is set with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears SCS to 00H.

Figure 21-7. Format of Sampling Clock Select Register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
SCS	0	0	0	0	0	0	SCS1	SCS0	FF47H	00H	R/W

SCS1	SCS0	INTP0 sampling clock selection		
			MCS = 1	MCS = 0
0	0	$f_{XX}/2^N$		
0	1	$f_{XX}/2^7$	$f_X/2^7$ (39.1 kHz)	$f_X/2^8$ (19.5 kHz)
1	0	$f_{XX}/2^5$	$f_X/2^5$ (156.3 kHz)	$f_X/2^6$ (78.1 kHz)
1	1	$f_{XX}/2^6$	$f_X/2^6$ (78.1 kHz)	$f_X/2^7$ (39.1 kHz)

Caution $f_{XX}/2^N$ is the clock supplied to the CPU and $f_{XX}/2^5$, $f_{XX}/2^6$, and $f_{XX}/2^7$ are clocks supplied to the peripheral hardware. $f_{XX}/2^N$ stops in the HALT mode.

Remarks 1. N: Value (N = 0 to 4) of bits 0 to 2 (PCC0 to PCC2) of processor clock control register (PCC)

2. f_{XX}: Main system clock frequency (f_X or $f_X/2$)

3. f_X: Main system clock oscillation frequency

4. MCS: Bit 0 of the oscillation mode select register (OSMS)

5. Values in parentheses apply to operation with f_X = 5.0 MHz.

21.5 Test Function

When the watch timer overflows and the port 4 falling edge is detected, the internal test input flag is set to 1, and the standby release signal is generated.

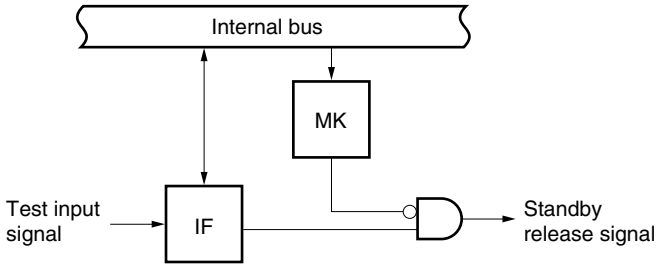
Unlike the interrupt function, vectored processing is not performed.

There are two test input sources as shown in Table 21-5. The basic configuration is shown in Figure 21-18.

Table 21-5. Test Input Sources

Test Input Sources		Internal/ External
Name	Trigger	
INTWT	Watch timer overflow	Internal
INTPT4	Falling edge detection at port 4	External

Figure 21-18. Basic Configuration of Test Function



Remark IF: Test input flag
MK: Test mask flag

21.5.1 Registers controlling test function

The test function is controlled by the following three registers.

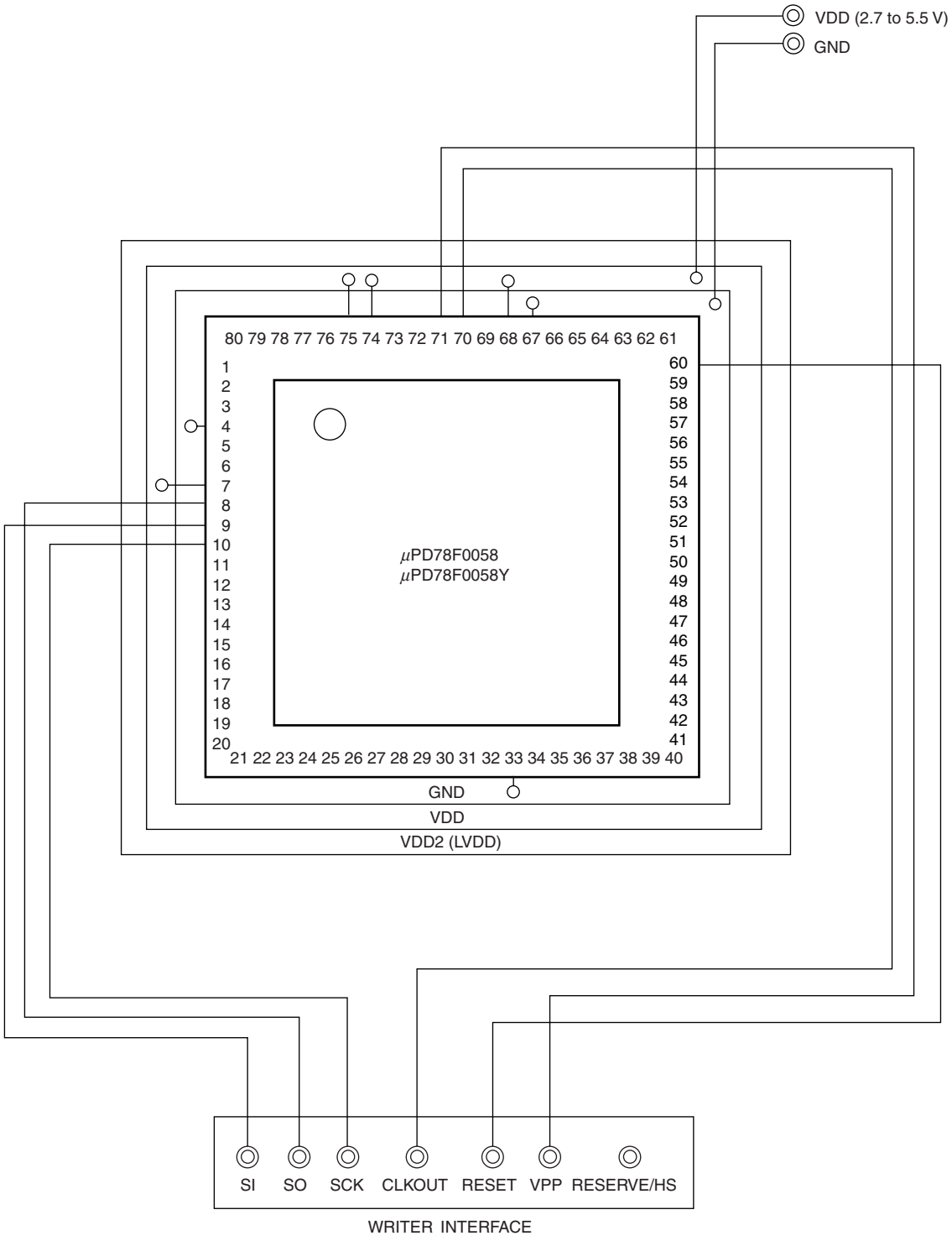
- Interrupt request flag register 1L (IF1L)
- Interrupt mask flag register 1L (MK1L)
- Key return mode register (KRM)

The names of the test input flags and test mask flags corresponding to the test input signals are listed in Table 21-6.

Table 21-6. Flags Corresponding to Test Input Signals

Test Input Signal Name	Test Input Flag	Test Mask Flag
INTWT	WTIF	WTMK
INTPT4	KRIF	KRMK

Figure 26-12. Wiring Example for Flash Writing Adapter in 3-Wire Serial I/O Mode (SIO ch-2)



Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag
				Note 1	Note 2		Z AC CY
16-bit data transfer	**MOVW**	rp, #word	3	6	–	rp ← word	
		saddrp, #word	4	8	10	(saddrp) ← word	
		sfrp, #word	4	–	10	sfrp ← word	
		AX, saddrp	2	6	8	AX ← (saddrp)	
		saddrp, AX	2	6	8	(saddrp) ← AX	
		AX, sfrp	2	–	8	AX ← sfrp	
		sfrp, AX	2	–	8	sfrp ← AX	
		AX, rp **Note 3**	1	4	–	AX ← rp	
		rp, AX **Note 3**	1	4	–	rp ← AX	
		AX, !addr16	3	10	12 + 2n	AX ← (addr16)	
		!addr16, AX	3	10	12 + 2m	(addr16) ← AX	
	XCHW	AX, rp **Note 3**	1	4	–	AX ↔ rp	
8-bit operation	**ADD**	A, #byte	2	4	–	A, CY ← A + byte	× × ×
		saddr, #byte	3	6	8	(saddr), CY ← (saddr) + byte	× × ×
		A, r **Note 4**	2	4	–	A, CY ← A + r	× × ×
		r, A	2	4	–	r, CY ← r + A	× × ×
		A, saddr	2	4	5	A, CY ← A + (saddr)	× × ×
		A, !addr16	3	8	9 + n	A, CY ← A + (addr16)	× × ×
		A, [HL]	1	4	5 + n	A, CY ← A + (HL)	× × ×
		A, [HL + byte]	2	8	9 + n	A, CY ← A + (HL + byte)	× × ×
		A, [HL + B]	2	8	9 + n	A, CY ← A + (HL + B)	× × ×
		A, [HL + C]	2	8	9 + n	A, CY ← A + (HL + C)	× × ×
	ADDC	A, #byte	2	4	–	A, CY ← A + byte + CY	× × ×
		saddr, #byte	3	6	8	(saddr), CY ← (saddr) + byte + CY	× × ×
		A, r **Note 4**	2	4	–	A, CY ← A + r + CY	× × ×
		r, A	2	4	–	r, CY ← r + A + CY	× × ×
		A, saddr	2	4	5	A, CY ← A + (saddr) + CY	× × ×
		A, !addr16	3	8	9 + n	A, CY ← A + (addr16) + CY	× × ×
		A, [HL]	1	4	5 + n	A, CY ← A + (HL) + CY	× × ×
		A, [HL + byte]	2	8	9 + n	A, CY ← A + (HL + byte) + CY	× × ×
		A, [HL + B]	2	8	9 + n	A, CY ← A + (HL + B) + CY	× × ×
		A, [HL + C]	2	8	9 + n	A, CY ← A + (HL + C) + CY	× × ×

Notes 1. When the internal high-speed RAM area is accessed or instruction that performs no data access is executed.

2. When an area except the internal high-speed RAM area is accessed

3. Only when rp = BC, DE, or HL

4. Except “r = A”

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

2. This clock cycle applies to the internal ROM program.

3. n is the number of waits when external memory expansion area is read from.

4. m is the number of waits when external memory expansion area is written to.

(v) SBI mode ($\overline{SCK0}$ ... Internal clock output) (μPD78005x only)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY5}	4.5 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.0 V ≤ V_{DD} < 4.5 V		3,200			ns
		1.8 V ≤ V_{DD} < 2.0 V		4,800			ns
$\overline{SCK0}$ high-/low-level width	t_{KH5}, t_{KL5}	4.5 V ≤ V_{DD} ≤ 5.5 V		$t_{KCY5}/2 - 50$			ns
		1.8 V ≤ V_{DD} < 4.5 V		$t_{KCY5}/2 - 150$			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK5}	4.5 V ≤ V_{DD} ≤ 5.5 V		100			ns
		2.0 V ≤ V_{DD} < 4.5 V		300			ns
		1.8 V ≤ V_{DD} < 2.0 V		400			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI5}			$t_{KCY5}/2$			ns
Delay time from $\overline{SCK0}$↓ to SB0, SB1 output	t_{KSO5}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 4.5 to 5.5 V	0		250	ns
			V_{DD} = 1.8 to 5.5 V	0		1,000	ns
SB0, SB1↓ from $\overline{SCK0}$↑	t_{KSB}			t_{KCY5}			ns
$\overline{SCK0}$↓ from SB0, SB1↓	t_{SBK}			t_{KCY5}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY5}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY5}			ns

Note R and C are the load resistance and load capacitance of the $\overline{SCK0}$, SB0, and SB1 output lines.

(vi) SBI mode ($\overline{SCK0}$ ... External clock input) (μPD78005x only)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY6}	4.5 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.0 V ≤ V_{DD} < 4.5 V		3,200			ns
		1.8 V ≤ V_{DD} < 2.0 V		4,800			ns
$\overline{SCK0}$ high-/low-level width	t_{KH6}, t_{KL6}	4.5 V ≤ V_{DD} ≤ 5.5 V		400			ns
		2.0 V ≤ V_{DD} < 4.5 V		1,600			ns
		1.8 V ≤ V_{DD} < 2.0 V		2,400			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK6}	4.5 V ≤ V_{DD} ≤ 5.5 V		100			ns
		2.0 V ≤ V_{DD} < 4.5 V		300			ns
		1.8 V ≤ V_{DD} < 2.0 V		400			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI6}			$t_{KCY6}/2$			ns
Delay time from $\overline{SCK0}$↓ to SB0, SB1 output	t_{KSO6}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 4.5 to 5.5 V	0		300	ns
			V_{DD} = 1.8 to 5.5 V	0		1,000	ns
SB0, SB1↓ from $\overline{SCK0}$↑	t_{KSB}			t_{KCY6}			ns
$\overline{SCK0}$↓ from SB0, SB1↓	t_{SBK}			t_{KCY6}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY6}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY6}			ns
$\overline{SCK0}$ rise/fall time	t_{R6}, t_{F6}	When using external device expansion function				160	ns
		When not using external device expansion function				1,000	ns

Note R and C are the load resistance and load capacitance of the SB0 and SB1 output lines.

(vii) I^2C bus mode (SCL ... Internal clock output) (μPD78005xY only)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCL cycle time	t_{KCY7}	R = 1 KΩ, C = 100 pF[Note]	2.7 V ≤ V_{DD} ≤ 5.5 V	10			μs
			2.0 V ≤ V_{DD} < 2.7 V	20			μs
			1.8 V ≤ V_{DD} < 2.0 V	30			μs
SCL high-level width	t_{KH7}		V_{DD} = 2.7 to 5.5 V	t_{KCY7} – 160			ns
			V_{DD} = 1.8 to 5.5 V	t_{KCY7} – 190			ns
SCL low-level width	t_{KL7}		V_{DD} = 4.5 to 5.5 V	t_{KCY7} – 50			ns
			V_{DD} = 1.8 to 5.5 V	t_{KCY7} – 100			ns
SDA0, SDA1 setup time (to SCL↑)	t_{SIK7}		2.7 V ≤ V_{DD} ≤ 5.5 V	200			ns
			2.0 V ≤ V_{DD} < 2.7 V	300			ns
			1.8 V ≤ V_{DD} < 2.0 V	400			ns
SDA0, SDA1 hold time (from SCL↓)	t_{KSI7}			0			ns
Delay time from SCL↓ to SDA0, SDA1 output	t_{KSO7}		4.5 V ≤ V_{DD} ≤ 5.5 V	0		300	ns
			2.0 V ≤ V_{DD} < 4.5 V	0		500	ns
			1.8 V ≤ V_{DD} < 2.0 V	0		600	ns
SDA0, SDA1↓ from SCL↑ or SDA0, SDA1↑ from SCL↓	t_{KSB}			200			ns
SCL↓ from SDA0, SDA1↓	t_{SBK}		V_{DD} = 2.0 to 5.5 V	400			ns
			V_{DD} = 1.8 to 5.5 V	500			ns
SDA0, SDA1 high-level width	t_{SBH}			500			ns

Note R and C are the load resistance and load capacitance of the SCL, SDA0, and SDA1 output lines.

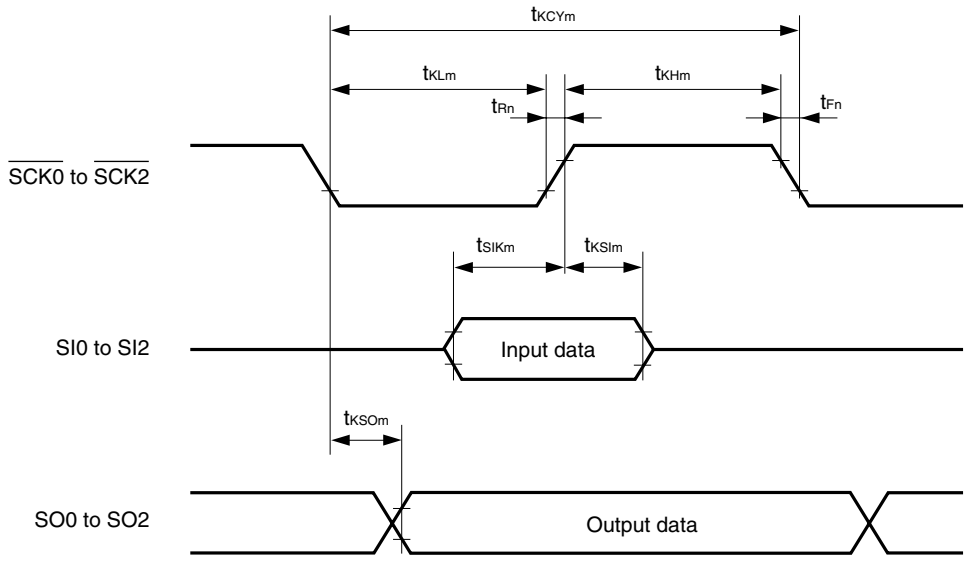
(viii) I^2C bus mode (SCL ... External clock input) (μPD78005xY only)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCL cycle time	t_{KCY8}			1,000			ns
SCL high-/low-level width	t_{KH8}, t_{KL8}	V_{DD} = 2.0 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		600			ns
SDA0, SDA1 setup time (to SCL↑)	t_{SIK8}	V_{DD} = 2.0 to 5.5 V		200			ns
		V_{DD} = 1.8 to 5.5 V			300		ns
SDA0, SDA1 hold time (from SCL↓)	t_{KSI8}			0			ns
Delay time from SCL↓ to SDA0, SDA1 output	t_{KSO8}	R = 1 kΩ, C = 100 pF[Note]	4.5 V ≤ V_{DD} ≤ 5.5 V	0		300	ns
			2.0 V ≤ V_{DD} < 4.5 V	0		500	ns
			1.8 V ≤ V_{DD} < 2.0 V	0		600	ns
SDA0, SDA1↓ from SCL↑ or SDA0, SDA1↑ from SCL↑	t_{KSB}			200			ns
SCL↓ from SDA0, SDA1↓	t_{SBK}	V_{DD} = 2.0 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		500			ns
SDA0, SDA1 high-level width	t_{SBH}	V_{DD} = 2.0 to 5.5 V		500			ns
		V_{DD} = 1.8 to 5.5 V		800			ns
SCL rise/fall time	t_{R8}, t_{F8}	When using external device expansion function				160	ns
		When not using external device expansion function				1	μs

Note R and C are the load resistance and load capacitance of the SDA0 and SDA1 output lines.

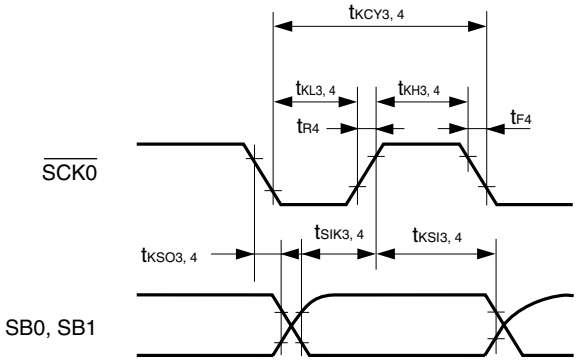
Serial Transfer Timing

3-wire serial I/O mode:

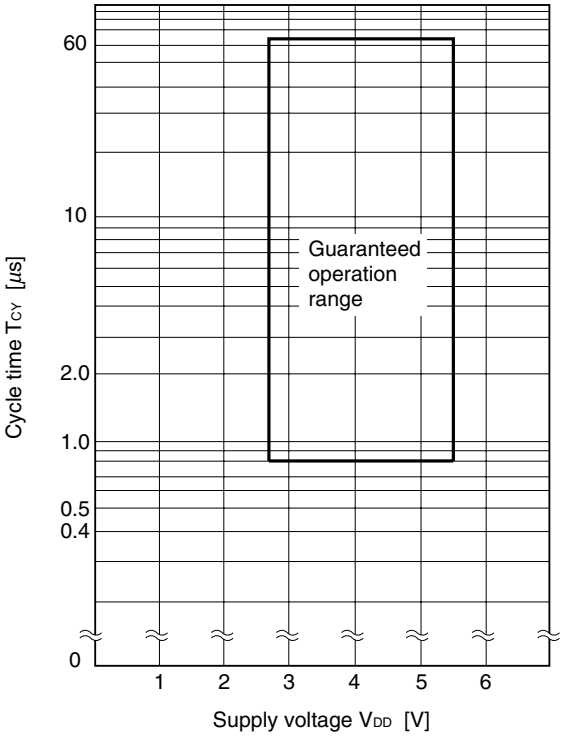


m = 1, 2, 9, 10, 13, 14
n = 2, 10, 14

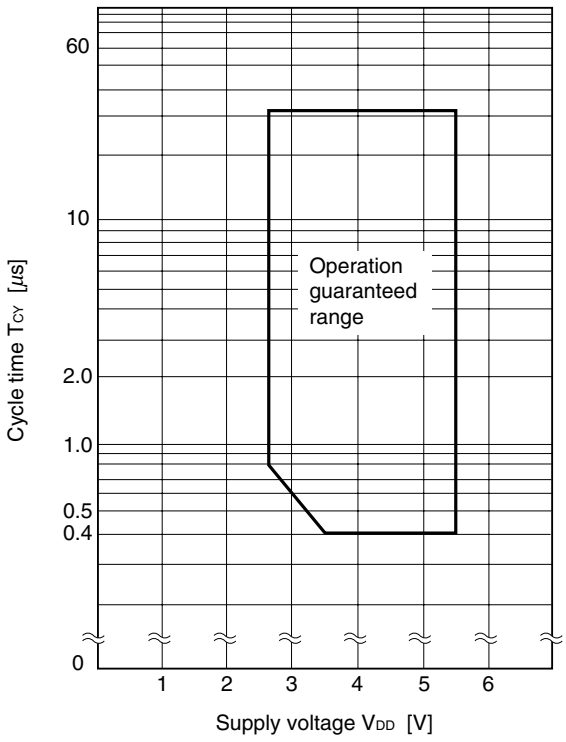
2-wire serial I/O mode:



T_{CY} vs. V_{DD} ($@f_{XX} = f_X/2$ main system clock operation)



T_{CY} vs. V_{DD} ($@f_{XX} = f_X$ main system clock operation)



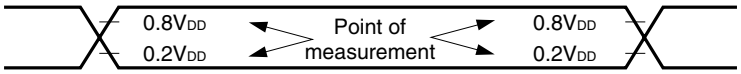
(iii) UART mode (dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		4.5 V ≤ V_{DD} ≤ 5.5 V			78,125	bps
		2.7 V ≤ V_{DD} < 4.5 V			39,063	bps

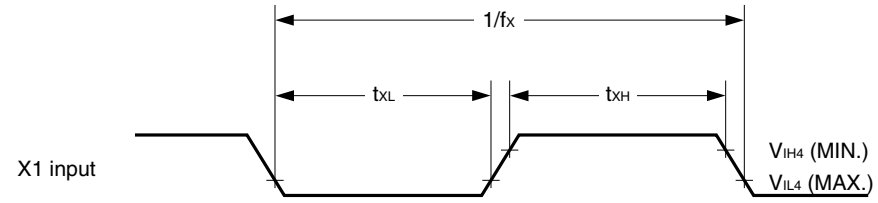
(iv) UART mode (external clock input)

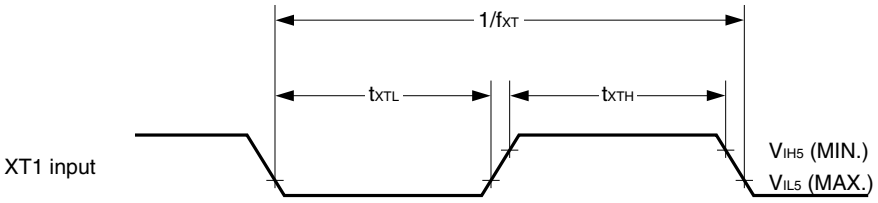
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK cycle time	t_{KCY15}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1,600			ns
ASCK high-/low-level width	t_{KH15}, t_{KL15}	4.5 V ≤ V_{DD} ≤ 5.5 V	400			ns
		2.7 V ≤ V_{DD} < 4.5 V	800			ns
Transfer rate		4.5 V ≤ V_{DD} ≤ 5.5 V			39,063	bps
		2.7 V ≤ V_{DD} < 4.5 V			19,531	bps
ASCK rise/fall time	t_{R15}, t_{F15}	V_{DD} = 4.5 to 5.5 V, when not using external device expansion function.			1,000	ns
		Other than above			160	ns

AC Timing Measurement Points (Excluding X1, XT1 Inputs)

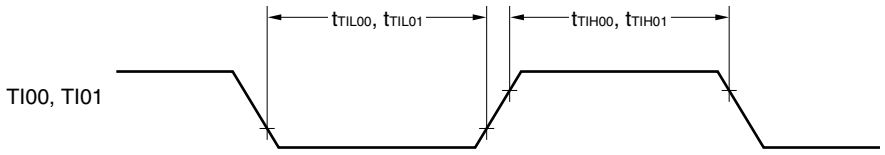


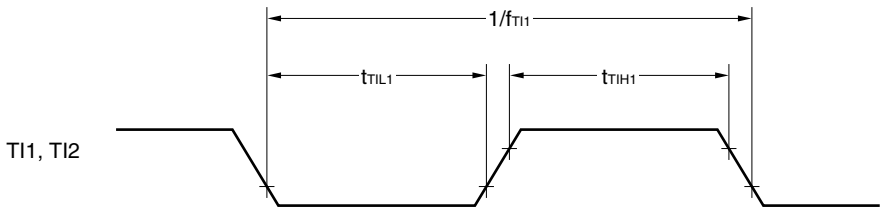
Clock Timing





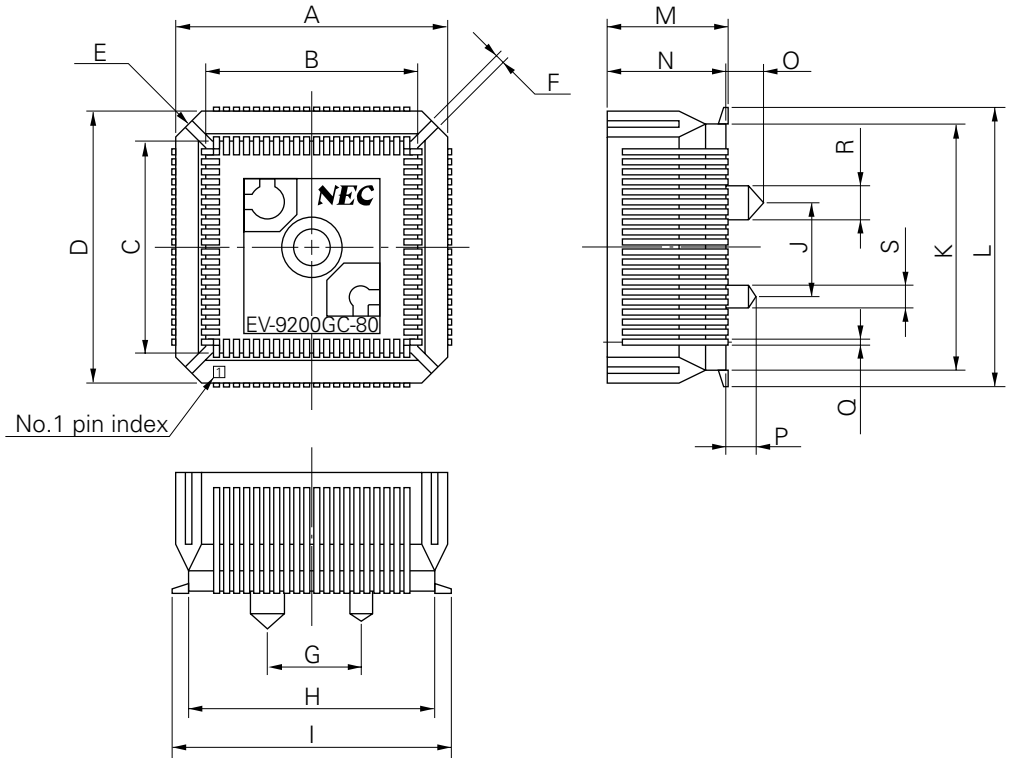
TI Timing





B.9 Drawing and Footprint for Conversion Socket (EV-9200GC-80)

Figure B-2. EV-9200GC-80 Drawing (For Reference Only)



EV-9200GC-80-G0

ITEM	MILLIMETERS	INCHES
A	18.0	0.709
B	14.4	0.567
C	14.4	0.567
D	18.0	0.709
E	4-C 2.0	4-C 0.079
F	0.8	0.031
G	6.0	0.236
H	16.0	0.63
I	18.7	0.736
J	6.0	0.236
K	16.0	0.63
L	18.7	0.736
M	8.2	0.323
O	8.0	0.315
N	2.5	0.098
P	2.0	0.079
Q	0.35	0.014
R	ϕ2.3	ϕ0.091
S	ϕ1.5	ϕ0.059