Renesas Electronics America Inc - UPD78F0058YGK-9EU-A Datasheet

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Major Revisions in This Edition (2/2)

Page	Description
p. 263	Modification of **Figure 14-5 A/D Converter Basic Operation** Addition of **Table 14-2 A/D Conversion Sampling Time and A/D Converter Start Delay Time**
pp. 267, 268	Addition of **14.5 How to Read A/D Converter Characteristics Table**
pp. 269, 270, 272, 273	**14.6 A/D Converter Cautions** Change of description in **(1) Power consumption in standby mode** Addition of **(3) Conflict operations** Addition of **(6) Input impedance of ANI0 to ANI7 pins** Addition of **(10) Timing at which A/D conversion result is undefined** Addition of **(11) Notes on board design** Addition of **(12) AV_{REF0} pin** Addition of **(13) Internal equivalent circuit of ANI0 to ANI7 pins and permissible signal source impedance**
p. 280	Addition of description of processing when D/A converter is not used in **15.5 D/A Converter Cautions (3) AV_{REF1} pin**
p. 379	Addition of **17.4.7 Restrictions in I^2C bus mode 2**
p. 468	Addition of **19.4.5 Restrictions in UART mode 2**
p. 477	Addition of Caution when interrupt is acknowledged to **Figure 21-2 Interrupt Request Flag Register Format**
p. 483	Addition of description on TI01/P01/INTP1 pin to **Figure 21-5 Format of External Interrupt Mode Register 0**
p. 525	Addition of Caution to **25.1 ROM Correction Function**
p. 535	Modification of **Table 26-1 Differences Between μPD78F0058, 78F0058Y and Mask ROM Versions**
pp. 538 to 549	Total revision of description on flash memory programming as **26.3 Flash Memory Characteristics**
pp. 567 to 596	Addition of **CHAPTER 28 ELECTRICAL SPECIFICATIONS (MASK ROM VERSION)**
pp. 597 to 626	Addition of **CHAPTER 29 ELECTRICAL SPECIFICATIONS (FLASH MEMORY VERSION)**
pp. 627 to 657	Addition of **CHAPTER 30 ELECTRICAL SPECIFICATIONS (FLASH MEMORY VERSION (V_{DD} = 2.2 V))**
pp. 658, 659	Addition of **CHAPTER 31 CHARACTERISTICS CURVES (REFERENCE VALUES)**
pp. 660, 661	Addition of **CHAPTER 32 PACKAGE DRAWINGS**
pp. 662 to 665	Addition of **CHAPTER 33 RECOMMENDED SOLDERING CONDITIONS**
pp. 666, 667	Correction of **APPENDIX A DIFFERENCES BETWEEN μPD78054, 78058F, AND 780058 SUBSERIES**
pp. 668 to 684	Total revision of **APPENDIX B DEVELOPMENT TOOLS** Transfer of description of embedded software to **APPENDIX B DEVELOPMENT TOOLS**

The mark ★ shows major revised points.

LIST OF TABLES (3/3)

- Vectored interrupt sources: 21
- Test inputs: 2
- Two types of on-chip clock oscillators (main system clock and subsystem clock)
- ★ Supply voltage: V_{DD} = 1.8 to 5.5 V (mask ROM version)
- ★ V_{DD} = 2.7[Note] to 5.5 V (μPD78F0058)

★ **Note** V_{DD} = 2.2 V can also be supplied to the μPD78F0058. For details, contact an NEC Electronics sales representative.

1.2 Applications

Car audio systems, cellular phones, pagers, printers, AV equipment, cameras, PPCs, vending machines, car electrical components, etc.

★ 1.3 Ordering Information

Part Number	Package	Internal ROM
μPD780053GC-×××-8BT	80-pin plastic QFP (14 × 14)	Mask ROM
μPD780053GK-×××-9EU	80-pin plastic TQFP (fine pitch) (12 × 12)	Mask ROM
μPD780054GC-×××-8BT	80-pin plastic QFP (14 × 14)	Mask ROM
μPD780054GK-×××-9EU	80-pin plastic TQFP (fine pitch) (12 × 12)	Mask ROM
μPD780055GC-×××-8BT	80-pin plastic QFP (14 × 14)	Mask ROM
μPD780055GK-×××-9EU	80-pin plastic TQFP (fine pitch) (12 × 12)	Mask ROM
μPD780056GC-×××-8BT	80-pin plastic QFP (14 × 14)	Mask ROM
μPD780056GK-×××-9EU	80-pin plastic TQFP (fine pitch) (12 × 12)	Mask ROM
μPD780058GC-×××-8BT	80-pin plastic QFP (14 × 14)	Mask ROM
μPD780058GK-×××-9EU	80-pin plastic TQFP (fine pitch) (12 × 12)	Mask ROM
★ μPD780058BGC-×××-8BT	80-pin plastic QFP (14 × 14)	Mask ROM
★ μPD780058BGK-×××-9EU	80-pin plastic TQFP (fine pitch) (12 × 12)	Mask ROM
μPD780053GC(A)-×××-8BT	80-pin plastic QFP (14 × 14)	Special
μPD780054GC(A)-×××-8BT	80-pin plastic QFP (14 × 14)	Special
μPD780055GC(A)-×××-8BT	80-pin plastic QFP (14 × 14)	Special
μPD780056GC(A)-×××-8BT	80-pin plastic QFP (14 × 14)	Special
μPD780058BGC(A)-×××-8BT	80-pin plastic QFP (14 × 14)	Special
μPD78F0058GC-8BT	80-pin plastic QFP (14 × 14)	Flash memory
μPD78F0058GK-9EU	80-pin plastic TQFP (fine pitch) (12 × 12)	Flash memory

Remark ××× indicates ROM code suffix.

For details of the quality grades and their applications, see **Quality Grades on NEC Electronics Semiconductor Devices** (Document No.: C11531E).

2.7 Outline of Functions

Item \ Part Number		μPD780053Y, 780053Y(A)	μPD780054Y, 780054Y(A)	μPD780055Y, 780055Y(A)	μPD780056Y, 780056Y(A)	μPD780058BY 780058BY(A)	μPD78F0058Y
Internal memory	ROM	Mask ROM					Flash memory
		24 KB	32 KB	40 KB	48 KB	60 KB	60 KB[Note 1]
	High-speed RAM	1,024 bytes					
	Buffer RAM	32 bytes					
	Expansion RAM	None				1,024 bytes	1,024 bytes[Note 2]
Memory space		64 KB					
General-purpose registers		8 bits × 8 × 4 banks					
Minimum instruction execution time		Function to vary minimum instruction execution time incorporated					
With main system clock selected		0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (@ 5.0 MHz operation)					
With subsystem clock selected		122 μs (@ 32.768 kHz operation)					
Instruction set		• 16-bit operation • Multiply/divide (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, and boolean operation) • BCD adjust, etc.					
I/O ports		Total: 68 • CMOS input: 2 • CMOS I/O: 62 • N-ch open-drain I/O: 4					
A/D converter		8-bit resolution × 8 channels					
★ Operating voltage range		V_{DD} = 1.8 to 5.5 V					V_{DD} = 2.7 to 5.5 V
D/A converter		8-bit resolution × 2 channels					
★ Operating voltage range		V_{DD} = 1.8 to 5.5 V					V_{DD} = 2.7 to 5.5 V
Serial interface		• 3-wire serial I/O/SBI/2-wire serial I/O mode selection possible: 1 channel • 3-wire serial I/O mode (on-chip max. 32 bytes auto-transmit/receive function): 1 channel • 3-wire serial I/O/UART mode (on-chip time-division transfer function) selectable: 1 channel					
Timer		• 16-bit timer/event counter: 1 channel • 8-bit timer/event counter: 2 channels • Watch timer: 1 channel • Watchdog timer: 1 channel					
Timer outputs		3: (14-bit PWM output enable: 1)					
Clock output		19.5 kHz, 39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz, 2.5 MHz, 5.0 MHz (main system clock: @ 5.0 MHz operation) 32.768 kHz (subsystem clock: @ 32.768 kHz operation)					
Buzzer output		1.2 kHz, 2.4 kHz, 4.9 kHz, 9.8 kHz (main system clock: @ 5.0 MHz operation)					

Notes 1. The capacity of the flash memory can be changed by using the internal memory switching register (IMS).

2. The capacity of the internal expansion RAM can be changed by using the internal expansion RAM size switching register (IXS).

4.2.8 P70 to P72 (Port 7)

P70 to P72 function as a 3-bit I/O port. Besides serving as I/O port pins, they also function as serial interface data I/O and clock I/O.

The following operating modes can be specified in 1-bit units.

(1) Port mode

P70 to P72 function as a 3-bit I/O port. They can be specified as input port or output in 1-bit units using port mode register 7 (PM7). When they are used as input port pins, on-chip pull-up resistors can be connected to them using pull-up resistor option register L (PUOL).

(2) Control mode

P70 to P72 function as serial interface data I/O and clock I/O.

(a) SI2, SO2

These are serial data I/O pins of the serial interface.

(b) $\overline{\text{SCK2}}$

This is a serial clock I/O pin of the serial interface.

(c) RxD0, TxD0

These are serial interface serial data I/O pins of the asynchronous serial interface.

(d) ASCK

This is a serial clock I/O pin of the asynchronous serial interface.

Caution When P70 to P72 are used as serial interface pins, the I/O and output latches must be set according to the function the user requires.
For the setting, see to the operation mode setting list in Table 19-2 Serial Interface Channel 2.

4.2.9 P120 to P127 (Port 12)

P120 to P127 function as an 8-bit I/O port. Besides serving as an I/O port pins, they also function as a real-time output port.

The following operating modes can be specified in 1-bit units.

(1) Port mode

P120 to P127 function as an 8-bit I/O port. They can be specified as input or output port in 1-bit units using port mode register 12 (PM12). When they are used as input port pins, on-chip pull-up resistors can be connected to them using pull-up resistor option register H (PUOH).

(2) Control mode

P120 to P127 function as a real-time output port (RTP0 to RTP7) that outputs data in synchronization with a trigger.

Table 6-2. Port Functions (μPD780058Y Subseries) (2/2)

Pin Name	Function		Alternate Function
P60	Port 6 8-bit I/O port Input/output can be specified in 1-bit units.	N-ch open-drain I/O port On-chip pull-up resistors can be specified by mask option. (Mask ROM version only). LEDs can be driven directly.	—
P61			
P62			
P63			
P64		If used as an input port, an on-chip pull-up resistor can be connected by setting software.	$\overline{RD}$
P65			$\overline{WR}$
P66			$\overline{WAIT}$
P67			ASTB
P70	Port 7 3-bit I/O port Input/output can be specified in 1-bit units. If used as an input port, an on-chip pull-up resistor can be connected by setting software.		SI2/RxD0
P71			SO2/TxD0
P72			$\overline{SCK2}$/ASCK
P120 to P127	Port 12 8-bit I/O port Input/output can be specified in 1-bit units. If used as an input port, on-chip pull-up resistor can be connected by setting software.		RTP0 to RTP7
P130 and P131	Port 13 2-bit I/O port Input/output mode can be specified in 1-bit units. If used as an input port, on-chip pull-up resistor can be connected by setting software.		ANO0, ANO1

(2) External event counter

The number of pulses of an externally input signal can be measured.

(3) Square-wave output

A square wave with any selected frequency can be output.

Table 9-4. Square-Wave Output Ranges When 8-Bit Timer/Event Counters 1 and 2 Are Used as 16-Bit Timer/Event Counter

Minimum Pulse Time		Maximum Pulse Time		Resolution	
MCS = 1	MCS = 0	MCS = 1	MCS = 0	MCS = 1	MCS = 0
$2 \times 1/f_X$ (400 ns)	$2^2 \times 1/f_X$ (800 ns)	$2^{17} \times 1/f_X$ (26.2 ms)	$2^{18} \times 1/f_X$ (52.4 ms)	$2 \times 1/f_X$ (400 ns)	$2^2 \times 1/f_X$ (800 ns)
$2^2 \times 1/f_X$ (800 ns)	$2^3 \times 1/f_X$ (1.6 μs)	$2^{18} \times 1/f_X$ (52.4 ms)	$2^{19} \times 1/f_X$ (104.9 ms)	$2^2 \times 1/f_X$ (800 ns)	$2^3 \times 1/f_X$ (1.6 μs)
$2^3 \times 1/f_X$ (1.6 μs)	$2^4 \times 1/f_X$ (3.2 μs)	$2^{19} \times 1/f_X$ (104.9 ms)	$2^{20} \times 1/f_X$ (209.7 ms)	$2^3 \times 1/f_X$ (1.6 μs)	$2^4 \times 1/f_X$ (3.2 μs)
$2^4 \times 1/f_X$ (3.2 μs)	$2^5 \times 1/f_X$ (6.4 μs)	$2^{20} \times 1/f_X$ (209.7 ms)	$2^{21} \times 1/f_X$ (419.4 ms)	$2^4 \times 1/f_X$ (3.2 μs)	$2^5 \times 1/f_X$ (6.4 μs)
$2^5 \times 1/f_X$ (6.4 μs)	$2^6 \times 1/f_X$ (12.8 μs)	$2^{21} \times 1/f_X$ (419.4 ms)	$2^{22} \times 1/f_X$ (838.9 ms)	$2^5 \times 1/f_X$ (6.4 μs)	$2^6 \times 1/f_X$ (12.8 μs)
$2^6 \times 1/f_X$ (12.8 μs)	$2^7 \times 1/f_X$ (25.6 μs)	$2^{22} \times 1/f_X$ (838.9 ms)	$2^{23} \times 1/f_X$ (1.7 s)	$2^6 \times 1/f_X$ (12.8 μs)	$2^7 \times 1/f_X$ (25.6 μs)
$2^7 \times 1/f_X$ (25.6 μs)	$2^8 \times 1/f_X$ (51.2 μs)	$2^{23} \times 1/f_X$ (1.7 s)	$2^{24} \times 1/f_X$ (3.4 s)	$2^7 \times 1/f_X$ (25.6 μs)	$2^8 \times 1/f_X$ (51.2 μs)
$2^8 \times 1/f_X$ (51.2 μs)	$2^9 \times 1/f_X$ (102.4 μs)	$2^{24} \times 1/f_X$ (3.4 s)	$2^{25} \times 1/f_X$ (6.7 s)	$2^8 \times 1/f_X$ (51.2 μs)	$2^9 \times 1/f_X$ (102.4 μs)
$2^9 \times 1/f_X$ (102.4 μs)	$2^{10} \times 1/f_X$ (204.8 μs)	$2^{25} \times 1/f_X$ (6.7 s)	$2^{26} \times 1/f_X$ (13.4 s)	$2^9 \times 1/f_X$ (102.4 μs)	$2^{10} \times 1/f_X$ (204.8 μs)
$2^{11} \times 1/f_X$ (409.6 μs)	$2^{12} \times 1/f_X$ (819.2 μs)	$2^{27} \times 1/f_X$ (26.8 s)	$2^{28} \times 1/f_X$ (53.7 s)	$2^{11} \times 1/f_X$ (409.6 μs)	$2^{12} \times 1/f_X$ (819.2 μs)

Remarks 1. f_X: Main system clock oscillation frequency

2. MCS: Bit 0 of oscillation mode select register (OSMS)

3. Values in parentheses apply to operation with f_X = 5.0 MHz.

(2) Interval timer mode

Interrupt requests are generated at the preset time intervals.

Table 11-2. Interval Times

Interval Time	MCS = 1	MCS = 0
$2^{11} \times 1/f_{XX}$	$2^{11} \times 1/f_X$ (410 μs)	$2^{12} \times 1/f_X$ (819 μs)
$2^{12} \times 1/f_{XX}$	$2^{12} \times 1/f_X$ (819 μs)	$2^{13} \times 1/f_X$ (1.64 ms)
$2^{13} \times 1/f_{XX}$	$2^{13} \times 1/f_X$ (1.64 ms)	$2^{14} \times 1/f_X$ (3.28 ms)
$2^{14} \times 1/f_{XX}$	$2^{14} \times 1/f_X$ (3.28 ms)	$2^{15} \times 1/f_X$ (6.55 ms)
$2^{15} \times 1/f_{XX}$	$2^{15} \times 1/f_X$ (6.55 ms)	$2^{16} \times 1/f_X$ (13.1 ms)
$2^{16} \times 1/f_{XX}$	$2^{16} \times 1/f_X$ (13.1 ms)	$2^{17} \times 1/f_X$ (26.2 ms)
$2^{17} \times 1/f_{XX}$	$2^{17} \times 1/f_X$ (26.2 ms)	$2^{18} \times 1/f_X$ (52.4 ms)
$2^{19} \times 1/f_{XX}$	$2^{19} \times 1/f_X$ (104.9 ms)	$2^{20} \times 1/f_X$ (209.7 ms)

Remarks 1. f_{XX}: Main system clock frequency (f_X or $f_X/2$)

2. f_X: Main system clock oscillation frequency

3. MCS: Bit 0 of oscillation mode select register (OSMS)

4. Values in parentheses apply to operation with f_X = 5.0 MHz.

CHAPTER 14 A/D CONVERTER

14.1 A/D Converter Functions

The A/D converter converts an analog input into a digital value. It consists of 8 channels (ANI0 to ANI7) with an 8-bit resolution.

The conversion method is based on successive approximation and the conversion result is held in the 8-bit A/D conversion result register (ADCR).

A/D conversion can be started in the following two ways.

(1) Hardware start

Conversion is started by trigger input (INTP3).

(2) Software start

Conversion is started by setting the A/D converter mode register (ADM).

One analog input channel is selected from ANI0 to ANI7 and A/D conversion is carried out. In the case of hardware start, A/D conversion stops when an A/D conversion operation ends, and an interrupt request (INTAD) is generated. In the case of software start, A/D conversion is repeated. Each time an A/D conversion operation ends, an interrupt request (INTAD) is generated.

14.2 A/D Converter Configuration

The A/D converter consists of the following hardware.

Table 14-1. A/D Converter Configuration

Item	Configuration
Analog inputs	8 channels (ANI0 to ANI7)
Control registers	A/D converter mode register (ADM) A/D converter input select register (ADIS) External interrupt mode register 1 (INTM1)
Registers	Successive approximation register (SAR) A/D conversion result register (ADCR)

(2) A/D converter input select register (ADIS)

This register determines whether the ANI0/P10 to ANI7/P17 pins should be used for analog input channels or ports. Pins other than those selected as analog input can be used as I/O ports.

ADIS is set with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears ADIS to 00H.

Cautions 1. Set the analog input channel using the following procedure.

(1) Set the number of analog input channels using ADIS.

(2) Using the A/D converter mode register (ADM), select one channel to undergo A/D conversion from among the channels set to analog input by ADIS.

2. No internal pull-up resistor can be used for the channels set to analog input by ADIS, irrespective of the value of bit 1 (PUO1) of pull-up resistor option register L (PUOL).

Figure 14-3. Format of A/D Converter Input Select Register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
ADIS	0	0	0	0	ADIS3	ADIS2	ADIS1	ADIS0	FF84H	00H	R/W

ADIS3	ADIS2	ADIS1	ADIS0	Number of analog input channel selection
0	0	0	0	No analog input channel (P10 to P17)
0	0	0	1	1 channels (ANI0, P11 to P17)
0	0	1	0	2 channels (ANI0, ANI1, P12 to P17)
0	0	1	1	3 channels (ANI0 to ANI2, P13 to P17)
0	1	0	0	4 channels (ANI0 to ANI3, P14 to P17)
0	1	0	1	5 channels (ANI0 to ANI4, P15 to P17)
0	1	1	0	6 channels (ANI0 to ANI5, P16, P17)
0	1	1	1	7 channels (ANI0 to ANI6, P17)
1	0	0	0	8 channels (ANI0 to ANI7)
Other than above				Setting prohibited

16.4 Operations of Serial Interface Channel 0

The following four operating modes are available for serial interface channel 0.

- Operation stop mode
- 3-wire serial I/O mode
- SBI mode
- 2-wire serial I/O mode

16.4.1 Operation stop mode

Serial transfer is not carried out in the operation stop mode. Thus, power consumption can be reduced. Serial I/O shift register 0 (SIO0) does not carry out shift operations either and thus it can be used as an ordinary 8-bit register.

In the operation stop mode, the P25/SI0/SB0, P26/SO0/SB1, and P27/$\overline{SCK0}$ pins can be used as ordinary I/O ports.

(1) Register setting

The operation stop mode is set by serial operating mode register 0 (CSIM0).

CSIM0 is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{RESET}$ input clears CSIM0 to 00H.

Symbol	<7>	<6>	<5>	4	3	2	1	0	Address	After reset	R/W
CSIM0	CSIE0	COI	WUP	CSIM04	CSIM03	CSIM02	CSIM01	CSIM00	FF60H	00H	R/W

R/W	CSIE0	Serial interface channel 0 operation control
	0	Operation stopped
	1	Operation enabled

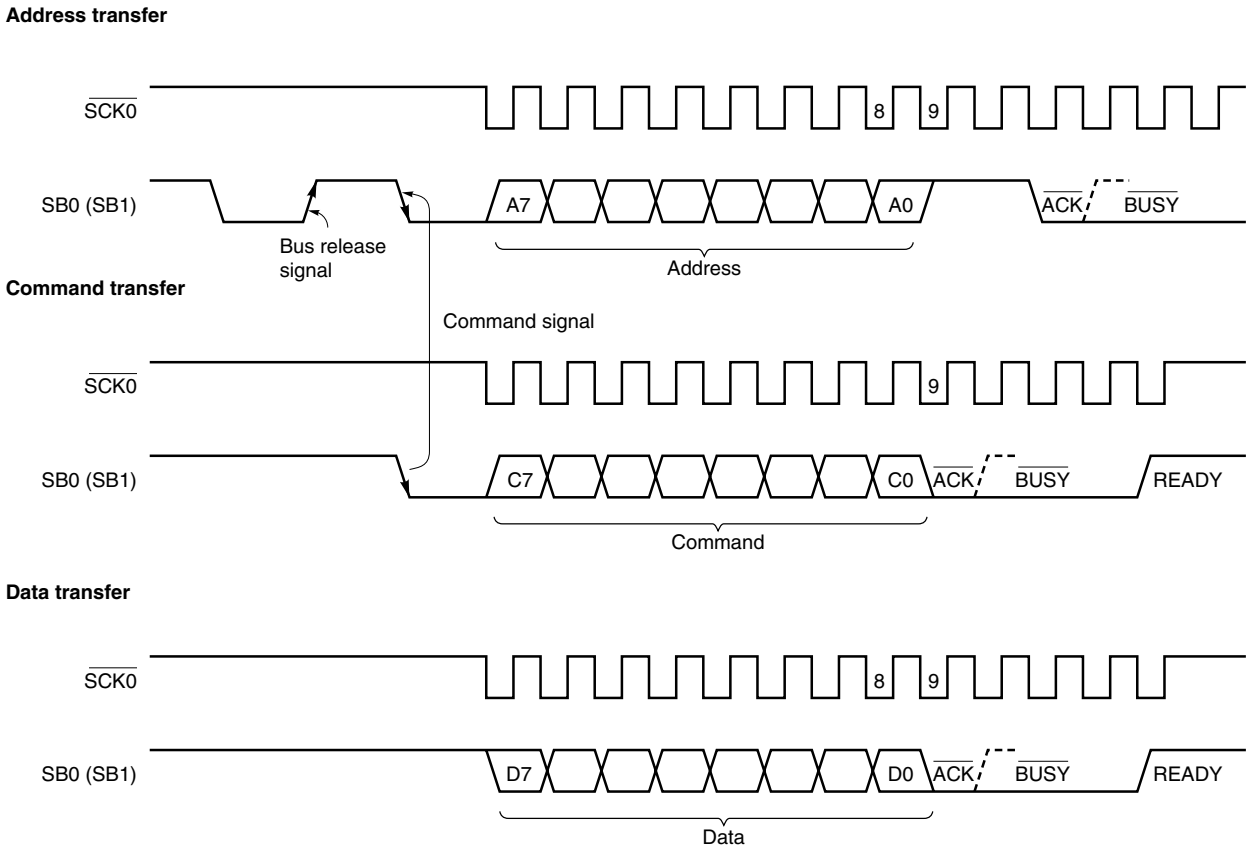
(2) SBI definition

The SBI serial data format and the signals to be used are defined as follows.

Serial data to be transferred by SBI consists of three kinds of data: “address”, “command”, and “data”.

Figure 16-11 shows the address, command, and data transfer timing.

Figure 16-11. SBI Transfer Timing



Remark The broken lines indicate the READY status.

The bus release signal and the command signal are output by the master device. $\overline{\text{BUSY}}$ is output by the slave device. $\overline{\text{ACK}}$ can be output by either the master or slave device (normally, the 8-bit data receiver outputs). Serial clocks continue to be output by the master device from 8-bit data transfer start to $\overline{\text{BUSY}}$ reset.

(2) Serial operating mode register 0 (CSIM0)

This register sets the serial interface channel 0 serial clock, operating mode, operation enable/stop wakeup function and displays the address comparator match signal.

CSIM0 is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears CSIM0 to 00H.

Caution Do not change the operating mode (3-wire serial I/O, 2-wire serial I/O, or SBI) while serial interface channel 0 is enabled to operate. To change the operating mode, stop the serial operation first.

Figure 17-4. Format of Serial Operating Mode Register 0

Symbol	<7>	<6>	<5>	4	3	2	1	0	Address	After reset	R/W
CSIM0	CSIE0	COI	WUP	CSIM04	CSIM03	CSIM02	CSIM01	CSIM00	FF60H	00H	R/W Note 1

R/W

CSIM01	CSIM00	Serial interface channel 0 clock selection
0	×	Input clock to $\overline{\text{SCK0}}$/SCL pin from off-chip
1	0	8-bit timer register 2 (TM2) output Note 2
1	1	Clock specified by bits 0 to 3 of timer clock select register 3 (TCL3)

R/W

CSIM 04	CSIM 03	CSIM 02	PM25	P25	PM26	P26	PM27	P27	Operation mode	Start Bit	SI0/SB0/SDA0/ P25 pin function	SO0/SB1/SDA1/ P26 pin function	$\overline{\text{SCK0}}$/SCL/P27 pin function
0	×	0	Note 3 1	Note 3 ×	0	0	0	1	3-wire serial I/O mode	MSB	SI0 Note 3 (Input)	SO0 (CMOS output)	$\overline{\text{SCK0}}$ (CMOS I/O)
		1								LSB			
1	1	0	Note 4 ×	Note 4 ×	0	0	0	1	2-wire serial I/O mode or I^2C bus mode	MSB	P25 (CMOS I/O)	SB1/SDA1 (N-ch open-drain I/O)	$\overline{\text{SCK0}}$/SCL (N-ch open-drain I/O)
		1	0	0	Note 4 ×	Note 4 ×	0	1			SB0/SDA0 (N-ch open-drain	P26 (CMOS I/O)	

R/W

WUP	Wake-up function control Note 5
0	Interrupt request signal generation with each serial transfer in any mode
1	Interrupt request signal generation when the address received after detecting start condition (when CMDD = 1) matches the slave address register (SVA) data in I^2C bus mode

R

COI	Slave address comparison result flag Note 6
0	Slave address register (SVA) not equal to serial I/O shift register 0 (SIO0) data
1	Slave address register (SVA) equal to serial I/O shift register 0 (SIO0) data

R/W

CSIE0	Serial interface channel 0 operation control
0	Operation stopped
1	Operation enabled

Notes 1. Bit 6 (COI) is a read-only bit.

2. In I^2C bus mode, the clock frequency becomes 1/16 of that output from TO2.

3. Can be used as P25 (CMOS input/output) when used only for transmission.

4. Can be used freely as a port function.

5. To use the wakeup function (WUP = 1), set bit 5 (SIC) of the interrupt timing specification register (SINT) to 1. Do not execute an instruction that writes serial I/O shift register 0 (SIO0) while WUP = 1.

6. When CSIE0 = 0, COI becomes 0.

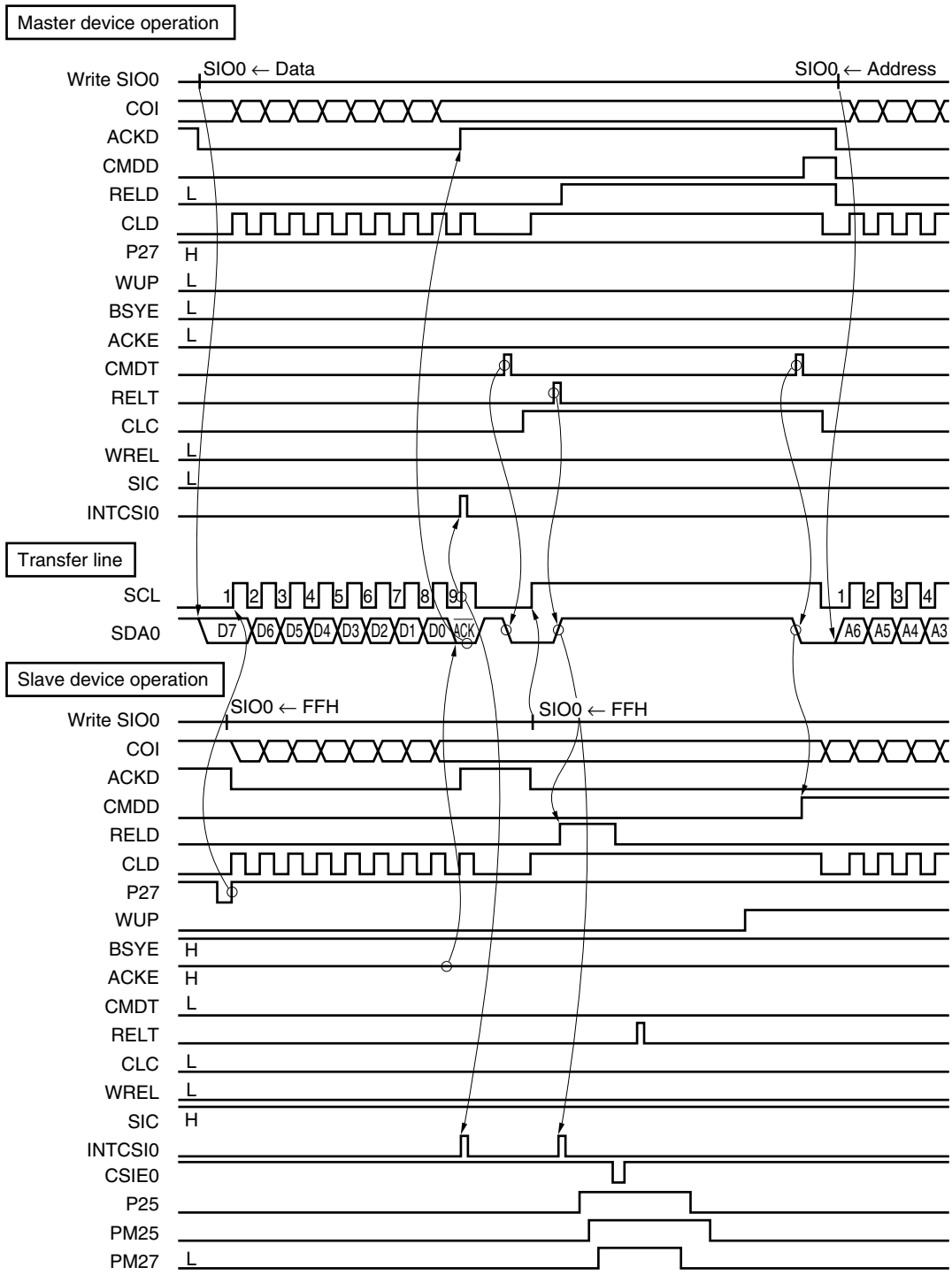
Remark ×: don't care

PM××: Port mode register

P××: Port output latch

Figure 17-22. Data Transmission from Master to Slave (Both Master and Slave Selected 9-Clock Wait) (3/3)

(c) Stop condition



A/D Converter Characteristics (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error[Note 1]		2.7 V ≤ AV_{REF0} < 4.5 V			±1.0	%FSR
		4.5 V ≤ AV_{REF0} ≤ 5.5 V			±0.6	%FSR
Conversion time	T_{CONV}	2.7 V ≤ AV_{REF0} ≤ 5.5 V	16		100	μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF0}	V
Reference voltage	AV_{REF0}		2.7		V_{DD}	V
AV_{REF0} current	I_{REF0}	When A/D converter is operating[Note 2]		500	1,500	μA
		When A/D converter is not operating[Note 3]		0	3	μA

Notes 1. Excludes quantization error (±1/2 LSB). This value is indicated as a ratio to the full-scale value (%FSR).
2. The current flowing to the AV_{REF0} pin when bit 7 (CS) of the A/D converter mode register (ADM) is 1.
3. The current flowing to the AV_{REF0} pin when bit 7 (CS) of the A/D converter mode register (ADM) is 0.

D/A Converter Characteristics (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution					8	bit
Overall error		R = 2 MΩ[Note 1]			±1.2	%
		R = 4 MΩ[Note 1]			±0.8	%
		R = 10 MΩ[Note 1]			±0.6	%
Settling time		C = 30 pF[Note 1]			15	μs
Output resistance	R_O	**Note 2**		8		kΩ
Analog reference voltage	AV_{REF1}		1.8		V_{DD}	V
AV_{REF1} current	I_{REF1}	**Note 2**			2.5	mA
Resistance between AV_{REF1} and AV_{SS}	R_{AIREF1}	DACS0, DACS1 = 55H[Note 2]	4	8		kΩ

Notes 1. R and C are the D/A converter output pin load resistance and load capacitance, respectively.
2. Value for one D/A converter channel

Remark DACS0 and DACS1: D/A conversion value set registers 0, 1

(b) Serial interface channel 1

(i) 3-wire serial I/O mode ($\overline{SCK1}$ ... Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY9}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1,600			ns
		2.2 V ≤ V_{DD} < 2.7 V	3,200			ns
$\overline{SCK1}$ high-/low-level width	t_{KH9}, t_{KL9}	V_{DD} = 4.5 to 5.5 V	$t_{KCY9}/2 - 50$			ns
		V_{DD} = 2.2 to 5.5 V	$t_{KCY9}/2 - 100$			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK9}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
		2.2 V ≤ V_{DD} < 2.7 V	300			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI9}		400			ns
SO1 output delay time from $\overline{SCK1}$↓	t_{KSO9}	C = 100 pF[Note]			300	ns

Note C is the load capacitance of the $\overline{SCK1}$ and SO1 output lines.

(ii) 3-wire serial I/O mode ($\overline{SCK1}$ ... External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY10}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1,600			ns
		2.2 V ≤ V_{DD} < 2.7 V	3,200			ns
$\overline{SCK1}$ high-/low-level width	t_{KH10}, t_{KL10}	4.5 V ≤ V_{DD} ≤ 5.5 V	400			ns
		2.7 V ≤ V_{DD} < 4.5 V	800			ns
		2.2 V ≤ V_{DD} < 2.7 V	1,600			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK10}		100			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KIS10}		400			ns
SO1 output delay time from $\overline{SCK1}$↓	t_{KSO10}	C = 100 pF[Note]			300	ns
$\overline{SCK1}$ rise/fall time	t_{R10}, t_{F10}	When using external device expansion function			160	ns
		When not using external device expansion function			1,000	ns

Note C is the load capacitance of the SO1 output line.

Remark ××××in the part number differs depending on the host machine and OS used.

μS××××RA78K0
μS××××CC78K0

××××	Host Machine	OS	Supply Medium
AB13	PC-9800 series, IBM PC/AT and compatibles	Windows (Japanese version)	3.5-inch 2HD FD
BB13		Windows (English version)	
AB17		Windows (Japanese version)	CD-ROM
BB17		Windows (English version)	
3P17	HP9000 series 700™	HP-UX™ (Rel. 10.10)	
3K17	SPARCstation™	SunOS™ (Rel. 4.1.4), Solaris™ (Rel. 2.5.1)	

μS××××DF780058
μS××××CC78K0-L

××××	Host Machine	OS	Supply Medium
AB13	PC-9800 series, IBM PC/AT and compatibles	Windows (Japanese version)	3.5-inch 2HD FD
BB13		Windows (English version)	
3P16	HP9000 series 700	HP-UX (Rel. 10.10)	DAT
3K13	SPARCstation	SunOS (Rel. 4.1.4), Solaris (Rel. 2.5.1)	3.5-inch 2HD FD
3K15			1/4-inch CGMT

B.3 Control Software

Project Manager	This is control software designed to enable efficient user program development in the Windows environment. All operations used in development of a user program, such as starting the editor, building, and starting the debugger, can be performed from the Project Manager. **<Caution>** The Project Manager is included in the assembler package (RA78K0). It can only be used in Windows.

B.4 Flash Memory Writing Tools

Flashpro III (Part number: FL-PR3, PG-FP3) Flashpro IV (Part number: FL-PR4, PG-FP4) Flash programmer	Flash programmer dedicated to microcontrollers with on-chip flash memory.
FA-80GC-8BT FA-80GK-9EU Flash memory writing adapter	Flash memory writing adapter used connected to Flashpro III/Flashpro IV. • FA-80GC-8BT: 80-pin plastic QFP (GC-8BT type) • FA-80GK-9EU: 80-pin plastic TQFP (GK-9EU type)

Remark FL-PR3, FL-PR4, FA-80GC-8EU, and FA-80GK-9EU are products of Naito Densei Machida Mfg. Co., Ltd.
Contact: +81-45-475-4191 Naito Densei Machida Mfg. Co., Ltd.

Edition	Revisions	Chapter
3rd edition	Deletion of following product • μPD780058Y	Throughout
	Addition of following products • μPD780058B, 780058BY, 780053(A), 780053Y(A), 780054(A), 780054Y(A), 780055(A), 780055Y(A), 780056(A), 780056Y(A), 780058B(A), 780058BY(A)	
	Deletion of following packages • 80-pin plastic QFP (GC-3B9 type) • 80-pin plastic TQFP (GK-BE9 type)	
	Addition of following package • 80-pin plastic TQFP (GK-9EU type)	
	1.1 Features, 1.7 Outline of Functions • Change of operating voltage range of A/D and D/A converters of μPD780058 and 78F0058 • Change of supply voltage of μPD78F0058	**CHAPTER 1 OUTLINE (μPD780058 SUBSERIES)**
	Addition of **1.9 Differences Between Standard Model and (A) Model**	
	2.1 Features, 2.7 Outline of Functions • Change of operating voltage range of A/D and D/A converters of μPD78F0058Y • Change of supply voltage of μPD78F0058Y	**CHAPTER 2 OUTLINE (μPD780058Y SUBSERIES)**
	Addition of **2.9 Differences Between Standard Model and (A) Model**	
	Change of processing when A/D converter is not used in **3.2.11 AV_{REF0}**	**CHAPTER 3 PIN FUNCTIONS (μPD780058 SUBSERIES)**
	Change of recommended connection of unused pins and connection of P60 to P63, AV_{REF1}, and V_{PP} pins in **Table 3-1 Pin I/O Circuit Types**	
	Change of processing when A/D converter is not used in **4.2.11 AV_{REF0}**	**CHAPTER 4 PIN FUNCTIONS (μPD780058Y SUBSERIES)**
	Change of recommended connection of unused pins and connection of P60 to P63, AV_{REF1}, and V_{PP} pins in **Table 4-1 Pin I/O Circuit Types**	
	Modification of Note 2 in **6.2.8 Port 6**	**CHAPTER 6 PORT FUNCTIONS**
	Addition of note on feedback resistor to **Figure 7-3 Format of Processor Clock Control Register**	**CHAPTER 7 CLOCK GENERATOR**
	Addition of **Table 8-5 INTP1/TI01 Pin Valid Edge and CR00 Capture Trigger Valid Edge**	**CHAPTER 8 16-BIT TIMER/EVENT COUNTER**
	Addition of **Table 8-6 INTP0/TI00 Pin Valid Edge and CR01 Capture Trigger Valid Edge**	
	Correction of note on valid edge of INTP0/TI00/P00 and INTP1/TI01/P01 pin in **Figure 8-8 Format of External Interrupt Mode Register 0**	
	Addition of **Figure 8-17 Configuration of PPG Output** Addition of **Figure 8-18 PPG Output Operation Timing**	
	8.5 16-Bit Timer/Event Counter Operating Cautions Addition of description on TI01/P01/INTP1 to **(5) Valid edge setting** Addition of **(c) One-shot pulse output function** to **(6) Re-trigger of one-shot pulse** Addition of **(8) Conflict operation** Addition of **(9) Timer operation** Addition of **(10) Capture operation** Addition of **(11) Compare operation** Addition of **(12) Edge detection**	
	Modification of note on changing count clock in **Figure 10-2 Format of Timer Clock Select Register 2**	**CHAPTER 10 WATCH TIMER**

Edition	Revisions	Chapter
3rd edition	Modification of note on changing count clock in **Figure 11-2 Format of Timer Clock Select Register 2**	**CHAPTER 11 WATCHDOG TIMER**
	Addition of note on rewriting TCL2 in **Figure 13-2 Format of Timer Clock Select Register 2**	**CHAPTER 13 BUZZER OUTPUT CONTROLLER**
	Modification of **Figure 14-5 A/D Converter Basic Operation** Addition of **Table 14-2 A/D Conversion Sampling Time and A/D Converter Start Delay Time**	**CHAPTER 14 A/D CONVERTER**
	Addition of **14.5 How to Read A/D Converter Characteristics Table**	
	14.6 A/D Converter Cautions Change of description in **(1) Power consumption in standby mode** Addition of **(3) Conflicting operations** Addition of **(6) Input impedance of ANI0 to ANI7 pins** Addition of **(10) Timing at which A/D conversion result is undefined** Addition of **(11) Notes on board design** Addition of **(12) AV_{REF0} pin** Addition of **(13) Internal equivalent circuit of ANI0 to ANI7 pins and permissible signal source impedance**	
	Addition of description of processing when D/A converter is not used in **15.5 D/A Converter Cautions (3) AV_{REF1} pin**	**CHAPTER 15 D/A CONVERTER**
	Addition of **17.4.7 Restrictions in I^2C bus mode 2**	**CHAPTER 17 SERIAL INTERFACE CHANNEL 0 (μPD780058Y SUBSERIES)**
	Addition of **19.4.5 Restrictions in UART mode 2**	**CHAPTER 19 SERIAL INTERFACE CHANNEL 2**
	Addition of Caution when interrupt is acknowledged to **Figure 21-2 Format of Interrupt Request Flag Register**	**CHAPTER 21 INTERRUPT AND TEST FUNCTIONS**
	Addition of description on TI01/P01/INTP1 pin to **Figure 21-5 Format of External Interrupt Mode Register 0**	
	Addition of Caution to **25.1 ROM Correction Function**	**CHAPTER 25 ROM CORRECTION**
	Modification of **Table 26-1 Differences Between μPD78F0058, 78F0058Y and Mask ROM Versions**	**CHAPTER 26 μPD78F0058, 78F0058Y**
	Total revision of description on flash memory programming as **26.3 Flash Memory Characteristics**	
	Addition of **CHAPTER 28 ELECTRICAL SPECIFICATIONS (MASK ROM VERSION)**	**CHAPTER 28 ELECTRICAL SPECIFICATIONS (MASK ROM VERSION)**
	Addition of **CHAPTER 29 ELECTRICAL SPECIFICATIONS (FLASH MEMORY VERSION)**	**CHAPTER 29 ELECTRICAL SPECIFICATIONS (FLASH MEMORY VERSION)**
	Addition of **CHAPTER 30 ELECTRICAL SPECIFICATIONS (FLASH MEMORY VERSION (V_{DD} = 2.2 V))**	**CHAPTER 30 ELECTRICAL SPECIFICATIONS (FLASH MEMORY VERSION (V_{DD} = 2.2 V))**
	Addition of **CHAPTER 31 CHARACTERISTICS CURVES (REFERENCE VALUES)**	**CHAPTER 31 CHARACTERISTICS CURVES (REFERENCE VALUES)**
	Addition of **CHAPTER 32 PACKAGE DRAWINGS**	**CHAPTER 32 PACKAGE DRAWINGS**

Edition	Revisions	Chapter
3rd edition	Addition of **CHAPTER 33 RECOMMENDED SOLDERING CONDITIONS**	**CHAPTER 33 RECOMMENDED SOLDERING CONDITIONS**
	Correction of **APPENDIX A DIFFERENCES BETWEEN μPD78054, 78058F, AND 780058**	**APPENDIX A DIFFERENCES BETWEEN μPD78054, 78058F, AND 780058 SUBSERIES**
	Total revision of **APPENDIX B DEVELOPMENT TOOLS** Transfer of description of embedded software to **APPENDIX B DEVELOPMENT TOOLS**	**APPENDIX B DEVELOPMENT TOOLS**