Welcome to E-XFL.COM

Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	DAI/O, EBI/EMI, I²C, Parallel, SPI
Clock Rate	25MHz
Non-Volatile Memory	ROM (144kB)
On-Chip RAM	82kB
Voltage - I/O	3.30V
Voltage - Core	1.80V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	128-LQFP (20x14)
Purchase URL	https://www.e-xfl.com/product-detail/cirrus-logic/cs497014-cvzr

Table 2. Device and Firmware Selection Guide

Device	Decode Processor (DSP-A)[1]	Matrix Processor Module (DSP-A)[1]	Virtualizer Processor Module (DSP-B)[1]	Post Processor Module (DSP-B)[1]
CS497014 300MACS	Stereo PCM (4:1/2:1 Down-sampling and 1:2/1:4 U-sampling Options)[2] Multichannel PCM (4:1/2:1 Down-sampling and 1:2/1:4 Up-sampling Options)[2] Dolby Digital MPEG-2 AAC LC 5.1 Dolby Digital Plus Dolby TrueHD[3]	Dolby Pro Logic II / IIx / IIz 7.1 SRS Circle Surround II / Circle Surround Auto / Circle Surround Decoder Optimized (Stereo In) Cirrus Original Multi-Channel Surround 2 (Effects / Reverb Processor) Crossbar (Down-mix / Up-mix) (Simultaneous Process)	Cirrus Virtualizer Technology Dolby Headphone 2 Dolby Virtual Speaker 2 SRS CS Headphone SRS TruSurround HD/HD4	APP (Advanced Post-processing) –Tone Control –Select 2 –PEQ (up to 11 Bands) –Delay (Speaker to Listening Position Alignment and/or Lip Sync) –7.1 Bass Manager –Audio Manager –4:1/2:1 Down-sampling[2] SRS TruVolume 7.1 Multichannel Dolby Volume Multichannel
CS497004 300MACS **CS497024** 300MACS	Same as CS497014 + DTS, DTS-ES, DTS96/24 DTS-HD Master Audio[3] DTS-HD High Res Audio[3] DTS Express 5.1	Same as CS497014 + DTS Neo:6, DTS Neural Surround		

1. Additional processing (MPMA, MPMB/VPM, PPM) post any of the HD audio decoders may be limited. Contact your Cirrus Logic FAE for the latest concurrency matrix.
2. Downsampling and Upsampling functionality is located in the operating system. The Cirrus Decimator (Down-Sampler) is also available as a separate post-processing module that is described in the application note AN288PPI.
3. The indicated HD audio decoder algorithms require external SDRAM. Consult your Cirrus Logic FAE for the recommended SDRAM size for your design.

2.1 Migrating from CS495xx(3) to CS4970x4

CS4970x4 was designed to provide an easy upgrade path from the CS495xx and CS4953x. There are some small differences the hardware designer should be aware of:

- The PLL supply voltage on the CS4970x4 is 3.3V vs. 1.8V on the CS495xx.
- The PLL filter topology is simpler when using the CS4970x4 rather than the CS495xx.
- The CS4970x4 adds support for Time-division multiplexing (TDM) mode on both audio input and output ports.
- The CS4970x4 does not support external static random access memory (SRAM) operation.
- The CS4970x4 external Synchronous dynamic random access memory (SDRAM) bus speed is fixed at 150 MHz vs. the 120 MHz maximum bus speed for the CS495xx. Some firmware modules also support a 75 MHz CS4970x4 SDRAM bus speed. Refer to AN304 for details.
- The CS4970x4 CLKOUT pin can output XTALI or XTALI/2. The CS495xx can only output XTALI.

2.2 Licensing

Licenses are required for all of the third party audio decoding/processing algorithms listed below, including the application notes. Contact your local Cirrus Sales representative for more information.

3 Code Overlays

The suite of software available for the CS4970x4 family consists of operating systems (OS) and a library of overlays. The overlays have been divided into three main groups: decoders, matrix processors, and postprocessors. All software components are defined in the following list:

Table 3. CS4970x4 DSP Memory Sizes

Memory Type	DSP A	DSP B
X	16K SRAM, 32K ROM	10K SRAM, 8K ROM
Y	24K SRAM, 32K ROM	16K SRAM, 16K ROM
P	8K SRAM, 32K ROM	8K SRAM, 24K ROM

4.1.2 DMA Controller

The powerful 12-channel DMA controller can move data between 8 on-chip resources. Each resource has its own arbiter: X, Y, and P RAM/ROMs on DSP A; X, Y, and P RAM/ROMs on DSP B; external memory; and the peripheral bus. Modulo and linear addressing modes are supported, with flexible start address and increment controls. The service interval for each DMA channel as well as up to 6 interrupt events, is programmable.

4.2 On-chip DSP Peripherals

4.2.1 Digital Audio Input Port (DAI)

The 12-channel (6-line) DAI port supports a wide variety of data input formats. The port is capable of accepting PCM or IEC61937. Up to 32-bit word lengths are supported. Additionally, support is provided for audio data input to the DSP via the DAI from an HDMI receiver.

The port has two independent slave-only clock domains. Each data input can be independently assigned to a clock domain. The sample rate of the input clock domains can be determined automatically by the DSP, which off-loads the task of monitoring the SPDIF receiver from the host. A time-stamping feature allows the input data to be sample-rate converted via software.

4.2.2 Digital Audio Output Port (DAO)

There are two DAO ports. Each port can output 8 channels of up to 32-bit PCM data. The port supports data rates from 32 kHz to 192 kHz. Each port can be configured as an independent clock domain in slave mode, or the ratio of the two clocks can be set to even multiples of each other in master mode. The two ports can also be ganged together into a single clock domain. Each port has one serial audio pin that can be configured as a 192-kHz SPDIF transmitter (data with embedded clock on a single line).

4.2.3 Serial Control Port 1 & 2 (I^2C or SPI)

There are two on-chip serial control ports that are capable of operating as master or slave in either I^2C or SPI modes. SCP1 defaults to slave operation. It is dedicated for external host-control and supports an external clock up to 50 MHz in SPI mode. This high clock speed enables very fast code download, control or data delivery. SCP2 defaults to master mode and is dedicated for booting from external serial Flash memory or for audio sub-system control.

4.2.4 External Memory Interface

The external memory interface controller supports up to 128 Mbits of SDRAM, using a 16-bit data bus.

4.2.5 General Purpose Input/Output (GPIO)

Many of the CS4970x4 peripheral pins are multiplexed with GPIO. Each GPIO can be configured as an output, an input, or an input with interrupt. Each input-pin interrupt can be configured as rising edge, falling edge, active-low, or active-high.

4.2.6 Phase-locked Loop (PLL)-based Clock Generator

The low-jitter PLL generates integer or fractional multiples of a reference frequency which are used to clock the DSP core and peripherals. Through a second PLL divider chain, a dependent clock domain can be output on the DAO port for driving audio converters. The CS4970x4 defaults to running from the external reference frequency and can be switched to use the PLL output after overlays have been loaded and configured, either

through master boot from an external FLASH or through host control. A built-in crystal oscillator circuit with a buffered output is provided. The buffered output frequency ratio is selectable between 1:1 (default) or 2:1.

4.3 DSP I/O Description

4.3.1 Multiplexed Pins

Many of the CS4970x4 pins are multi-functional. For details on pin functionality please refer to the *CS4970x4 System Designer's Guide.*

4.3.2 Termination Requirements

Open-drain pins on the CS4970x4 must be pulled high for proper operation. Please refer to the *CS4970x4 System Designer's Guide* to identify which pins are open-drain and what value of pull-up resistor is required for proper operation.

Mode select pins on the CS4970x4 are used to select the boot mode upon the rising edge of reset. A detailed explanation of termination requirements for each communication mode select pin can be found in the *CS4970x4 System Designer's Guide*.

4.3.3 Pads

The CS4970x4 I/O operates from the 3.3 V supply and is tolerant within 5 V.

4.4 Application Code Security

The external program code may be encrypted by the programmer to protect any intellectual property it may contain. A secret, customer-specific key is used to encrypt the program code that is to be stored external to the device.

5 Characteristics and Specifications

Note: All data sheet minimum and maximum timing parameters are guaranteed over the rated voltage and temperature. All data sheet typical parameters are measured under the following conditions: T = 25 °C, C_L = 20 pF, VDD = 1.8 V, VDDA = VDDIO = 3.3 V, GNDD = GNDIO = GNDA = 0 V.

5.1 Absolute Maximum Ratings

(GNDD = GNDIO = GNDA = 0 V; all voltages with respect to 0 V)

Parameter	Symbol	Min	Max	Unit
DC power supplies: Core supply	VDD	–0.3	2.0	V
PLL supply	VDDA	–0.3	3.6	V
I/O supply	VDDIO	–0.3	3.6	V
|VDDA – VDDIO|		—	0.3	V
Input pin current, any pin except supplies	I_{in}	—	+/- 10	mA
Input voltage on PLL_REF_RES	V_{filt}	-0.3	3.6	V
Input voltage on I/O pins	V_{inio}	-0.3	5.0	V
Storage temperature	T_{stg}	-65	150	°C

CAUTION: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

5.8 Switching Characteristics — Internal Clock

Parameter	Symbol	Min	Max	Unit
Internal DCLK frequency[1]	F_{dclk}	—	–	MHz
CS497004-CQZ CS497004-CQZR CS497024-CVZ CS497024-CVZR CS497014-CVZ CS497014-CVZR CS497024-CVZ CS497024-CVZR		F_{xtal}	131	
Internal DCLK period[1]	DCLKP	—	–	ns
CS497004-CQZ CS497004-CQZR CS497024-CVZ CS497024-CVZR CS497014-CVZ CS497014-CVZR CS497024-CVZ CS497024-CVZR		7.63	$1/F_{xtal}$	

1. After initial power-on reset, $F_{dclk} = F_{xtal}$. After initial kick-start commands, the PLL is locked to max F_{dclk} and remains locked until the next power-on reset.

5.9 Switching Characteristics — Serial Control Port - SPI Slave Mode

Parameter	Symbol	Min	Typical	Max	Units
SCP_CLK frequency[1,2]	f_{spisck}	—	—	25	MHz
SCP_$\overline{CS}$ falling to SCP_CLK rising[2]	t_{spicss}	24	—	—	ns
SCP_CLK low time[2]	t_{spickl}	20	—	—	ns
SCP_CLK high time[2]	t_{spickh}	20	—	—	ns
Setup time SCP_MOSI input	t_{spidsu}	5	—	—	ns
Hold time SCP_MOSI input	t_{spidh}	5	—	—	ns
SCP_CLK low to SCP_MISO output valid[2]	t_{spidov}	—	—	11	ns
SCP_CLK falling to SCP_$\overline{IRQ}$ rising[2]	$t_{spiirqh}$	—	—	20	ns
SCP_$\overline{CS}$ rising to SCP_$\overline{IRQ}$ falling[2]	$t_{spiirql}$	0	—	—	ns
SCP_CLK low to SCP_$\overline{CS}$ rising[2]	t_{spicsh}	24	—	—	ns
SCP_$\overline{CS}$ rising to SCP_MISO output high-Z	$t_{spicsdz}$	—	20	—	ns
SCP_CLK rising to SCP_$\overline{BSY}$ falling[2]	$t_{spicbsyl}$	—	3∗DCLKP+20	—	ns

1. The specification f_{spisck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application. Flow control using the SCP_$\overline{BSY}$ pin should be implemented to prevent overflow of the input data buffer. At boot the maximum speed is Fxtal/3.
2. When SCP1 is in SPI slave mode, very slow rise and fall times of the SCP_CLK edges may make the edges of the SCP_CLK more susceptible to noise, resulting in non-smooth edges. Any glitch at the threshold levels of the SCP port input signals could result in abnormal operation of the port. In systems that have noise coupling onto SCP_CLK, slow rise and fall times may cause host communication problems. Increasing rise time makes host communication more reliable.

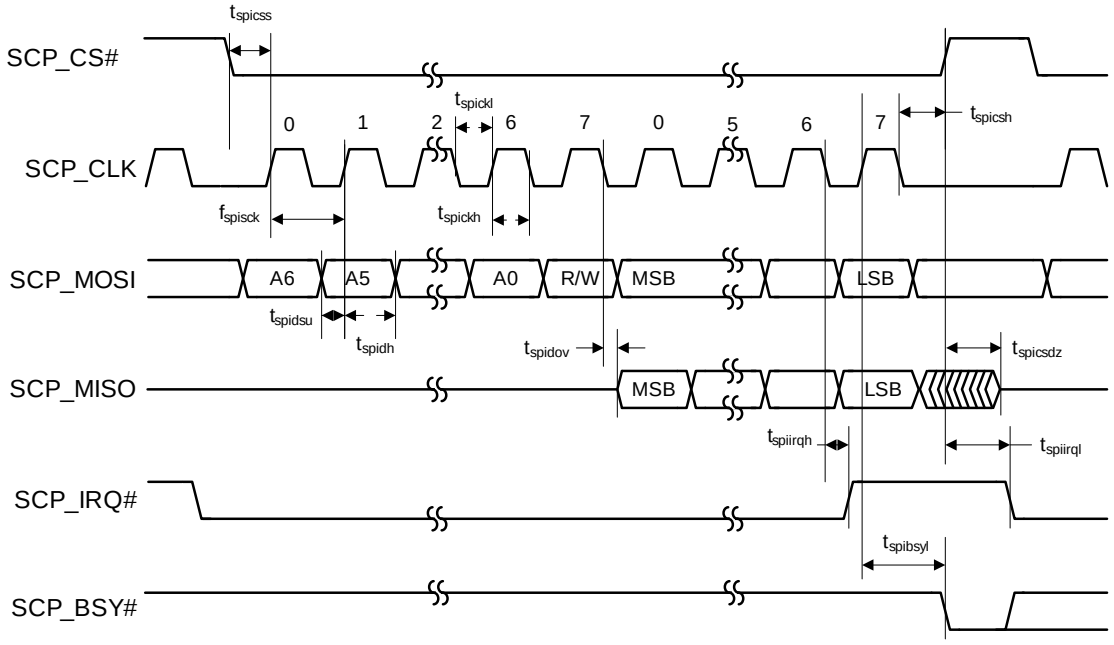


Figure 3. Serial Control Port - SPI Slave Mode Timing

5.10 Switching Characteristics — Serial Control Port - SPI Master Mode

Parameter	Symbol	Min	Typical	Max	Units
SCP_CLK frequency[1, 2]	f_{spisck}	—	—	$F_{xtal}/2$	MHz
SCP_$\overline{CS}$ falling to SCP_CLK rising [3]	t_{spicss}	—	11*DCLKP + (SCP_CLK PERIOD)/2	—	ns
SCP_CLK low time	t_{spickl}	16.9	—	—	ns
SCP_CLK high time	t_{spickh}	16.9	—	—	ns
Setup time SCP_MISO input	t_{spidsu}	11	—	—	ns
Hold time SCP_MISO input	t_{spidh}	5	—	—	ns
SCP_CLK low to SCP_MOSI output valid	t_{spidov}	—	—	11	ns
SCP_CLK low to SCP_$\overline{CS}$ falling	t_{spicsl}	7	—	—	ns
SCP_CLK low to SCP_$\overline{CS}$ rising	t_{spicsh}	—	11*DCLKP + (SCP_CLK PERIOD)/2	—	ns
Bus free time between active SCP_$\overline{CS}$	t_{spicsx}	—	3*DCLKP	—	ns
SCP_CLK falling to SCP_MOSI output high-Z	t_{spidz}	—	—	20	ns

1. The specification f_{spisck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application.
2. See Section 5.7.
3. SCP_CLK PERIOD refers to the period of SCP_CLK as being used in a given application. It does not refer to a tested parameter.

.

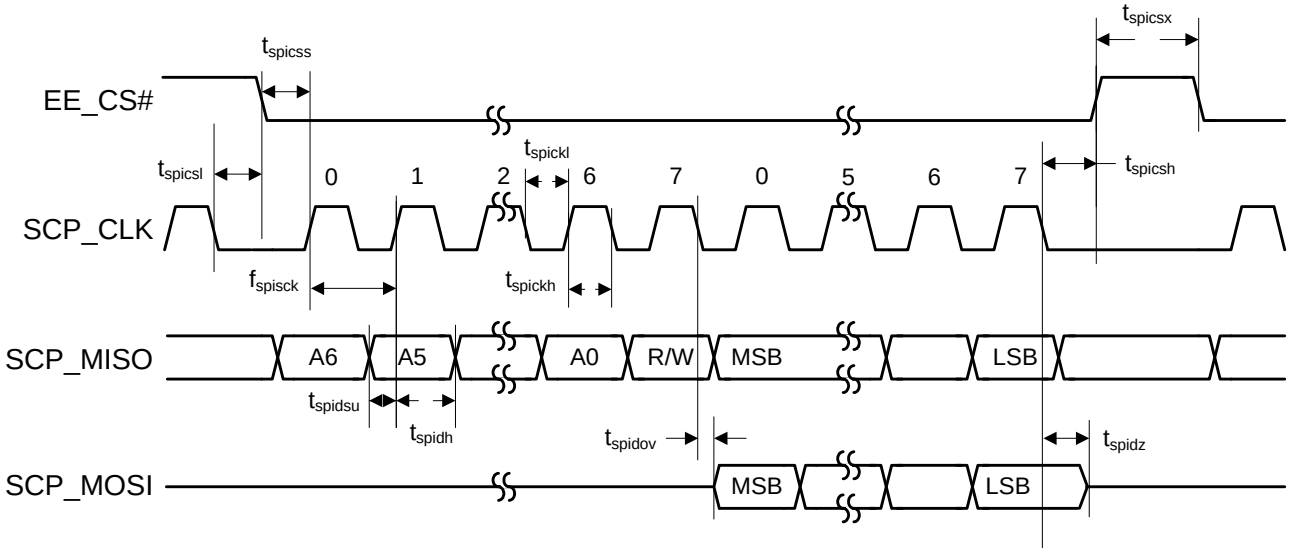


Figure 4. Serial Control Port - SPI Master Mode Timing

5.11 Switching Characteristics — Serial Control Port - I²C Slave Mode

Parameter	Symbol	Min	Typical	Max	Units
SCP_CLK frequency[1]	f_{iicck}	—	—	400	kHz
SCP_CLK low time	t_{iicckl}	1.25	—	—	µs
SCP_CLK high time	t_{iicckh}	1.25	—	—	µs
SCP_SCK rising to SCP_SDA rising or falling for START or STOP condition	$t_{iicckcmd}$	1.25	—	—	µs
START condition to SCP_CLK falling	$t_{iicstscl}$	1.25	—	—	µs
SCP_CLK falling to STOP condition	t_{iicstp}	2.5	—	—	µs
Bus free time between STOP and START conditions	t_{iicbft}	3	—	—	µs
Setup time SCP_SDA input valid to SCP_CLK rising	t_{iicsu}	100	—	—	ns
Hold time SCP_SDA input after SCP_CLK falling[2]	t_{iich}	0	—	—	ns
SCP_CLK low to SCP_SDA out valid	t_{iicdov}	—	—	18	ns
SCP_CLK falling to SCP_$\overline{IRQ}$ rising	$t_{iicirqh}$	—	—	3∗DCLKP + 40	ns
NAK condition to SCP_$\overline{IRQ}$ low	$t_{iicirql}$	—	3∗DCLKP + 20	—	ns
SCP_CLK rising to SCB_$\overline{BSY}$ low	$t_{iicbsyl}$	—	3∗DCLKP + 20	—	ns

1. The specification f_{iicck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application. Flow control using the SCP_$\overline{BSY}$ pin should be implemented to prevent overflow of the input data buffer.
2. This parameter is measured from the ViL level at the falling edge of the clock.

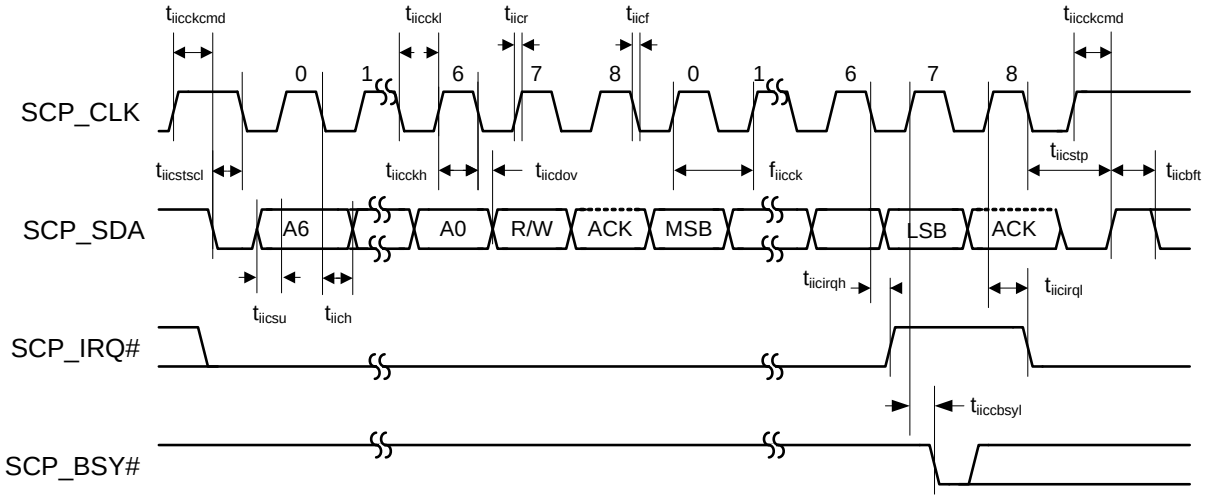


Figure 5. Serial Control Port - I²C Slave Mode Timing

Parameter	Symbol	Min	Typical	Max	Unit
Delay between $\overline{\text{PCP\_RD}}$ then $\overline{\text{PCP\_CS}}$ low or $\overline{\text{PCP\_CS}}$ then $\overline{\text{PCP\_RD}}$ low	t_{icdr}	0	—	—	ns
Data valid after $\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_RD}}$ low	t_{idd}	—	—	18	ns
$\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_RD}}$ low for read	t_{irpw}	24	—	—	ns
Data hold time after $\overline{\text{PCP\_CS}}$ or $\overline{\text{PCP\_RD}}$ high	t_{idhr}	8	—	—	ns
Data high-Z after $\overline{\text{PCP\_CS}}$ or $\overline{\text{PCP\_RD}}$ high	t_{idis}	—	—	18	ns
$\overline{\text{PCP\_CS}}$ or $\overline{\text{PCP\_RD}}$ high to $\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_RD}}$ low for next read[1]	t_{ird}	30	—	—	ns
$\overline{\text{PCP\_CS}}$ or $\overline{\text{PCP\_RD}}$ high to $\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_WR}}$ low for next write[1]	t_{irdtw}	30	—	—	ns
$\overline{\text{PCP\_RD}}$ rising to $\overline{\text{PCP\_IRQ}}$ rising	$t_{irdirqhl}$	—	—	12	ns
Write					
Delay between $\overline{\text{PCP\_WR}}$ then $\overline{\text{PCP\_CS}}$ low or $\overline{\text{PCP\_CS}}$ then $\overline{\text{PCP\_WR}}$ low	t_{icdw}	0	—	—	ns
Data setup before $\overline{\text{PCP\_CS}}$ or $\overline{\text{PCP\_WR}}$ high	t_{idsu}	8	—	—	ns
$\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_WR}}$ low for write	t_{iwpw}	24	—	—	ns
Data hold after $\overline{\text{PCP\_CS}}$ or $\overline{\text{PCP\_WR}}$ high	t_{idhw}	8	—	—	ns
$\overline{\text{PCP\_CS}}$ or $\overline{\text{PCP\_WR}}$ high to $\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_RD}}$ low for next read[1]	t_{iwtrd}	30	—	—	ns
$\overline{\text{PCP\_CS}}$ or $\overline{\text{PCP\_WR}}$ high to $\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_WR}}$ low for next write[1]	t_{iwd}	30	—	—	ns
$\overline{\text{PCP\_WR}}$ rising to $\overline{\text{PCP\_BSY}}$ falling	$t_{iwrbsyl}$	—	2*DCLKP + 20	—	ns

1. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application. Hardware handshaking on the PCP_$\overline{\text{BSY}}$ pin/bit should be observed to prevent overflowing the input data buffer. *CS4953x4/CS4970x4 System Designer's Guide* should be consulted for the firmware speed limitations.

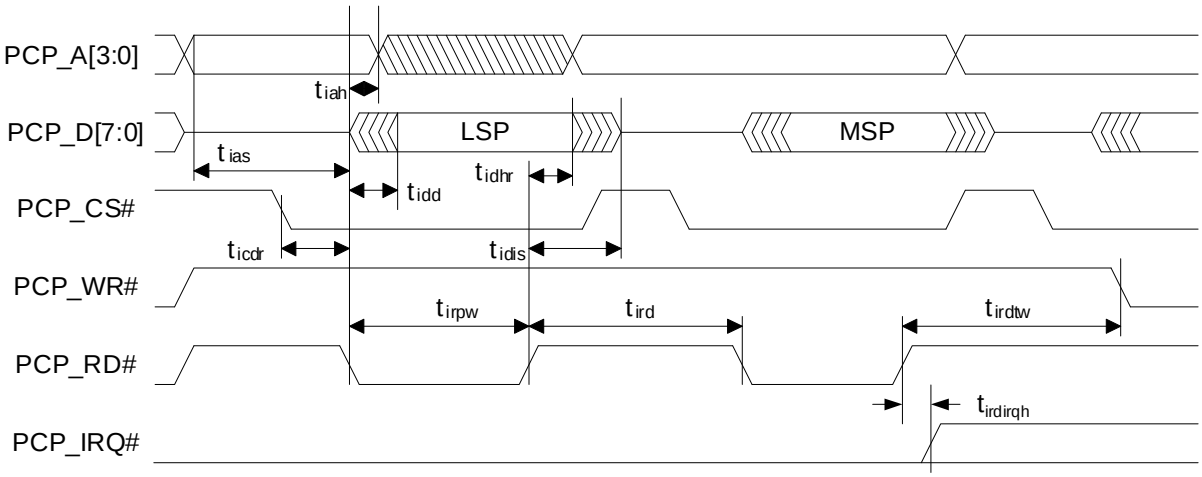


Figure 7. Parallel Control Port - Intel® Slave Mode Read Cycle

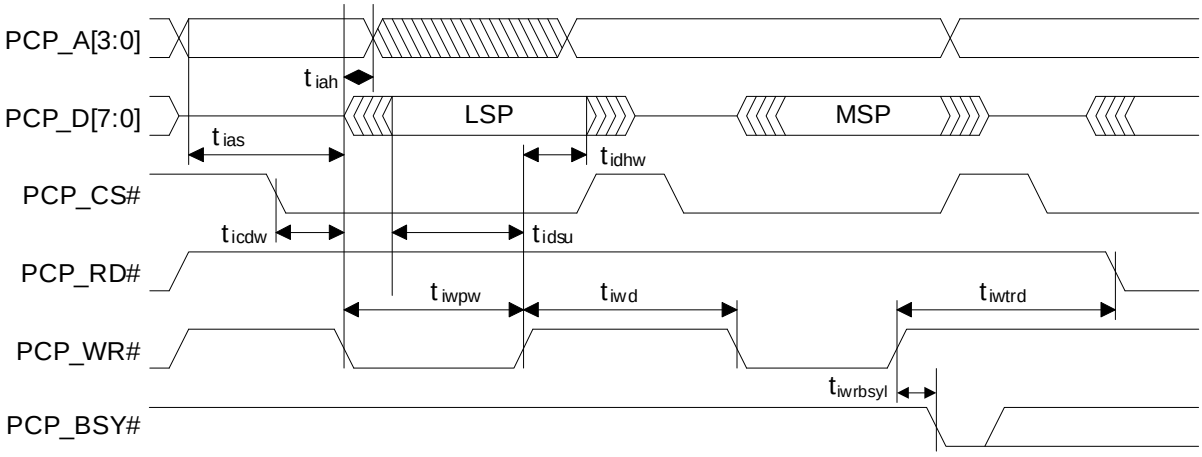


Figure 8. Parallel Control Port - Intel Slave Mode Write Cycle

5.14 Switching Characteristics — Parallel Control Port - Motorola Slave Mode

Parameter	Symbol	Min	Typical	Max	Unit
Address setup before $\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_DS}}$ low	t_{mas}	5	—	—	ns
Address hold time after $\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_DS}}$ low	t_{mah}	5	—	—	ns
Read					
Delay between $\overline{\text{PCP\_DS}}$ then $\overline{\text{PCP\_CS}}$ low or $\overline{\text{PCP\_CS}}$ then $\overline{\text{PCP\_DS}}$ low	t_{mcdr}	0	—	—	ns
Data valid after $\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_DS}}$ low with PCP_R/W high	t_{mdd}	—	—	19	ns
$\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_DS}}$ low for read	t_{mrpw}	24	—	—	ns
Data hold time after $\overline{\text{PCP\_CS}}$ or $\overline{\text{PCP\_DS}}$ high after read	t_{mdhr}	8	—	—	ns
Data high-Z after $\overline{\text{PCP\_CS}}$ or $\overline{\text{PCP\_DS}}$ high after read	t_{mdis}	—	—	18	ns
$\overline{\text{PCP\_CS}}$ or $\overline{\text{PCP\_DS}}$ high to $\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_DS}}$ low for next read[1]	t_{mrd}	30	—	—	ns
$\overline{\text{PCP\_CS}}$ or $\overline{\text{PCP\_DS}}$ high to $\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_DS}}$ low for next write[1]	t_{mrdtw}	30	—	—	ns
PCP_RW rising to PCP_IRQ falling	$t_{mrwirqh}$	—	—	12	ns
Write					
Delay between $\overline{\text{PCP\_DS}}$ then $\overline{\text{PCP\_CS}}$ low or $\overline{\text{PCP\_CS}}$ then $\overline{\text{PCP\_DS}}$ low	t_{mcdw}	0	—	—	ns
Data setup before $\overline{\text{PCP\_CS}}$ or $\overline{\text{PCP\_DS}}$ high	t_{mdsu}	8	—	—	ns
$\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_DS}}$ low for write	t_{mwpw}	24	—	—	ns
$\overline{\text{PCP\_R/W}}$ setup before $\overline{\text{PCP\_CS}}$ AND $\overline{\text{PCP\_DS}}$ low	t_{mrwsu}	24	—	—	ns
PCP_R/W hold time after PCP_CS or PCP_DS high	t_{mrwhld}	8	—	—	ns
Data hold after $\overline{\text{PCP\_CS}}$ or $\overline{\text{PCP\_DS}}$ high	t_{mdhw}	8	—	—	ns
$\overline{\text{PCP\_CS}}$ or $\overline{\text{PCP\_DS}}$ high to $\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_DS}}$ low with $\overline{\text{PCP\_R/W}}$ high for next read[1]	t_{mwtrd}	30	—	—	ns
$\overline{\text{PCP\_CS}}$ or $\overline{\text{PCP\_DS}}$ high to $\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_DS}}$ low for next write[1]	t_{mwd}	30	—	—	ns
$\overline{\text{PCP\_RW}}$ rising to $\overline{\text{PCP\_BSY}}$ falling	$t_{mrwbsyl}$	—	2*DCLKP + 20	—	ns

1. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application. Hardware handshaking on the PCP_$\overline{\text{BSY}}$ pin/bit should be observed to prevent overflowing the input data buffer. *CS4953x4/CS4970x4 System Designer's Guide* should be consulted for the firmware speed limitations.

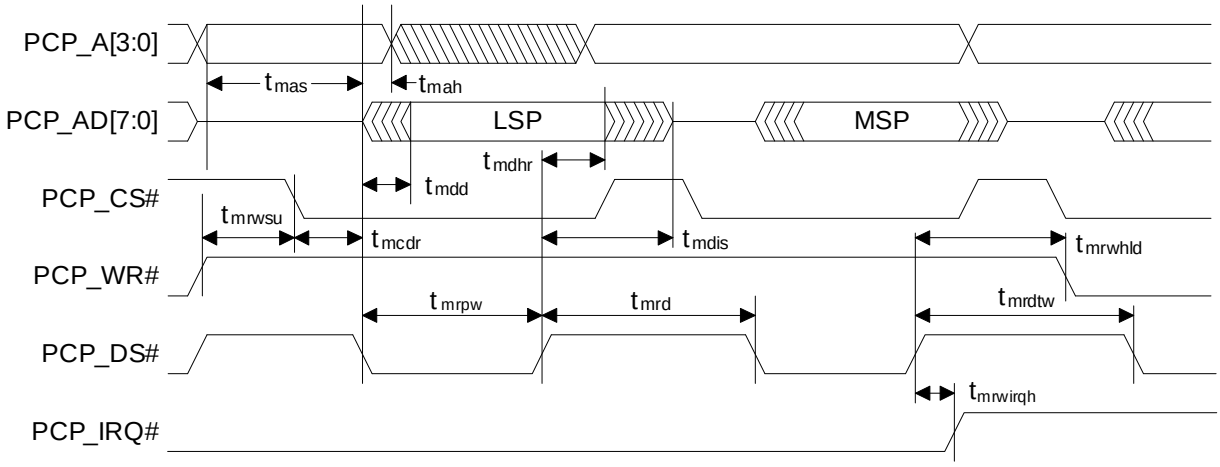


Figure 9. Parallel Control Port - Motorola® Slave Mode Read Cycle Timing

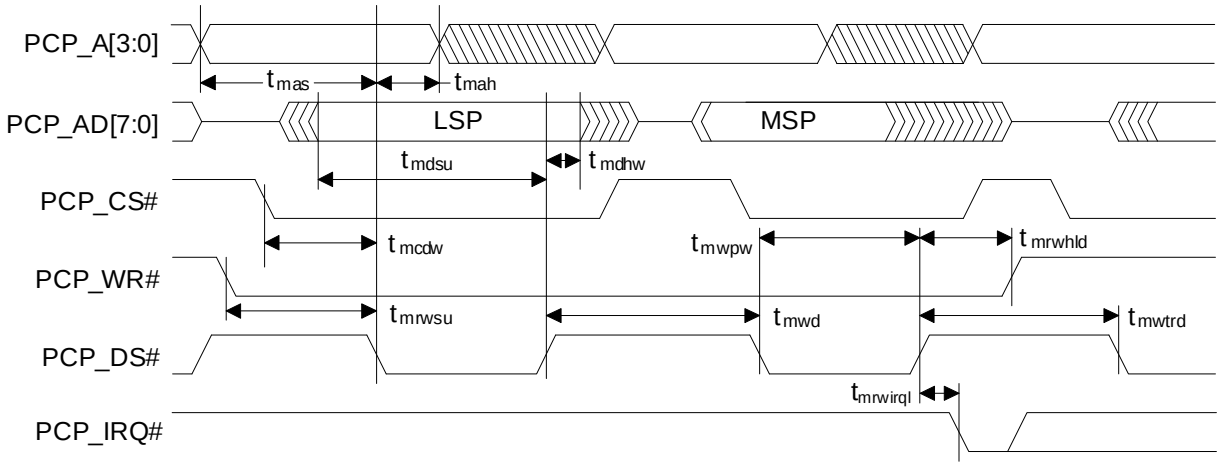


Figure 10. Parallel Control Port - Motorola Slave Mode Write Cycle Timing

5.15 Switching Characteristics — Digital Audio Slave Input Port

Parameter	Symbol	Min	Max	Unit
DAI_SCLK period	$T_{daiclkp}$	40	—	ns
DAI_SCLK duty cycle	—	45	55	%
DAI_LRCLK transition from DAI_SCLK active edge	$t_{daisstlr}$	10	—	ns
DAI_SCLK active edge from DAI_LRCLK transition	$t_{daislrts}$	10	—	ns
Setup time DAI_DATAn	t_{daidsu}	10	—	ns
Hold time DAI_DATAn	t_{daidh}	5	—	ns

Note: In these diagrams, falling edge is the inactive edge of DAI_SCLK.

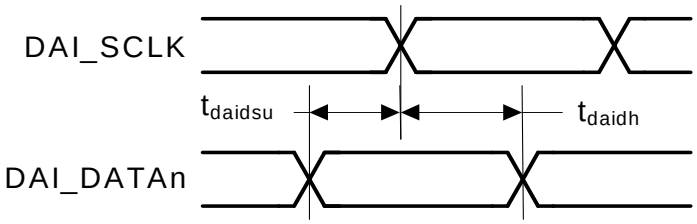


Figure 11. Digital Audio Input (DAI) Port Timing Diagram

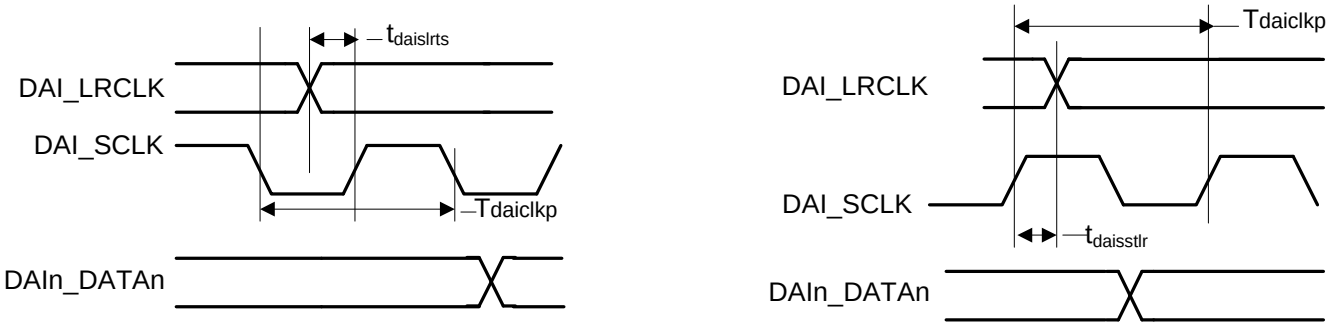
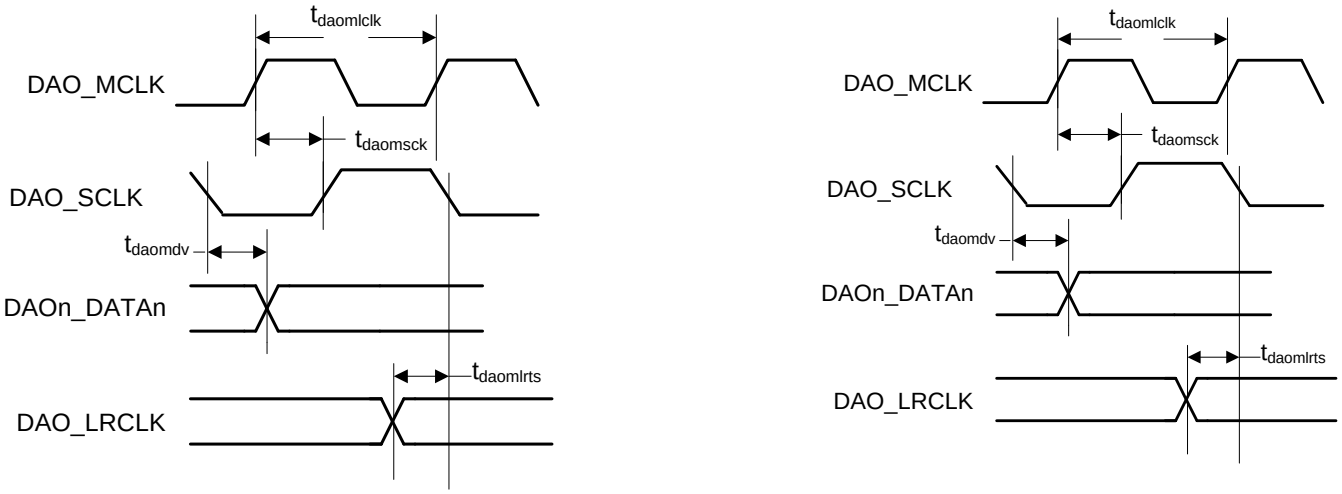


Figure 12. DAI Slave Timing Diagram

5.16 Switching Characteristics — Digital Audio Output Port

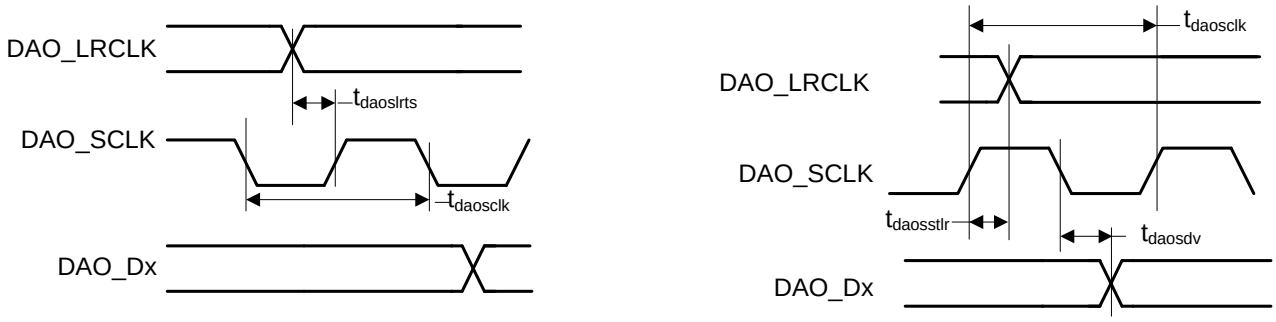
Parameter	Symbol	Min	Max	Unit
DAO_MCLK period	$T_{daomclk}$	40	—	ns
DAO_MCLK duty cycle	—	45	55	%
DAO_SCLK period for Master or Slave mode[1]	$T_{daosclk}$	40	—	ns
DAO_SCLK duty cycle for Master or Slave mode[1]	—	40	60	%
Master Mode (Output A1 Mode)[1,2]				
DAO_SCLK delay from DAO_MCLK rising edge, DAO_MCLK as an input	$t_{daomsck}$	—	19	ns
DAO_SCLK delay from DAO_LRCLK transition[3]	$t_{daomlrts}$	—	8	ns
DAO_LRCLK delay from DAO_SCLK transition[3]	$t_{daomstlr}$	—	8	ns
DAO1_DATA[3..0], DAO2_DATA[1..0] delay from DAO_SCLK transition[3]	t_{daomdv}	—	10	ns
Slave Mode (Output A0 Mode)[4]				
DAO_SCLK active edge to DAO_LRCLK transition	$t_{daosstlr}$	10	—	ns
DAO_LRCLK transition to DAO_SCLK active edge	$t_{daoslrts}$	10	—	ns
DAO_Dx delay from DAO_SCLK inactive edge	t_{daosdv}	—	12.5	ns

1. Master mode timing specifications are characterized, not production tested.
2. Master mode is defined as the CS4970x4 driving both DAO_SCLK, DAO_LRCLK. When MCLK is an input, it is divided to produce DAO_SCLK, DAO_LRCLK.
3. This timing parameter is defined from the non-active edge of DAO_SCLK. The active edge of DAO_SCLK is the point at which the data is valid.
4. Slave mode is defined as DAO_SCLK, DAO_LRCLK driven by an external source.



Note: In these diagrams, falling edge is the inactive edge of DAO_SCLK.

Figure 13. Digital Audio Port Output Timing Master Mode



Note: In these diagrams, Falling edge is the inactive edge of DAO_SCLK

Figure 14. Digital Audio Output Timing, Slave Mode (Relationship LRCLK to SCLK)

5.17 Switching Characteristics — SDRAM Interface

Refer to Figure 15 through Figure 18.

(SD_CLKOUT = SD_CLKIN)

Parameter	Symbol	Min	Typical	Max	Unit
SD_CLKIN high time	t_{sdclkh}	2.3	—	—	ns
SD_CLKIN low time	t_{sdclkl}	2.3	—	—	ns
SD_CLKOUT rise/fall time	$t_{sdclkrf}$	—	—	1	ns
SD_CLKOUT Frequency	—	—	150	—	MHz
SD_CLKOUT duty cycle	—	45	—	55	%
SD_CLKOUT rising edge to signal valid	t_{sdcmdv}	—	—	3.8	ns
Signal hold from SD_CLKOUT rising edge	t_{sdcmdh}	—	1.1	—	ns
SD_CLKOUT rising edge to SD_DQMn valid	t_{sddqv}	—	3.8	—	ns
SD_DQMn hold from SD_CLKOUT rising edge	t_{sddqh}	1.38	—	—	ns
SD_DATA valid setup to SD_CLKIN rising edge	t_{sddsu}	1.3	—	—	ns
SD_DATA valid hold to SD_CLKIN rising edge	t_{sddh}	2.1	—	—	ns
SD_CLKOUT rising edge to ADDRn valid	t_{sdav}	—	3.8	—	ns

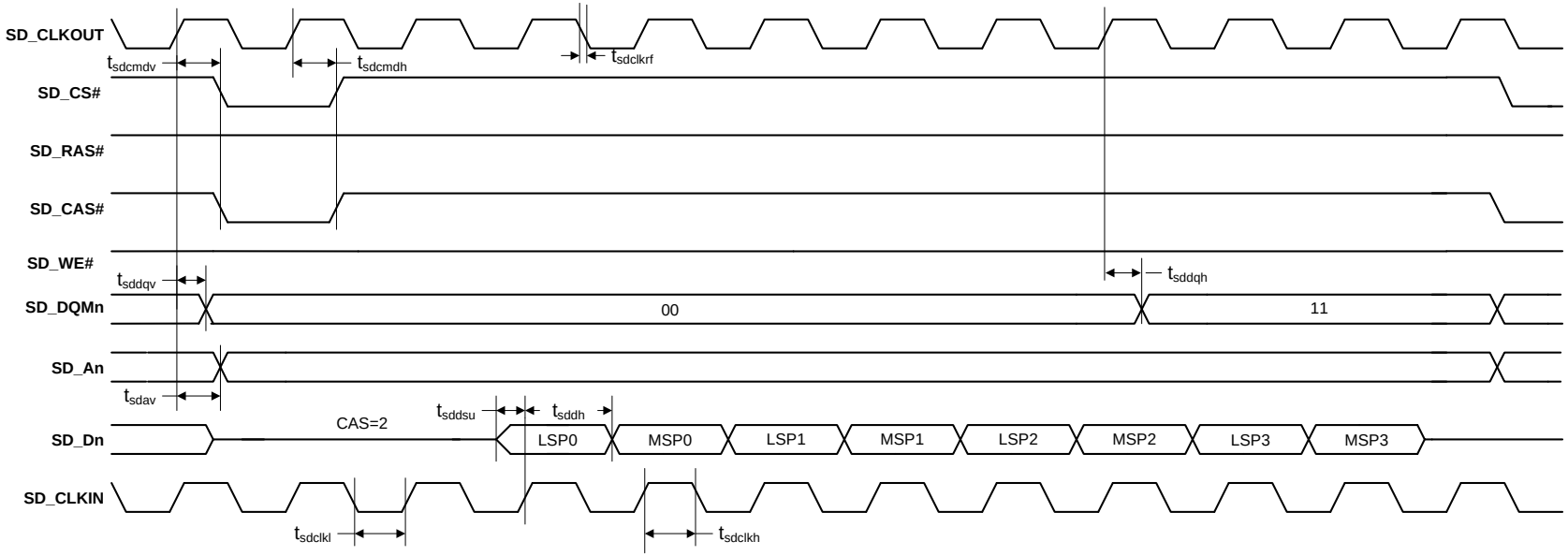


Figure 15. External Memory Interface - SDRAM Burst Read Cycle

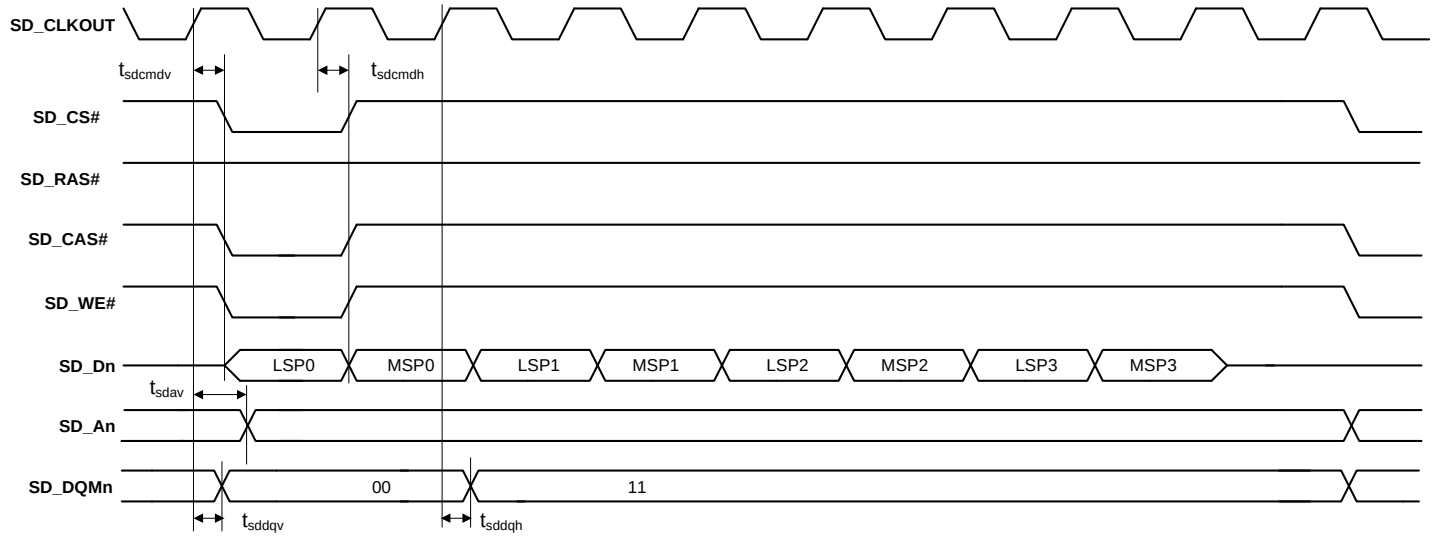


Figure 16. External Memory Interface - SDRAM Burst Write Cycle

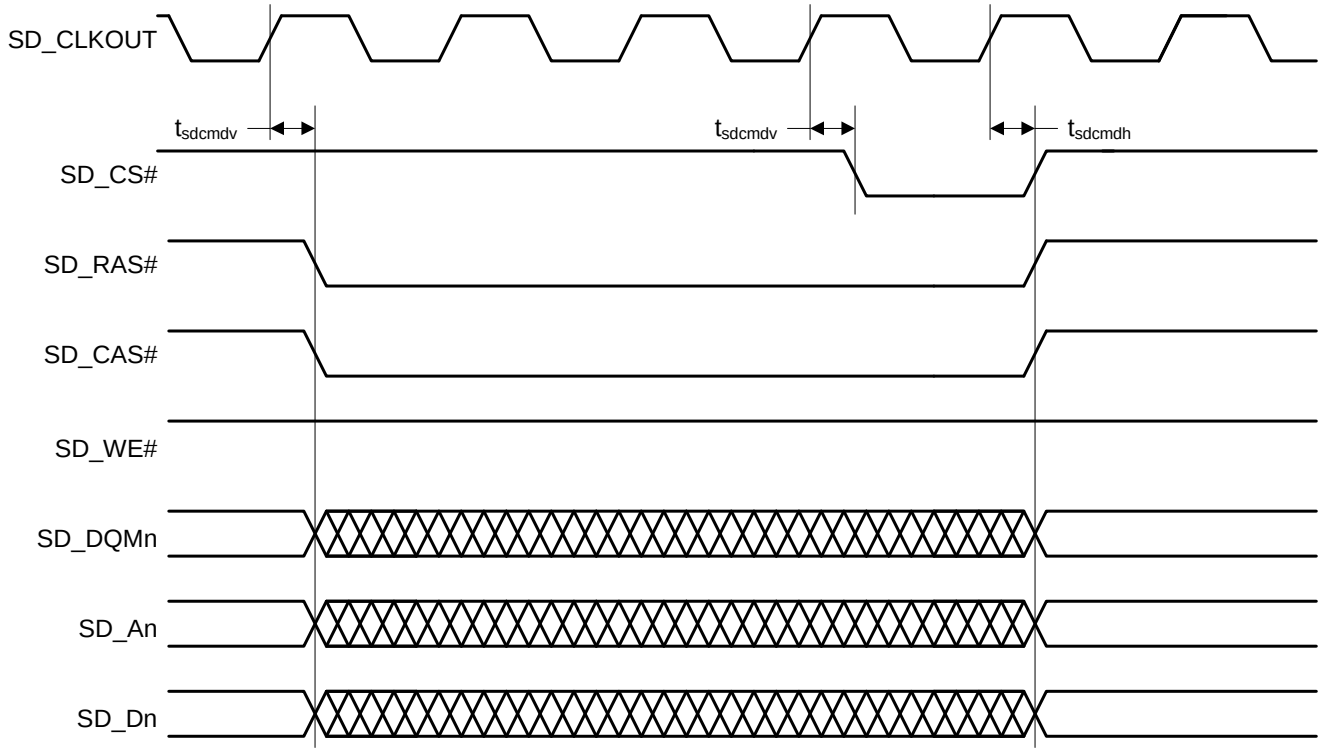


Figure 17. External Memory Interface - SDRAM Auto Refresh Cycle

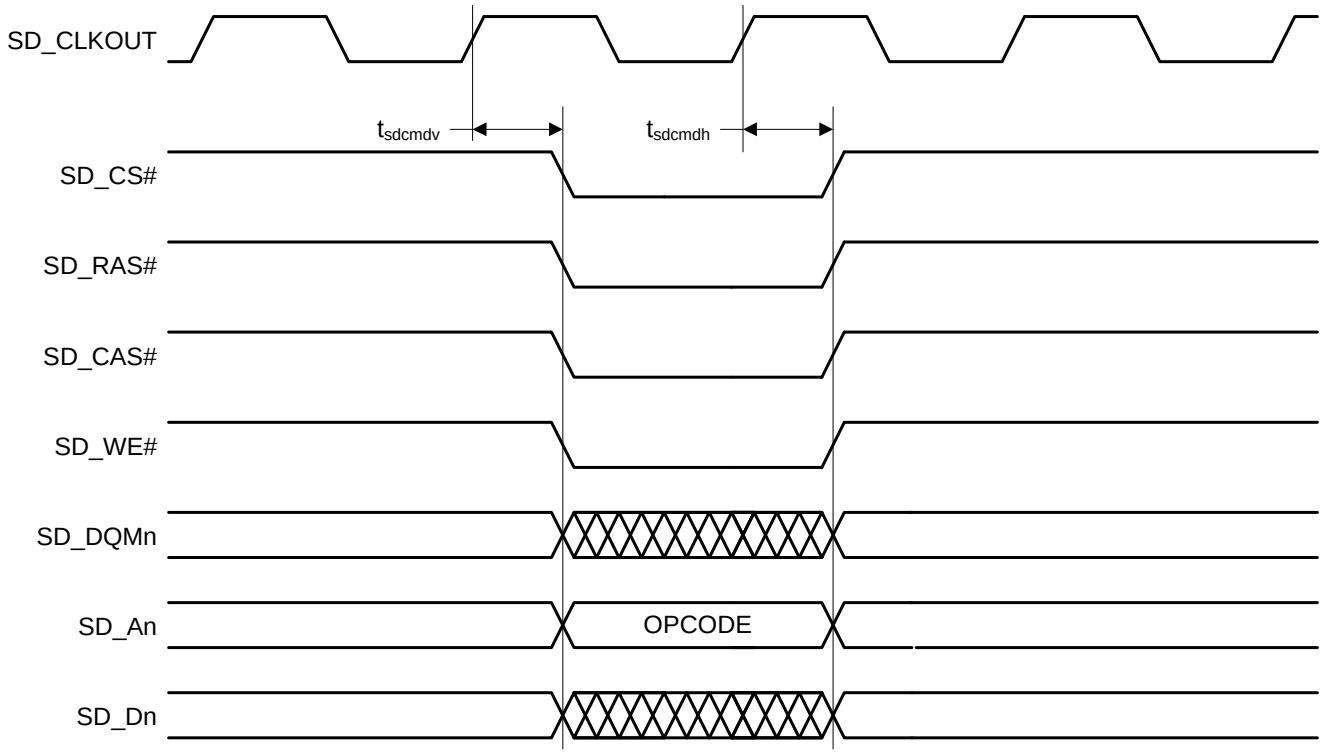


Figure 18. External Memory Interface - SDRAM Load Mode Register Cycle

9 Package Mechanical Drawings

9.1 128-Pin LQFP Package Drawing

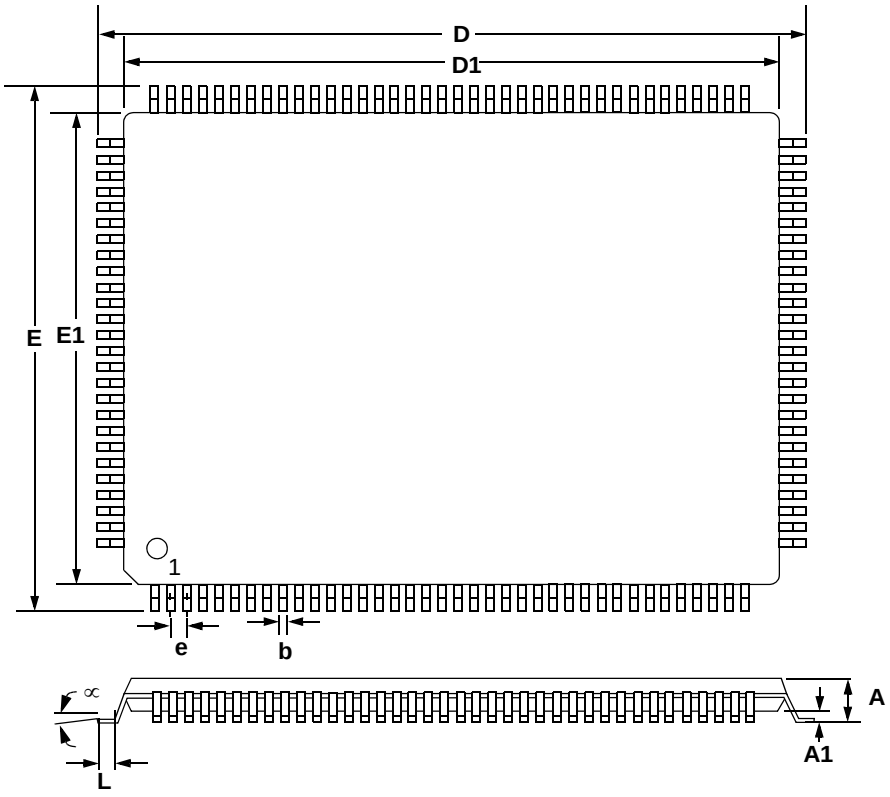


Figure 20. 128-Pin LQFP Package Drawing

Table 6. 128-Pin LQFP Package Characteristics

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.60	—	—	.063”
A1	0.05	—	0.15	.002”	—	.006”
b	0.17	0.22	0.27	.007”	.009”	.011”
D	22.00 BSC			.866”		
D1	20.00 BSC			.787”		
E	16.00 BSC			.630”		
E1	14.00 BSC			.551”		
e	0.50 BSC			.020”		
q	0°	3.5	7°	0°	3.5	7°
L	0.45	0.60	0.75	.018”	.024”	.030”
L1	1.00 REF			.039” REF		
TOLERANCES OF FORM AND POSITION						
ddd	0.08			.003”		

10 Revision History

Revision	Date	Changes
PP9	November, 2010	Added “Status” column and footnote 1 to Table 4.
PP10	March, 2011	Added Tj conditions to Section 5.2. Changed 500 ma to 350 ma in Section 5.4. Updated Section 5.15 “Switching Characteristics — Digital Audio Slave Input Port” on page 21. Updated Section 5.16 “Switching Characteristics — Digital Audio Output Port” on page 22.
PP11	February, 2012	Added max internal DCLK frequency and min internal DCLK period to Section 5.8. Added notes to Section 5.9. Updated tspickl and tspickh values in Section 5.10. Updated tdaosdv max value in Section 5.16.
PP12	October, 2013	Updated note in Section 2 overview. Minor change to Section 2.1 title.
F1	February, 2014	Updated note in Section 2 overview regarding CS4970x4. Changed status of CS497024-CVZ and CS497024-CVZR to “Active” in Table 4.

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find the one nearest you, go to www.cirrus.com.

IMPORTANT NOTICE

Cirrus Logic, Inc. and its subsidiaries ("Cirrus") believe that the information contained in this document is accurate and reliable. However, the information is subject to change without notice and is provided "AS IS" without warranty of any kind (express or implied). Customers are advised to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, indemnification, and limitation of liability. No responsibility is assumed by Cirrus for the use of this information, including use of this information as the basis for manufacture or sale of any items, or for infringement of patents or other rights of third parties. This document is the property of Cirrus and by furnishing this information, Cirrus grants no license, express or implied under any patents, mask work rights, copyrights, trademarks, trade secrets or other intellectual property rights. Cirrus owns the copyrights associated with the information contained herein and gives consent for copies to be made of the information only for use within your organization with respect to Cirrus integrated circuits or other products of Cirrus. This consent does not extend to other copying such as copying for general distribution, advertising or promotional purposes, or for creating any work for resale.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). CIRRUS PRODUCTS ARE NOT DESIGNED, AUTHORIZED OR WARRANTED FOR USE IN PRODUCTS SURGICALLY IMPLANTED INTO THE BODY, AUTOMOTIVE SAFETY OR SECURITY DEVICES, LIFE SUPPORT PRODUCTS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF CIRRUS PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK AND CIRRUS DISCLAIMS AND MAKES NO WARRANTY, EXPRESS, STATUTORY OR IMPLIED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR PARTICULAR PURPOSE, WITH REGARD TO ANY CIRRUS PRODUCT THAT IS USED IN SUCH A MANNER. IF THE CUSTOMER OR CUSTOMER'S CUSTOMER USES OR PERMITS THE USE OF CIRRUS PRODUCTS IN CRITICAL APPLICATIONS, CUSTOMER AGREES, BY SUCH USE, TO FULLY INDEMNIFY CIRRUS, ITS OFFICERS, DIRECTORS, EMPLOYEES, DISTRIBUTORS AND OTHER AGENTS FROM ANY AND ALL LIABILITY, INCLUDING ATTORNEYS' FEES AND COSTS, THAT MAY RESULT FROM OR ARISE IN CONNECTION WITH THESE USES.

Cirrus Logic, Cirrus, Cirrus Logic logo designs, Cirrus Framework, and DSP Condenser are trademarks of Cirrus Logic, Inc. All other brand and product names in this document may be trademarks or service marks of their respective owners.

THX is a registered trademark of THX, Ltd. THX Select 2 and THX Ultra 2 are trademarks of THX, Ltd.

Dolby, Dolby Digital, Dolby Headphone, Virtual Speaker, Pro Logic, Audistry, and Dolby Volume are registered trademarks of Dolby Laboratories, Inc. AAC, AC-3, Dolby TrueHD, and Dolby Volume 258 are trademarks of Dolby Laboratories, Inc. Supply of an implementation of Dolby Technology does not convey a license nor imply a right under any patent, or any other industrial or Intellectual Property Right of Dolby Laboratories, to use the Implementation in any finished end-user or ready-to-use final product. It is hereby notified that a license for such use is required from Dolby Laboratories.

DTS and DTS Neo:6 are registered trademarks of the Digital Theater Systems, Inc. DTS-ES 96/24, DTS-ES, DTS 6.1, DTS 96/24, DTS Neural Surround, and DTS Express are trademarks of Digital Theater Systems, Inc. It is hereby notified that a third-party license from DTS is necessary to distribute software of DTS in any finished end-user or ready-to-use final product.

SRS, SRS 3D, SRS CS Auto, SRS CS Headphone, SRS Circle Cinema 3D, SRS Circle Surround, SRS Circle Surround II, SRS GEQ, SRS Hardlimiter, SRS Headphone, SRS Headphone 360, SRS HPF, SRS StudioSound HD, SRS TruEQ, SRS TruMedia, SRS TruSurround, SRS TruSurround XT, SRS TruSurround HD, SRS TruSurround HD4, SRS TruVolume, SRS VIP+, SRS WOW, SRS WOW XT, SRS WOW HD are either trademarks or registered trademarks of SRS Labs, Inc. SRS, SRS 3D, SRS CS Auto, SRS CS Headphone, SRS Circle Cinema 3D, SRS Circle Surround, SRS Circle Surround II, SRS GEQ, SRS Hardlimiter, SRS Headphone, SRS Headphone 360, SRS HPF, SRS StudioSound HD, SRS TruEQ, SRS TruMedia, SRS TruSurround, SRS TruSurround XT, SRS TruSurround HD, SRS TruSurround HD4, SRS TruVolume, SRS VIP+, SRS WOW, SRS WOW XT, SRS WOW HD technologies are incorporated under license from SRS Labs, Inc. SRS, SRS 3D, SRS CS Auto, SRS CS Headphone, SRS Circle Cinema 3D, SRS Circle Surround, SRS Circle Surround II, SRS GEQ, SRS Hardlimiter, SRS Headphone, SRS Headphone 360, SRS HPF, SRS StudioSound HD, SRS TruEQ, SRS TruMedia, SRS TruSurround, SRS TruSurround XT, SRS TruSurround HD, SRS TruSurround HD4, SRS TruVolume, SRS VIP+, SRS WOW, SRS WOW XT, SRS WOW HD technologies incorporated in the Cirrus Logic CS4953xx products are owned by SRS Labs, a U.S. Corporation and licensed to Cirrus Logic, Inc. Purchaser of Cirrus Logic CS4953xx products must sign a license for use of the chip and display of the SRS Labs trademarks. Any products incorporating the Cirrus Logic CS4953xx products must be sent to SRS Labs for review. SRS, SRS 3D, SRS CS Auto, SRS CS Headphone, SRS Circle Cinema 3D, SRS Circle Surround, SRS Circle Surround II, SRS GEQ, SRS Hardlimiter, SRS Headphone, SRS Headphone 360, SRS HPF, SRS Studio-Sound HD, SRS TruEQ, SRS TruMedia, SRS TruSurround, SRS TruSurround XT, SRS TruSurround HD, SRS TruSurround HD4, SRS TruVolume, SRS VIP+, SRS WOW, SRS WOW XT, SRS WOW HD technologies are protected under US and foreign patents issued and/or pending. Neither the purchase of the Cirrus Logic CS4953xx products, nor the corresponding sale of audio enhancement equipment conveys the right to sell commercialized recordings made with any SRS technology/solution. SRS Labs requires all set makers to comply with all rules and regulations as outlined in the SRS Trademark Usage Manual.

Motorola is a registered trademark of Motorola, Inc. SPI is a trademark of Motorola, Inc.

Intel is a registered trademark of Intel Corporation.

I^2C is a trademark of Philips Semiconductor.