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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	DAI/O, EBI/EMI, I²C, Parallel, SPI
Clock Rate	25MHz
Non-Volatile Memory	ROM (144kB)
On-Chip RAM	82kB
Voltage - I/O	3.30V
Voltage - Core	1.80V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	128-LQFP (20x14)
Purchase URL	https://www.e-xfl.com/product-detail/cirrus-logic/cs497024-dvz

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Table 3. CS4970x4 DSP Memory Sizes

Memory Type	DSP A	DSP B
X	16K SRAM, 32K ROM	10K SRAM, 8K ROM
Y	24K SRAM, 32K ROM	16K SRAM, 16K ROM
P	8K SRAM, 32K ROM	8K SRAM, 24K ROM

4.1.2 DMA Controller

The powerful 12-channel DMA controller can move data between 8 on-chip resources. Each resource has its own arbiter: X, Y, and P RAM/ROMs on DSP A; X, Y, and P RAM/ROMs on DSP B; external memory; and the peripheral bus. Modulo and linear addressing modes are supported, with flexible start address and increment controls. The service interval for each DMA channel as well as up to 6 interrupt events, is programmable.

4.2 On-chip DSP Peripherals

4.2.1 Digital Audio Input Port (DAI)

The 12-channel (6-line) DAI port supports a wide variety of data input formats. The port is capable of accepting PCM or IEC61937. Up to 32-bit word lengths are supported. Additionally, support is provided for audio data input to the DSP via the DAI from an HDMI receiver.

The port has two independent slave-only clock domains. Each data input can be independently assigned to a clock domain. The sample rate of the input clock domains can be determined automatically by the DSP, which off-loads the task of monitoring the SPDIF receiver from the host. A time-stamping feature allows the input data to be sample-rate converted via software.

4.2.2 Digital Audio Output Port (DAO)

There are two DAO ports. Each port can output 8 channels of up to 32-bit PCM data. The port supports data rates from 32 kHz to 192 kHz. Each port can be configured as an independent clock domain in slave mode, or the ratio of the two clocks can be set to even multiples of each other in master mode. The two ports can also be ganged together into a single clock domain. Each port has one serial audio pin that can be configured as a 192-kHz SPDIF transmitter (data with embedded clock on a single line).

4.2.3 Serial Control Port 1 & 2 (I^2C or SPI)

There are two on-chip serial control ports that are capable of operating as master or slave in either I^2C or SPI modes. SCP1 defaults to slave operation. It is dedicated for external host-control and supports an external clock up to 50 MHz in SPI mode. This high clock speed enables very fast code download, control or data delivery. SCP2 defaults to master mode and is dedicated for booting from external serial Flash memory or for audio sub-system control.

4.2.4 External Memory Interface

The external memory interface controller supports up to 128 Mbits of SDRAM, using a 16-bit data bus.

4.2.5 General Purpose Input/Output (GPIO)

Many of the CS4970x4 peripheral pins are multiplexed with GPIO. Each GPIO can be configured as an output, an input, or an input with interrupt. Each input-pin interrupt can be configured as rising edge, falling edge, active-low, or active-high.

4.2.6 Phase-locked Loop (PLL)-based Clock Generator

The low-jitter PLL generates integer or fractional multiples of a reference frequency which are used to clock the DSP core and peripherals. Through a second PLL divider chain, a dependent clock domain can be output on the DAO port for driving audio converters. The CS4970x4 defaults to running from the external reference frequency and can be switched to use the PLL output after overlays have been loaded and configured, either

5.2 Recommended Operating Conditions

(GNDD = GNDIO = GNDA = 0 V; all voltages with respect to 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
DC power supplies: Core supply	VDD	1.71	1.8	1.89	V
PLL supply	VDDA	3.13	3.3	3.46	V
I/O supply	VDDIO	3.13	3.3	3.46	V
|VDDA – VDDIO|			0		V
Ambient operating temperature Commercial Grade (CQZ/CVZ)	T_A	0	+25	+ 70	°C
Commercial	T_j	0		+125	ºC

Note: It is recommended that the 3.3 V IO supply come up ahead of or simultaneously with the 1.8 V core supply.

5.3 Digital DC Characteristics

(Measurements performed under static conditions.)

Parameter	Symbol	Min	Typ	Max	Unit
High-level input voltage	V_{IH}	2.0	—	—	V
Low-level input voltage, except XTI	V_{IL}	—	—	0.8	V
Low-level input voltage, XTI	V_{ILXTI}	—	—	0.6	V
Input Hysteresis	V_{hys}	—	0.4	—	V
High-level output voltage (I_O = -4mA), except XTI, SDRAM pins	V_{OH}	VDDIO * 0.9	—	—	V
Low-level output voltage (I_O = 4mA), except XTI, SDRAM pins	V_{OL}	—	—	VDDIO * 0.1	V
SDRAM High-level output voltage (I_O = -8mA)	V_{OH}	VDDIO * 0.9	—	—	V
SDRAM Low-level output voltage (I_O = 8mA)	V_{OL}	—	—	VDDIO * 0.1	V
Input leakage current (all digital pins with internal pull-up resistors disabled)	I_{IN}	—	—	5	µA
Input leakage current (all digital pins with internal pull-up resistors enabled, and XTI)	I_{IN-PU}	—	—	70	µA

5.4 Power Supply Characteristics

(Measurements performed under operating conditions.)

Parameter	Min	Typ	Max	Unit
Power supply current:				
Core and I/O operating: VDD[1]	—	350	—	mA
PLL operating: VDDA	—	3.5	—	mA
With external memory and most ports operating: VDDIO	—	120	—	mA

1.Dependent on application firmware and DSP clock speed.

5.5 Thermal Data (128-pin LQFP)

Parameter	Symbol	Min	Typ	Max	Unit
Thermal Resistance (Junction to Ambient)	θ_{ja}				°C / Watt
Two-layer Board[1]		—	53	—	
Four-layer Board[2]		—	44	—	
Thermal Resistance (Junction to Top of Package)	ψ_{jt}				°C / Watt
Two-layer Board[1]		—	.45	—	
Four-layer Board[2]		—	.39	—	

Notes:
1. Two-layer board is specified as a 76 mm X 114 mm, 1.6 mm thick FR-4 material with 1-oz. copper covering 20% of the top and bottom layers.
2. Four-layer board is specified as a 76 mm X 114 mm, 1.6 mm thick FR-4 material with 1-oz. copper covering 20% of the top and bottom layers and 0.5-oz. copper covering 90% of the internal power plane and ground plane layers.
3. To calculate the die temperature for a given power dissipation

   T_j = Ambient Temperature + [(Power Dissipation in Watts) * θ_{ja}]
4. To calculate the case temperature for a given power dissipation

   $T_c = T_j$ - [(Power Dissipation in Watts) * ψ_{jt}

5.8 Switching Characteristics — Internal Clock

Parameter	Symbol	Min	Max	Unit
Internal DCLK frequency[1]	F_{dclk}	—	–	MHz
CS497004-CQZ CS497004-CQZR CS497024-CVZ CS497024-CVZR CS497014-CVZ CS497014-CVZR CS497024-CVZ CS497024-CVZR		F_{xtal}	131	
Internal DCLK period[1]	DCLKP	—	–	ns
CS497004-CQZ CS497004-CQZR CS497024-CVZ CS497024-CVZR CS497014-CVZ CS497014-CVZR CS497024-CVZ CS497024-CVZR		7.63	$1/F_{xtal}$	

1. After initial power-on reset, $F_{dclk} = F_{xtal}$. After initial kick-start commands, the PLL is locked to max F_{dclk} and remains locked until the next power-on reset.

5.9 Switching Characteristics — Serial Control Port - SPI Slave Mode

Parameter	Symbol	Min	Typical	Max	Units
SCP_CLK frequency[1,2]	f_{spisck}	—	—	25	MHz
SCP_$\overline{CS}$ falling to SCP_CLK rising[2]	t_{spicss}	24	—	—	ns
SCP_CLK low time[2]	t_{spickl}	20	—	—	ns
SCP_CLK high time[2]	t_{spickh}	20	—	—	ns
Setup time SCP_MOSI input	t_{spidsu}	5	—	—	ns
Hold time SCP_MOSI input	t_{spidh}	5	—	—	ns
SCP_CLK low to SCP_MISO output valid[2]	t_{spidov}	—	—	11	ns
SCP_CLK falling to SCP_$\overline{IRQ}$ rising[2]	$t_{spiirqh}$	—	—	20	ns
SCP_$\overline{CS}$ rising to SCP_$\overline{IRQ}$ falling[2]	$t_{spiirql}$	0	—	—	ns
SCP_CLK low to SCP_$\overline{CS}$ rising[2]	t_{spicsh}	24	—	—	ns
SCP_$\overline{CS}$ rising to SCP_MISO output high-Z	$t_{spicsdz}$	—	20	—	ns
SCP_CLK rising to SCP_$\overline{BSY}$ falling[2]	$t_{spicbsyl}$	—	3∗DCLKP+20	—	ns

1. The specification f_{spisck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application. Flow control using the SCP_$\overline{BSY}$ pin should be implemented to prevent overflow of the input data buffer. At boot the maximum speed is Fxtal/3.
2. When SCP1 is in SPI slave mode, very slow rise and fall times of the SCP_CLK edges may make the edges of the SCP_CLK more susceptible to noise, resulting in non-smooth edges. Any glitch at the threshold levels of the SCP port input signals could result in abnormal operation of the port. In systems that have noise coupling onto SCP_CLK, slow rise and fall times may cause host communication problems. Increasing rise time makes host communication more reliable.

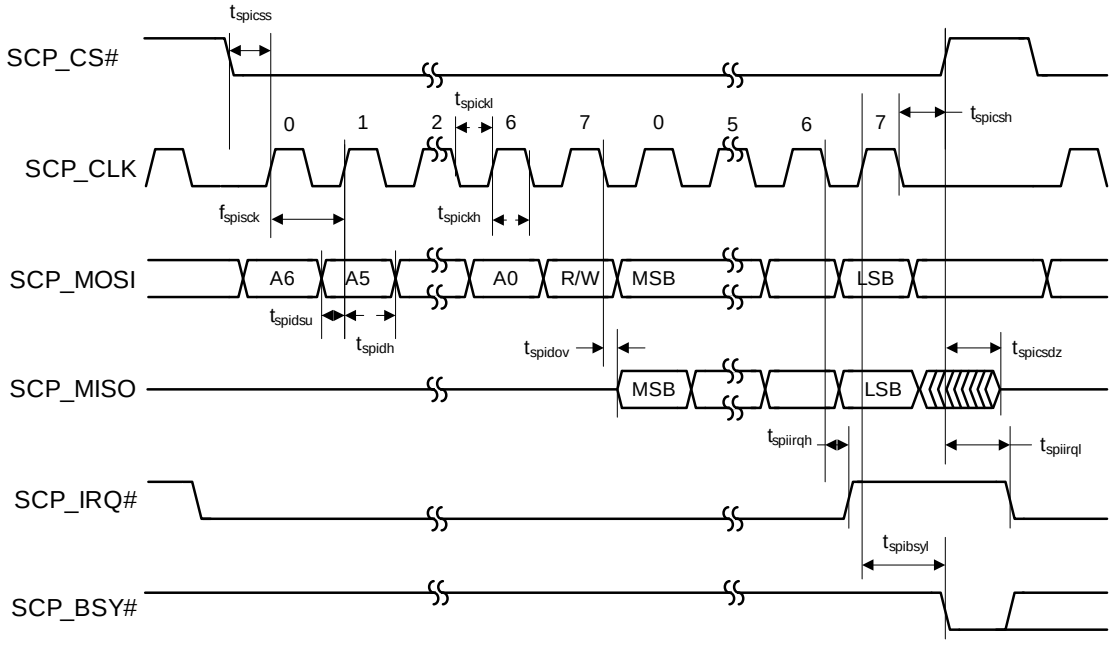


Figure 3. Serial Control Port - SPI Slave Mode Timing

5.11 Switching Characteristics — Serial Control Port - I²C Slave Mode

Parameter	Symbol	Min	Typical	Max	Units
SCP_CLK frequency[1]	f_{iicck}	—	—	400	kHz
SCP_CLK low time	t_{iicckl}	1.25	—	—	µs
SCP_CLK high time	t_{iicckh}	1.25	—	—	µs
SCP_SCK rising to SCP_SDA rising or falling for START or STOP condition	$t_{iicckcmd}$	1.25	—	—	µs
START condition to SCP_CLK falling	$t_{iicstscl}$	1.25	—	—	µs
SCP_CLK falling to STOP condition	t_{iicstp}	2.5	—	—	µs
Bus free time between STOP and START conditions	t_{iicbft}	3	—	—	µs
Setup time SCP_SDA input valid to SCP_CLK rising	t_{iicsu}	100	—	—	ns
Hold time SCP_SDA input after SCP_CLK falling[2]	t_{iich}	0	—	—	ns
SCP_CLK low to SCP_SDA out valid	t_{iicdov}	—	—	18	ns
SCP_CLK falling to SCP_$\overline{IRQ}$ rising	$t_{iicirqh}$	—	—	3∗DCLKP + 40	ns
NAK condition to SCP_$\overline{IRQ}$ low	$t_{iicirql}$	—	3∗DCLKP + 20	—	ns
SCP_CLK rising to SCB_$\overline{BSY}$ low	$t_{iicbsyl}$	—	3∗DCLKP + 20	—	ns

1. The specification f_{iicck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application. Flow control using the SCP_$\overline{BSY}$ pin should be implemented to prevent overflow of the input data buffer.
2. This parameter is measured from the ViL level at the falling edge of the clock.

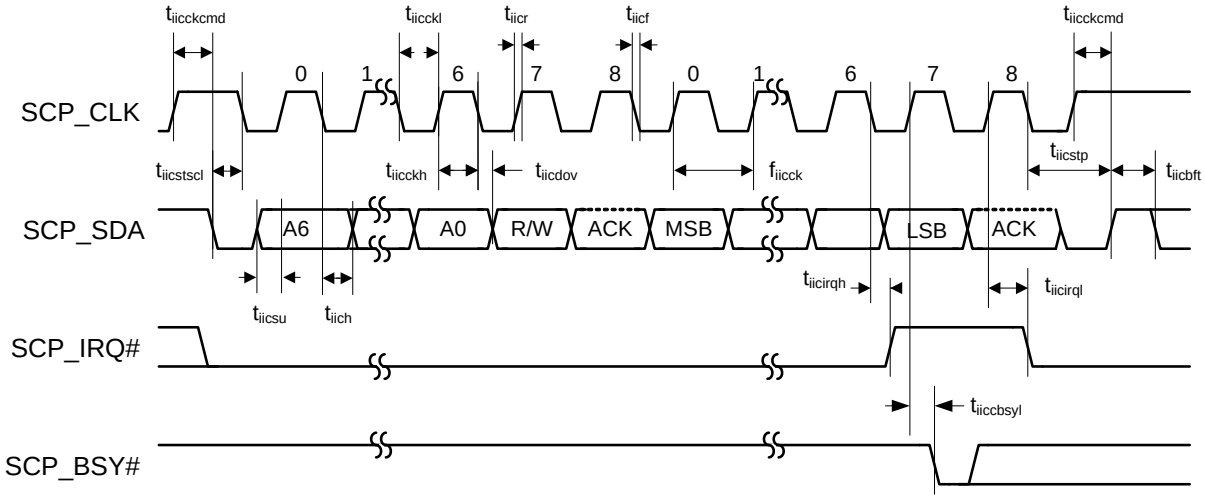


Figure 5. Serial Control Port - I²C Slave Mode Timing

Parameter	Symbol	Min	Typical	Max	Unit
Delay between $\overline{\text{PCP\_RD}}$ then $\overline{\text{PCP\_CS}}$ low or $\overline{\text{PCP\_CS}}$ then $\overline{\text{PCP\_RD}}$ low	t_{icdr}	0	—	—	ns
Data valid after $\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_RD}}$ low	t_{idd}	—	—	18	ns
$\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_RD}}$ low for read	t_{irpw}	24	—	—	ns
Data hold time after $\overline{\text{PCP\_CS}}$ or $\overline{\text{PCP\_RD}}$ high	t_{idhr}	8	—	—	ns
Data high-Z after $\overline{\text{PCP\_CS}}$ or $\overline{\text{PCP\_RD}}$ high	t_{idis}	—	—	18	ns
$\overline{\text{PCP\_CS}}$ or $\overline{\text{PCP\_RD}}$ high to $\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_RD}}$ low for next read[1]	t_{ird}	30	—	—	ns
$\overline{\text{PCP\_CS}}$ or $\overline{\text{PCP\_RD}}$ high to $\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_WR}}$ low for next write[1]	t_{irdtw}	30	—	—	ns
$\overline{\text{PCP\_RD}}$ rising to $\overline{\text{PCP\_IRQ}}$ rising	$t_{irdirqhl}$	—	—	12	ns
Write					
Delay between $\overline{\text{PCP\_WR}}$ then $\overline{\text{PCP\_CS}}$ low or $\overline{\text{PCP\_CS}}$ then $\overline{\text{PCP\_WR}}$ low	t_{icdw}	0	—	—	ns
Data setup before $\overline{\text{PCP\_CS}}$ or $\overline{\text{PCP\_WR}}$ high	t_{idsu}	8	—	—	ns
$\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_WR}}$ low for write	t_{iwpw}	24	—	—	ns
Data hold after $\overline{\text{PCP\_CS}}$ or $\overline{\text{PCP\_WR}}$ high	t_{idhw}	8	—	—	ns
$\overline{\text{PCP\_CS}}$ or $\overline{\text{PCP\_WR}}$ high to $\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_RD}}$ low for next read[1]	t_{iwtrd}	30	—	—	ns
$\overline{\text{PCP\_CS}}$ or $\overline{\text{PCP\_WR}}$ high to $\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_WR}}$ low for next write[1]	t_{iwd}	30	—	—	ns
$\overline{\text{PCP\_WR}}$ rising to $\overline{\text{PCP\_BSY}}$ falling	$t_{iwrbsyl}$	—	2*DCLKP + 20	—	ns

1. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application. Hardware handshaking on the PCP_$\overline{\text{BSY}}$ pin/bit should be observed to prevent overflowing the input data buffer. *CS4953x4/CS4970x4 System Designer's Guide* should be consulted for the firmware speed limitations.

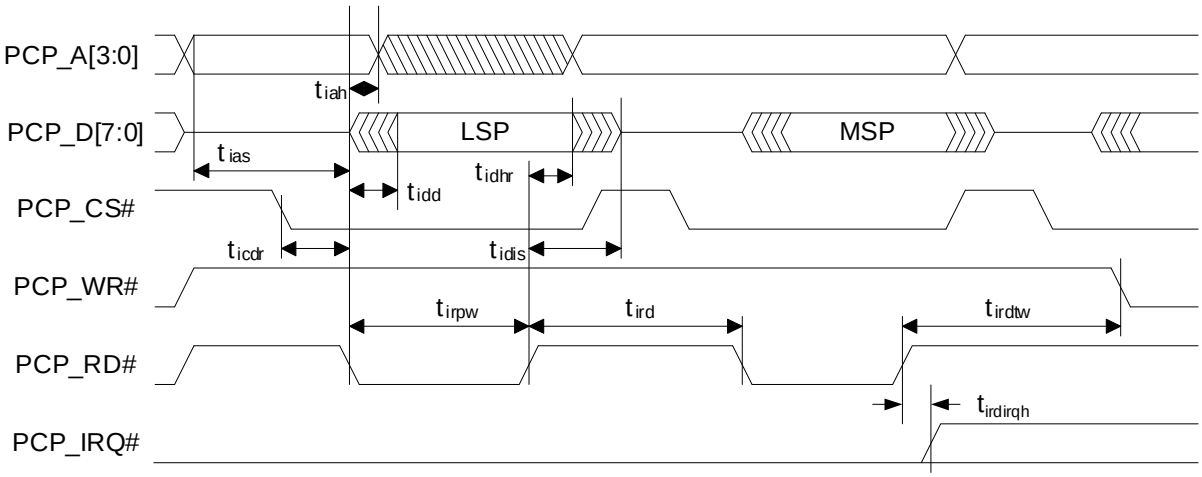


Figure 7. Parallel Control Port - Intel® Slave Mode Read Cycle

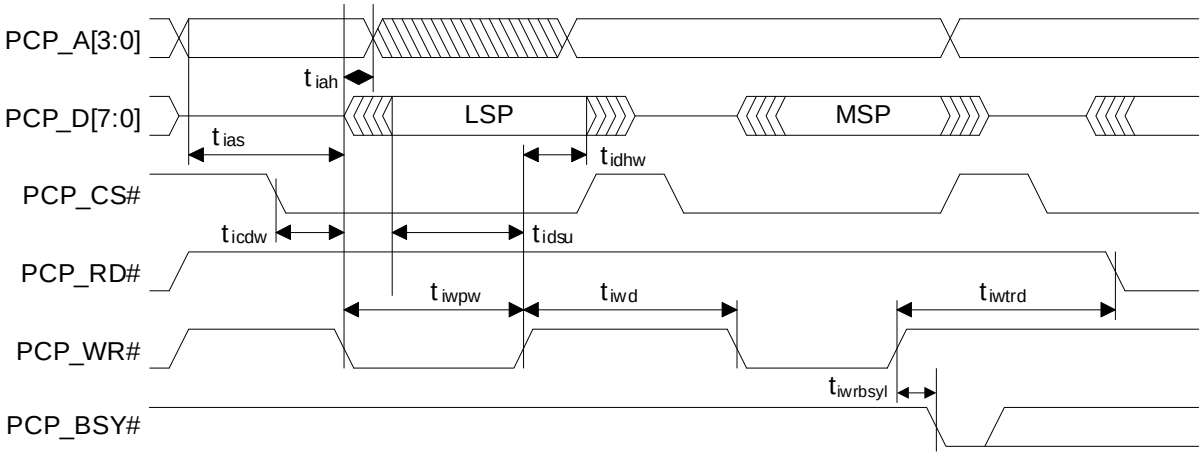


Figure 8. Parallel Control Port - Intel Slave Mode Write Cycle

5.14 Switching Characteristics — Parallel Control Port - Motorola Slave Mode

Parameter	Symbol	Min	Typical	Max	Unit
Address setup before $\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_DS}}$ low	t_{mas}	5	—	—	ns
Address hold time after $\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_DS}}$ low	t_{mah}	5	—	—	ns
Read					
Delay between $\overline{\text{PCP\_DS}}$ then $\overline{\text{PCP\_CS}}$ low or $\overline{\text{PCP\_CS}}$ then $\overline{\text{PCP\_DS}}$ low	t_{mcdr}	0	—	—	ns
Data valid after $\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_DS}}$ low with PCP_R/W high	t_{mdd}	—	—	19	ns
$\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_DS}}$ low for read	t_{mrpw}	24	—	—	ns
Data hold time after $\overline{\text{PCP\_CS}}$ or $\overline{\text{PCP\_DS}}$ high after read	t_{mdhr}	8	—	—	ns
Data high-Z after $\overline{\text{PCP\_CS}}$ or $\overline{\text{PCP\_DS}}$ high after read	t_{mdis}	—	—	18	ns
$\overline{\text{PCP\_CS}}$ or $\overline{\text{PCP\_DS}}$ high to $\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_DS}}$ low for next read[1]	t_{mrd}	30	—	—	ns
$\overline{\text{PCP\_CS}}$ or $\overline{\text{PCP\_DS}}$ high to $\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_DS}}$ low for next write[1]	t_{mrdtw}	30	—	—	ns
PCP_RW rising to PCP_IRQ falling	$t_{mrwirqh}$	—	—	12	ns
Write					
Delay between $\overline{\text{PCP\_DS}}$ then $\overline{\text{PCP\_CS}}$ low or $\overline{\text{PCP\_CS}}$ then $\overline{\text{PCP\_DS}}$ low	t_{mcdw}	0	—	—	ns
Data setup before $\overline{\text{PCP\_CS}}$ or $\overline{\text{PCP\_DS}}$ high	t_{mdsu}	8	—	—	ns
$\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_DS}}$ low for write	t_{mwpw}	24	—	—	ns
$\overline{\text{PCP\_R/W}}$ setup before $\overline{\text{PCP\_CS}}$ AND $\overline{\text{PCP\_DS}}$ low	t_{mrwsu}	24	—	—	ns
PCP_R/W hold time after PCP_CS or PCP_DS high	t_{mrwhld}	8	—	—	ns
Data hold after $\overline{\text{PCP\_CS}}$ or $\overline{\text{PCP\_DS}}$ high	t_{mdhw}	8	—	—	ns
$\overline{\text{PCP\_CS}}$ or $\overline{\text{PCP\_DS}}$ high to $\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_DS}}$ low with $\overline{\text{PCP\_R/W}}$ high for next read[1]	t_{mwtrd}	30	—	—	ns
$\overline{\text{PCP\_CS}}$ or $\overline{\text{PCP\_DS}}$ high to $\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_DS}}$ low for next write[1]	t_{mwd}	30	—	—	ns
$\overline{\text{PCP\_RW}}$ rising to $\overline{\text{PCP\_BSY}}$ falling	$t_{mrwbsyl}$	—	2*DCLKP + 20	—	ns

1. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application. Hardware handshaking on the PCP_$\overline{\text{BSY}}$ pin/bit should be observed to prevent overflowing the input data buffer. *CS4953x4/CS4970x4 System Designer's Guide* should be consulted for the firmware speed limitations.

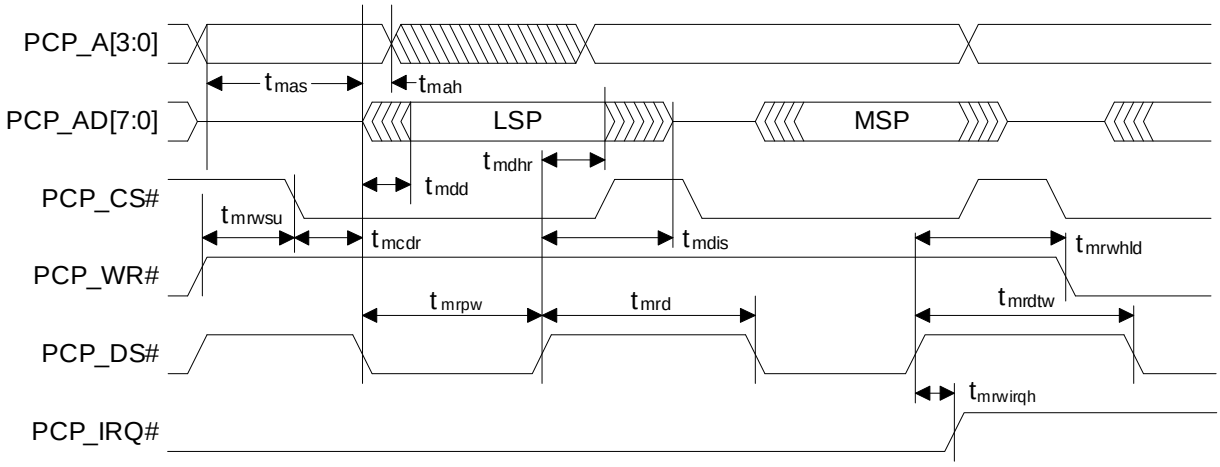


Figure 9. Parallel Control Port - Motorola® Slave Mode Read Cycle Timing

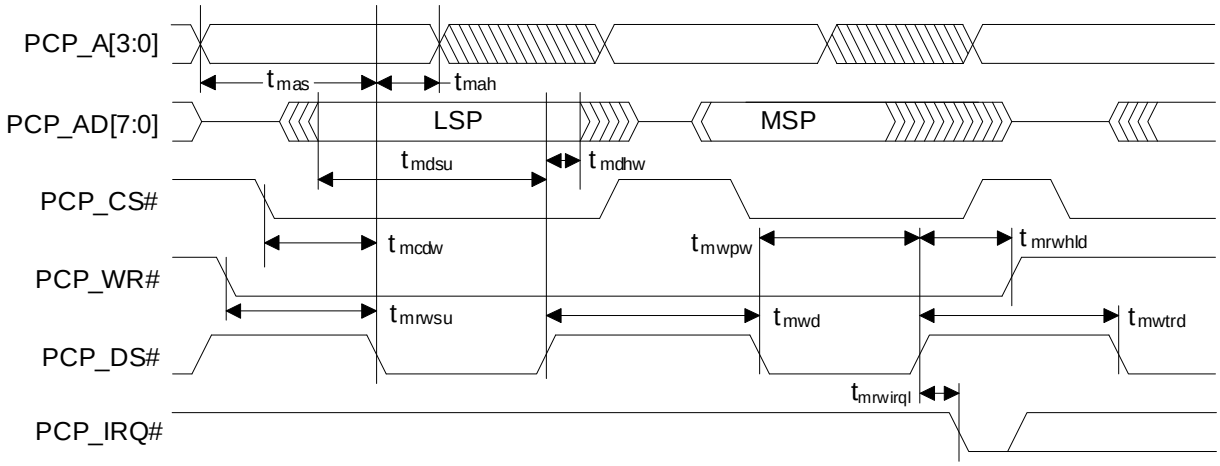
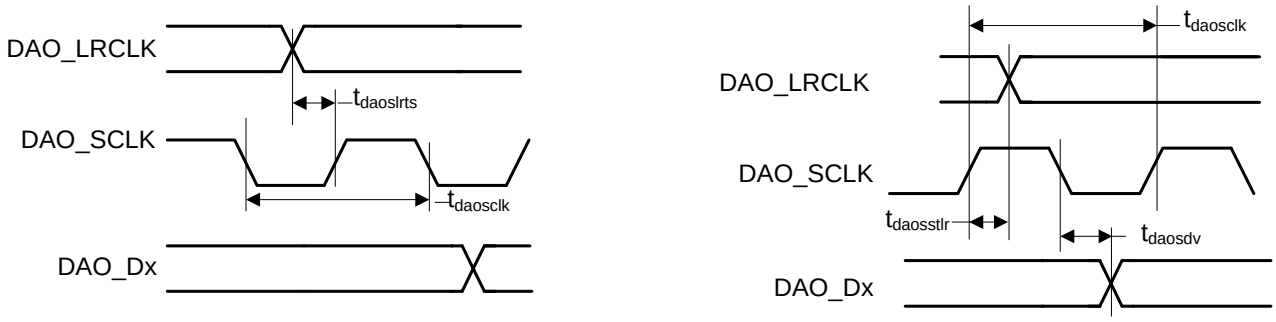


Figure 10. Parallel Control Port - Motorola Slave Mode Write Cycle Timing



Note: In these diagrams, Falling edge is the inactive edge of DAO_SCLK

Figure 14. Digital Audio Output Timing, Slave Mode (Relationship LRCLK to SCLK)

5.17 Switching Characteristics — SDRAM Interface

Refer to Figure 15 through Figure 18.

(SD_CLKOUT = SD_CLKIN)

Parameter	Symbol	Min	Typical	Max	Unit
SD_CLKIN high time	t_{sdclkh}	2.3	—	—	ns
SD_CLKIN low time	t_{sdclkl}	2.3	—	—	ns
SD_CLKOUT rise/fall time	$t_{sdclkrf}$	—	—	1	ns
SD_CLKOUT Frequency	—	—	150	—	MHz
SD_CLKOUT duty cycle	—	45	—	55	%
SD_CLKOUT rising edge to signal valid	t_{sdcmdv}	—	—	3.8	ns
Signal hold from SD_CLKOUT rising edge	t_{sdcmdh}	—	1.1	—	ns
SD_CLKOUT rising edge to SD_DQMn valid	t_{sddqv}	—	3.8	—	ns
SD_DQMn hold from SD_CLKOUT rising edge	t_{sddqh}	1.38	—	—	ns
SD_DATA valid setup to SD_CLKIN rising edge	t_{sddsu}	1.3	—	—	ns
SD_DATA valid hold to SD_CLKIN rising edge	t_{sddh}	2.1	—	—	ns
SD_CLKOUT rising edge to ADDRn valid	t_{sdav}	—	3.8	—	ns

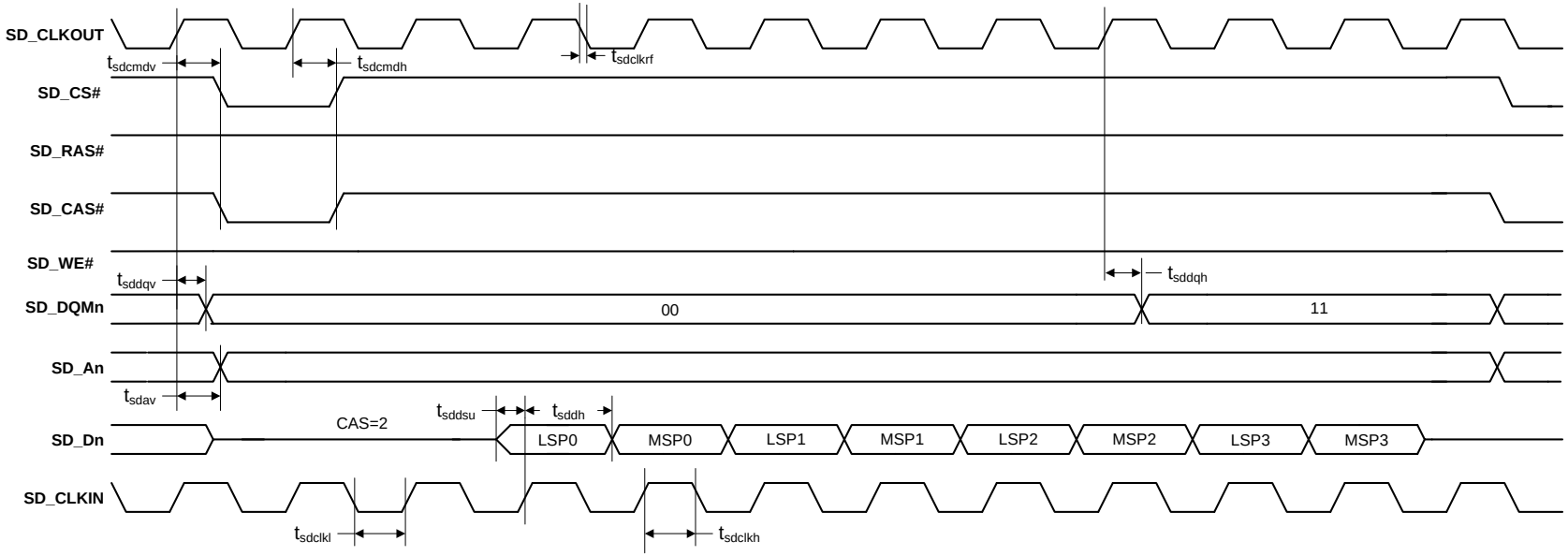


Figure 15. External Memory Interface - SDRAM Burst Read Cycle

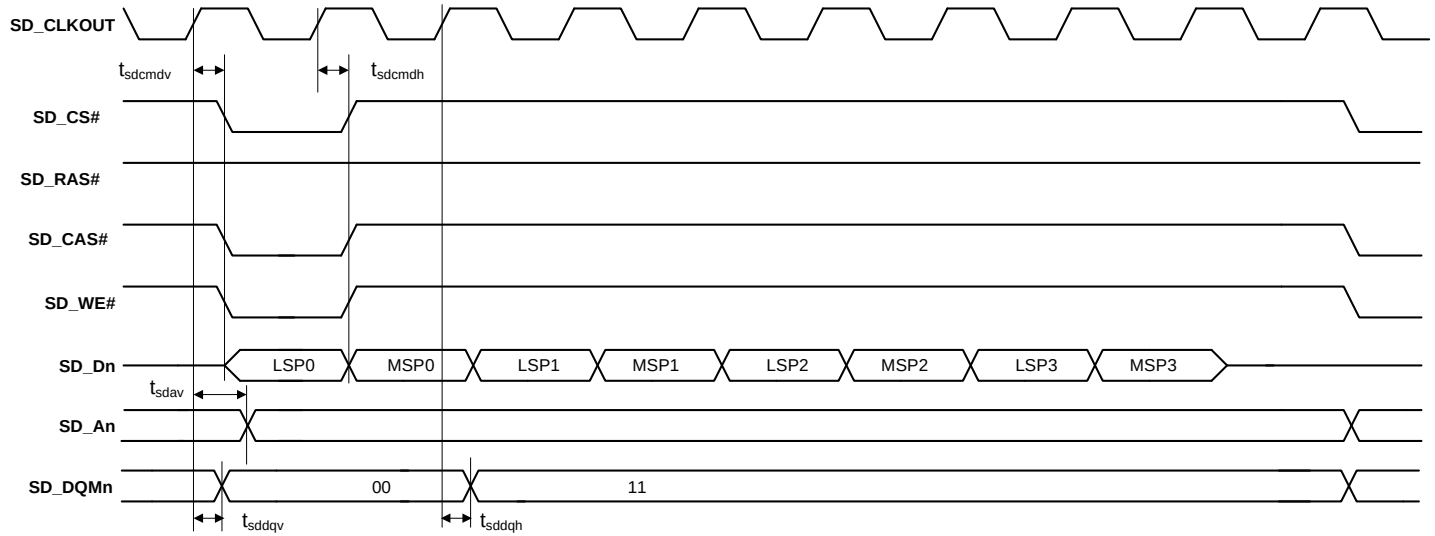


Figure 16. External Memory Interface - SDRAM Burst Write Cycle

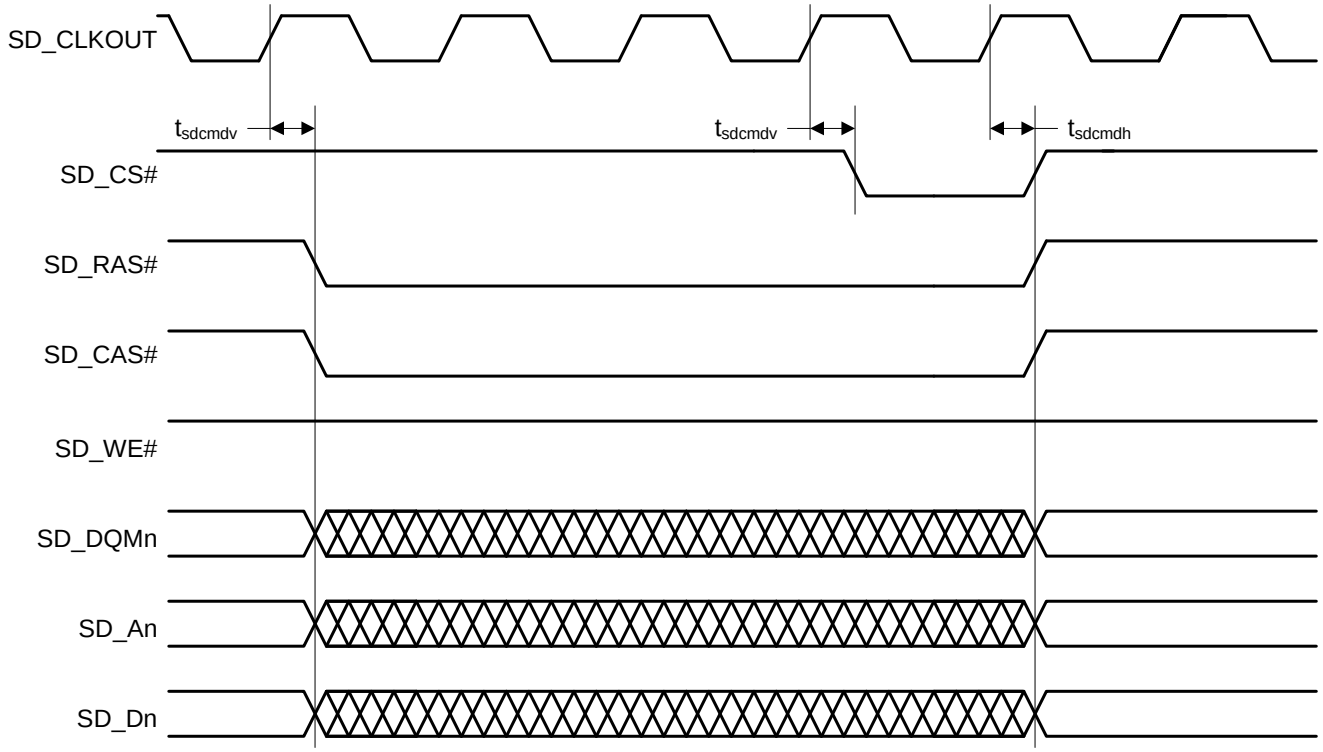


Figure 17. External Memory Interface - SDRAM Auto Refresh Cycle

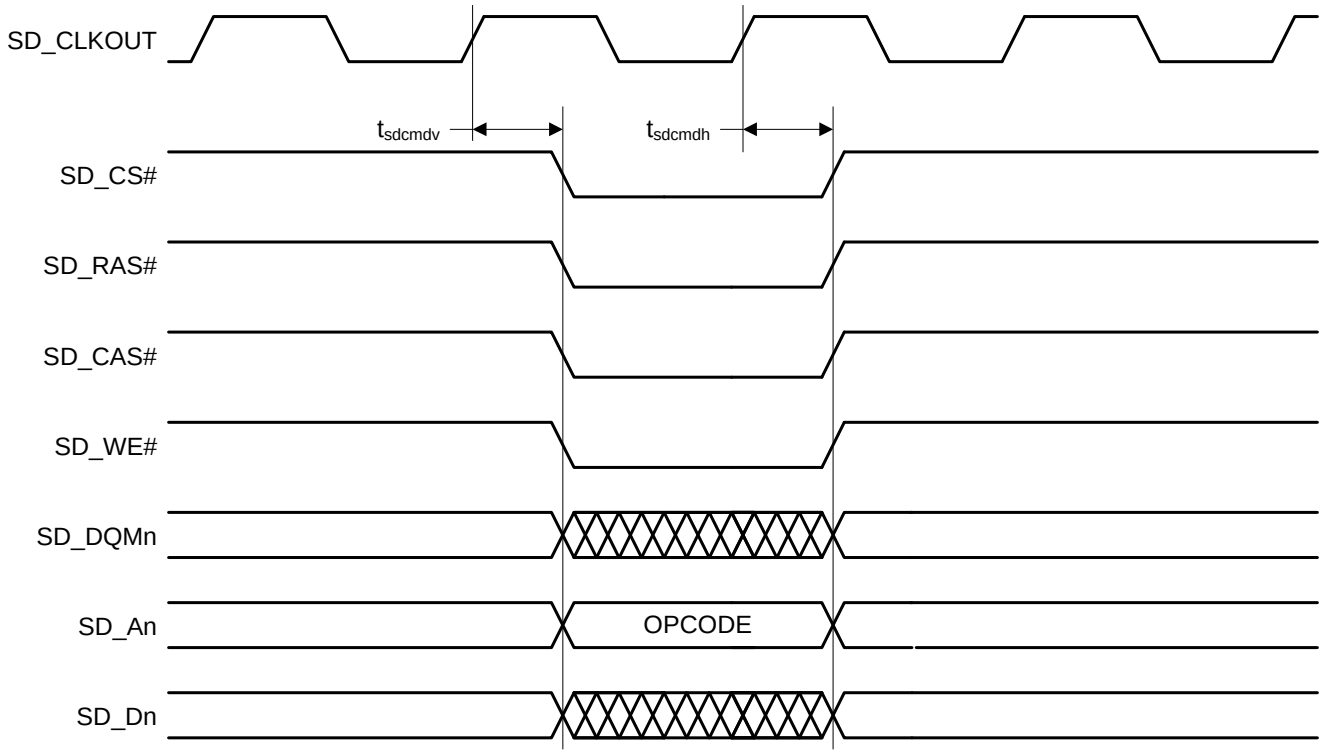


Figure 18. External Memory Interface - SDRAM Load Mode Register Cycle

6 Ordering Information

The CS4970x4 family part number is described as follows:

CS497NNI-XYZ

where

NN - Product Number Variant

I - ROM ID Number

X - Product Grade

Y - Package Type

Z - Lead (Pb) Free

Table 4. Ordering Information

Part No.	Status	Grade	Temp. Range	Package
CS497014-CVZ	Active	Commercial	0 to +70 °C	128-pin LQFP
CS47014-CVZR[1]	Active	Commercial	0 to +70 °C	
CS497024-CVZ	Active	Commercial	0 to +70 °C	128-pin LQFP
CS497024-CVZR[1]	Active	Commercial	0 to +70 °C	

1. R = Tape and reel

Note: Please contact the factory for availability of the -D (automotive grade) package.

7 Environmental, Manufacturing, and Handling Information

Table 5. Environmental, Manufacturing, & Handling Information

Model Number	Peak Reflow Temp	MSL Rating*	Max Floor Life
CS497014-CVZ	260 °C	3	7 Days
CS47014-CVZR	260 °C	3	7 Days
CS497024-CVZ	260 °C	3	7 Days
CS497024-CVZR	260 °C	3	7 Days

* MSL (Moisture Sensitivity Level) as specified by IPC/JEDEC J-STD-020.

8 Device Pin-Out Diagram

8.1 128-Pin LQFP Pin-Out Diagram

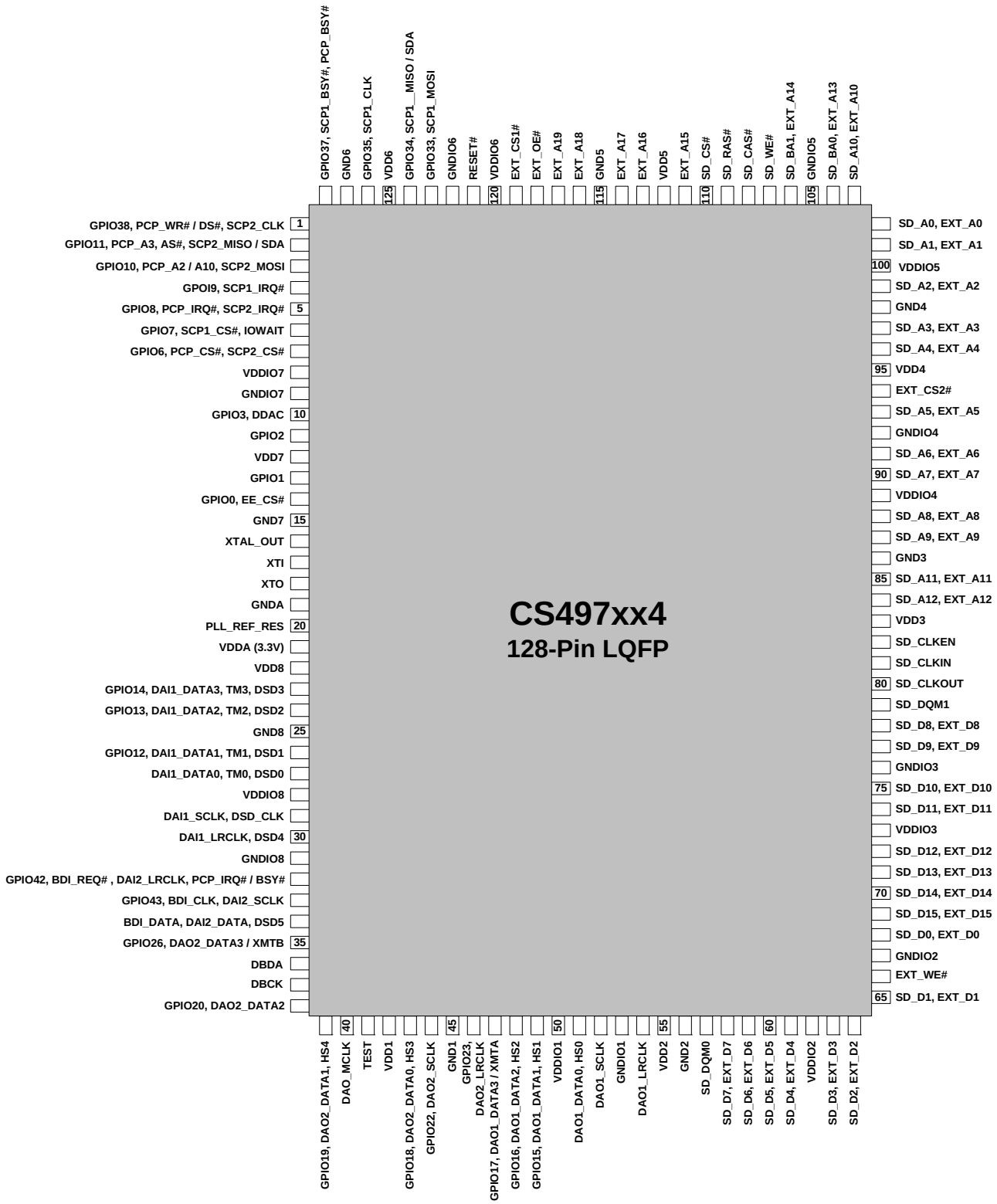


Figure 19. 128-Pin LQFP Pin-Out Diagram

9 Package Mechanical Drawings

9.1 128-Pin LQFP Package Drawing

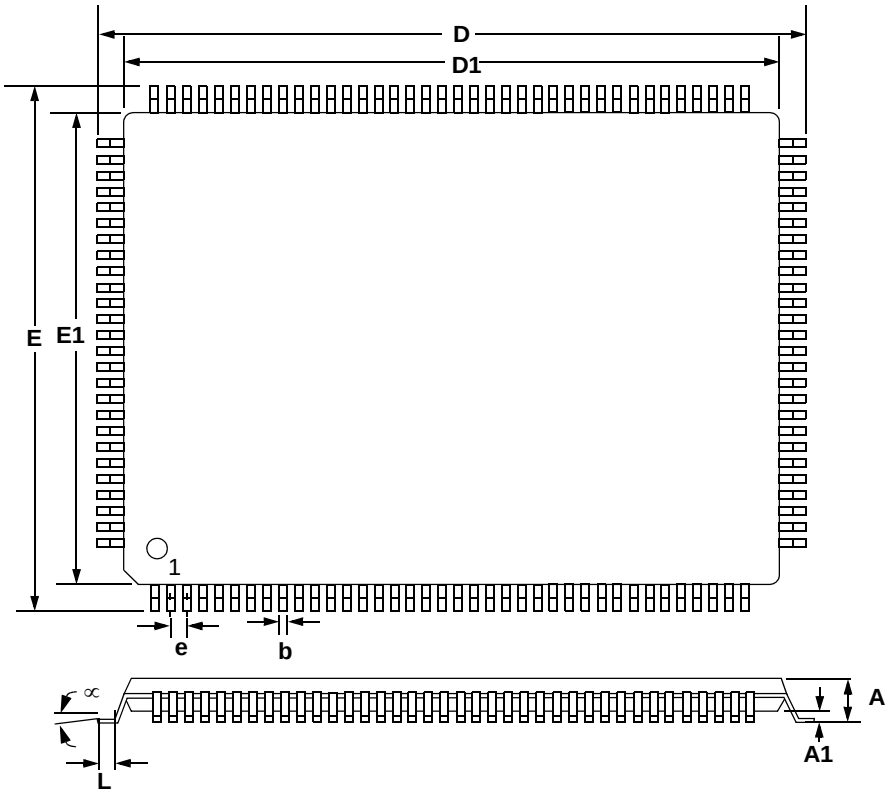


Figure 20. 128-Pin LQFP Package Drawing

Table 6. 128-Pin LQFP Package Characteristics

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.60	—	—	.063”
A1	0.05	—	0.15	.002”	—	.006”
b	0.17	0.22	0.27	.007”	.009”	.011”
D	22.00 BSC			.866”		
D1	20.00 BSC			.787”		
E	16.00 BSC			.630”		
E1	14.00 BSC			.551”		
e	0.50 BSC			.020”		
q	0°	3.5	7°	0°	3.5	7°
L	0.45	0.60	0.75	.018”	.024”	.030”
L1	1.00 REF			.039” REF		
TOLERANCES OF FORM AND POSITION						
ddd	0.08			.003”		

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find the one nearest you, go to www.cirrus.com.