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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	DAI/O, EBI/EMI, I²C, Parallel, SPI
Clock Rate	25MHz
Non-Volatile Memory	ROM (144kB)
On-Chip RAM	82kB
Voltage - I/O	3.30V
Voltage - Core	1.80V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	128-LQFP (20x14)
Purchase URL	https://www.e-xfl.com/product-detail/cirrus-logic/cs497024-dvzr

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1 Documentation Strategy

The CS4970x4 data sheet describes the CS4970x4 family of multichannel audio decoders. This document should be used in conjunction with the following documents when evaluating or designing a system around the CS4970x4 family of processors.

Table 1. CS4970x4 Related Documentation

Document Name	Description
CS4970x4 Data Sheet	This document
CS495314/CS4970x4 System Designer's Guide	A new consolidated documentation set that includes: • Detailed system design information including Typical Connection Diagrams, Boot-Procedures, Pin Descriptions, Etc. Also describes use of DSP Condenser tool. • Detailed firmware design information including signal processing flow diagrams and control API information
AN288 - *CS4953xx/CS4970x4 Firmware User's Manual*	Includes detailed firmware design information including signal processing flow diagrams and control API information

The scope of the CS4970x4 data sheet is primarily to provide hardware specifications of the CS4970x4 family of devices. This includes hardware functionality, characteristic data, pinout, and packaging information.

The intended audience for the CS4970x4 data sheet is the system PCB designer, MCU programmer, and the quality control engineer.

2 Overview

The CS4970x4 DSP Family, combined with Cirrus Logic's comprehensive library of audio processing algorithms, enables the development of next-generation high-definition audio solutions. Cirrus Logic also provides a broad array of digital interface products and audio converters to meet your audio system-level design requirements.

Note: The CS4970x4 is available in a 128-pin LQFP package.

The audio processing features of the CS4970x4 product family are a superset of audio features available in the CS4953xx product family.

Refer to Table 2 on page 5 for the speed and firmware features of the CS4970x4 product family.

Table 2. Device and Firmware Selection Guide

Device	Decode Processor (DSP-A)[1]	Matrix Processor Module (DSP-A)[1]	Virtualizer Processor Module (DSP-B)[1]	Post Processor Module (DSP-B)[1]
CS497014 300MACS	Stereo PCM (4:1/2:1 Down-sampling and 1:2/1:4 U-sampling Options)[2] Multichannel PCM (4:1/2:1 Down-sampling and 1:2/1:4 Up-sampling Options)[2] Dolby Digital MPEG-2 AAC LC 5.1 Dolby Digital Plus Dolby TrueHD[3]	Dolby Pro Logic II / IIx / IIz 7.1 SRS Circle Surround II / Circle Surround Auto / Circle Surround Decoder Optimized (Stereo In) Cirrus Original Multi-Channel Surround 2 (Effects / Reverb Processor) Crossbar (Down-mix / Up-mix) (Simultaneous Process)	Cirrus Virtualizer Technology Dolby Headphone 2 Dolby Virtual Speaker 2 SRS CS Headphone SRS TruSurround HD/HD4	APP (Advanced Post-processing) –Tone Control –Select 2 –PEQ (up to 11 Bands) –Delay (Speaker to Listening Position Alignment and/or Lip Sync) –7.1 Bass Manager –Audio Manager –4:1/2:1 Down-sampling[2] SRS TruVolume 7.1 Multichannel Dolby Volume Multichannel
CS497004 300MACS **CS497024** 300MACS	Same as CS497014 + DTS, DTS-ES, DTS96/24 DTS-HD Master Audio[3] DTS-HD High Res Audio[3] DTS Express 5.1	Same as CS497014 + DTS Neo:6, DTS Neural Surround		

1. Additional processing (MPMA, MPMB/VPM, PPM) post any of the HD audio decoders may be limited. Contact your Cirrus Logic FAE for the latest concurrency matrix.
2. Downsampling and Upsampling functionality is located in the operating system. The Cirrus Decimator (Down-Sampler) is also available as a separate post-processing module that is described in the application note AN288PPI.
3. The indicated HD audio decoder algorithms require external SDRAM. Consult your Cirrus Logic FAE for the recommended SDRAM size for your design.

2.1 Migrating from CS495xx(3) to CS4970x4

CS4970x4 was designed to provide an easy upgrade path from the CS495xx and CS4953x. There are some small differences the hardware designer should be aware of:

- The PLL supply voltage on the CS4970x4 is 3.3V vs. 1.8V on the CS495xx.
- The PLL filter topology is simpler when using the CS4970x4 rather than the CS495xx.
- The CS4970x4 adds support for Time-division multiplexing (TDM) mode on both audio input and output ports.
- The CS4970x4 does not support external static random access memory (SRAM) operation.
- The CS4970x4 external Synchronous dynamic random access memory (SDRAM) bus speed is fixed at 150 MHz vs. the 120 MHz maximum bus speed for the CS495xx. Some firmware modules also support a 75 MHz CS4970x4 SDRAM bus speed. Refer to AN304 for details.
- The CS4970x4 CLKOUT pin can output XTALI or XTALI/2. The CS495xx can only output XTALI.

2.2 Licensing

Licenses are required for all of the third party audio decoding/processing algorithms listed below, including the application notes. Contact your local Cirrus Sales representative for more information.

3 Code Overlays

The suite of software available for the CS4970x4 family consists of operating systems (OS) and a library of overlays. The overlays have been divided into three main groups: decoders, matrix processors, and postprocessors. All software components are defined in the following list:

- **OS/Kernel** - Encompasses all non-audio processing tasks, including loading data from external memory, processing host messages, calling audio-processing subroutines, auto-detection, error concealment, etc.
- **Decoders** - Any module that initially writes data into the audio I/O buffers, e.g. AC-3™, DTS, PCM, etc. All the decoding/processing algorithms listed require delivery of PCM or IEC61937-packed, compressed data via I^2S- or LJ-formatted digital audio to the CS4970x4 from A/D converters, SPDIF Rx, HDMI Rx, etc.
- **Matrix-processors** - Any module that processes audio I/O buffer PCM data in-place before the Post-processors. Generally speaking, these modules alter the number of valid channels in the audio I/O buffer through processes like Virtualization (n⇨2 channels) or Matrix Decoding (2⇨n channels). Examples are Dolby ProLogic IIx and DTS Neo:6.
- **Virtualizer-processor** - Any module that encodes PCM data into fewer output channels than input channels (n⇨2 channels) with the effect of providing “phantom” speakers to represent the physical audio channels that were eliminated. Examples are Dolby Headphone 2 and Dolby Virtual Speaker 2. Generally speaking, these modules reduce the number of valid channels in the audio I/O buffer.
- **Post-processors** - Any module that processes audio I/O buffer PCM data in-place after the matrix processors. Examples are bass management, audio manager, tone control, EQ, delay, customer-specific effects, Dolby Headphone/Virtual Speaker, etc.

The overlay structure reduces the time required to reconfigure the DSP when a processing change is requested. Each overlay can be reloaded independently without disturbing the other overlays. For example, when a new decoder is selected, the OS, matrix-, and post-processors do not need to be reloaded — only the new decoder (the same is true for the other overlays).

4 Hardware Functional Description

4.1 Coyote DSP Core

The CS4970x4 is a dual-core Coyote DSP with separate X and Y data and P code memory spaces. Each core is a high-performance, 32-bit, user-programmable, fixed-point DSP that is capable of performing two multiply accumulate (MAC) operations per clock cycle. Each core has eight 72-bit accumulators, four X- and four Y-data registers, and 12 index registers.

Both DSP cores are coupled to a flexible DMA engine. The DMA engine can move data between peripherals such as the digital audio input (DAI) and digital audio output (DAO), external memory, or any DSP core memory, all without the intervention of the DSP. The DMA engine offloads data move instructions from the DSP core, leaving more MIPS available for signal processing instructions.

CS4970x4 functionality is controlled by application codes that are stored in on-board ROM or downloaded to the CS4970x4 from a host MCU or external FLASH/EEPROM. Users can choose to use standard audio decoder and post-processor modules which are available from Cirrus Logic.

The CS4970x4 is suitable for audio decoder, audio post-processor, audio encoder, DVD audio/video player, and digital broadcast decoder applications.

4.1.1 DSP Memory

Each DSP core has its own on-chip data and program RAM and ROM and does not require external memory for any of today’s popular audio algorithms including Dolby Digital Surround EX, AAC Multichannel, DTS-ES 96/24, and THX Ultra2. However, if the end-system design requires support of the new high-definition audio formats, external SDRAM will be needed to support Dolby TrueHD and DTS-HD master audio.

The memory maps for the DSPs are as follows. All memory sizes are composed of 32-bit words.

Table 3. CS4970x4 DSP Memory Sizes

Memory Type	DSP A	DSP B
X	16K SRAM, 32K ROM	10K SRAM, 8K ROM
Y	24K SRAM, 32K ROM	16K SRAM, 16K ROM
P	8K SRAM, 32K ROM	8K SRAM, 24K ROM

4.1.2 DMA Controller

The powerful 12-channel DMA controller can move data between 8 on-chip resources. Each resource has its own arbiter: X, Y, and P RAM/ROMs on DSP A; X, Y, and P RAM/ROMs on DSP B; external memory; and the peripheral bus. Modulo and linear addressing modes are supported, with flexible start address and increment controls. The service interval for each DMA channel as well as up to 6 interrupt events, is programmable.

4.2 On-chip DSP Peripherals

4.2.1 Digital Audio Input Port (DAI)

The 12-channel (6-line) DAI port supports a wide variety of data input formats. The port is capable of accepting PCM or IEC61937. Up to 32-bit word lengths are supported. Additionally, support is provided for audio data input to the DSP via the DAI from an HDMI receiver.

The port has two independent slave-only clock domains. Each data input can be independently assigned to a clock domain. The sample rate of the input clock domains can be determined automatically by the DSP, which off-loads the task of monitoring the SPDIF receiver from the host. A time-stamping feature allows the input data to be sample-rate converted via software.

4.2.2 Digital Audio Output Port (DAO)

There are two DAO ports. Each port can output 8 channels of up to 32-bit PCM data. The port supports data rates from 32 kHz to 192 kHz. Each port can be configured as an independent clock domain in slave mode, or the ratio of the two clocks can be set to even multiples of each other in master mode. The two ports can also be ganged together into a single clock domain. Each port has one serial audio pin that can be configured as a 192-kHz SPDIF transmitter (data with embedded clock on a single line).

4.2.3 Serial Control Port 1 & 2 (I^2C or SPI)

There are two on-chip serial control ports that are capable of operating as master or slave in either I^2C or SPI modes. SCP1 defaults to slave operation. It is dedicated for external host-control and supports an external clock up to 50 MHz in SPI mode. This high clock speed enables very fast code download, control or data delivery. SCP2 defaults to master mode and is dedicated for booting from external serial Flash memory or for audio sub-system control.

4.2.4 External Memory Interface

The external memory interface controller supports up to 128 Mbits of SDRAM, using a 16-bit data bus.

4.2.5 General Purpose Input/Output (GPIO)

Many of the CS4970x4 peripheral pins are multiplexed with GPIO. Each GPIO can be configured as an output, an input, or an input with interrupt. Each input-pin interrupt can be configured as rising edge, falling edge, active-low, or active-high.

4.2.6 Phase-locked Loop (PLL)-based Clock Generator

The low-jitter PLL generates integer or fractional multiples of a reference frequency which are used to clock the DSP core and peripherals. Through a second PLL divider chain, a dependent clock domain can be output on the DAO port for driving audio converters. The CS4970x4 defaults to running from the external reference frequency and can be switched to use the PLL output after overlays have been loaded and configured, either

5.6 Switching Characteristics—$\overline{\text{RESET}}$

Parameter	Symbol	Min	Max	Unit
$\overline{\text{RESET}}$ minimum pulse width low	T_{rstl}	1	—	µs
All bidirectional pins high-Z after $\overline{\text{RESET}}$ low	T_{rst2z}	—	100	ns
Configuration pins setup before $\overline{\text{RESET}}$ high	T_{rstsu}	50	—	ns
Configuration pins hold after $\overline{\text{RESET}}$ high	T_{rsthld}	20	—	ns

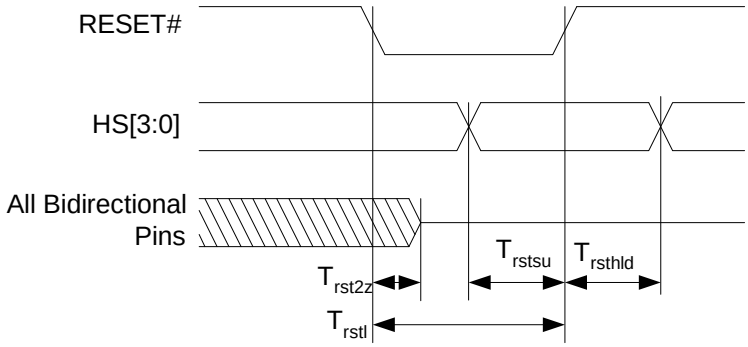

Figure 1. $\overline{\text{RESET}}$ Timing

5.7 Switching Characteristics — XTI

Parameter	Symbol	Min	Max	Unit
External Crystal operating frequency[1]	F_{xtal}	12.288	24.576	MHz
XTI period	T_{clki}	41	81.4	ns
XTI high time	T_{clkih}	16.4	—	ns
XTI low time	T_{clkil}	16.4	—	ns
External Crystal Load Capacitance (parallel resonant)[2]	C_L	10	18	pF
External Crystal Equivalent Series Resistance	ESR	—	50	Ω

1. Part characterized with the following crystal frequency values: 12.288 and 24.576 MHz.
2. C_L refers to the total load capacitance as specified by the crystal manufacturer. Crystals which require a C_L outside this range should be avoided. The crystal oscillator circuit design should follow the crystal manufacturer's recommendation for load capacitor selection.

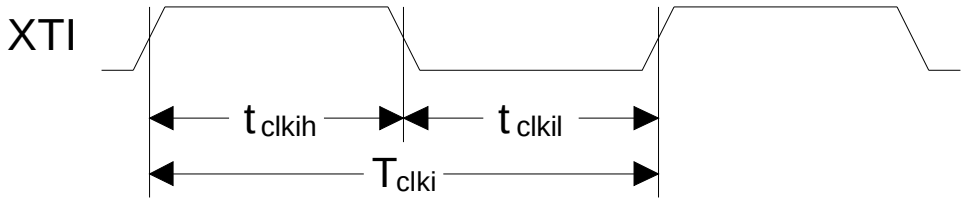

Figure 2. XTI Timing

5.9 Switching Characteristics — Serial Control Port - SPI Slave Mode

Parameter	Symbol	Min	Typical	Max	Units
SCP_CLK frequency[1,2]	f_{spisck}	—	—	25	MHz
SCP_$\overline{CS}$ falling to SCP_CLK rising[2]	t_{spicss}	24	—	—	ns
SCP_CLK low time[2]	t_{spickl}	20	—	—	ns
SCP_CLK high time[2]	t_{spickh}	20	—	—	ns
Setup time SCP_MOSI input	t_{spidsu}	5	—	—	ns
Hold time SCP_MOSI input	t_{spidh}	5	—	—	ns
SCP_CLK low to SCP_MISO output valid[2]	t_{spidov}	—	—	11	ns
SCP_CLK falling to SCP_$\overline{IRQ}$ rising[2]	$t_{spiirqh}$	—	—	20	ns
SCP_$\overline{CS}$ rising to SCP_$\overline{IRQ}$ falling[2]	$t_{spiirql}$	0	—	—	ns
SCP_CLK low to SCP_$\overline{CS}$ rising[2]	t_{spicsh}	24	—	—	ns
SCP_$\overline{CS}$ rising to SCP_MISO output high-Z	$t_{spicsdz}$	—	20	—	ns
SCP_CLK rising to SCP_$\overline{BSY}$ falling[2]	$t_{spicbsyl}$	—	3∗DCLKP+20	—	ns

1. The specification f_{spisck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application. Flow control using the SCP_$\overline{BSY}$ pin should be implemented to prevent overflow of the input data buffer. At boot the maximum speed is Fxtal/3.
2. When SCP1 is in SPI slave mode, very slow rise and fall times of the SCP_CLK edges may make the edges of the SCP_CLK more susceptible to noise, resulting in non-smooth edges. Any glitch at the threshold levels of the SCP port input signals could result in abnormal operation of the port. In systems that have noise coupling onto SCP_CLK, slow rise and fall times may cause host communication problems. Increasing rise time makes host communication more reliable.

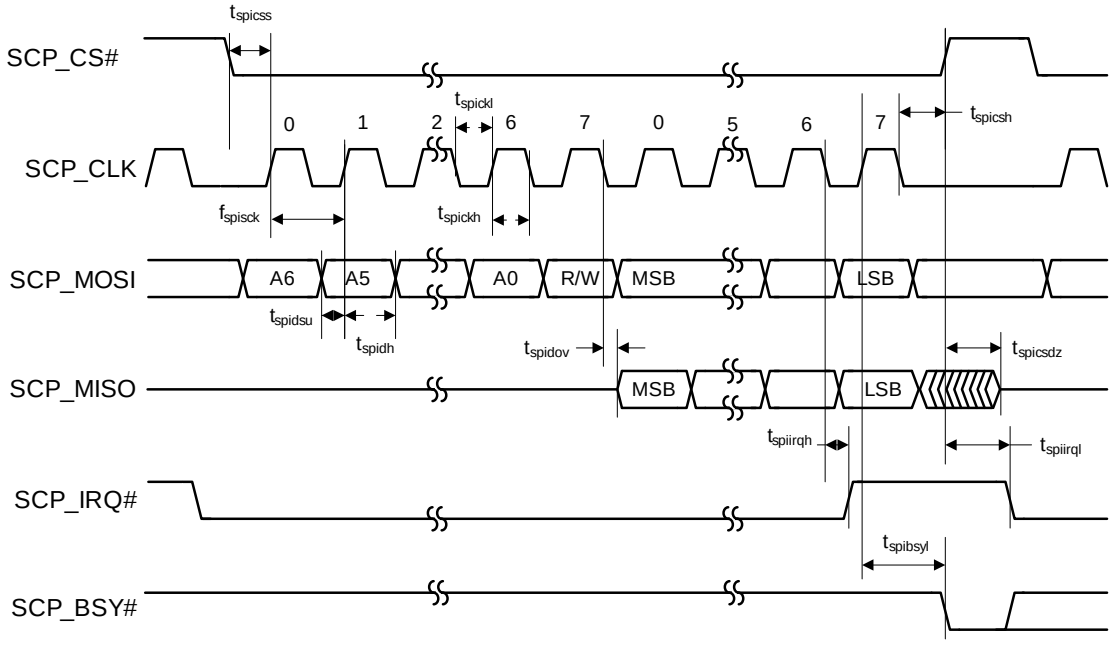

Figure 3. Serial Control Port - SPI Slave Mode Timing

5.10 Switching Characteristics — Serial Control Port - SPI Master Mode

Parameter	Symbol	Min	Typical	Max	Units
SCP_CLK frequency[1, 2]	f_{spisck}	—	—	$F_{xtal}/2$	MHz
SCP_$\overline{CS}$ falling to SCP_CLK rising [3]	t_{spicss}	—	11*DCLKP + (SCP_CLK PERIOD)/2	—	ns
SCP_CLK low time	t_{spickl}	16.9	—	—	ns
SCP_CLK high time	t_{spickh}	16.9	—	—	ns
Setup time SCP_MISO input	t_{spidsu}	11	—	—	ns
Hold time SCP_MISO input	t_{spidh}	5	—	—	ns
SCP_CLK low to SCP_MOSI output valid	t_{spidov}	—	—	11	ns
SCP_CLK low to SCP_$\overline{CS}$ falling	t_{spicsl}	7	—	—	ns
SCP_CLK low to SCP_$\overline{CS}$ rising	t_{spicsh}	—	11*DCLKP + (SCP_CLK PERIOD)/2	—	ns
Bus free time between active SCP_$\overline{CS}$	t_{spicsx}	—	3*DCLKP	—	ns
SCP_CLK falling to SCP_MOSI output high-Z	t_{spidz}	—	—	20	ns

1. The specification f_{spisck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application.
2. See Section 5.7.
3. SCP_CLK PERIOD refers to the period of SCP_CLK as being used in a given application. It does not refer to a tested parameter.

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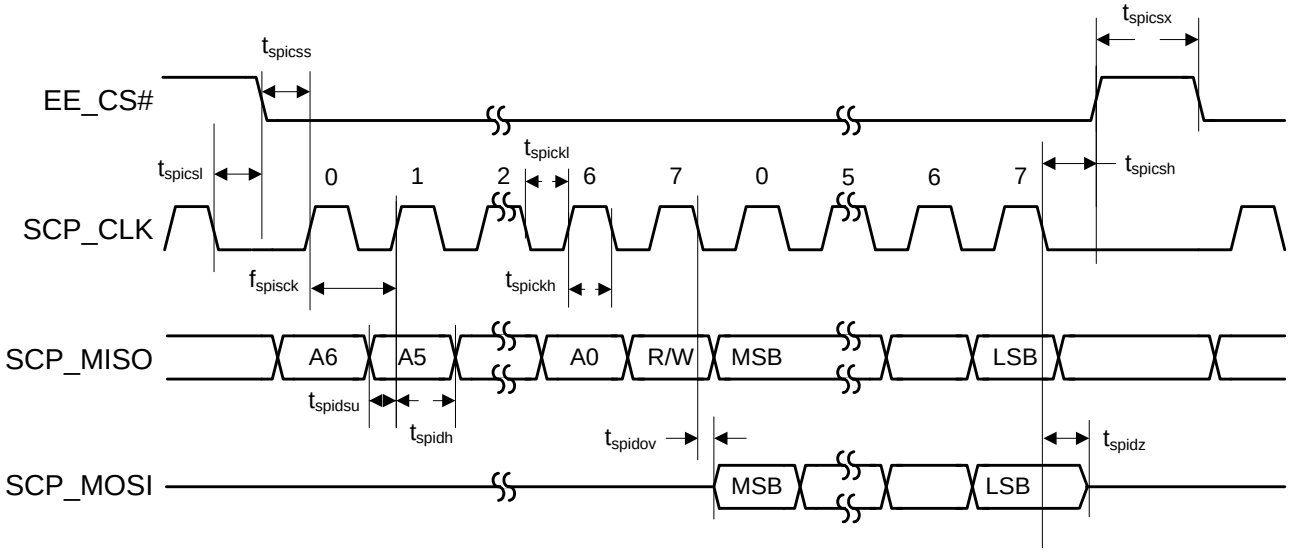


Figure 4. Serial Control Port - SPI Master Mode Timing

5.11 Switching Characteristics — Serial Control Port - I²C Slave Mode

Parameter	Symbol	Min	Typical	Max	Units
SCP_CLK frequency[1]	f_{iicck}	—	—	400	kHz
SCP_CLK low time	t_{iicckl}	1.25	—	—	µs
SCP_CLK high time	t_{iicckh}	1.25	—	—	µs
SCP_SCK rising to SCP_SDA rising or falling for START or STOP condition	$t_{iicckcmd}$	1.25	—	—	µs
START condition to SCP_CLK falling	$t_{iicstscl}$	1.25	—	—	µs
SCP_CLK falling to STOP condition	t_{iicstp}	2.5	—	—	µs
Bus free time between STOP and START conditions	t_{iicbft}	3	—	—	µs
Setup time SCP_SDA input valid to SCP_CLK rising	t_{iicsu}	100	—	—	ns
Hold time SCP_SDA input after SCP_CLK falling[2]	t_{iich}	0	—	—	ns
SCP_CLK low to SCP_SDA out valid	t_{iicdov}	—	—	18	ns
SCP_CLK falling to SCP_$\overline{IRQ}$ rising	$t_{iicirqh}$	—	—	3∗DCLKP + 40	ns
NAK condition to SCP_$\overline{IRQ}$ low	$t_{iicirql}$	—	3∗DCLKP + 20	—	ns
SCP_CLK rising to SCB_$\overline{BSY}$ low	$t_{iicbsyl}$	—	3∗DCLKP + 20	—	ns

1. The specification f_{iicck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application. Flow control using the SCP_$\overline{BSY}$ pin should be implemented to prevent overflow of the input data buffer.
2. This parameter is measured from the ViL level at the falling edge of the clock.

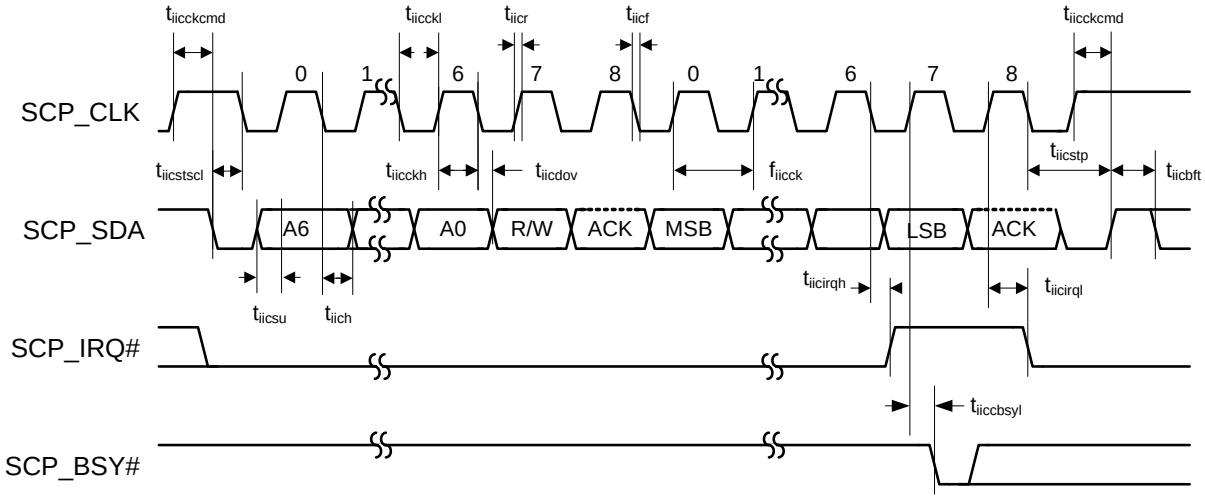


Figure 5. Serial Control Port - I²C Slave Mode Timing

5.12 Switching Characteristics — Serial Control Port - I²C Master Mode

Parameter	Symbol	Min	Max	Units
SCP_CLK frequency[1]	f_{iicck}	—	400	kHz
SCP_CLK low time	t_{iicckl}	1.25	—	µs
SCP_CLK high time	t_{iicckh}	1.25	—	µs
SCP_SCK rising to SCP_SDA rising or falling for START or STOP condition	$t_{iicckcmd}$	1.25	—	µs
START condition to SCP_CLK falling	$t_{iicstscl}$	1.25	—	µs
SCP_CLK falling to STOP condition	t_{iicstp}	2.5	—	µs
Bus free time between STOP and START conditions	t_{iicbft}	3	—	µs
Setup time SCP_SDA input valid to SCP_CLK rising	t_{iicsu}	100	—	ns
Hold time SCP_SDA input after SCP_CLK falling[2]	t_{iich}	0	—	ns
SCP_CLK low to SCP_SDA out valid	t_{iicdov}	—	36	ns

1. The specification f_{iicck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application.
2. This parameter is measured from the ViL level at the falling edge of the clock.

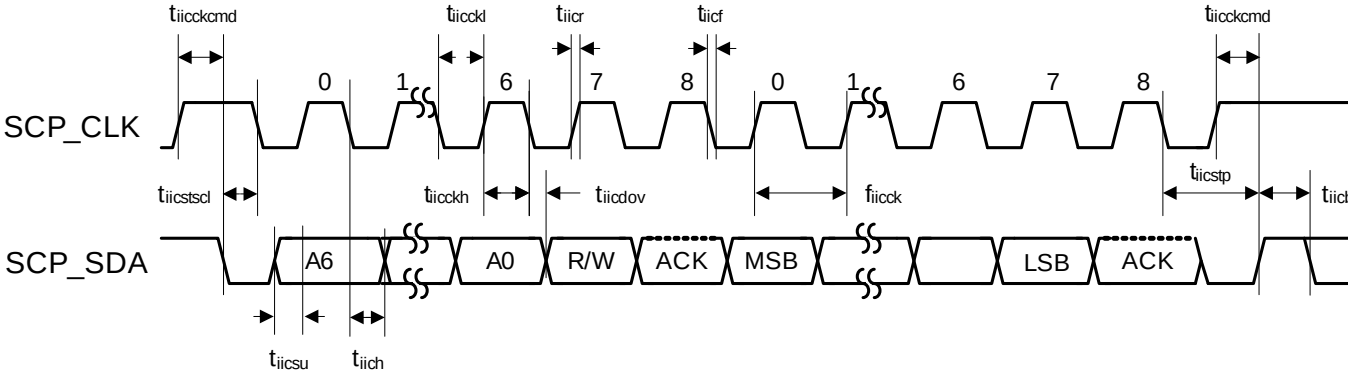


Figure 6. Serial Control Port - I²C Master Mode Timing

5.13 Switching Characteristics — Parallel Control Port - Intel Slave Mode

Parameter	Symbol	Min	Typical	Max	Unit
Address setup before $\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_RD}}$ low or $\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_WR}}$ low	t_{ias}	5	—	—	ns
Address hold time after $\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_RD}}$ low or $\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_WR}}$ high	t_{iah}	5	—	—	ns
Read					

Parameter	Symbol	Min	Typical	Max	Unit
Delay between $\overline{\text{PCP\_RD}}$ then $\overline{\text{PCP\_CS}}$ low or $\overline{\text{PCP\_CS}}$ then $\overline{\text{PCP\_RD}}$ low	t_{icdr}	0	—	—	ns
Data valid after $\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_RD}}$ low	t_{idd}	—	—	18	ns
$\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_RD}}$ low for read	t_{irpw}	24	—	—	ns
Data hold time after $\overline{\text{PCP\_CS}}$ or $\overline{\text{PCP\_RD}}$ high	t_{idhr}	8	—	—	ns
Data high-Z after $\overline{\text{PCP\_CS}}$ or $\overline{\text{PCP\_RD}}$ high	t_{idis}	—	—	18	ns
$\overline{\text{PCP\_CS}}$ or $\overline{\text{PCP\_RD}}$ high to $\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_RD}}$ low for next read[1]	t_{ird}	30	—	—	ns
$\overline{\text{PCP\_CS}}$ or $\overline{\text{PCP\_RD}}$ high to $\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_WR}}$ low for next write[1]	t_{irdtw}	30	—	—	ns
$\overline{\text{PCP\_RD}}$ rising to $\overline{\text{PCP\_IRQ}}$ rising	$t_{irdirqhl}$	—	—	12	ns
Write					
Delay between $\overline{\text{PCP\_WR}}$ then $\overline{\text{PCP\_CS}}$ low or $\overline{\text{PCP\_CS}}$ then $\overline{\text{PCP\_WR}}$ low	t_{icdw}	0	—	—	ns
Data setup before $\overline{\text{PCP\_CS}}$ or $\overline{\text{PCP\_WR}}$ high	t_{idsu}	8	—	—	ns
$\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_WR}}$ low for write	t_{iwpw}	24	—	—	ns
Data hold after $\overline{\text{PCP\_CS}}$ or $\overline{\text{PCP\_WR}}$ high	t_{idhw}	8	—	—	ns
$\overline{\text{PCP\_CS}}$ or $\overline{\text{PCP\_WR}}$ high to $\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_RD}}$ low for next read[1]	t_{iwtrd}	30	—	—	ns
$\overline{\text{PCP\_CS}}$ or $\overline{\text{PCP\_WR}}$ high to $\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_WR}}$ low for next write[1]	t_{iwd}	30	—	—	ns
$\overline{\text{PCP\_WR}}$ rising to $\overline{\text{PCP\_BSY}}$ falling	$t_{iwrbsyl}$	—	2*DCLKP + 20	—	ns

1. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application. Hardware handshaking on the PCP_$\overline{\text{BSY}}$ pin/bit should be observed to prevent overflowing the input data buffer. *CS4953x4/CS4970x4 System Designer's Guide* should be consulted for the firmware speed limitations.

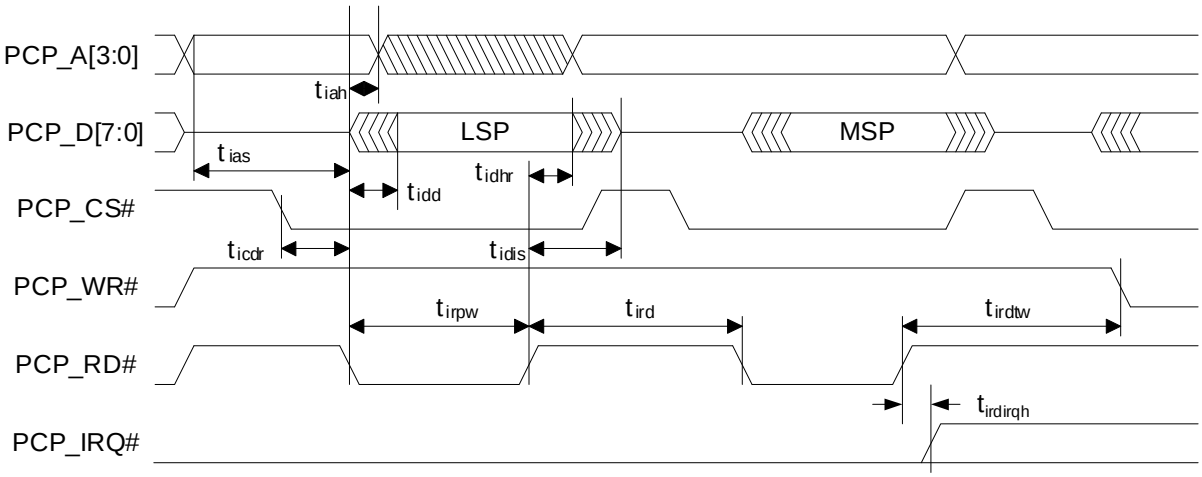


Figure 7. Parallel Control Port - Intel® Slave Mode Read Cycle

5.14 Switching Characteristics — Parallel Control Port - Motorola Slave Mode

Parameter	Symbol	Min	Typical	Max	Unit
Address setup before $\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_DS}}$ low	t_{mas}	5	—	—	ns
Address hold time after $\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_DS}}$ low	t_{mah}	5	—	—	ns
Read					
Delay between $\overline{\text{PCP\_DS}}$ then $\overline{\text{PCP\_CS}}$ low or $\overline{\text{PCP\_CS}}$ then $\overline{\text{PCP\_DS}}$ low	t_{mcdr}	0	—	—	ns
Data valid after $\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_DS}}$ low with PCP_R/W high	t_{mdd}	—	—	19	ns
$\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_DS}}$ low for read	t_{mrpw}	24	—	—	ns
Data hold time after $\overline{\text{PCP\_CS}}$ or $\overline{\text{PCP\_DS}}$ high after read	t_{mdhr}	8	—	—	ns
Data high-Z after $\overline{\text{PCP\_CS}}$ or $\overline{\text{PCP\_DS}}$ high after read	t_{mdis}	—	—	18	ns
$\overline{\text{PCP\_CS}}$ or $\overline{\text{PCP\_DS}}$ high to $\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_DS}}$ low for next read[1]	t_{mrd}	30	—	—	ns
$\overline{\text{PCP\_CS}}$ or $\overline{\text{PCP\_DS}}$ high to $\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_DS}}$ low for next write[1]	t_{mrdtw}	30	—	—	ns
PCP_RW rising to PCP_IRQ falling	$t_{mrwirqh}$	—	—	12	ns
Write					
Delay between $\overline{\text{PCP\_DS}}$ then $\overline{\text{PCP\_CS}}$ low or $\overline{\text{PCP\_CS}}$ then $\overline{\text{PCP\_DS}}$ low	t_{mcdw}	0	—	—	ns
Data setup before $\overline{\text{PCP\_CS}}$ or $\overline{\text{PCP\_DS}}$ high	t_{mdsu}	8	—	—	ns
$\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_DS}}$ low for write	t_{mwpw}	24	—	—	ns
$\overline{\text{PCP\_R/W}}$ setup before $\overline{\text{PCP\_CS}}$ AND $\overline{\text{PCP\_DS}}$ low	t_{mrwsu}	24	—	—	ns
PCP_R/W hold time after PCP_CS or PCP_DS high	t_{mrwhld}	8	—	—	ns
Data hold after $\overline{\text{PCP\_CS}}$ or $\overline{\text{PCP\_DS}}$ high	t_{mdhw}	8	—	—	ns
$\overline{\text{PCP\_CS}}$ or $\overline{\text{PCP\_DS}}$ high to $\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_DS}}$ low with $\overline{\text{PCP\_R/W}}$ high for next read[1]	t_{mwtrd}	30	—	—	ns
$\overline{\text{PCP\_CS}}$ or $\overline{\text{PCP\_DS}}$ high to $\overline{\text{PCP\_CS}}$ and $\overline{\text{PCP\_DS}}$ low for next write[1]	t_{mwd}	30	—	—	ns
$\overline{\text{PCP\_RW}}$ rising to $\overline{\text{PCP\_BSY}}$ falling	$t_{mrwbsyl}$	—	2*DCLKP + 20	—	ns

1. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application. Hardware handshaking on the PCP_$\overline{\text{BSY}}$ pin/bit should be observed to prevent overflowing the input data buffer. *CS4953x4/CS4970x4 System Designer's Guide* should be consulted for the firmware speed limitations.

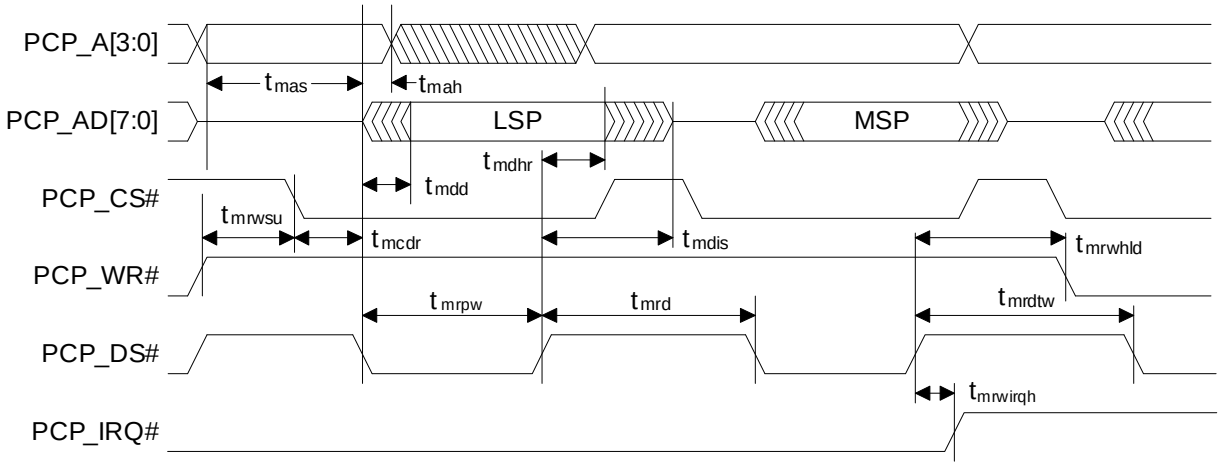


Figure 9. Parallel Control Port - Motorola® Slave Mode Read Cycle Timing

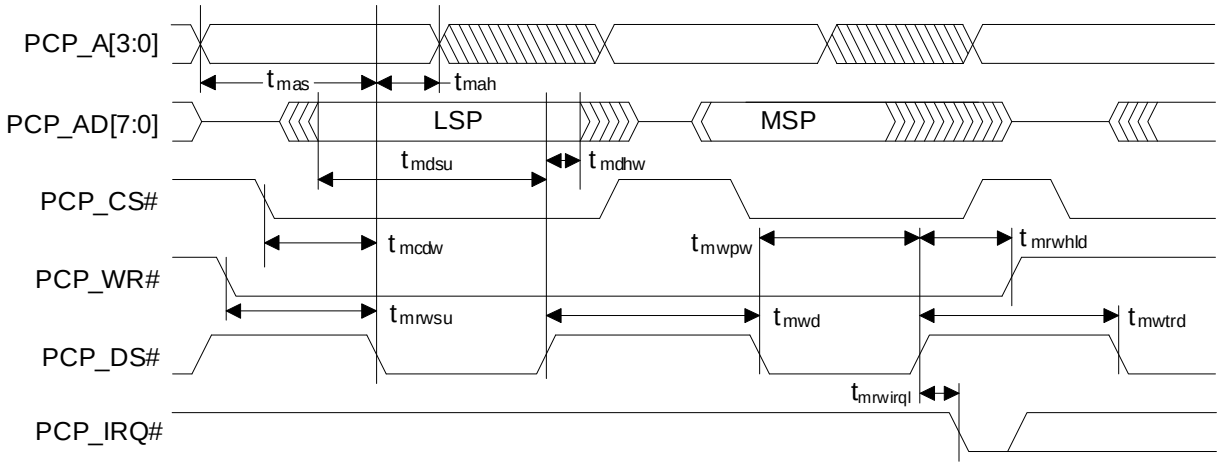


Figure 10. Parallel Control Port - Motorola Slave Mode Write Cycle Timing

5.15 Switching Characteristics — Digital Audio Slave Input Port

Parameter	Symbol	Min	Max	Unit
DAI_SCLK period	$T_{daiclkp}$	40	—	ns
DAI_SCLK duty cycle	—	45	55	%
DAI_LRCLK transition from DAI_SCLK active edge	$t_{daisstlr}$	10	—	ns
DAI_SCLK active edge from DAI_LRCLK transition	$t_{daislrts}$	10	—	ns
Setup time DAI_DATAn	t_{daidsu}	10	—	ns
Hold time DAI_DATAn	t_{daidh}	5	—	ns

Note: In these diagrams, falling edge is the inactive edge of DAI_SCLK.

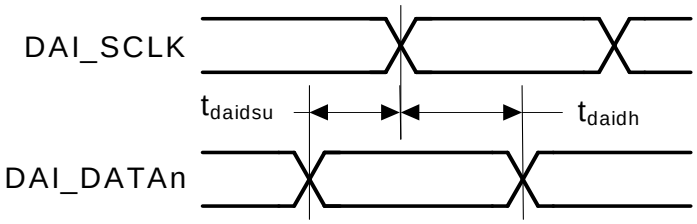


Figure 11. Digital Audio Input (DAI) Port Timing Diagram

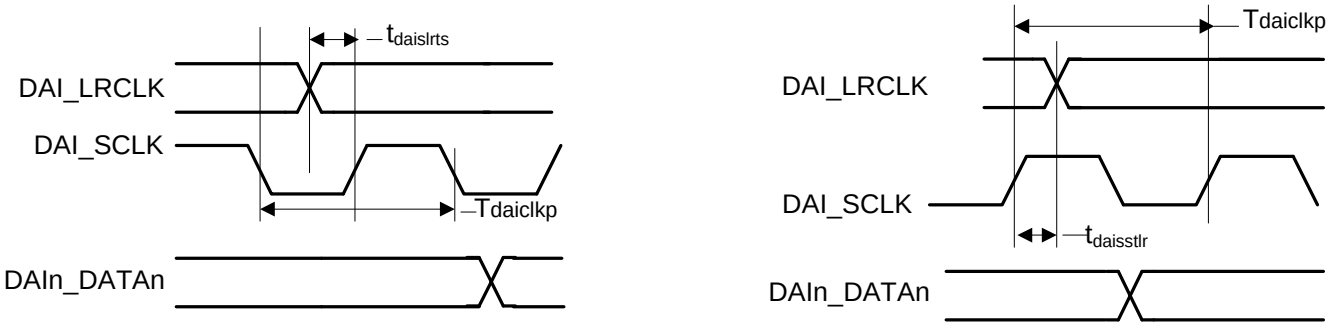
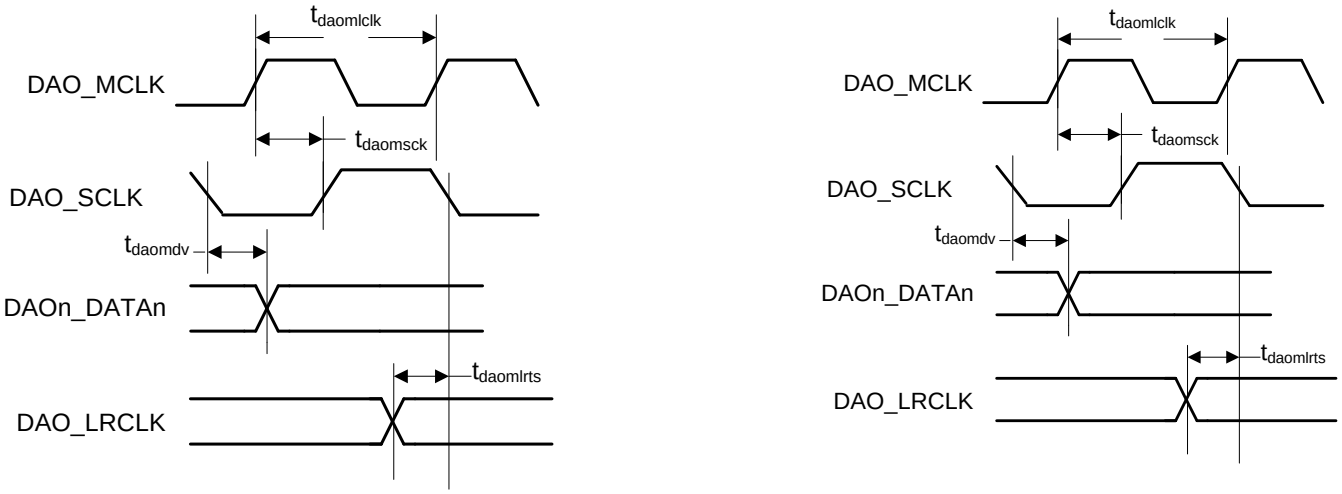


Figure 12. DAI Slave Timing Diagram

5.16 Switching Characteristics — Digital Audio Output Port

Parameter	Symbol	Min	Max	Unit
DAO_MCLK period	$T_{daomclk}$	40	—	ns
DAO_MCLK duty cycle	—	45	55	%
DAO_SCLK period for Master or Slave mode[1]	$T_{daosclk}$	40	—	ns
DAO_SCLK duty cycle for Master or Slave mode[1]	—	40	60	%
Master Mode (Output A1 Mode)[1,2]				
DAO_SCLK delay from DAO_MCLK rising edge, DAO_MCLK as an input	$t_{daomsck}$	—	19	ns
DAO_SCLK delay from DAO_LRCLK transition[3]	$t_{daomlrts}$	—	8	ns
DAO_LRCLK delay from DAO_SCLK transition[3]	$t_{daomstlr}$	—	8	ns
DAO1_DATA[3..0], DAO2_DATA[1..0] delay from DAO_SCLK transition[3]	t_{daomdv}	—	10	ns
Slave Mode (Output A0 Mode)[4]				
DAO_SCLK active edge to DAO_LRCLK transition	$t_{daosstlr}$	10	—	ns
DAO_LRCLK transition to DAO_SCLK active edge	$t_{daoslrts}$	10	—	ns
DAO_Dx delay from DAO_SCLK inactive edge	t_{daosdv}	—	12.5	ns

1. Master mode timing specifications are characterized, not production tested.
2. Master mode is defined as the CS4970x4 driving both DAO_SCLK, DAO_LRCLK. When MCLK is an input, it is divided to produce DAO_SCLK, DAO_LRCLK.
3. This timing parameter is defined from the non-active edge of DAO_SCLK. The active edge of DAO_SCLK is the point at which the data is valid.
4. Slave mode is defined as DAO_SCLK, DAO_LRCLK driven by an external source.



Note: In these diagrams, falling edge is the inactive edge of DAO_SCLK.

Figure 13. Digital Audio Port Output Timing Master Mode

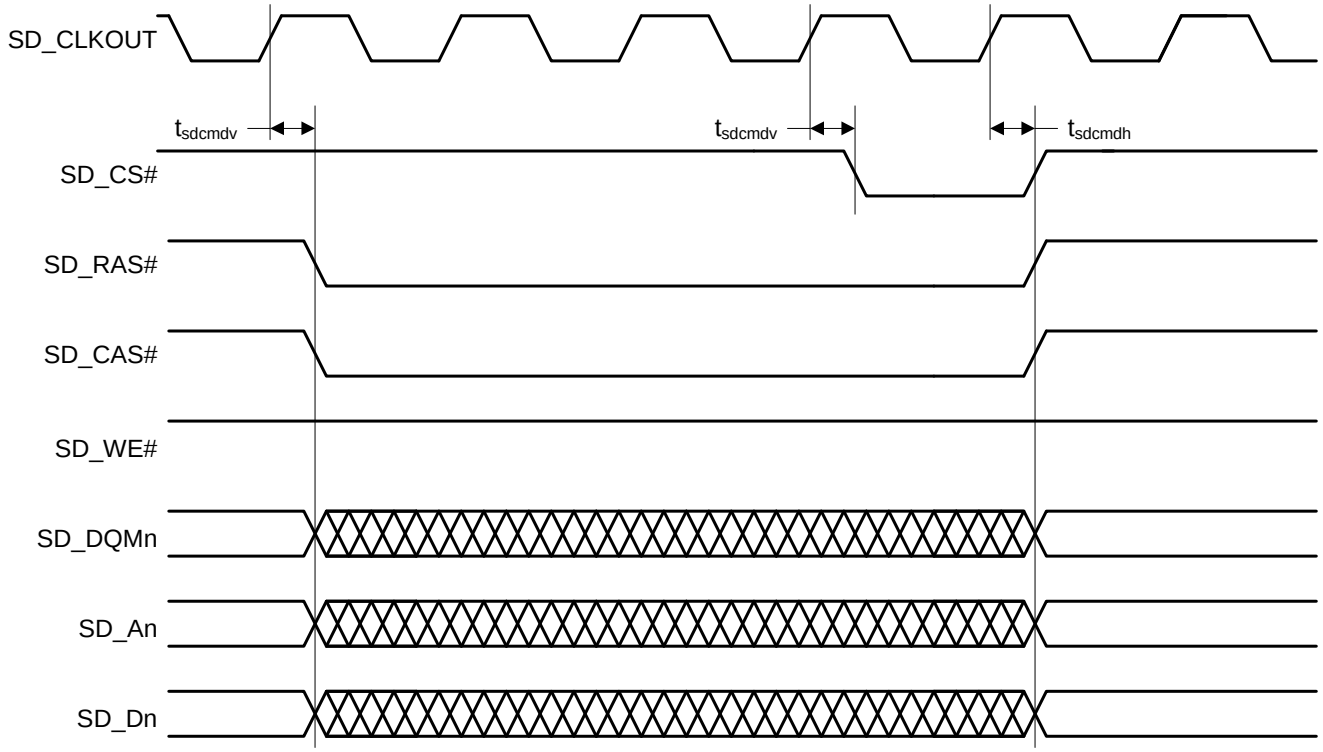


Figure 17. External Memory Interface - SDRAM Auto Refresh Cycle

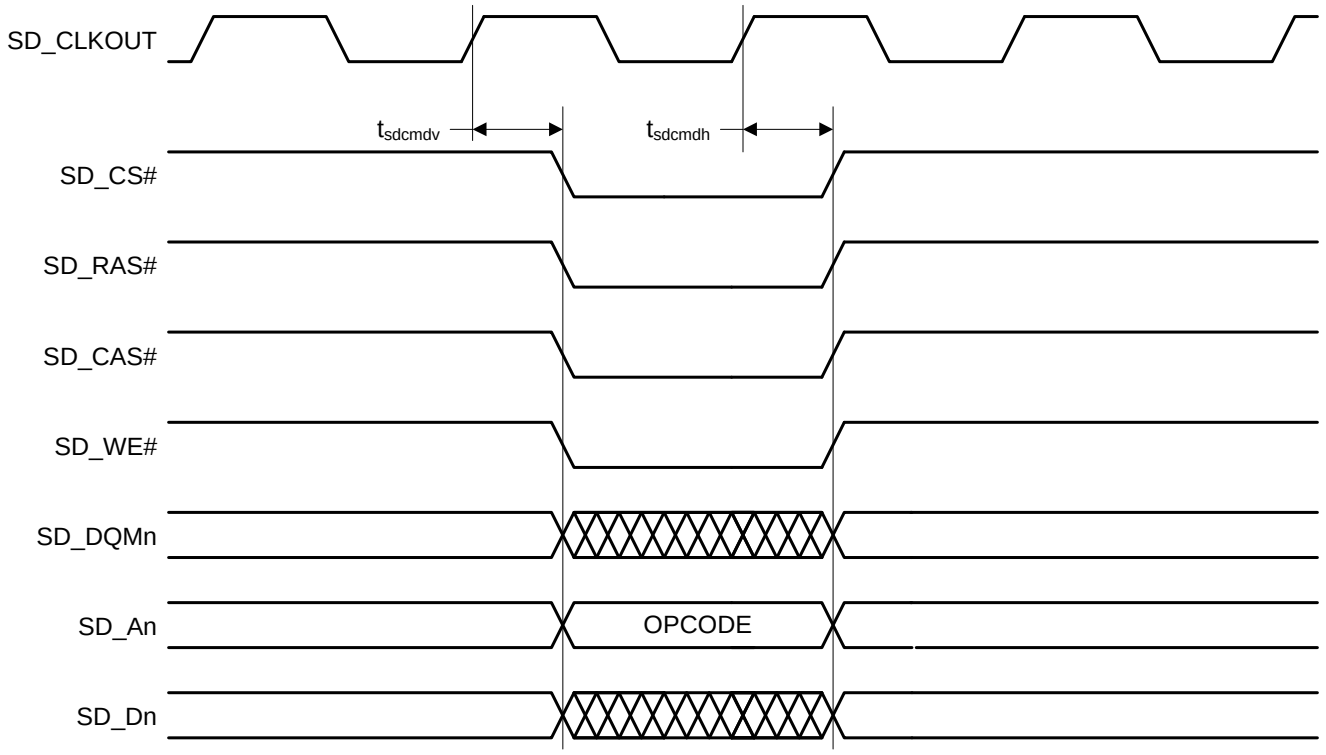


Figure 18. External Memory Interface - SDRAM Load Mode Register Cycle

6 Ordering Information

The CS4970x4 family part number is described as follows:

CS497NNI-XYZ

where

NN - Product Number Variant

I - ROM ID Number

X - Product Grade

Y - Package Type

Z - Lead (Pb) Free

Table 4. Ordering Information

Part No.	Status	Grade	Temp. Range	Package
CS497014-CVZ	Active	Commercial	0 to +70 °C	128-pin LQFP
CS47014-CVZR[1]	Active	Commercial	0 to +70 °C	
CS497024-CVZ	Active	Commercial	0 to +70 °C	128-pin LQFP
CS497024-CVZR[1]	Active	Commercial	0 to +70 °C	

1. R = Tape and reel

Note: Please contact the factory for availability of the -D (automotive grade) package.

7 Environmental, Manufacturing, and Handling Information

Table 5. Environmental, Manufacturing, & Handling Information

Model Number	Peak Reflow Temp	MSL Rating*	Max Floor Life
CS497014-CVZ	260 °C	3	7 Days
CS47014-CVZR	260 °C	3	7 Days
CS497024-CVZ	260 °C	3	7 Days
CS497024-CVZR	260 °C	3	7 Days

* MSL (Moisture Sensitivity Level) as specified by IPC/JEDEC J-STD-020.

8 Device Pin-Out Diagram

8.1 128-Pin LQFP Pin-Out Diagram

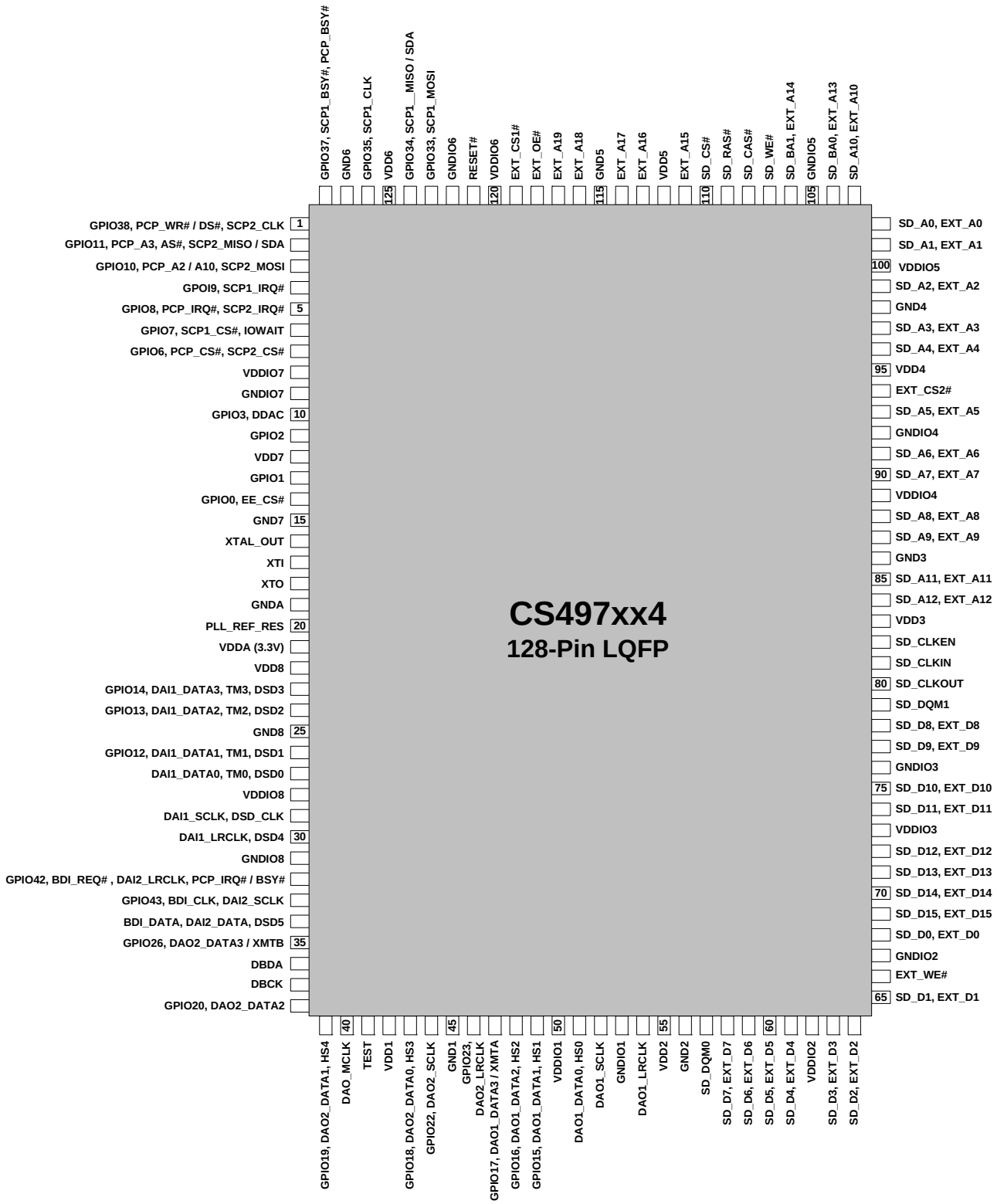


Figure 19. 128-Pin LQFP Pin-Out Diagram

10 Revision History

Revision	Date	Changes
PP9	November, 2010	Added “Status” column and footnote 1 to Table 4.
PP10	March, 2011	Added Tj conditions to Section 5.2. Changed 500 ma to 350 ma in Section 5.4. Updated Section 5.15 “Switching Characteristics — Digital Audio Slave Input Port” on page 21. Updated Section 5.16 “Switching Characteristics — Digital Audio Output Port” on page 22.
PP11	February, 2012	Added max internal DCLK frequency and min internal DCLK period to Section 5.8. Added notes to Section 5.9. Updated tspickl and tspickh values in Section 5.10. Updated tdaosdv max value in Section 5.16.
PP12	October, 2013	Updated note in Section 2 overview. Minor change to Section 2.1 title.
F1	February, 2014	Updated note in Section 2 overview regarding CS4970x4. Changed status of CS497024-CVZ and CS497024-CVZR to “Active” in Table 4.