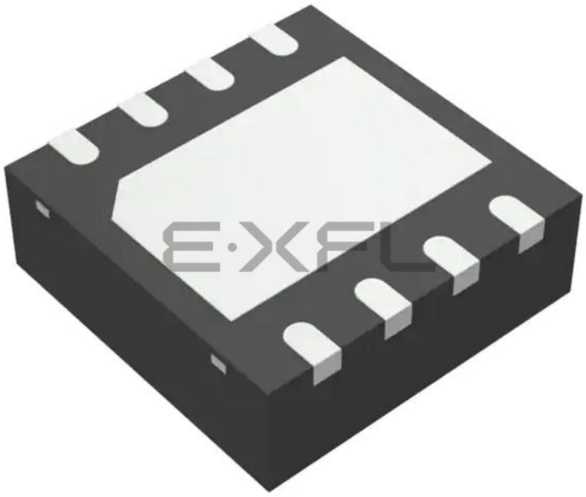
NXP USA Inc. - A7102CHTK2/T0BC2AJ Datasheet



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What Are Embedded - Microcontrollers - Application Specific?

Application specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	Authentication
Core Processor	MX51
Program Memory Type	-
Controller Series	-
RAM Size	-
Interface	I²C
Number of I/O	-
Voltage - Supply	2.5V ~ 3.6V
Operating Temperature	-40°C ~ 90°C (TA)
Mounting Type	Surface Mount
Package / Case	8-VDFN Exposed Pad
Supplier Device Package	8-HVSON (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/a7102chtk2-t0bc2aj

2. General description

2.1 A71CH naming conventions

The following table explains the naming conventions of the commercial product name of the A71CH products. Every A71CH product gets assigned such a commercial name, which includes also customer and application specific data.

The A71CH commercial names have the following format.

A71CHxagpp(p)/mvsrrff

The ‘A71CH’ is a constant, all other letters are variables, which are explained in Table 1.

Table 1. A71CH commercial name format

Variable	Meaning	Values	Description
x	IC hardware specification code	1	standard operational ambient temperature: –25 °C to +85 °C I^{2}C interface supported
		2	standard operational ambient temperature: –40 °C to +90 °C I^{2}C interface supported
a	embedded operating system code	C	Java card operating system
g	embedded application firmware (applet) code	H	H is a fixed value = IoT security applet pre installed
pp(p)	package type code dd(d)= Delivery Type, TK2= HVSON8 (4x4)		
m	Manufacturing Site Code	T	
v	Silicon Version Code	0	
s	Silicon Version Subcode	B	
rr	ROM Code ID		
ff	FabKey ID		

2.2 I^{2}C interface

The A71CH has an I^{2}C interface in slave mode, supporting data rates up to 400 kbit/s operating in Fast-Mode (FM). The I^{2}C interface is using the Smartcard I^{2}C protocol as defined in Ref. 3 which is based on SMBus.

2.3 Security licensing

NXP Semiconductors has obtained a patent license for SPA and DPA countermeasures from Cryptography Research Incorporated (CRI). This license covers both hardware and software countermeasures. It is important to customers that countermeasures within the operation system are covered under this license agreement with CRI. Further details can be obtained on request.

3. Features and benefits

3.1 Key benefits

- Secure, zero-touch connectivity
- End-to-end security, from chip to edge to cloud
- Secure credential injection for IC-level root of trust
- Fast design-in with complete product support package
- Easy to integrate with different MCU platforms

3.2 Security features

The A71CH security concepts includes many security measures to protect the chip.

The A71CH operates fully autonomously based on an integrated Javacard operating system and applet. Direct memory access is possible by the fixed functionalities of the applet only. With that, the content from the memory is fully isolated from the host system.

Attack protection by integrated design measures in the chip layout, the logic and the functional blocks.

3.3 Cryptography features

The A71CH Secure Element provides the following functionality:

- Protected Access storage, generation, insertion or deletion of 4 key pairs (ECC NIST P-256)
- Systematic enforced authentication
- Secure key management
- Protected Access storage, insertion or deletion of 3 public keys
- Signature generation and verification (ECDSA)
- Shared secret calculation for Key Agreement (ECDH or ECDH-E)
- Protected Access storage and use of 2 monotonic counters (32 bits each)
- Protected Access storage, insertion or deletion of symmetric secrets (8x 128 bits); longer keys can be used by using a ConstructedSecret type
- Content protected access to keys
- A unique chip ID (18 bytes)
- HKDF key derivation using the symmetric secrets as key, Extract & Expand or Expand only modes
- HMAC SHA256 calculation in one shot or sequential
- Freezing of credentials (= OTP behavior)
- Secure channel SCPO3 GP support
- (Optional) trust provisioning of key pairs, public keys, symmetric secrets, etc.
- Possibility to lock the A71CH module as transport lock mechanism

ECC keys and operations support the following ECC curve:

- NIST P-256

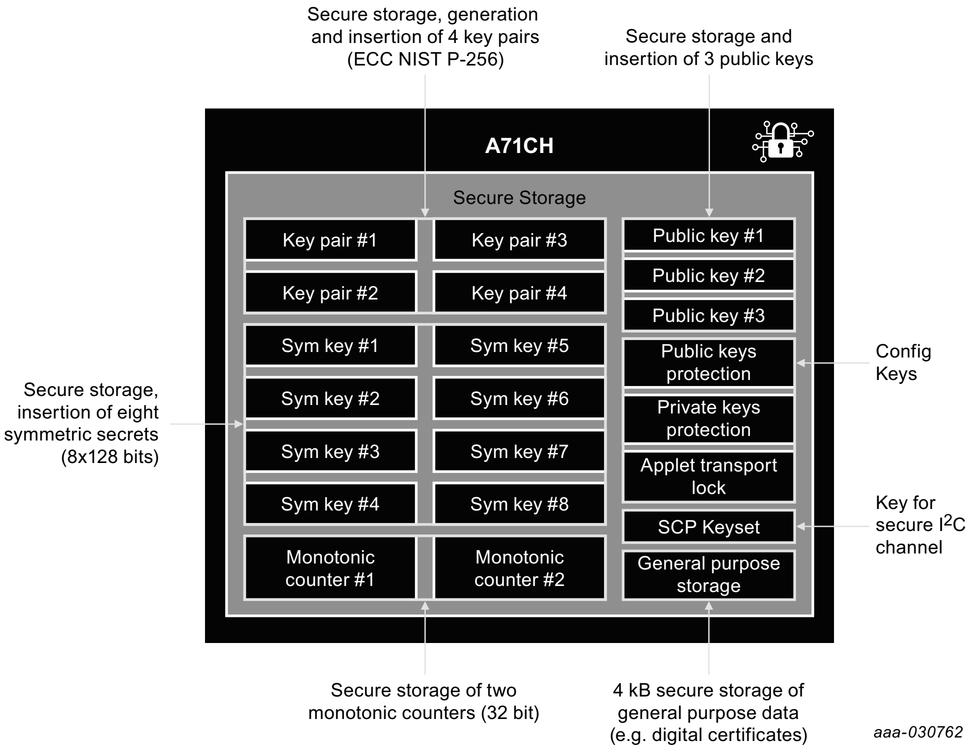

Fig 2. Protected key storage & provisioning of credentials

3.4 Functional features

- Dedicated MX51 security CPU
- 400 kbit/s I²C Fast-mode interface
- –40 °C to +90 °C operational ambient temperature (A7102)
- On-chip Javacard operating system
- 40 μA typical sleep mode current with I²C pads in tristate mode
- 10 μA max deep sleep mode current with I²C pads in tristate mode
- High-performance Public Key Infrastructure (PKI)
- EEPROM with min 500,000 cycles endurance and min 25 years retention time
- HVSON8 package

4. Applications

4.1 Use Cases and target applications

- A710xCH EXAMPLE USE CASES
  - Secure connection to public/private clouds, edge computing platforms, infrastructure
  - Secure Amazon Web Services-compliant connectivity
  - Secure commissioning
  - Device-to-device authentication
  - Proof of origin / anti-counterfeiting
  - Key storage and data protection
  - Secure provisioning of credentials
  - Ecosystem protection
- A710xCH TARGET APPLICATIONS
  - Connected industrial devices
  - Sensor networks
  - IP cameras
  - Home gateways
  - Home appliances

Table 6. A71CH type table

Credential/ State	Amount	Description
Asymmetric Key Pairs	4 x ECDSA NIST P-256 private + public key	Not set, not locked
Asymmetric Public Keys	3 x ECDSA NIST P-256 public keys	Not set, not locked
Config Keys	3 x AES128	Not set, cannot be locked
Symmetric Secret	8 x 128 bit key data	Not set, cannot be locked
Monotonic Counter	2 x upcounting counter with 32 bit	Counter set to 0, cannot be locked
SCP channel	SCP03 keyset with 3 AES128 keys	Keys not set, SCP03 not active
GP Data	128 segments of 32 bytes each	All bytes set to 0x00
Plain Injection Mode		Plain secrets can be inserted
Debug Mode		Debug Mode is active
TransportLock		Module can be set to "LOCKED"

6. Marking

Table 7. Marking codes

Type number	Marking code
A710x..TK2/...	Line A: 710* (* = ‘1’ for A7101, ‘2’ for A7102, ‘3’ for A7103) Line B: **** (**** = 4 digit Batch code[1]) Line C: ZnD***0 (*** = 3 digit Date code[2]) Z: diffusion center, SSMC Systems on Silicon Manufactoring (SSMC), Singapore n: assembly center D: code to indicate conformance to RHF-2006 0: Mask version code

[1] Batch code: 5 digits available, 2 for DBSN, 2 for ASID: mark "YY ZZ" or 4 digits available, 2 for DBSN, 2 for ASID: mark “YYZZ”
The Assembly Sequence ID (ASID) is a 2-digit indicator that counts the number of assembly batches (transport lots) within one diffusion batch id and one weekly date code. The week start and end dates are defined by the assembly center algorithm. The ASID is assigned sequentially starting with 01 and ranging through 99, then each digit ranges upper case alphabet letters in combination with numeric, then numeric in combination with upper case alphabet letters, then upper case alphabet letters in combination with upper case alphabet letters providing 1175 possible values within a week-code. The numeric zero ‘0’ is only allowed within the sequence of 01 to 99. The alphabet letter ‘O’ is not allowed to avoid confusion with numeric ‘0’.

The Diffusion Batch Sequence Number (DBSN) is a 2-digit indicator that counts the number of diffusion batches (DBID) within one Package Type (i.e. HVSON8) and one weekly date code. The DBSN is assigned sequentially starting with 01 and ranging through 99, then each digit ranges upper case alphabet letters in combination with numeric, then numeric in combination with upper case alphabet letters, then upper case alphabet letters in combination with upper case alphabet letters providing 1175 possible values within a week-code. The numeric zero ‘0’ is only allowed within the sequence of 01 to 99. The alphabet letter ‘O’ is not allowed to avoid confusion with numeric ‘0’.

[2] 3 digit Date code: “YWW”
“Y” is a code indicating the year in which the IC is assembled. Examples: for year 1999 is Y = 9, for year 2000 is Y = 0, for year 2001 is Y = 1. ”WW” is a code indicating the week in which the IC is assembled. It is determined from the date the assembly transport lot is created or alternately the date die is issued from die stores to assembly start or the date die attach (Diebond) occurs or the date encapsulation occurs. Examples: for week 01 is WW = 01, for week 52 is WW = 52, for week 53 is WW = 53.

In the case of bumped die (WL-CSP) the code indicates the week in which the IC was bumped.

7. Functional description

7.1 Functional diagram

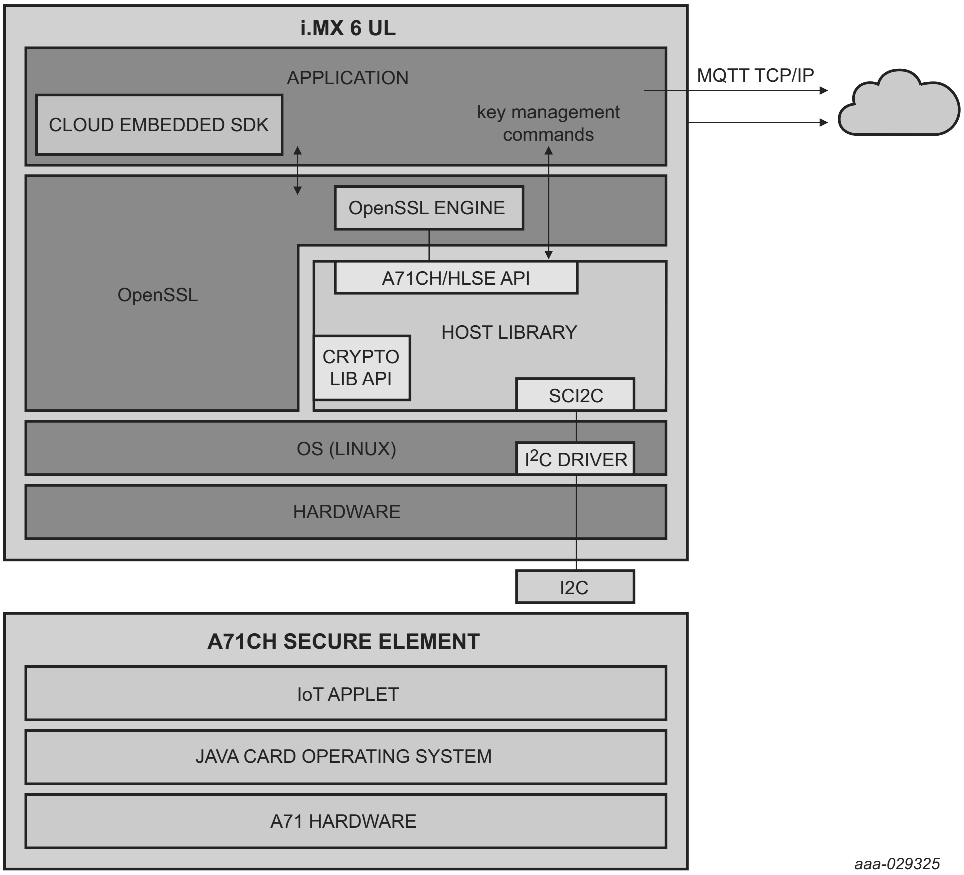

Fig 3. A71CH functional diagram - example Open SSL

The A71CH uses I^{2}C as communication interface as described in the following section. The A71CH commands are wrapped using the Smartcard I^2 protocol (SCI2C). The detailed documentation for the A71CH commands [ref to APDU Spec] and SCI2C encapsulation (Ref. 3) is available in NXP docstore.”

In order to simplify the product usage a host library was created which takes care for the A71CH commands and SCI2C protocol encapsulation. The host library for various platforms is available for download with complete sources on the A71CH website.

7.2 Credential Storage & Memory

The I^{2}C interface of the A71CH is supporting a Smart Card I^{2}C (SCIIC) Protocol using an Inter-IC (I^{2}C) based physical interface and data link layer using Fast-mode (FM) up to 400 kBit/s, a SMBus based network layer and bus protocol as well as a mapping layer to convey [ISO/IEC 7816-4] based communication. This protocol is specified in [Ref to SCI^{2}C].

The A71CH enters automatically into SLEEP mode after 312 ms of inactivity on the I²C lines and also wakes up automatically from SLEEP mode. In SLEEP mode, all internal clocks are stopped. The IOs hold the logical states they had at the time IDLE was activated. During SLEEP mode security sensors HVS, LVS, LTS, HTS, Light Sensors, Glitch Sensors and Active Shielding are disabled.

There are two ways to exit from the SLEEP mode:

- A reset signal on RST_N
- An External Interrupt edge triggered by a falling edge on I2C_SDA

7.5.2 DEEP SLEEP mode

The A71CHx provides a special sleep mode offering maximum power saving. It is reached by pulling RST_N to a logic zero level for more than 500 µs.

While in deep sleep mode the internal power is completely switched off and only the IO pads stay supplied. All digital pads will stay in high-Z mode.

To leave the DEEP SLEEP mode RST_N has to be released and set to a logic „1“ level.

8. Pinning information

8.1 Pinning

8.1.1 Pinning HVSON8

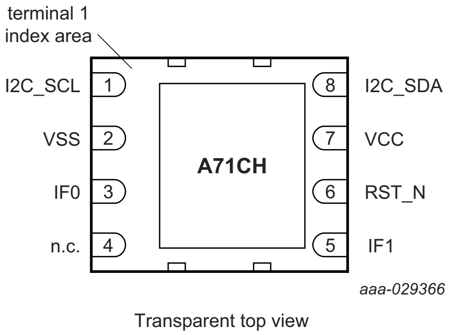

Fig 4. Pin configuration for HVSON-8 (SOT909-1)

Table 9. Pin description HVSON8

Symbol	Pin	Description
I2C_SCL	1	I²C clock
VSS	2	ground
IF0	3	interface activation, apply high on startup
n.c.	4	not connected
IF1	5	I²C address selection
RST_N	6	reset input, active LOW
VCC	7	power supply voltage input
I2C_SDA	8	I²C data

9. Package outline

Fig 5. Package outline SOT909-1

10. Packing information

10.1 Reel packing

The A71CH product is available on 7” tape on reel and 13” tape on reel. Details are provided in Table 10.

Table 10. Reel packing options

Package type	Reel type	Minimum packing quantity
HVSON8	7” tape on reel	1500
HVSON8	13” tape on reel[1]	6000

[1] For details about packing method, product orientation, tape dimensions and labeling for A71 parts in HVSON8 package having an ordering code (12NC) ending 118 refer to Ref. 2.

11. Electrical and timing characteristics

The electrical interface characteristics of static (DC) and dynamic (AC) parameters for pads and functions used for I^2C are in accordance with the NXP I^2C specification (see Ref. 1).

12. Limiting values

Table 11. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to VSS (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			-0.3	+4.6	V
V_I	input voltage	any signal pad		-0.3	+4.6	V
I_I	input current	pad I2C_SDA, I2C_SCL		-	10	mA
I_O	output current	pad I2C_SDA, I2C_SCL		-	10	mA
I_{lu}	latch-up current	$V_I < 0$ V or $V_I > V_{DD}$		-	100	mA
V_{esd_hbm}	electrostatic discharge voltage (Human Body Model)	pads VCC, VSS, RST_N, I2C_SDA, I2C_SCL	[1]		± 2.0	kV
V_{esd_cdm}	electrostatic discharge voltage (Charge Device Model)	pads VCC, VSS, RST_N, I2C_SDA, I2C_SCL	[3]		± 500	V
P_{tot}	Total power dissipation		[2]	-	1	W
T_{stg}	Storage temperature			-55	+125	°C

[1] MIL Standard 883-D method 3015; human body model; C = 100 pF, R = 1.5 kΩ; T_{amb} = −25 °C to +85 °C.

[2] Depending on appropriate thermal resistance of the package.

[3] JESD22-C101, JEDEC Standard Field induced charge device model test method.

14. Characteristics

14.1 DC characteristics

Measurement conventions

Testing measurements are performed at the contact pads of the device under test. All voltages are defined with respect to the ground contact pad VSS. All currents flowing into the device are considered positive.

14.1.1 General and I^{2}C I/O interface

Table 13. Electrical DC characteristics of I2C_SCL, I2C_SDA and RST_N

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Input/Output: I2C_SCL, I2C_SDA in push-pull mode							
V_{IH}	HIGH level input voltage			0.7 V_{DD}		V_{Imax}[1]	V
V_{IL}	LOW level input voltage			-0.5		0.3 V_{DD}	V
I_{IH}	HIGH level input current in input mode	$V_{IHmin} < V_I < V_{IHmax}$				± 10	µA
I_{IL}	LOW level input current	$V_{ILmin} < V_I < V_{ILmax}$				± 10	µA
V_{OH}	HIGH level output voltage	I_{OH} = –3.0 mA; 3V3 mode	[2]	0.7 V_{DD}			V
		I_{OH} = –3.0 mA; 1V8 mode	[2]	0.7 V_{DD}			V
V_{OL}	LOW level output voltage	I_{OL} = 3.0 mA 3V3 mode				0.4	V
		I_{OL} = 2.0 mA 1V8 mode				0.2 V_{DD}	V
Input/Output: I2C_SCL, I2C_SDA in open-drain mode							
V_{IH}	HIGH level input voltage			0.7 V_{DD}		V_{Imax}[1]	V
V_{IL}	LOW level input voltage			-0.5		0.3 V_{DD}	V
I_{IH}	HIGH level input current in input mode	$V_{IHmin} < V_I < V_{IHmax}$				± 10	µA
I_{IL}	LOW level input current	$V_{ILmin} < V_I < V_{ILmax}$				± 10	µA
V_{OL}	LOW level output voltage	I_{OL} = 3.0 mA 3V3 mode				0.4	V
		I_{OL} = 2.0 mA 1V8 mode				0.2 V_{DD}	V
Input: RST_N							
V_{IH1}	HIGH level input voltage			0.7 V_{DD}		V_{Imax}[1]	V
V_{IL1}	LOW level input voltage			-0.3		0.3 V_{DD}	V
I_{IH1}	HIGH level RST_N input current	$V_{IH1min} \leq V_I \leq V_{DD}$	[3]			± 20	µA
I_{IL1}	LOW level RST_N input current	$0\ V \leq V_I \leq V_{IL1max}$;	[3]			± 20	µA

[1] Maximum value according to Table 12 “Recommended operating conditions”

14.1.2 I²C interface at 3V3 mode operation[1]

Table 14. Electrical characteristics of IC supply voltage V_{DD}; V_{SS} = 0 V; T_{amb} = -40 to +90 °C

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply							
V_{DD}	supply voltage range	3V3 mode range CPU in free running mode		2.50	3.3	3.6	V
I_{DD}	no coprocessor active	CPU in free running mode			6.3	7.0	mA
	EPROM programming in progress	CPU in free running mode			7.3	8.0	mA
	AES coprocessor active	CPU in free running mode			9.3	10.3	mA
	ECC coprocessor active	CPU in free running mode			13.7	15.1	mA
$I_{DD(SLP)}$	supply current SLEEP mode	T_{amb} = 25 °C			45	150	µA
$I_{DD(DSLP)}$	supply current deep sleep mode	RST_N at 0V, T_{amb} = 25 °C				10	µA
		RST_N at 0V, T_{amb} = 90 °C				10	µA

[1] All appropriately marked values are typical values and only referenced for information. They are subject to change without notice.

14.1.3 I^{2}C interface at 1V8 mode operation[1]

Table 15. Electrical characteristics of IC supply voltage V_{DD}; V_{SS} = 0 V; T_{amb} = -40 to +90 °C

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply							
V_{DD}	supply voltage range	1V8 mode range		1.62	1.8	1.98	V
I_{DD}	no coprocessor active	CPU in free running mode			2.45		mA
	AES coprocessor active	CPU in free running mode			2.7		mA
	ECC coprocessor active	CPU in free running mode			7.5		mA
$I_{DD(SLP)}$	supply current SLEEP mode	T_{amb} = 25 °C			40	80	μA
$I_{DD(DSLP)}$	supply current deep sleep mode	RST_N at 0V, $T_{amb} = 25$ °C				10	μA
		RST_N at 0V, $T_{amb} = 90$ °C				10	μA

[1] All appropriately marked values are typical values and only referenced for information. They are subject to change without notice.

14.2 AC characteristics

Table 16. Non-volatile memory timing characteristics; V_{DD} = 1.8 V ± 10% or 3 V ± 10% V; V_{SS} = 0 V; T_{amb} = -40 to 90 °C

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{EEP}	EEPROM erase + program time				2.7		ms
t_{EEE}	EEPROM erase time				1.7		ms
t_{EEW}	EEPROM program time				1.0		ms
t_{EER}	EEPROM data retention time	T_{amb} = +55 °C		25			years
N_{EEC}	EEPROM endurance (number of programming cycles)			5×10^5			cycles

Table 17. Electrical AC characteristics of I2C_SDA, I2C_SCL, and RST_N[1]; V_{DD} = 1.8 V ± 10% or 3 V ± 10% V; V_{SS} = 0 V; T_{amb} = -40 to 90 °C

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Input/Output: I2C_SDA, I2C_SCL in open-drain mode							
tr_{IO}	I/O Input rise time	Input/reception mode	[4]			1	μs
tf_{IO}	I/O Input fall time	Input/reception mode	[4]			1	μs
tf_{OIO}	I/O Output fall time	Output/transmission mode; C_L = 30 pF	[4]			0.3	μs
f_{CLK}	External clock frequency in I^{2}C applications	t_{CLKW}, T_{amb} and V_{DD} in their spec'd limits		-		400	kHz
t_{CLKW}	Clock pulse width i.r.t. clock period (positive pulse duty cycle of CLK)		[3]	40		60	%
Inputs: RST_N							
t_{RW}	Reset pulse width (RST_N low) without entering deep sleep mode			40		400	μs
t_{RDSLP}	Reset pulse width (RST_N low) to enter deep sleep mode			500			μs
t_{WKP}	Wake-up time from SLEEP mode	$f_{CLKmin} < f_{CLK} < f_{CLKmax}$		-	8	10	μs

Table 17. Electrical AC characteristics of I2C_SDA, I2C_SCL, and RST_N[1]; V_{DD} = 1.8 V ± 10% or 3 V ± 10% V; V_{SS} = 0 V; T_{amb} = -40 to 90 °C

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{WKPIO}	Pad LOW time for wake-up from SLEEP mode	level triggered ext.int.		-	8	10	µs
		edge triggered ext.int.		-	8	10	µs
t_{WKPRST}	RST_N LOW time for wake-up from SLEEP mode			40		-	µs
t_{WKWT}	Time from SLEEP mode wake/up event to I2C_SDA valid				50	100	ns
C_{PIN}	Pin capacitances RST_N, I2C_SDA, /I2C_SCL	Test frequency = 1 MHz; T_{amb} = 25 °C		-		10	pF

[1] All appropriately marked values are typical values and only referenced for information. They are subject to change without notice.

[2] t_r is defined as rise time between 20% and 80% of the signal amplitude.
t_f is defined as fall time between 80% and 20% of the signal amplitude.

[3] During AC testing the inputs RST_N, I2C_SDA, I2C_SCL are driven at 0 V to +0.3 V for a LOW input level and at V_{DD} –0.3 V to V_{DD} for a HIGH input level. Clock period and signal pulse (duty cycle) timing is measured at 50% of V_{DD}.

[4] t_r is defined as rise time between 30% and 70% of the signal amplitude.
t_f is defined as fall time between 70% and 30% of the signal amplitude.

Fig 8. External clock drive and AC test timing reference points of I2C_SDA, I2C_SCL, and RST_N (see Table note [3] and Table note [4]) in open drain mode

14.3 EMC/EMI

EMC and EMI resistance according to IEC 61967-4.

15. Abbreviations

Table 18. Abbreviations

Acronym	Description
AES	Advanced Encryption Standard
CRC	Cyclic Redundancy Check
DES	Digital Encryption Standard
DPA	Differential Power Analysis
DSS	Digital Signature Standard
ECC	Elliptic Curve Cryptography
EEPROM	Electrically Erasable Programmable Read-Only Memory
I/O	Input/Output
MAC	Message Authentication Code
OS	Operating System
PKI	Public Key Infrastructure
SFI	Single Fault Injection
SHA	Secure Hash Algorithm

16. References

[1] I^{2}C-bus specification and user manual, Rev. 3.0 — June-19-2007, NXP Semiconductors

[2] SOT909-1; HVSON8; Reel pack; Ordering code (12NC) ending 118; Packing Information; Rev. 2 — 19 April 2013

[3] Application note SCIIC Protocol Specification, Application note, Rev 1.x, AN12207 (document number an19501x)

17. Revision history

Table 19. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
449311	20180801	Data sheet		
Modifications:	• Updated specification status • Updated Table 1 “A71CH commercial name format” • Updated Section 2.2 “I2C interface” • Added Figure 2 “Protected key storage & provisioning of credentials” • Updated Table 3 “A71CH type table” • Updated Table 4 “A71CH development tools type table” • Added Section 5.2 “Configuration” • Updated Table 5 “A71CH feature table” • Added Section 6 “Marking” • Added Section 7.2 “Credential Storage & Memory” • Updated Section 7.3 “I2C Interface” • Updated Section 7.5.1 “SLEEP mode” • Updated Table 12 “Recommended operating conditions” • Updated Section 14.1 “DC characteristics” • Updated Table 16 “Non-volatile memory timing characteristics; V_{DD} = 1.8 V ± 10% or 3 V ± 10% V; V_{SS} = 0 V; T_{amb} = -40 to 90 °C” • Updated Section 14.2 “AC characteristics” • Added Table 17 “Electrical AC characteristics of I2C_SDA, I2C_SCL, and RST_N[1]; V_{DD} = 1.8 V ± 10% or 3 V ± 10% V; V_{SS} = 0 V; T_{amb} = -40 to 90 °C” • Added Figure 8 “External clock drive and AC test timing reference points of I2C_SDA, I2C_SCL, and RST_N (see Table note [3] and Table note [4]) in open drain mode” • Updated Section 16 “References”			
449310	20180221	Objective short data sheet		
Modifications:	• Initial version			

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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