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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	44MHz
Connectivity	I²C, SPI
Peripherals	POR, PWM, WDT
Number of I/O	16
Program Memory Size	62KB (31K x16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 32
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 10x12b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	36-UFBGA, WLCSP
Supplier Device Package	36-WLCSP (3.4x3.4)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc7023bcbz62i-r7

Table 4. SPI Master Mode Timing (Phase Mode = 1)

Parameter	Description	Min	Typ	Max	Unit
t_{SL}	SCLK low pulse width[1]		(SPIDIV + 1) × t_{UCLK}		ns
t_{SH}	SCLK high pulse width[1]		(SPIDIV + 1) × t_{UCLK}		ns
t_{DAV}	Data output valid after SCLK edge			25	ns
t_{DSU}	Data input setup time before SCLK edge[1]	1 × t_{UCLK}			ns
t_{DHD}	Data input hold time after SCLK edge[1]	2 × t_{UCLK}			ns
t_{DF}	Data output fall time		5	12.5	ns
t_{DR}	Data output rise time		5	12.5	ns
t_{SR}	SCLK rise time		5	12.5	ns
t_{SF}	SCLK fall time		5	12.5	ns

[1] t_{UCLK} = 23.9 ns. It corresponds to the 41.78 MHz internal clock from the PLL before the clock divider.

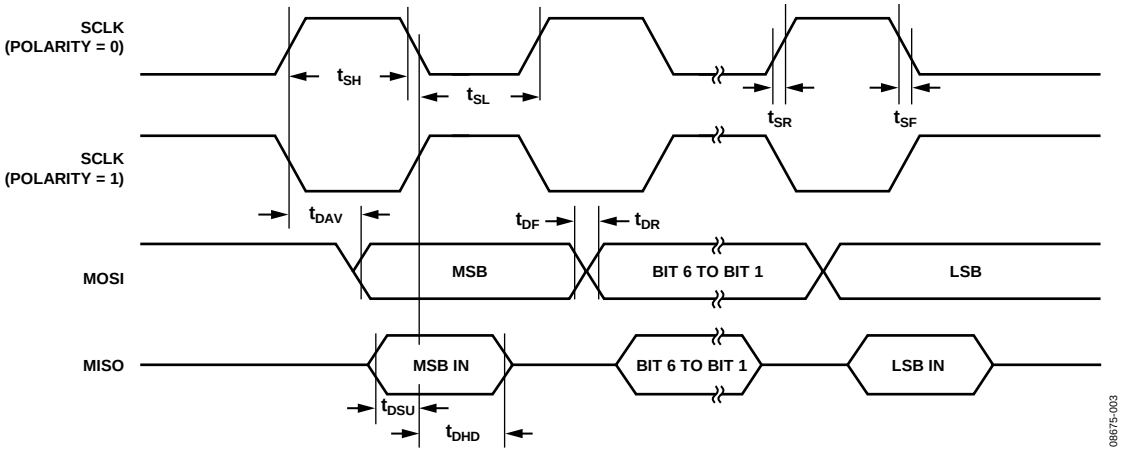

Figure 3. SPI Master Mode Timing (Phase Mode = 1)

Table 5. SPI Master Mode Timing (Phase Mode = 0)

Parameter	Description	Min	Typ	Max	Unit
t_{SL}	SCLK low pulse width[1]		(SPIDIV + 1) × t_{UCLK}		ns
t_{SH}	SCLK high pulse width[1]		(SPIDIV + 1) × t_{UCLK}		ns
t_{DAV}	Data output valid after SCLK edge			25	ns
t_{DOSU}	Data output setup before SCLK edge			75	ns
t_{DSU}	Data input setup time before SCLK edge[1]	1 × t_{UCLK}			ns
t_{DHD}	Data input hold time after SCLK edge[1]	2 × t_{UCLK}			ns
t_{DF}	Data output fall time		5	12.5	ns
t_{DR}	Data output rise time		5	12.5	ns
t_{SR}	SCLK rise time		5	12.5	ns
t_{SF}	SCLK fall time		5	12.5	ns

[1] t_{UCLK} = 23.9 ns. It corresponds to the 41.78 MHz internal clock from the PLL before the clock divider.

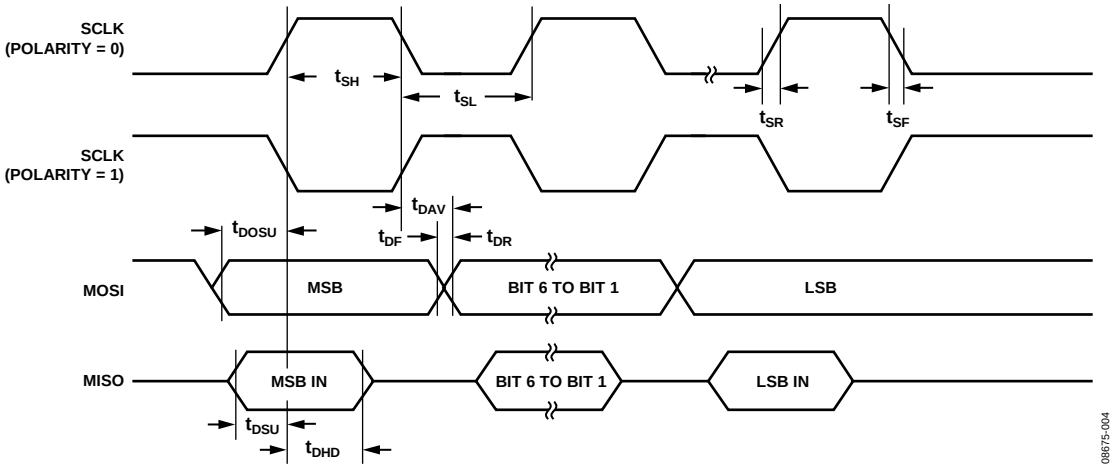

Figure 4. SPI Master Mode Timing (Phase Mode = 0)

Table 7. SPI Slave Mode Timing (Phase Mode = 0)

Parameter	Description	Min	Typ	Max	Unit
$t_{\overline{SS}}$	$\overline{SS}$ to SCLK edge	200			ns
t_{SL}	SCLK low pulse width[1]		(SPIDIV + 1) × t_{UCLK}		ns
t_{SH}	SCLK high pulse width[1]		(SPIDIV + 1) × t_{UCLK}		ns
t_{DAV}	Data output valid after SCLK edge			25	ns
t_{DSU}	Data input setup time before SCLK edge[1]	1 × t_{UCLK}			ns
t_{DHD}	Data input hold time after SCLK edge[1]	2 × t_{UCLK}			ns
t_{DF}	Data output fall time		5	12.5	ns
t_{DR}	Data output rise time		5	12.5	ns
t_{SR}	SCLK rise time		5	12.5	ns
t_{SF}	SCLK fall time		5	12.5	ns
t_{DOCS}	Data output valid after $\overline{SS}$ edge			25	ns
t_{SFS}	$\overline{SS}$ high after SCLK edge	0			ns

[1] t_{UCLK} = 23.9 ns. It corresponds to the 41.78 MHz internal clock from the PLL before the clock divider.

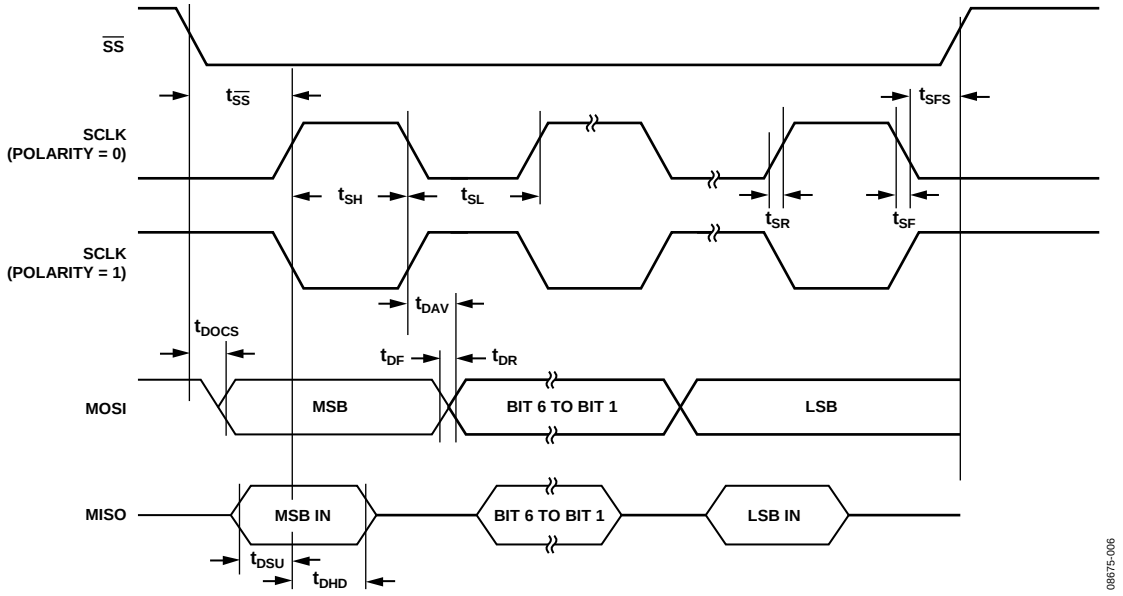

Figure 6. SPI Slave Mode Timing (Phase Mode = 0)

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

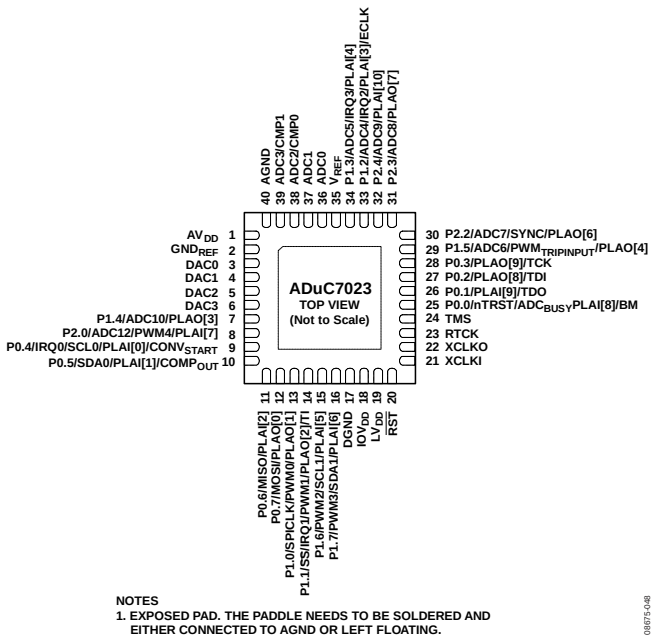

Figure 7. 40-Lead LFCSP Pin Configuration

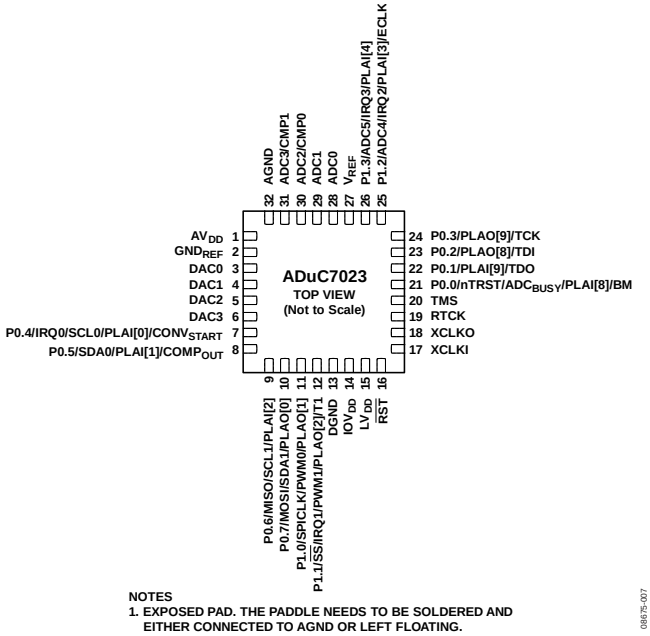

Figure 8. 32-Lead LFCSP Pin Configuration

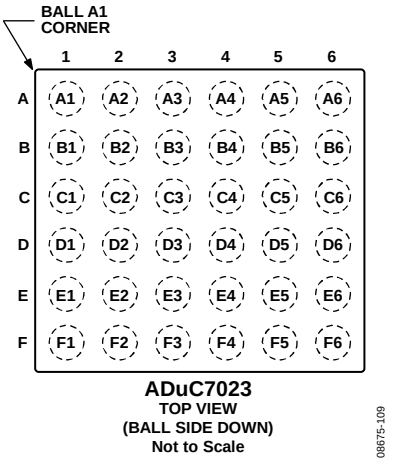

Figure 9. 36-Lead WLCSP Pin Configuration

Table 9. Pin Function Descriptions

Pin No.				
40-LFCSP	**32-LFCSP**	**36-WLCSP**	**Mnemonic**	**Description**
0	0	N/A	Exposed Paddle	Exposed Pad. The paddle needs to be soldered and either connected to AGND or left floating.
36	28	A4	ADC0	Single-Ended or Differential Analog Input 0.
37	29	B4	ADC1	Single-Ended or Differential Analog Input 1.
38	30	A5	ADC2/CMP0	Single-Ended or Differential Analog Input 2/Comparator Positive Input.
39	31	B5	ADC3/CMP1	Single-Ended or Differential Analog Input 3/Comparator Negative Input.
32	N/A	B2	P2.4/ADC9/PLAI[10]	General-Purpose Input and Output Port 2.4/ADC Single-Ended or Differential Analog Input/Programmable Logic Array Input Element 10. By default, this pin is configured as a digital input with a weak pull-up resistor enabled.

ADCCN Register

Name: ADCCN

Address: 0xFFFF0508

Default value: 0x01

Access: Read/write

Function: ADCCN is an ADC negative channel selection register. This MMR is described in Table 26.

Table 26. ADCCN MMR Bit Designation

Bit	Value	Description
7 to 5		Reserved.
4 to 0		Negative channel selection bits.
	00000	ADC0.
	00001	ADC1.
	00010	ADC2.
	00011	ADC3.
	00100	ADC4.
	00101	ADC5.
	00110	ADC6.
	00111	ADC7.
	01000	ADC8.
	01001	ADC9.
	01010	ADC10.
	01011	Reserved
	01100	ADC12.
	01101	Reserved
	01110	Reserved
	01111	DAC1.
	10000	Temperature sensor.
	10001	AGND (self-diagnostic feature).
	10010	Internal reference (self-diagnostic feature).
	10011	Reserved
	Others	Reserved.

ADCSTA Register

Name: ADCSTA

Address: 0xFFFF050C

Default Value: 0x00

Access: Read

Function: ADCSTA is an ADC status register that indicates when an ADC conversion result is ready. The ADCSTA register contains only one bit, ADCReady (Bit 0), representing the status of the ADC. This bit is set at the end of an ADC conversion, generating an ADC interrupt. It is cleared automatically by reading the ADCDAT MMR. When the ADC is performing a conversion, the status of the ADC can be read externally via the ADC_{BUSY} pin. This pin is high during a conversion. When the conversion is finished, ADC_{BUSY} goes back low. This information can be available on P0.0 (see the General-Purpose Input/Output section) if enabled in the ADCCON register.

ADCDAT Register

Name: ADCDAT

Address: 0xFFFF0510

Default value: 0x00000000

Access: Read

Function: ADCDAT is an ADC data result register. Hold the 12-bit ADC result as shown in Figure 22.

ADCRST Register

Name: ADCRST

Address: 0xFFFF0514

Default Value: 0x00

Access: Read/write

Function: ADCRST resets the digital interface of the ADC. Writing any value to this register resets all the ADC registers to their default value.

NONVOLATILE FLASH/EE MEMORY

The ADuC7023 incorporates Flash/EE memory technology on chip to provide the user with nonvolatile, in-circuit reprogrammable memory space.

Like EEPROM, flash memory can be programmed in-system at a byte level, although it must first be erased. The erase is performed in page blocks. As a result, flash memory is often and more correctly referred to as Flash/EE memory.

The Flash/EE memory represents a step closer to the ideal memory device that includes nonvolatility, in-circuit programmability, high density, and low cost. Incorporated in the ADuC7023, Flash/EE memory technology allows the user to update program code space in-circuit, without needing to replace one-time programmable (OTP) devices at remote operating nodes.

Each part contains a 64 kB array of Flash/EE memory. The lower 62 kB are available to the user, and the upper 2 kB contain permanently embedded firmware, allowing in-circuit serial download. These 2 kB of embedded firmware also contain a power-on configuration routine that downloads factory-calibrated coefficients to the various calibrated peripherals (such as ADC, temperature sensor, and band gap references). This 2 kB embedded firmware is hidden from user code.

Flash/EE Memory Reliability

The Flash/EE memory arrays on the parts are fully qualified for two key Flash/EE memory characteristics: Flash/EE memory cycling endurance and Flash/EE memory data retention.

Endurance quantifies the ability of the Flash/EE memory to be cycled through many program, read, and erase cycles. A single endurance cycle is composed of four independent, sequential events, defined as:

1. Initial page erase sequence.
2. Read/verify sequence (single Flash/EE).
3. Byte program sequence memory.
4. Second read/verify sequence (endurance cycle).

In reliability qualification, every half word (16-bit wide) location of the three pages (top, middle, and bottom) in the Flash/EE memory is cycled 10,000 times from 0x0000 to 0xFFFF. As indicated in Table 1, the Flash/EE memory endurance qualification is carried out in accordance with JEDEC Retention Lifetime Specification A117 over the industrial temperature range of −40° to +125°C. The results allow the specification of a minimum endurance figure over a supply temperature of 10,000 cycles.

Retention quantifies the ability of the Flash/EE memory to retain its programmed data over time. Again, the parts are qualified in accordance with the formal JEDEC Retention Lifetime Specification (A117) at a specific junction temperature (T_J = 85°C). As part of this qualification procedure, the Flash/EE memory is cycled to its specified endurance limit before data retention is characterized. This means that the Flash/EE memory is guaranteed to retain its data for its fully specified retention lifetime every time the Flash/EE memory is reprogrammed. In addition, note that retention lifetime, based on activation energy of 0.6 eV, derates with T_J as shown in Figure 30.

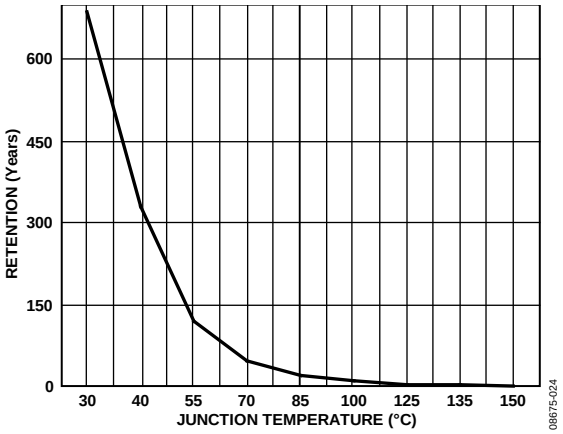

Figure 30. Flash/EE Memory Data Retention

PROGRAMMING

The 62 kB of Flash/EE memory can be programmed in circuit, using the serial download mode or the provided JTAG mode.

Downloading (In-Circuit Programming) via I²C

The ADuC7023 facilitates code download via the the I²C port. The parts enter download mode after a reset or power cycle if the BM pin is pulled low through an external 1 kΩ resistor and Flash Addess 0x80014 = 0xFFFFFFFF. Once in download mode, the user can download code to the full 62 kB of Flash/EE memory while the device is in-circuit in its target application hardware. An executable PC I²C download is provided as part of the development system for serial downloading via the I²C. A USB to I²C download dongle can be purchased from Analog Devices, Inc. This board connects to the USB port of a PC and to the I²C port of the ADuC7023. The part number is USB-I2C/LIN-CONV-Z.

The AN-806 Application Note describes the protocol for serial downloading via the I²C in more detail.

JTAG Access

The JTAG protocol uses the on-chip JTAG interface to facilitate code download and debug.

The JTAG interface is active as long as the part is not in download mode; that is, the P0.0/BM pin = 0 and Address 0x80014 = 0xFFFFFFFF at reset.

When debugging, user code must not write to the bits in GP0CON/GP0DAT corresponding to P0.0/P0.1/P0.2 and P0.3 pins. If user code changes the state of any of these pins, JTAG debug pods are not able to connect to the ADuC7023. In case this happens, the user should have a function in code that can be called externally to mass erase the part. Alternatively, the user should ensure that Flash Address 0x80014 is erased to allow erasing of the part through the I²C interface.

FEEMOD Register

Name: FEEMOD

Address: 0xFFFFF804

Default value: 0x0000

Access: Read/write

Function: FEEMOD sets the operating mode of the flash control interface. Table 32 shows FEEMOD MMR bit designations.

Table 32. FEEMOD MMR Bit Designations

Bit	Description
15 to 9	Reserved.
8	Reserved. Always set this bit to 0.
7 to 5	Reserved. Always set this bit to 0 except when writing keys. See the Sequence to Write the Key section.
4	Flash/EE interrupt enable. This bit is set by the user to enable the Flash/EE interrupt. The interrupt occurs when a command is complete. This bit is cleared by the user to disable the Flash/EE interrupt.
3	Erase/write command protection. This bit is set by the user to enable the erase and write commands. This bit is cleared to protect the Flash/EE against erase/write command.
2 to 0	Reserved. Always set this bit to 0.

FEECON Register

Name: FEECON

Address: 0xFFFFF808

Default value: 0x07

Access: Read/write

Function: FEECON is an 8-bit command register. The commands are described in Table 33.

Table 33. Command Codes in FEECON

Code	Command	Description
0x00[1]	Null	Idle state.
0x01[1]	Single read	Load FEEDAT with the 16-bit data. Indexed by FEEADR.
0x02[1]	Single write	Write FEEDAT at the address pointed by FEEADR. This operation takes 50 µs.
0x03[1]	Erase/write	Erase the page indexed by FEEADR, and write FEEDAT at the location pointed by FEEADR. This operation takes approximately 24 ms.
0x04[1]	Single verify	Compare the contents of the location pointed by FEEADR to the data in FEEDAT. The result of the comparison is returned in FEESTA Bit 1.
0x05[1]	Single erase	Erase the page indexed by FEEADR.
0x06[1]	Mass erase	Erase 62 kB of user space. The 2 kB of kernel are protected. This operation takes 2.48 sec. To prevent accidental execution, a command sequence is required to execute this instruction. See the Command Sequence for Executing a Mass Erase section.
0x07	Reserved	Reserved.
0x08	Reserved	Reserved.
0x09	Reserved	Reserved.
0x0A	Reserved	Reserved.
0x0B	Signature	Give a signature of the 64 kB of Flash/EE in the 24-bit FEESIGN MMR. This operation takes 32,778 clock cycles.
0x0C	Protect	This command can run one time only. The value of FEEPRO is saved and removed only with a mass erase (0x06) or the key (FEEADR/FEEDAT).

REMAP Register

Name: REMAP

Address: 0xFFFF0220

Default value: 0x00

Access: Read/write

Table 36. REMAP MMR Bit Designations

Bit	Name	Description
7 to 5		Reserved.
4		Read-only bit. Indicates the size of the Flash/EE memory available. If this bit is set, only 32 kB of Flash/EE memory is available.
3		Read-only bit. Indicates the size of the SRAM memory available. If this bit is set, only 4 kB of SRAM is available.
2 to 1	JTAFO	Read only bits. See the P0.0/BM description for further details. The kernel sets these bits to [11] if BM = 0 and 0x80014 ≠ 0xFFFFFFFF at reset. If these bits are set to [00], then P0.1/P0.2/P0.3 are configured as JTAG pins. P0.1/P0.2 cannot be used as GPIO. P0.3 can be used as GPIO, but this disables JTAG access. If these bits are set to [1x], then P0.1/P0.2/P0.3 are configured as GPIO pins. P0.1/P0.2/P0.3 can also be used as JTAG, but JTAG access is disabled if they are used as GPIO. These bits are configured by the kernel after any reset sequence and depend on the state of P0.0 and the value at Address 0x80014 during the last reset sequence.
0	Remap	Remap bit. This bit is set by the user to remap the SRAM to Address 0x00000000. This bit is cleared automatically after reset to remap the Flash/EE memory to Address 0x00000000.

Reset Operation

There are four kinds of reset: external, power-on, watchdog expiration, and software force. The RSTSTA register indicates the source of the last reset, and RSTCLR allows clearing of the RSTSTA register. These registers can be used during a reset exception service routine to identify the source of the reset. If RSTSTA is null, the reset is external.

The RSTCFG register allows different peripherals to retain their state after a watchdog or software reset.

RSTSTA Register

Name: RSTSTA

Address: 0xFFFF0230

Default value: 0x01

Access: Read/write

Table 37. RSTSTA MMR Bit Designations

Bit	Description
7 to 3	Reserved.
2	Software reset. This bit is set by the user to force a software reset. This bit is cleared by setting the corresponding bit in RSTCLR.
1	Watchdog timeout. This bit is set automatically when a watchdog timeout occurs. This bit is cleared by setting the corresponding bit in RSTCLR.
0	Power-on reset. This bit is set automatically when a power-on reset occurs. This bit is cleared by setting the corresponding bit in RSTCLR.

RSTCLR Register

Name: RSTCLR

Address: 0xFFFF0234

Default value: 0x00

Access: Write

Function: Note that to clear the RSTSTA register, users must write the Value 0x07 to the RSTCLR register.

RSTCFG Register

Name: RSTCFG

Address: 0xFFFF024C

Default value: 0x00

Access: Read/write

OTHER ANALOG PERIPHERALS

DAC

The ADuC7023 incorporates four, 12-bit voltage output DACs on chip. Each DAC has a rail-to-rail voltage output buffer capable of driving 5 kΩ/100 pF.

Each DAC has two selectable ranges: 0 V to V_{REF} (internal band gap 2.5 V reference) and 0 V to AV_{DD}.

The signal range is 0 V to AV_{DD}.

By setting RSTCFG Bit 2, the DAC output pins can retain their state during a watchdog or software reset.

MMRs Interface

Each DAC is independently configurable through a control register and a data register. These two registers are identical for the four DACs. Only DAC0CON (see Table 40) and DAC0DAT (see Table 41) are described in detail in this section.

DACxCON Registers

Name	Address	Default Value	Access
DAC0CON	0xFFFF0600	0x00	R/W
DAC1CON	0xFFFF0608	0x00	R/W
DAC2CON	0xFFFF0610	0x00	R/W
DAC3CON	0xFFFF0618	0x00	R/W

Table 40. DAC0CON MMR Bit Designations

Bit	Value	Name	Description
7			Reserved.
6		DACBY	This bit is set to bypass the DAC output buffer. This bit is cleared to enable the DAC output buffer.
5		DACCLK	DAC update rate. This bit is set by the user to update the DAC using Timer1. This bit is cleared by the user to update the DAC using HCLK (core clock).
4		DACCLR	DAC clear bit. This bit is set by the user to enable normal DAC operation. This bit is cleared by the user to reset data register of the DAC to 0.
3			Reserved. This bit remains at 0.
2			Reserved. This bit remains at 0.
1 to 0			DAC range bits.
	00		Power-down mode. The DAC output is in tristate.
	01		Reserved.
	10		0 V to V_{REF} (2.5 V) range.
	11		0 V to AV_{DD} range.

DACxDAT Registers

Name	Address	Default Value	Access
DAC0DAT	0xFFFF0604	0x00000000	R/W
DAC1DAT	0xFFFF060C	0x00000000	R/W
DAC2DAT	0xFFFF0614	0x00000000	R/W
DAC3DAT	0xFFFF061C	0x00000000	R/W

Table 41. DAC0DAT MMR Bit Designations

Bit	Description
31 to 28	Reserved.
27 to 16	12-bit data for DAC0.
15 to 0	Reserved.

Using the DACs

The on-chip DAC architecture consists of a resistor string DAC followed by an output buffer amplifier. The functional equivalent is shown in Figure 32.

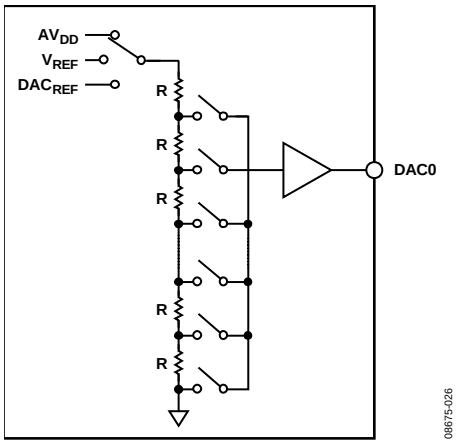

Figure 32. DAC Structure

As illustrated in Figure 32, the reference source for each DAC is user-selectable in software. It can be either AV_{DD} or V_{REF}. In 0-to-AV_{DD} mode, the DAC output transfer function spans from 0 V to the voltage at the AV_{DD} pin. In 0-to-V_{REF} mode, the DAC output transfer function spans from 0 V to the internal 2.5 V reference, V_{REF}.

The DAC output buffer amplifier features a true, rail-to-rail output stage implementation. This means that when unloaded, each output is capable of swinging to within less than 5 mV of both AV_{DD} and ground. Moreover, the DAC linearity specification (when driving a 5 kΩ resistive load to ground) is guaranteed through the full transfer function except Code 0 to Code 100, and, in 0-to-AV_{DD} mode only, Code 3995 to Code 4095.

Linearity degradation near ground and V_{DD} is caused by saturation of the output amplifier, and a general representation of its effects (neglecting offset and gain error) is illustrated in Figure 33. The dotted line in Figure 33 indicates the ideal transfer function, and the solid line represents what the transfer function may look like with endpoint nonlinearities due to saturation of the output amplifier. Figure 33 represents a transfer function in 0-to-AV_{DD}

Comparator Interface

The comparator interface consists of a 16-bit MMR, CMPCON, which is described in Table 46.

CMPCON Register

Name: CMPCON

Address: 0xFFFF0444

Default value: 0x0000

Access: Read/write

Table 46. CMPCON MMR Bit Descriptions

Bit	Value	Name	Description
15 to 11			Reserved.
10		CMPEN	Comparator enable bit. This bit is set by the user to enable the comparator. This bit is cleared by the user to disable the comparator.
9 to 8		CMPIN	Comparator negative input select bits.
	00		$AV_{DD}/2$.
	01		ADC3 input.
	10		DAC0 output.
	11		Reserved.
7 to 6		CMPOC	Comparator output configuration bits.
	00		Reserved.
	01		Reserved.
	10		Output on $COMP_{OUT}$.
	11		IRQ.
5		CMPOL	Comparator output logic state bit. When low, the comparator output is high if the positive input (CMP0) is above the negative input (CMP1). When high, the comparator output is high if the positive input is below the negative input.
4 to 3		CMPRES	Response time.
	00		5 µs response time typical for large signals (2.5 V differential). 17 µs response time typical for small signals (0.65 mV differential).
	11		3 µs typical.
	01/10		Reserved.
2		CMPHYST	Comparator hysteresis bit. This bit is set by the user to have a hysteresis of about 7.5 mV. This bit is cleared by the user to have no hysteresis.
1		CMPORI	Comparator output rising edge interrupt. This bit is set automatically when a rising edge occurs on the monitored voltage (CMP0). This bit is cleared by the user by writing a 1 to this bit.
0		CMPOFI	Comparator output rallying edge interrupt. This bit is set automatically when a falling edge occurs on the monitored voltage (CMP0). This bit is cleared by user.

GP2PAR Register

Name	GP2PAR
Address	0xFFFFF44C
Default value	0x00000000
Access	Read/write
Function	GP2PAR programs the parameters for Port 0, Port 1, and Port 2. Note that the GP2DAT MMR must always be written after changing the GP2PAR MMR.

Table 57. GPxPAR MMR Bit Descriptions

Bit	Description
31	Reserved.
30 to 29	Drive strength Px.7.
28	Pull-up disable Px.7.
27	Reserved.
26 to 26	Drive strength Px.6.
24	Pull-up disable Px.6.
23	Reserved.
22 to 21	Drive strength Px.5.
20	Pull-up disable Px.5.
19	Reserved.
18 to 17	Drive strength Px.4.
16	Pull-up disable Px.4.
15	Reserved.
14 to 13	Drive strength Px.3.
12	Pull-up disable Px.3.
11	Reserved.
10 to 9	Drive strength Px.2.
8	Pull-up disable Px.2.
7	Reserved.
6 to 5	Drive strength Px.1.
4	Pull-up disable Px.1.
3	Reserved.
2 to 1	Drive strength Px.0.
0	Pull-up disable Px.0.

Table 58. GPIO Drive Strength Control Bits Descriptions

Control Bits Value	Description
00	Medium drive strength.
01	Low drive strength.
1x	High drive strength.

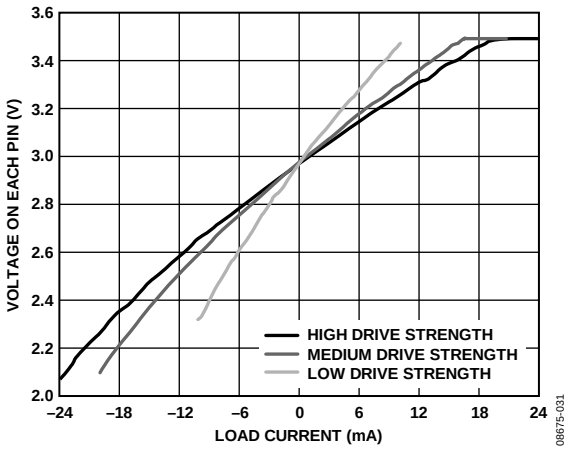

Figure 37. Programmable Strength for High Level

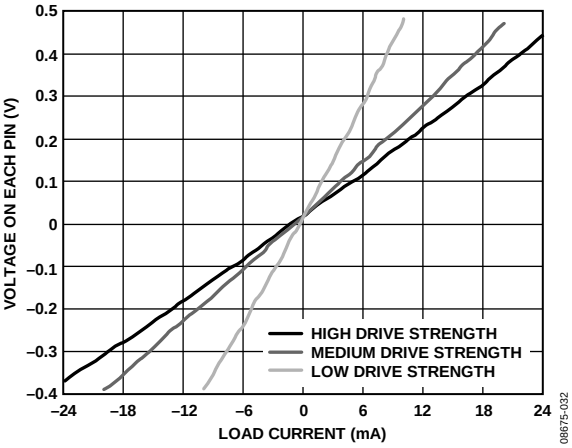

Figure 38. Programmable Strength for Low Level

The drive strength bits can be written one time only after reset. More writing to related bits has no effect on changing drive strength. The GPIO drive strength and pull-up disable is not always adjustable for the GPIO port. Some control bits cannot be changed (see Table 59).

Table 59. GPxPAR Control Bits Access Descriptions[1]

Bit	GP0PAR	GP1PAR	GP2PAR
31	Reserved	Reserved	Reserved
30 to 29	R/W	R/W	Reserved
28	R/W	R/W	Reserved
27	Reserved	Reserved	Reserved
26 to 26	R/W	R/W	Reserved
24	R/W	R/W	Reserved
23	Reserved	Reserved	Reserved
22 to 21	R/W	R (b00)	Reserved
20	R/W	R/W	Reserved
19	Reserved	Reserved	Reserved
18 to 17	R (b00)	R (b00)	R (b00)
16	R/W	R/W	R/W
15	Reserved	Reserved	Reserved
14 to 13	R (b00)	R (b00)	R (b00)
12	R/W	R/W	R/W
11	Reserved	Reserved	Reserved

Table 62. GPxCLR MMR Bit Descriptions

Bit	Description
31 to 24	Reserved.
23 to 16	Data port x clear bit. This bit is set to 1 by the user to clear the bit on Port x; this bit also clears the corresponding bit in the GPxDAT MMR. This bit is cleared to 0 by the user; this bit does not affect the data out.
15 to 0	Reserved.

SERIAL PERIPHERAL INTERFACE

The ADuC7023 integrates a complete hardware serial peripheral interface (SPI) on chip. SPI is an industry standard, synchronous serial interface that allows eight bits of data to be synchronously transmitted and simultaneously received, that is, full duplex up to a maximum bit rate of 20 Mbps.

The SPI port can be configured for master or slave operation and typically consists of four pins: MISO, MOSI, SCLK, and SPI$\overline{SS}$.

MISO (Master In, Slave Out) Pin

The MISO pin is configured as an input line in master mode and an output line in slave mode. The MISO line on the master (data in) should be connected to the MISO line in the slave device (data out). The data is transferred as byte wide (8-bit) serial data, MSB first.

MOSI (Master Out, Slave In) Pin

The MOSI pin is configured as an output line in master mode and an input line in slave mode. The MOSI line on the master (data out) should be connected to the MOSI line in the slave device (data in). The data is transferred as byte wide (8-bit) serial data, MSB first.

SCLK (Serial Clock I/O) Pin

The master serial clock (SCLK) synchronizes the data being transmitted and received through the MOSI SCLK period. Therefore, a byte is transmitted/received after eight SCLK periods. The SCLK pin is configured as an output in master mode and as an input in slave mode.

In master mode, polarity and phase of the clock are controlled by the SPICON register, and the bit rate is defined in the SPIDIV register as follows:

$$f_{SERIAL\ CLOCK} = \frac{f_{UCLK}}{2 \times (1 + SPIDIV)}$$

where:

f_{UCLK} is the clock selected by POWCON1 Bit 7 to Bit 6.

The maximum speed of the SPI clock is independent on the clock divider bits.

In slave mode, the SPICON register must be configured with the phase and polarity of the expected input clock. The slave accepts data from an external master up to 10 Mbps.

In both master and slave modes, data is transmitted on one edge of the SCLK signal and sampled on the other. Therefore, it is important that the polarity and phase are configured the same for the master and slave devices.

SPI Chip Select ($\overline{SS}$ Input) Pin

In SPI slave mode, a transfer is initiated by the assertion of $\overline{SS}$, which is an active low input signal. The SPI port then transmits and receives 8-bit data until the transfer is concluded by deassertion of $\overline{SS}$. In slave mode, $\overline{SS}$ is always an input.

In SPI master mode, the $\overline{SS}$ is an active low output signal. It asserts itself automatically at the beginning of a transfer and deasserts itself upon completion.

Configuring External Pins for SPI Functionality

P1.1 is the slave chip select pin. In slave mode, this pin is an input and must be driven low by the master. In master mode, this pin is an output and goes low at the beginning of a transfer and high at the end of a transfer.

P1.0 is the SCLK pin.

P0.6 is the master in, slave out (MISO) pin.

P0.7 is the master out, slave in (MOSI) pin.

To configure these pins for SPI mode, see the General-Purpose Input/Output section.

SPI Registers

The following MMR registers control the SPI interface: SPISTA, SPIRX, SPITX, SPIDIV, and SPICON.

SPI Status Register

Name: SPISTA

Address: 0xFFFF0A00

Default value: 0x0000

Access: Read

Function: This 32-bit MMR contains the status of the SPI interface in both master and slave modes.

Table 80. Feedback Configuration

Bit	Value	PLAELM0	PLAELM1 to PLAELM7	PLAELM8	PLAELM9 to PLAELM15
10 to 9	00	Element 15	Element 0	Element 7	Element 8
	01	Element 2	Element 2	Element 10	Element 10
	10	Element 4	Element 4	Element 12	Element 12
	11	Element 6	Element 6	Element 14	Element 14
8 to 7	00	Element 1	Element 1	Element 9	Element 9
	01	Element 3	Element 3	Element 11	Element 11
	10	Element 5	Element 5	Element 13	Element 13
	11	Element 7	Element 7	Element 15	Element 15

PLAADC Register

Name: PLAADC

Address: 0xFFFF0B48

Default value: 0x00000000

Access: Read/write

Function: PLAADC is the PLA source for the ADC start conversion signal.

Table 81. PLAADC MMR Bit Descriptions

Bit	Value	Description
31 to 5		Reserved.
4		ADC start conversion enable bit. This bit is set by the user to enable ADC start conversion from PLA. This bit is cleared by the user to disable ADC start conversion from PLA.
3 to 0		ADC start conversion source.
	0000	PLA Element 0.
	0001	PLA Element 1.
	0010	PLA Element 2.
	0011	PLA Element 3.
	0100	PLA Element 4.
	0101	PLA Element 5.
	0110	PLA Element 6.
	0111	PLA Element 7.
	1000	PLA Element 8.
	1001	PLA Element 9.
	1010	PLA Element 10.
	1011	PLA Element 11.
	1100	PLA Element 12.
	1101	PLA Element 13.
	1110	PLA Element 14.
	1111	PLA Element 15.

PLADIN Register

Name: PLADIN

Address: 0xFFFF0B4C

Default value: 0x00000000

Access: Read/write

Function: PLADIN is a data input MMR for PLA.

Table 82. PLADIN MMR Bit Descriptions

Bit	Description
31 to 16	Reserved.
15 to 0	Input bit to Element 15 to Element 0.

PLADOUT Register

Name: PLADOUT

Address: 0xFFFF0B50

Default value: 0x00000000

Access: Read

Function: PLADOUT is a data output MMR for PLA. This register is always updated.

Table 83. PLADOUT MMR Bit Descriptions

Bit	Description
31 to 16	Reserved.
15 to 0	Output bit from Element 15 to Element 0.

PLALCK Register

Name: PLALCK

Address: 0xFFFF0B54

Default value: 0x00

Access: Write

Function: PLALCK is a PLA lock option. Bit 0 is written only once. When set, it does not allow modifying any of the PLA MMRs, except PLADIN. A PLA tool is provided in the development system to easily configure PLA.

PWM0COM0 Compare Register

Name: PWM0COM0

Address: 0xFFFF0F84

Default value: 0x0000

Access: Read and write

Function: PWM0 output pin goes high when the PWM timer reaches the count value stored in this register.

PWM0COM1 Compare Register

Name: PWM0COM1

Address: 0xFFFF0F88

Default value: 0x0000

Access: Read and write

Function: PWM0 output pin goes low when the PWM timer reaches the count value stored in this register.

PWM0COM2 Compare Register

Name: PWM0COM2

Address: 0xFFFF0F8C

Default value: 0x0000

Access: Read and write

Function: PWM1 output pin goes low when the PWM timer reaches the count value stored in this register.

PWM0LEN Register

Name: PWM0LEN

Address: 0xFFFF0F90

Default value: 0x0000

Access: Read and write

Function: PWM1 output pin goes high when the PWM timer reaches the value stored in this register.

PWM1COM0 Compare Register

Name: PWM1COM0

Address: 0xFFFF0F94

Default value: 0x0000

Access: Read and write

Function: PWM2 output pin goes high when the PWM timer reaches the count value stored in this register.

PWM1COM1 Compare Register

Name: PWM1COM1

Address: 0xFFFF0F98

Default value: 0x0000

Access: Read and write

Function: PWM2 output pin goes low when the PWM timer reaches the count value stored in this register.

PWM1COM2 Compare Register

Name: PWM1COM2

Address: 0xFFFF0F9C

Default value: 0x0000

Access: Read and write

Function: PWM3 output pin goes low when the PWM timer reaches the count value stored in this register.

PWM1LEN Register

Name: PWM1LEN

Address: 0xFFFF0FA0

Default value: 0x0000

Access: Read and write

Function: PWM3 output pin goes high when the PWM timer reaches the value stored in this register.

PROCESSOR REFERENCE PERIPHERALS

INTERRUPT SYSTEM

There are 22 interrupt sources on the ADuC7023 that are controlled by the interrupt controller. Most interrupts are generated from the on-chip peripherals, such as ADC. Four additional interrupt sources are generated from external interrupt request pins, IRQ0, IRQ1, IRQ2, and IRQ3. The ARM7TDMI CPU core only recognizes interrupts as one of two types, a normal interrupt request IRQ or a fast interrupt request FIQ. All the interrupts can be masked separately.

The control and configuration of the interrupt system is managed through nine interrupt related registers, four dedicated to IRQ, and four dedicated to FIQ. An additional MMR is used to select the programmed interrupt source. The bits in each IRQ and FIQ registers represent the same interrupt source as described in Table 88.

The ADuC7023 contains a vectored interrupt controller (VIC) that supports nested interrupts up to eight levels. The VIC also allows the programmer to assign priority levels to all interrupt sources. Interrupt nesting is enabled by setting the ENIRQN bit in the IRQCONN register. A number of extra MMRs are used when the full-vectored interrupt controller is enabled.

IRQSTA/FIQSTA should be saved immediately upon entering the interrupt service routine (ISR) to ensure that all valid interrupt sources are serviced.

Table 88. IRQ/FIQ MMRs Bit Description

Bit	Description
0	All interrupts OR'ed (FIQ only).
1	SWI.
2	Timer0.
3	Timer1.
4	Watchdog timer (Timer 2).
5	Flash control.
6	ADC channel.
7	PLL lock.
8	I^2C0 master.
9	I^2C0 slave.
10	I^2C1 master.
11	I^2C1 slave.
12	SPI.
13	External IRQ0.
14	Comparator.
15	PSM.
16	External IRQ1.
17	PLA IRQ0.
18	External IRQ2.
19	External IRQ3.
20	PLA IRQ1.
21	PWM.

IRQ

The interrupt request (IRQ) is the exception signal to enter the IRQ mode of the processor. It is used to service general-purpose interrupt handling of internal and external events.

The four 32-bit registers dedicated to IRQ are: IRQSTA, IRQSIG, IRQEN, and IRQCLR.

IRQSTA Register

Name: IRQSTA

Address: 0xFFFF0000

Default value: 0x00000000

Access: Read

Function: IRQSTA (read-only register) provides the current-enabled IRQ source status. When set to 1, that source generates an active IRQ request to the ARM7TDMI core. There is no priority encoder or interrupt vector generation. This function is implemented in software in a common interrupt handler routine. All 32 bits are logically OR'ed to create the IRQ signal to the ARM7TDMI core.

IRQSIG Register

Name: IRQSIG

Address: 0xFFFF0004

Default value: 0x00XXX000

Access: Read

Function: IRQSIG reflects the status of the different IRQ sources. If a peripheral generates an IRQ signal, the corresponding bit in the IRQSIG is set; otherwise, it is cleared. The IRQSIG bits are cleared when the interrupt in the particular peripheral is cleared. All IRQ sources can be masked in the IRQEN MMR. IRQSIG is read-only.

IRQP0 Register

Name: IRQP0

Address: 0xFFFF0020

Default value: 0x00000000

Access: Read and write

Table 92. IRQP0 MMR Bit Designations

Bit	Name	Description
31	Reserved	Reserved bit
30 to 28	PLLPI	A priority level of 0 to 7 can be set for PLL lock interrupt.
27	Reserved	Reserved bit
26 to 24	ADCPI	A priority level of 0 to 7 can be set for the ADC interrupt source.
23	Reserved	Reserved bit
22 to 20	FlashPI	A priority level of 0 to 7 can be set for the Flash controller interrupt source.
19	Reserved	Reserved bit.
18 to 16	T2PI	A priority level of 0 to 7 can be set for Timer2.
15	Reserved	Reserved bit.
14 to 12	T1PI	A priority level of 0 to 7 can be set for Timer1.
11	Reserved	Reserved bit.
10 to 8	T0PI	A priority level of 0 to 7 can be set for Timer0.
7	Reserved	Reserved bit
6 to 4	SWINTP	A priority level of 0 to 7 can be set for the software interrupt source.
3 to 0	Reserved	Interrupt 0 cannot be prioritized.

IRQP1 Register

Name: IRQP1

Address: 0xFFFF0024

Default value: 0x00000000

Access: Read and write

Table 93. IRQP1 MMR Bit Designations

Bit	Name	Description
31	Reserved	Reserved bit.
30 to 28	PSMPI	A priority level of 0 to 7 can be set for the power supply monitor interrupt source.
27	Reserved	Reserved bit.
26 to 24	COMPI	A priority level of 0 to 7 can be set for comparator.
23	Reserved	Reserved bit.
22 to 20	IRQ0PI	A priority level of 0 to 7 can be set for IRQ0.
19	Reserved	Reserved bit.
18 to 16	SPIPI	A priority level of 0 to 7 can be set for SPI.
15	Reserved	Reserved bit.
14 to 12	I2C1SPI	A priority level of 0 to 7 can be set for I^2C1 slave.
11	Reserved	Reserved bit.
10 to 8	I2C1MPI	A priority level of 0 to 7 can be set for I^2C1 master.
7	Reserved	Reserved bits.
6 to 4	I2C0SPI	A priority level of 0 to 7 can be set for I^2C0 slave.
3	Reserved	Reserved bits.
2 to 0	I2C0MPI	A priority level of 0 to 7 can be set for I^2C0 master.

IRQP2 Register

Name: IRQP2

Address: 0xFFFF0028

Default value: 0x00000000

Access: Read and write

Table 94. IRQP2 MMR Bit Designations

Bit	Name	Description
31 to 23	Reserved	Reserved bit.
22 to 20	PWMPI	A priority level of 0 to 7 can be set for PWM.
19	Reserved	Reserved bit.
18 to 16	PLA1PI	A priority level of 0 to 7 can be set for PLA IRQ1.
15	Reserved	Reserved bit.
14 to 12	IRQ3PI	A priority level of 0 to 7 can be set for IRQ3.
11	Reserved	Reserved bit.
10 to 8	IRQ2PI	A priority level of 0 to 7 can be set for IRQ2.
7	Reserved	Reserved bit.
6 to 4	PLA0PI	A priority level of 0 to 7 can be set for PLA IRQ0.
3	Reserved	Reserved bit.
2 to 0	IRQ1PI	A priority level of 0 to 7 can be set for IRQ1.

FIQSTAN Register

If IRQCONN Bit 1 is asserted and FIQVEC is read, then one of these bits assert. The bit that asserts depends on the priority of the FIQ. If the FIQ is of Priority 0, then Bit 0 asserts. If the FIQ is of Priority 1, then Bit 1 asserts, and so forth.

When a bit is set in this register, all interrupts of that priority and lower are blocked.

To clear a bit in this register, all bits of a higher priority must be cleared first. It is only possible to clear one bit at a time. For example, if this register is set to 0x09, then writing 0xFF changes the register to 0x08 and writing 0xFF a second time changes the register to 0x00.

Name: FIQSTAN

Address: 0xFFFF013C

Default value: 0x00000000

Access: Read/write

Table 98. FIQSTAN MMR Bit Designations

Bit	Name	Description
31 to 8	Reserved	These bits are reserved and should not be written to.
7 to 0		This bit is set to 1 to enables nesting of FIQ interrupts. When this bit is cleared, it means no nesting or prioritization of FIQs is allowed.

External Interrupts and PLA interrupts

The ADuC7023 provides up to four external interrupt sources and two PLA interrupt sources. These external interrupts can be individually configured as level or rising/falling edge triggered.

To enable the external interrupt source or the PLA interrupt source, the appropriate bit must be set in the FIQEN or IRQEN register. To select the required edge or level to trigger on, the IRQCONE register must be appropriately configured.

To properly clear an edge-based external IRQ interrupt or an edge-based PLA interrupt, set the appropriate bit in the IRQCLRE register.

IRQCONE Register

Name: IRQCONE

Address: 0xFFFF0034

Default value: 0x00000000

Access: Read and write

Table 99. IRQCONE MMR Bit Designations

Bit	Value	Name	Description
31 to 12		Reserved	These bits are reserved and should not be written to.
11 to 10	11	PLA1SRC[1:0]	PLA IRQ1 triggers on falling edge.
	10		PLA IRQ1 triggers on rising edge.
	01		PLA IRQ1 triggers on low level.
	00		PLA IRQ1 triggers on high level.
9 to 8	11	IRQ3SRC[1:0]	External IRQ3 triggers on falling edge.
	10		External IRQ3 triggers on rising edge.
	01		External IRQ3 triggers on low level.
	00		External IRQ3 triggers on high level.
7 to 6	11	IRQ2SRC[1:0]	External IRQ2 triggers on falling edge.
	10		External IRQ2 triggers on rising edge.
	01		External IRQ2 triggers on low level.
	00		External IRQ2 triggers on high level.
5 to 4	11	PLA0SRC[1:0]	PLA IRQ0 triggers on falling edge.
	10		PLA IRQ0 triggers on rising edge.
	01		PLA IRQ0 triggers on low level.
	00		PLA IRQ0 triggers on high level.
3 to 2	11	IRQ1SRC[1:0]	External IRQ1 triggers on falling edge.
	10		External IRQ1 triggers on rising edge.
	01		External IRQ1 triggers on low level.
	00		External IRQ1 triggers on high level.
1 to 0	11	IRQ0SRC[1:0]	External IRQ0 triggers on falling edge.
	10		External IRQ0 triggers on rising edge.
	01		External IRQ0 triggers on low level.
	00		External IRQ0 triggers on high level.

The Timer0 interface consists of four MMRs: T0LD, T0VAL, T0CON, and T0CLRI.

T0LD Register

Name: T0LD

Address: 0xFFFF0300

Default value: 0x0000

Access: Read/write

T0LD is a 16-bit load register that holds the 16-bit value that is loaded into the counter.

T0VAL Register

Name: T0VAL

Address: 0xFFFF0304

Default Value: 0xFFFF

Access: Read

T0VAL is a 16-bit read-only register representing the current state of the counter.

T0CON Register

Name: T0CON

Address: 0xFFFF0308

Default value: 0x0000

Access: R/W

T0CON is the configuration MMR described in Table 102.

Table 102. T0CON MMR Bit Descriptions

Bit	Value	Description
15 to 8		Reserved.
7		Timer0 enable bit. This bit is set by the user to enable Timer0. This bit is cleared by the user to disable Timer0 by default.
6		Timer0 mode. This bit is set by the user to operate in periodic mode. This bit is cleared by the user to operate in free-running mode. Default mode.
5 to 4		Clock select bits.
	00	HCLK.
	01	UCLK.
	10	Internal 32768 Hz oscillator.
	11	Reserved.
3 to 2	00	Source clock/1. Default value.
	01	Source clock/16.
	10	Source clock/256.
	11	Undefined. Equivalent to 00.
1 to 0		Reserved.

T0CLRI Register

Name: T0CLRI

Address: 0xFFFF030C

Default value: 0xXX

Access: Write

T0CLRI is an 8-bit register. Writing any value to this register clears the interrupt.

The following is the recommended procedure for servicing the Timer 0 interrupt:

```
void  IRQ_Handler(void) __irq
{
  if(IRQSTA & BIT2) // Timer0 IRQ?
  {
    T0CLRI = 0;   //clear Timer0 interrupt
    T0CON = 0x00; //disable Timer0 interrupt
    T0CON = 0xC8; //enable Timer0 interrupt
  }
}
```

Timer1 (General-Purpose Timer)

Timer1 is a general-purpose, 32-bit timer (count down or count up) with a programmable prescaler. The source can be the 32 kHz external crystal, the undivided system, the core clock, or P1.1 (maximum frequency 44 MHz). This source can be scaled by a factor of 1, 16, 256, or 32,768.

The counter can be formatted as a standard 32-bit value or as hours, minutes, seconds, hundredths.

Timer1 has a capture register (T1CAP) that can be triggered by a selected IRQ source initial assertion. This feature can be used to determine the assertion of an event more accurately than the precision allowed by the RTOS timer when the IRQ is serviced.

Timer1 can be used to start ADC conversions as shown in the block diagram in Figure 43.

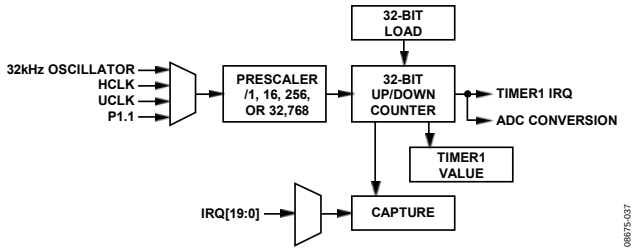

Figure 43. Timer1 Block Diagram

The Timer1 interface consists of five MMRs: T1LD, T1VAL, T1CON, T1CLRI, and T1CAP.

DEVELOPMENT TOOLS

PC-BASED TOOLS

Four types of development systems are available for the ADuC7023 family. The ADuC7023 QuickStart Plus is intended for new users who want to have a comprehensive hardware development environment.

These systems consist of the following PC-based (Windows® compatible) hardware and software development tools.

Hardware

The hardware system uses the ADuC7023 evaluation board, a serial port programming cable, and a RDI-compliant JTAG emulator (included in the ADuC7023 QuickStart Plus only).

Software

The software system has an integrated development environment, incorporating an assembler, compiler, and nonintrusive JTAG-based debugger. The software sytem uses a serial downloader software and example code.

Miscellaneous

The miscellaneous systems use CD-ROM documentation.

IN-CIRCUIT I²C DOWNLOADER

An I²C-based serial downloader is available at www.analog.com. This software requires an USB-to-I²C adaptor board available from Analog Devices. The part number for this USB-to-I²C adapter is USB-I2C/LIN-CONV-Z.

ORDERING GUIDE

Model[1]	ADC Channels	DAC Channels	FLASH/ RAM	GPIO	Downloader	Temperature Range	Package Description	Package Option	Ordering Quantity
ADuC7023BCP6Z62I	12	4	62 kB/8 kB	20	I^2C	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-10	490
ADuC7023BCP6Z62IRL	12	4	62 kB/8 kB	20	I^2C	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-10	2,500
ADuC7023BCP6Z62IR7	12	4	62 kB/8 kB	20	I^2C	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-10	750
ADuC7023BCPZ62I	6	4	62 kB/8 kB	12	I^2C	−40°C to +125°C	32-Lead LFCSP_WQ	CP-32-11	490
ADuC7023BCPZ62I-RL	6	4	62 kB/8 kB	12	I^2C	−40°C to +125°C	32-Lead LFCSP_WQ	CP-32-11	5,000
ADuC7023BCPZ62I-R7	6	4	62 kB/8 kB	12	I^2C	−40°C to +125°C	32-Lead LFCSP_WQ	CP-32-11	1,500
ADuC7023BCBZ62I-R7	10	4	62 kB/8 kB	16	I^2C	−40°C to +125°C	36-Ball WLCSP	CB-36-03	1,500
EVAL-ADuC7023QSPZ							ADuC7023 QuickStart Plus Development System Using 32-Pin ADuC7023		
EVAL-ADuC7023QSPZ1							ADuC7023 QuickStart Plus Development System Using 40-Pin ADuC7023		
EVAL-ADuC7023QSPZ2							ADuC7023 QuickStart Plus Development System Using 36-Ball ADuC7023		

[1] Z = RoHS Compliant Part.