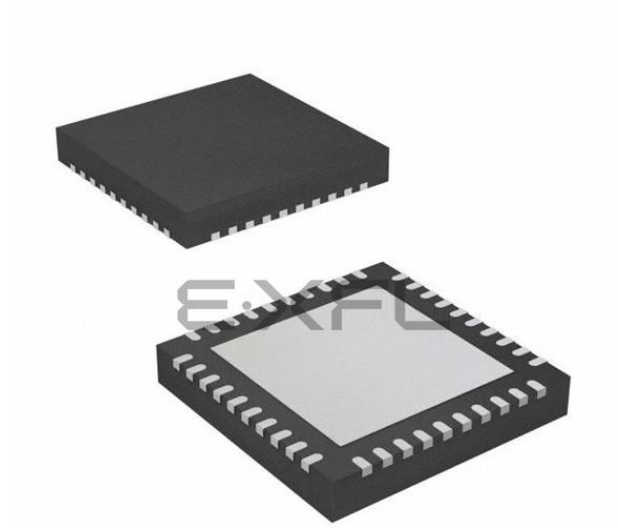

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	44MHz
Connectivity	I²C, SPI
Peripherals	POR, PWM, WDT
Number of I/O	20
Program Memory Size	62KB (31K x16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 32
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 12x12b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	40-WFQFN Exposed Pad, CSP
Supplier Device Package	40-LFCSP-WQ (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc7023bcp6z62i

Table 7. SPI Slave Mode Timing (Phase Mode = 0)

Parameter	Description	Min	Typ	Max	Unit
$t_{\overline{SS}}$	$\overline{SS}$ to SCLK edge	200			ns
t_{SL}	SCLK low pulse width[1]		(SPIDIV + 1) × t_{UCLK}		ns
t_{SH}	SCLK high pulse width[1]		(SPIDIV + 1) × t_{UCLK}		ns
t_{DAV}	Data output valid after SCLK edge			25	ns
t_{DSU}	Data input setup time before SCLK edge[1]	1 × t_{UCLK}			ns
t_{DHD}	Data input hold time after SCLK edge[1]	2 × t_{UCLK}			ns
t_{DF}	Data output fall time		5	12.5	ns
t_{DR}	Data output rise time		5	12.5	ns
t_{SR}	SCLK rise time		5	12.5	ns
t_{SF}	SCLK fall time		5	12.5	ns
t_{DOCS}	Data output valid after $\overline{SS}$ edge			25	ns
t_{SFS}	$\overline{SS}$ high after SCLK edge	0			ns

[1] t_{UCLK} = 23.9 ns. It corresponds to the 41.78 MHz internal clock from the PLL before the clock divider.

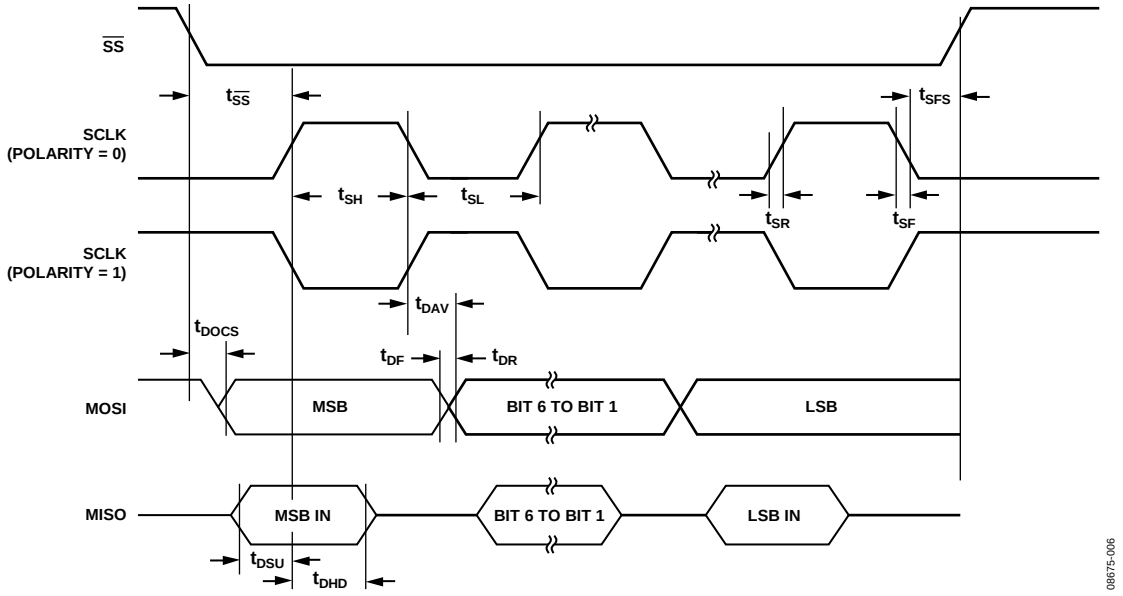

Figure 6. SPI Slave Mode Timing (Phase Mode = 0)

Pin No.				
40-LFCSP	32-LFCSP	36-WLCSP	Mnemonic	Description
31	N/A	A1	P2.3/ADC8/PLAO[7]	General-Purpose Input and Output Port 2.3/ADC Single-Ended or Differential Analog Input 8/Programmable Logic Array Output Element 7. By default, this pin is configured as a digital input with a weak pull-up resistor enabled. When used as ADC input, pull-up resistor should be disabled manually.
30	N/A	B1	P2.2/ADC7/SYNC/PLAO[6]	General-Purpose Input and Output Port 2.2/ADC Single-Ended or Differential Analog Input 7/PWM Sync/Programmable Logic Array Output Element 6. By default, this pin is configured as a digital input with a weak pull-up resistor enabled. When used as ADC input, pull-up resistor should be disabled manually.
8	N/A	E6	P2.0/ADC12/PWM4/PLAI[7]	General-Purpose Input and Output Port 2.0/ADC Single-Ended or Differential Analog Input 12/PWM Output 4/Programmable Logic Array Input Element 7. By default, this pin is configured as a digital input with a weak pull-up resistor enabled. When used as an ADC input, it is not possible to disable the internal pull-up resister. This means that this pin has a higher leakage current value than other analog input pins.
2	2	C4	GND_{REF}	Ground Voltage Reference for the ADC. For optimal performance, the analog power supply should be separated from DGND.
3	3	C5	DAC0	DAC0 Voltage Output or ADC Input.
4	4	C6	DAC1	DAC1 Voltage Output or ADC Input.
5	5	D5	DAC2	DAC2 Voltage Output
6	6	D6	DAC3	DAC3 Voltage Output
24	20	D2	TMS	Test Mode Select, JTAG Test Port Input. Debug and download access. This pin has an internal pull-up resistor to IOV_{DD}. In some cases an external pull-up resistor is also required to ensure the part does not enter an erroneous state.
25	21	D1	P0.0/nTRST/ADC_{BUSY}/PLAI[8]/BM	This is a multifunction pin as follows: General-Purpose Input and Output Port 0.0. By default, this pin is configured as GPIO. JTAG Reset Input. Debug and download access. If this pin is held low, JTAG access is not possible because the JTAG interface is held in reset and P0.1/P0.2/P0.3 are configured as GPIO pins. ADC Busy Signal. Programmable Logic Array Input Element 8. Boot Mode Entry Pin. The ADuC7023 enters I^2C download mode if BM is low at reset with a flash address 0x80014 = 0xFFFFFFFF. The ADuC7023 executes code if BM is pulled high at reset or if BM is low at reset with a flash address 0x80014 not equal to 0xFFFFFFFF.
26	22	C1	P0.1/PLAI[9]/TDO	The default value of this pin depends on the level of P0.0/BM. If P0.0/BM = 0, this pin defaults to a general purpose input. If P0.0/BM = 1, this pin defaults to a JTAG test data output pin and does not work as a GPIO. This is a multifunction pin as follows: General-Purpose Input and Output Port 0.1. Programmable Logic Array Input Element 9. Test Data Out, JTAG Test Port Output. Debug and download access. When debugging the part via JTAG, this pin must not be toggled by user code, and the GP0CON/GP0DAT register bits affecting this pin must not be changed as doing so disables JTAG access.
27	23	C2	P0.2/PLAO[8]/TDI	The default value of this pin depends on the level of P0.0/BM. If P0.0/BM = 0, this pin defaults to a general purpose input. If P0.0/BM = 1, this pin defaults to a JTAG test data input pin and does not work as a GPIO. This is a multifunction pin as follows: General-Purpose Input and Output Port 0.2. Programmable Logic Array Output Element 8. Test Data In, JTAG Test Port Input. Debug and download access. When debugging the part via JTAG, this pin must not be toggled by user code, and the GP0CON/GP0DAT register bits affecting this pin must not be changed as doing so disables JTAG access.

Pin No.				
40-LFCSP	32-LFCSP	36-WLCSP	Mnemonic	Description
28	24	C3	P0.3/PLAO[9]/TCK	The default value of this pin depends on the level of P0.0/BM. If P0.0/BM = 0, this pin defaults to a general purpose input. If P0.0/BM = 1, this pin defaults to a JTAG test data clock pin. This is a multifunction pin as follows: General-Purpose Input and Output Port 0.3. Programmable Logic Array Output Element 9. Test Clock, JTAG Test Port Clock Input. Debug and download access. When debugging the part via JTAG, this pin must not be toggled by user code and the GP0CON/GP0DAT register bits affecting this pin must not be changed as doing so disables JTAG access.
17	13	E3	DGND	Digital Ground.
18	14	F3	IOV_{DD}	3.3 V Supply for GPIO and Input of the On-Chip Voltage Regulator.
19	15	D3	LV_{DD}	2.6 V Output of the On-Chip Voltage Regulator. This output must be connected to a 0.47 µF capacitor to DGND only.
20	16	F2	$\overline{RST}$	Reset Input, Active Low.
23	19	E1	RTCK	Return JTAG Clock Signal. This is not the standard JTAG clock signal. It is an output signal from the JTAG controller. If using a 20-lead JTAG header, connect to Pin 11.
9	7	F6	P0.4/IRQ0/SCL0/PLAI[0]/CONV	General-Purpose Input and Output Port 0.4/External Interrupt Request 0/ I^2C0 Clock Signal/Programmable Logic Array Input Element 0/ADC External Convert Start. By default, this pin is configured as a digital input with a weak pull-up resistor enabled.
10	8	E5	P0.5/SDA0/PLAI[1]/$COMP_{OUT}$	General-Purpose Input and Output Port 0.5/I^2C0 Data Signal/ Programmable Logic Array Input Element 1/Voltage Comparator Output. By default, this pin is configured as a digital input with a weak pull-up resistor enabled.
	9	F5	P0.6/MISO/SCL1/PLAI[2]	General-Purpose Input and Output Port 0.6/SPI MISO Signal/I^2C1 Clock On 32-Lead and 36-Ball Packages/Programmable Logic Array Input Element 2. By default, this pin is configured as a digital input with a weak pull-up resistor enabled.
	10	D4	P0.7/MOSI/SDA1/PLAO[0]	General-Purpose Input and Output Port 0.7/SPI MOSI Signal/I^2C1 Data Signal On 32-Lead and 36-Ball Packages/Programmable Logic Array Output Element 0. By default, this pin is configured as a digital input with a weak pull-up resistor enabled.
11			P0.6/MISO/PLAI[2]	General-Purpose Input and Output Port 0.6/SPI MISO Signal/Programmable Logic Array Input Element 2. By default, this pin is configured as a digital input with a weak pull-up resistor enabled.
12			P0.7/MOSI/PLAO[0]	General-Purpose Input and Output Port 0.7/SPI MOSI Signal/Programmable Logic Array Output Element 0. By default this pin is configured as a digital input with a weak pull-up reisistor enabled.
21	17	F1	XCLKI	Input to the Crystal Oscillator Inverter and Input to the Internal Clock Generator Circuits. Connect to DGND if unused.
22	18	E2	XCLKO	Output from the Crystal Oscillator Inverter. Leave unconnected if unused.
16	N/A	N/A	P1.7/PWM3/SDA1/PLAI[6]	General-Purpose Input and Output Port 1.7/PWM Output 3/I^2C1 Data Signal/Programmable Logic Array Input Element 6. By default, this pin is configured as a digital input with a weak pull-up resistor enabled.
15	N/A	N/A	P1.6/PWM2/SCL1/PLAI[5]	General-Purpose Input and Output Port 1.6/PWM Output 2/I^2C1 Clock Signal/Programmable Logic Array Input Element 5. By default, this pin is configured as a digital input with a weak pull-up resistor enabled.
29	N/A	N/A	P1.5/ADC6/$PWM_{TRIPINPUT}$/PLAO[4]	General-Purpose Input and Output Port 1.5/ADC Single-Ended or Differential Analog Input 6/$PWM_{TRIPINPUT}$/Programmable Logic Array Output Element 4. By default, this pin is configured as a digital input with a weak pull-up resistor enabled. When used as ADC input, the pull-up resistor should be disabled manually.
7	N/A	N/A	P1.4/ADC10/PLAO[3]	General-Purpose Input and Output Port 1.4/ADC Single-Ended or Differential Analog Input 10/Programmable Logic Array Output Element 3. By default, this pin is configured as a digital input with a weak pull-up resistor enabled. When used as ADC input, the pull-up resistor should be disabled manually.

Table 12. Timer Address Base = 0xFFFF0300

Address	Name	Byte	Access Type	Default Value[1]	Description
0x0300	T0LD	2	R/W	0x0000	Timer0 load register.
0x0304	T0VAL	2	R	0xFFFF	Timer0 value register.
0x0308	T0CON	2	R/W	0x0000	Timer0 control MMR.
0x030C	T0CLRI	1	W	0xXX	Timer0 interrupt clear register.
0x0320	T1LD	4	R/W	0x00000000	Timer1 load register.
0x0324	T1VAL	4	R	0xFFFFFFFF	Timer1 value register
0x0328	T1CON	4	R/W	0x00000000	Timer1 control MMR.
0x032C	T1CLRI	1	W	0xXX	Timer1 interrupt clear register.
0x0330	T1CAP	4	R	0x00000000	Timer1 capture register.
0x0360	T2LD	2	R/W	0x0000	Timer2 load register.
0x0364	T2VAL	2	R	0xFFFF	Timer2 value register.
0x0368	T2CON	2	R/W	0x0000	Timer2 control MMR.
0x036C	T2CLRI	1	W	0xXX	Timer2 interrupt clear register.

[1] N/A means not applicable.

Table 13. PLL/PSM Base Address = 0xFFFF0400

Address	Name	Byte	Access Type	Default Value[1]	Description
0x0404	POWKEY1	2	W	0xXXXX	POWCON0 prewrite key.
0x0408	POWCON0	1	R/W	0x00	Power control and core speed control register.
0x040C	POWKEY2	2	W	0xXXXX	POWCON0 postwrite key.
0x0410	PLLKEY1	2	W	0xXXXX	PLLCON prewrite key.
0x0414	PLLCON	1	R/W	0x21	PLL clock source selection MMR.
0x0418	PLLKEY2	2	W	0xXXXX	PLLCON postwrite key.
0x0434	POWKEY3	2	W	0xXXXX	POWCON1 prewrite key.
0x0438	POWCON1	2	R/W	0x0004	Power control and core speed control register.
0x043C	POWKEY4	2	W	0xXXXX	POWCON1 postwrite key.
0x0440	PSMCON	2	R/W	0x0008	Power supply monitor control register.
0x0444	CMPCON	2	R/W	0x0000	Comparator control register.

[1] N/A means not applicable.

Table 14. Reference Base Address = 0xFFFF0480

Address: 0x048C

Name: REFCON

Byte: 1

Access type: Read/write

Default value: 0x00

Description: Reference control register.

Table 15. ADC Address Base = 0xFFFF0500

Address	Name	Byte	Access Type	Default Value	Description
0x0500	ADCCON	2	R/W	0x0600	ADC control MMR.
0x0504	ADCCP	1	R/W	0x00	ADC positive channel selection register.
0x0508	ADCCN	1	R/W	0x01	ADC negative channel selection register.
0x050C	ADCSTA	1	R	0x00	ADC status MMR.
0x0510	ADCDAT	4	R	0x00000000	ADC data output MMR.
0x0514	ADCRST	1	R/W	0x00	ADC reset MMR.

Address	Name	Byte	Access Type	Default Value	Description
0x0914	I2C1MCNT1	1	R	0x00	I^2C1 master current read count register. This register contains the number of bytes already received during a read from slave sequence.
0x0918	I2C1ADR0	1	R/W	0x00	I^2C1 address byte register. Write the required slave address in here prior to communications.
0x091C	I2C1ADR1	1	R/W	0x00	I^2C1 address byte register. Write the required slave address in here prior to communications. Used in 10-bit mode only.
0x0924	I2C1DIV	2	R/W	0x1F1F	I^2C1 clock control register. Used to configure the SCL frequency.
0x0928	I2C1SCON	2	R/W	0x0000	I^2C1 slave control register.
0x092C	I2C1SSTA	2	R/W	0x0000	I^2C1 slave status register.
0x0930	I2C1SRX	1	R	0x00	I^2C1 slave receive register.
0x0934	I2C1STX	1	W	0x00	I^2C1 slave transmit register.
0x0938	I2C1ALT	1	R/W	0x00	I^2C1 hardware general call recognition register.
0x093C	I2C1ID0	1	R/W	0x00	I^2C1 slave ID0 register. Slave bus ID register.
0x0940	I2C1ID1	1	R/W	0x00	I^2C1 slave ID1 register. Slave bus ID register.
0x0944	I2C1ID2	1	R/W	0x00	I^2C1 slave ID2 register. Slave bus ID register.
0x0948	I2C1ID3	1	R/W	0x00	I^2C1 slave ID3 register. Slave bus ID register.
0x094C	I2C1FSTA	2	R/W	0x0000	I^2C1 FIFO status register. Used in both master and slave modes.

Table 19. SPI Base Address = 0xFFFF0A00

Address	Name	Byte	Access Type	Default Value	Description
0x0A00	SPISTA	2	R	0x0000	SPI status MMR.
0x0A04	SPIRX	1	R	0x00	SPI receive MMR.
0x0A08	SPITX	1	W	0xXX	SPI transmit MMR.
0x0A0C	SPIDIV	1	R/W	0x00	SPI baud rate select MMR.
0x0A10	SPICON	2	R/W	0x0000	SPI control MMR.

Table 20. PLA Base Address = 0XFFFF0B00

Address	Name	Byte	Access Type	Default Value	Description
0x0B00	PLAELM0	2	R/W	0x0000	PLA Element 0 control register.
0x0B04	PLAELM1	2	R/W	0x0000	PLA Element 1 control register.
0x0B08	PLAELM2	2	R/W	0x0000	PLA Element 2 control register.
0x0B0C	PLAELM3	2	R/W	0x0000	PLA Element 3 control register.
0x0B10	PLAELM4	2	R/W	0x0000	PLA Element 4 control register.
0x0B14	PLAELM5	2	R/W	0x0000	PLA Element 5 control register.
0x0B18	PLAELM6	2	R/W	0x0000	PLA Element 6 control register.
0x0B1C	PLAELM7	2	R/W	0x0000	PLA Element 7 control register.
0x0B20	PLAELM8	2	R/W	0x0000	PLA Element 8 control register.
0x0B24	PLAELM9	2	R/W	0x0000	PLA Element 9 control register.
0x0B28	PLAELM10	2	R/W	0x0000	PLA Element 10 control register.
0x0B2C	PLAELM11	2	R/W	0x0000	PLA Element 11 control register.
0x0B30	PLAELM12	2	R/W	0x0000	PLA Element 12 control register.
0x0B34	PLAELM13	2	R/W	0x0000	PLA Element 13 control register.
0x0B38	PLAELM14	2	R/W	0x0000	PLA Element 14 control register.
0x0B3C	PLAELM15	2	R/W	0x0000	PLA Element 15 control register.
0x0B40	PLACLK	1	R/W	0x00	PLA clock select register.
0x0B44	PLAIRQ	4	R/W	0x00000000	PLA interrupt control register.
0x0B48	PLAADC	4	R/W	0x00000000	PLA ADC trigger control register.
0x0B4C	PLADIN	4	R/W	0x00000000	PLA data in register.
0x0B50	PLADOUT	4	R	0x00000000	PLA data out register.
0x0B54	PLALCK	1	W	0x00	PLA lock register.

TYPICAL OPERATION

When configured via the ADC control and channel selection registers, the ADC converts the analog input and provides a 12-bit result in the ADC data register.

The top four bits are the sign bits. The 12-bit result is placed from Bit 16 to Bit 27 as shown in Figure 22. Note that in fully differential mode, the result is represented in twos complement format. In single-ended mode, the result is represented in straight binary format.

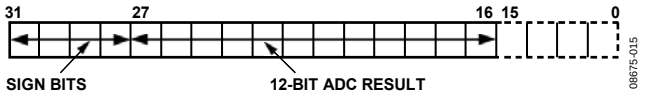

Figure 22. ADC Result Format

The same format is used in DACxDAT, simplifying the software.

Current Consumption

The ADC in standby mode, that is, powered up but not converting, typically consumes 640 μA. The internal reference adds 140 μA. During conversion, the extra current is 0.3 μA multiplied by the sampling frequency (in kHz).

Timing

Figure 23 gives details of the ADC timing. Users control the ADC clock speed and the number of acquisition clocks in the ADCCON MMR. By default, the acquisition time is eight clocks, and the clock divider is two. The number of extra clocks (such as bit trial or write) is set to 19, which gives a sampling rate of 774 kSPS. For conversion on the temperature sensor, set ADCCON = 0x37A3. When using multiple channels including the temperature sensor, the timing settings revert to the user-defined settings after reading the temperature sensor channel.

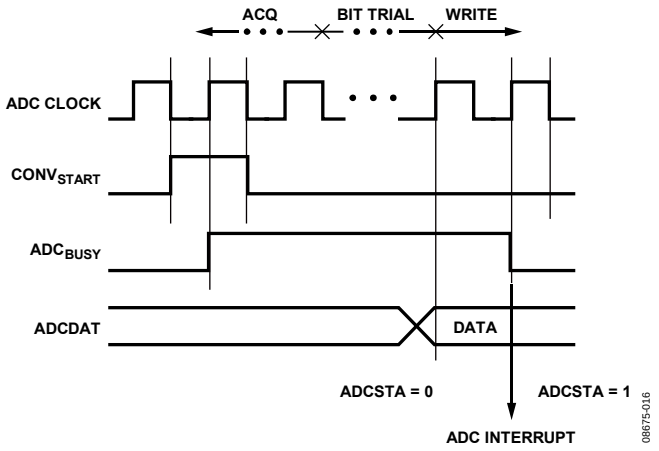

Figure 23. ADC Timing

MMR INTERFACE

The ADC is controlled and configured via the eight MMRs described in this section.

ADCCON Register

Name: ADCCON

Address: 0xFFFF0500

Default value: 0x0600

Access: Read/write

Function: ADCCON is an ADC control register that allows the programmer to enable the ADC peripheral, select the mode of operation of the ADC (either in single-ended mode or fully differential mode), and select the conversion type. This MMR is described in Table 24.

Table 24. ADCCON MMR Bit Designations

Bit	Value	Description
15 to 14		Reserved.
13		Temperature sensor conversion enable. Set to 1 for temperature sensor conversions and single software conversions. Set to 0 for normal ADC conversions.
12 to 10		ADC clock speed.
	000	f_{ADC}/1. This divider is provided to obtain 1 MSPS ADC with an external clock <41.78 MHz.
	001	f_{ADC}/2 (default value).
	010	f_{ADC}/4.
	011	f_{ADC}/8.
	100	f_{ADC}/16.
	101	f_{ADC}/32.
9 to 8		ADC acquisition time.
	00	2 clocks.
	01	4 clocks.
	10	8 clocks (default value).
	11	16 clocks.

ADCCN Register

Name: ADCCN

Address: 0xFFFF0508

Default value: 0x01

Access: Read/write

Function: ADCCN is an ADC negative channel selection register. This MMR is described in Table 26.

Table 26. ADCCN MMR Bit Designation

Bit	Value	Description
7 to 5		Reserved.
4 to 0		Negative channel selection bits.
	00000	ADC0.
	00001	ADC1.
	00010	ADC2.
	00011	ADC3.
	00100	ADC4.
	00101	ADC5.
	00110	ADC6.
	00111	ADC7.
	01000	ADC8.
	01001	ADC9.
	01010	ADC10.
	01011	Reserved
	01100	ADC12.
	01101	Reserved
	01110	Reserved
	01111	DAC1.
	10000	Temperature sensor.
	10001	AGND (self-diagnostic feature).
	10010	Internal reference (self-diagnostic feature).
	10011	Reserved
	Others	Reserved.

ADCSTA Register

Name: ADCSTA

Address: 0xFFFF050C

Default Value: 0x00

Access: Read

Function: ADCSTA is an ADC status register that indicates when an ADC conversion result is ready. The ADCSTA register contains only one bit, ADCReady (Bit 0), representing the status of the ADC. This bit is set at the end of an ADC conversion, generating an ADC interrupt. It is cleared automatically by reading the ADCDAT MMR. When the ADC is performing a conversion, the status of the ADC can be read externally via the ADC_{BUSY} pin. This pin is high during a conversion. When the conversion is finished, ADC_{BUSY} goes back low. This information can be available on P0.0 (see the General-Purpose Input/Output section) if enabled in the ADCCON register.

ADCDAT Register

Name: ADCDAT

Address: 0xFFFF0510

Default value: 0x00000000

Access: Read

Function: ADCDAT is an ADC data result register. Hold the 12-bit ADC result as shown in Figure 22.

ADCRST Register

Name: ADCRST

Address: 0xFFFF0514

Default Value: 0x00

Access: Read/write

Function: ADCRST resets the digital interface of the ADC. Writing any value to this register resets all the ADC registers to their default value.

The C1 capacitors in Figure 27 are typically 4 pF and can be primarily attributed to pin capacitance. The resistors are lumped components made up of the on resistance of the switches. The value of these resistors is typically about 100 Ω. The C2 capacitors are the ADC sampling capacitors and typically have a capacitance of 16 pF.

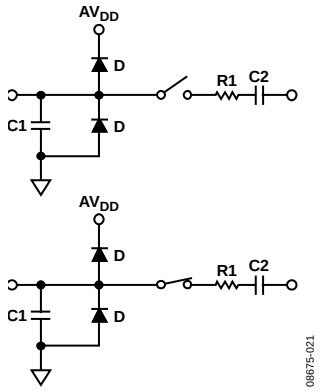

Figure 27. Equivalent Analog Input Circuit Conversion Phase: Switches Open, Track Phase: Switches Closed

For ac applications, removing high frequency components from the analog input signal is recommended by using an RC low-pass filter on the relevant analog input pins. In applications where harmonic distortion and signal-to-noise ratio are critical, the analog input should be driven from a low impedance source. Large source impedances significantly affect the ac performance of the ADC. This can necessitate the use of an input buffer amplifier. The choice of the op amp is a function of the particular application. Figure 28 and Figure 29 give an example of an ADC front end.

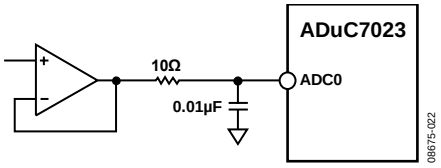

Figure 28. Buffering Single-Ended Differential Input

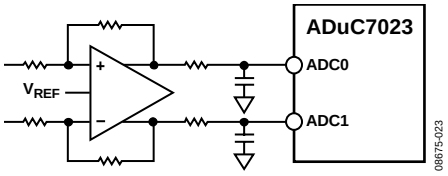

Figure 29. Buffering Differential Inputs

When no amplifier is used to drive the analog input, limit the source impedance to values lower than 1 kΩ. The maximum source impedance depends on the amount of total harmonic distortion (THD) that can be tolerated. The THD increases as the source impedance increases and the performance degrades.

DRIVING THE ANALOG INPUTS

Internal or external references can be used for the ADC. When operating in differential mode, there are restrictions on the common-mode input signal (V_{CM}), which is dependent upon the reference value and supply voltage used to ensure that the signal remains within the supply rails. Table 27 gives some calculated V_{CM} minimum and V_{CM} maximum values.

Table 27. V_{CM} Ranges

AV_{DD}	V_{REF}	V_{CM} Min	V_{CM} Max	Signal Peak-to-Peak
3.3 V	2.5 V	1.25 V	2.05 V	2.5 V
	2.048 V	1.024 V	2.276 V	2.048 V
	1.25 V	0.75 V	2.55 V	1.25 V
3.0 V	2.5 V	1.25 V	1.75 V	2.5 V
	2.048 V	1.024 V	1.976 V	2.048 V
	1.25 V	0.75 V	2.25 V	1.25 V

CALIBRATION

By default, the factory-set values written to the ADC offset (ADCOF) and gain coefficient registers (ADCGN) yield optimum performance in terms of endpoint errors and linearity for standalone operation of the part (see the Specifications section). If system calibration is required, it is possible to modify the default offset and gain coefficients to improve endpoint errors, but note that any modification to the factory-set ADCOF and ADCGN values can degrade ADC linearity performance.

For system offset error correction, the ADC channel input stage must be tied to AGND. A continuous software ADC conversion loop must be implemented by modifying the value in ADCOF until the ADC result (ADCDAT) reads Code 0 to Code 1. If the ADCDAT value is greater than 1, ADCOF should be decremented until ADCDAT reads Code 0 to Code 1. Offset error correction is done digitally and has a resolution of 0.25 LSB and a range of ±3.125% of V_{REF}.

For system gain error correction, the ADC channel input stage must be tied to V_{REF}. A continuous software ADC conversion loop must be implemented to modify the value in ADCGN until the ADCDAT reads Code 4094 to Code 4095. If the ADCDAT value is less than 4094, ADCGN should be incremented until ADCDAT reads Code 4094 to Code 4095. Similar to the offset calibration, the gain calibration resolution is 0.25 LSB with a range of ±3% of V_{REF}.

TEMPERATURE SENSOR

The ADuC7023 provides a voltage output from an on-chip band gap reference that is proportional to absolute temperature. This voltage output can also be routed through the front-end ADC multiplexer (effectively an additional ADC channel input), facilitating an internal temperature sensor channel, measuring die temperature.

An ADC temperature sensor conversion differs from a standard ADC voltage. The ADC performance specifications do not apply to the temperature sensor.

Chopping of the internal amplifier should be enabled using the TSCON register. To enable this mode, the user must set Bit 0 of TSCON. The user must also take two consecutive ADC readings and average them in this mode.

SECURITY

The 62 kB of Flash/EE memory available to the user can be read and write protected.

Bit 31 of the FEEPRO/FEEHIDE MMR (see Table 34) protects the 62 kB from being read through JTAG programming mode. The other 31 bits of this register protect writing to the flash memory. Each bit protects four pages, that is, 2 kB. Write protection is activated for all types of access.

Three Levels of Protection

Protection can be set and removed by writing directly into FEEHIDE MMR. This protection does not remain after reset.

Protection can be set by writing into FEEPRO MMR. It only takes effect after a save protection command (0x0C) and a reset. The FEEPRO MMR is protected by a key to avoid direct access. The key is saved once and must be entered again to modify FEEPRO. A mass erase sets the key back to 0xFFFF but also erases all the user code.

Flash can be permanently protected by using the FEEPRO MMR and a particular value of key: 0xDEADDEAD. Entering the key again to modify the FEEPRO register is not allowed.

Sequence to Write the Key

1. Write the bit in FEEPRO corresponding to the page to be protected.
2. Enable key protection by setting Bit 6 of FEEMOD (Bit 5 must equal 0).
3. Write a 32-bit key in FEEADR, FEEDAT.
4. Run the write key command 0x0C in FEECON; wait for the read to be successful by monitoring FEESTA.
5. Reset the part.

To remove or modify the protection, the same sequence is used with a modified value of FEEPRO. If the key chosen is the value 0xDEAD, the memory protection cannot be removed. Only a mass erase unprotects the part, but it also erases all user code.

The sequence to write the key is illustrated in the following example (this protects writing Page 4 to Page 7 of the Flash):

```
FEEPRO=0xFFFFFFFD;  //Protect Page 4 to
                     Page 7
FEEMOD=0x48; //Write key enable
FEEADR=0x1234;      //16 bit key value
FEEDAT=0x5678;      //16 bit key value
FEECON= 0x0C;       //Write key command
```

Follow the same sequence to protect the part permanently with FEEADR = 0xDEAD and FEEDAT = 0xDEAD.

FLASH/EE CONTROL INTERFACE

Serial and JTAG programming use the Flash/EE control interface, which includes the eight MMRs outlined in this section.

FEESTA Register

Name: FEESTA

Address: 0xFFFFF800

Default value: 0x20

Access: Read

Function: FEESTA is a read-only register that reflects the status of the flash control interface as described in Table 31.

Table 31. FEESTA MMR Bit Designations

Bit	Description
7 to 6	Reserved.
5	Reserved.
4	Reserved.
3	Flash interrupt status bit. This bit is set automatically when an interrupt occurs, that is, when a command is complete and the Flash/EE interrupt enable bit in the FEEMOD register is set. This bit is cleared when reading FEESTA register.
2	Flash/EE controller busy. This bit is set automatically when the controller is busy. This bit is cleared automatically when the controller is not busy.
1	Command fail. This bit is set automatically when a command is not completed. This bit is cleared automatically when reading FEESTA register.
0	Command pass. This bit is set by the MicroConverter when a command is completed. This bit is cleared automatically when reading the FEESTA register.

Table 38. RSTCFG MMR Bit Designations

Bit	Description
7 to 3	Reserved. Always set to 0.
2	This bit is set to 1 to configure the DAC outputs to retain their state after a watchdog or software reset. This bit is cleared for the DAC pins and registers to return to their default state.
1	Reserved. Always set to 0.
0	This bit is set to 1 to configure the GPIO pins to retain their state after a watchdog or software reset. This bit is cleared for the GPIO pins and registers to return to their default state.

RSTKEY1 Register

Name: RSTKEY1

Address: 0xFFFF0248

Default value: 0xXX

Access Write

RSTKEY2Register

Name: RSTKEY2

Address: 0xFFFF0250

Default value: 0xXX

Access: Write

Table 39. RSTCFG Write Sequence

Name	Code
RSTKEY1	0x76
RSTCFG	User value
RSTKEY2	0xB1

DACBKEY0 Register

Name: DACBKEY0

Address: 0xFFFF0650

Default value: 0x0000

Access: Write

DACBKEY1 Register

Name: DACBKEY1

Address: 0xFFFF0658

Default value: 0x0000

Access: Write

Table 44. DACBCFG Write Sequence

Name	Code
DACBKEY0	0x9A
DACBCFG	User value
DACBKEY1	0x0C

POWER SUPPLY MONITOR

The power supply monitor regulates the IOV_{DD} supply on the ADuC7023. It indicates when the IOV_{DD} supply pin drops below a supply trip point. The monitor function is controlled via the PSMCON register. If enabled in the IRQEN or FIQEN register, the monitor interrupts the core using the PSMI bit in the PSMCON MMR. This bit is immediately cleared when CMP goes high.

This monitor function allows the user to save working registers to avoid possible data loss due to low supply or brownout conditions. It also ensures that normal code execution does not resume until a safe supply level has been established.

PSMCON Register

Name: PSMCON

Address: 0xFFFF0440

Default value: 0x0008

Access: Read/write

Table 45. PSMCON MMR Bit Descriptions

Bit	Name	Description
3	CMP	Comparator bit. This is a read-only bit that directly reflects the state of the comparator. Read 1 indicates the IOV_{DD} supply is above its selected trip point, or the PSM is in power-down mode. Read 0 indicates the IOV_{DD} supply is below its selected trip point. This bit should be set before leaving the interrupt service routine.
2	TP	Trip point selection bits. 0 = 2.79 V. 1 = reserved.
1	PSMEN	Power supply monitor enable bit. This bit is set to 1 to enable the power supply monitor circuit. This bit is cleared to 0 to disable the power supply monitor circuit.
0	PSMI	Power supply monitor interrupt bit. This bit is set high by the MicroConverter once CMP goes low, indicating low I/O supply. The PSMI bit can be used to interrupt the processor. Once CMP returns high, the PSMI bit can be cleared by writing a 1 to this location. A 0 write has no effect. There is no timeout delay; PSMI can be immediately cleared once CMP goes high.

COMPARATOR

The ADuC7023 integrates voltage comparators. The positive input is multiplexed with ADC2, and the negative input has two options: ADC3 or DAC0. The output of the comparator can be configured to generate a system interrupt, be routed directly to the programmable logic array, start an ADC conversion, or be on an external pin, $COMP_{OUT}$, as shown in Figure 34.

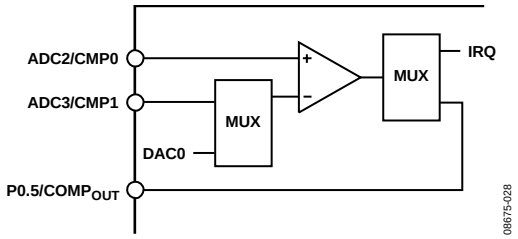

Figure 34. Comparator

Hysteresis

Figure 35 shows how the input offset voltage and hysteresis terms are defined. Input offset voltage (V_{OS}) is the difference between the center of the hysteresis range and the ground level. This can either be positive or negative. The hysteresis voltage (V_H) is ½ the width of the hysteresis range.

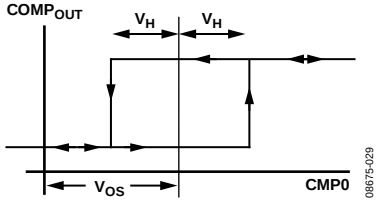

Figure 35. Comparator Hysteresis Transfer Function

Table 62. GPxCLR MMR Bit Descriptions

Bit	Description
31 to 24	Reserved.
23 to 16	Data port x clear bit. This bit is set to 1 by the user to clear the bit on Port x; this bit also clears the corresponding bit in the GPxDAT MMR. This bit is cleared to 0 by the user; this bit does not affect the data out.
15 to 0	Reserved.

SERIAL PERIPHERAL INTERFACE

The ADuC7023 integrates a complete hardware serial peripheral interface (SPI) on chip. SPI is an industry standard, synchronous serial interface that allows eight bits of data to be synchronously transmitted and simultaneously received, that is, full duplex up to a maximum bit rate of 20 Mbps.

The SPI port can be configured for master or slave operation and typically consists of four pins: MISO, MOSI, SCLK, and SPI$\overline{SS}$.

MISO (Master In, Slave Out) Pin

The MISO pin is configured as an input line in master mode and an output line in slave mode. The MISO line on the master (data in) should be connected to the MISO line in the slave device (data out). The data is transferred as byte wide (8-bit) serial data, MSB first.

MOSI (Master Out, Slave In) Pin

The MOSI pin is configured as an output line in master mode and an input line in slave mode. The MOSI line on the master (data out) should be connected to the MOSI line in the slave device (data in). The data is transferred as byte wide (8-bit) serial data, MSB first.

SCLK (Serial Clock I/O) Pin

The master serial clock (SCLK) synchronizes the data being transmitted and received through the MOSI SCLK period. Therefore, a byte is transmitted/received after eight SCLK periods. The SCLK pin is configured as an output in master mode and as an input in slave mode.

In master mode, polarity and phase of the clock are controlled by the SPICON register, and the bit rate is defined in the SPIDIV register as follows:

$$f_{SERIAL\ CLOCK} = \frac{f_{UCLK}}{2 \times (1 + SPIDIV)}$$

where:

f_{UCLK} is the clock selected by POWCON1 Bit 7 to Bit 6.

The maximum speed of the SPI clock is independent on the clock divider bits.

In slave mode, the SPICON register must be configured with the phase and polarity of the expected input clock. The slave accepts data from an external master up to 10 Mbps.

In both master and slave modes, data is transmitted on one edge of the SCLK signal and sampled on the other. Therefore, it is important that the polarity and phase are configured the same for the master and slave devices.

SPI Chip Select ($\overline{SS}$ Input) Pin

In SPI slave mode, a transfer is initiated by the assertion of $\overline{SS}$, which is an active low input signal. The SPI port then transmits and receives 8-bit data until the transfer is concluded by deassertion of $\overline{SS}$. In slave mode, $\overline{SS}$ is always an input.

In SPI master mode, the $\overline{SS}$ is an active low output signal. It asserts itself automatically at the beginning of a transfer and deasserts itself upon completion.

Configuring External Pins for SPI Functionality

P1.1 is the slave chip select pin. In slave mode, this pin is an input and must be driven low by the master. In master mode, this pin is an output and goes low at the beginning of a transfer and high at the end of a transfer.

P1.0 is the SCLK pin.

P0.6 is the master in, slave out (MISO) pin.

P0.7 is the master out, slave in (MOSI) pin.

To configure these pins for SPI mode, see the General-Purpose Input/Output section.

SPI Registers

The following MMR registers control the SPI interface: SPISTA, SPIRX, SPITX, SPIDIV, and SPICON.

SPI Status Register

Name: SPISTA

Address: 0xFFFF0A00

Default value: 0x0000

Access: Read

Function: This 32-bit MMR contains the status of the SPI interface in both master and slave modes.

Table 63. SPISTA MMR Bit Designations

Bit	Name	Description
15 to 12		Reserved bits.
11	SPIREX	SPI Rx FIFO excess bytes present. This bit is set when there are more bytes in the Rx FIFO than indicated in the SPIMDE bits in SPICON. This bit is cleared when the number of bytes in the FIFO is equal or less than the number in SPIMDE.
10 to 8	SPIRXFSTA[2:0]	SPI Rx FIFO status bits. [000] = Rx FIFO is empty. [001] = 1 valid byte in the FIFO. [010] = 2 valid byte in the FIFO. [011] = 3 valid byte in the FIFO. [100] = 4 valid byte in the FIFO.
7	SPIFOF	SPI Rx FIFO overflow status bit. This bit is set when the Rx FIFO is full when new data is loaded to the FIFO. This bit generates an interrupt except when SPIRFLH is set in SPICON. This bit is cleared when the SPISTA register is read.
6	SPIRXIRQ	SPI Rx IRQ status bit. This bit is set when a receive interrupt occurs. This bit is set when SPITMDE in SPICON is cleared and the required number of bytes have been received. This bit is cleared when the SPISTA register is read.
5	SPITXIRQ	SPI Tx IRQ status bit. This bit is set when a transmit interrupt occurs. This bit is set when SPITMDE in SPICON is set and the required number of bytes have been transmitted. This bit is cleared when the SPISTA register is read.
4	SPITXUF	SPI Tx FIFO underflow. This bit is set when a transmit is initiated without any valid data in the Tx FIFO. This bit generates an interrupt except when SPITFLH is set in SPICON. This bit is cleared when the SPISTA register is read.
3 to 1	SPITXFSTA[2:0]	SPI Tx FIFO status bits. [000] = Tx FIFO is empty. [001] = 1 valid byte in the FIFO. [010] = 2 valid byte in the FIFO. [011] = 3 valid byte in the FIFO. [100] = 4 valid byte in the FIFO.
0	SPIISTA	SPI interrupt status bit. This bit is set to 1 when an SPI based interrupt occurs. This bit is cleared after reading SPISTA.

SPIRX Register

Name: SPIRX

Address: 0xFFFF0A04

Default value: 0x00

Access: Read

Function: This 8-bit MMR is the SPI receive register.

SPITX Register

Name: SPITX

Address: 0xFFFF0A08

Default value: 0xXX

Access: Write

Function: This 8-bit MMR is the SPI transmit register.

SPIDIV Register

Name:	SPIDIV
Address:	0xFFFF0A0C
Default value:	0x00
Access:	Read/write
Function:	This 6-bit MMR is the SPI baud rate selection register. (Note that the maximum value of this MMR is 0x3F.)

SPI Control Register

Name:	SPICON
Address:	0xFFFF0A10
Default value:	0x0000
Access:	Read/write
Function:	This 16-bit MMR configures the SPI peripheral in both master and slave modes.

Table 73. I2CxSSTA MMR Bit Designations

Bit	Name	Description
15		Reserved bit.
14	I2CSTA	This bit is set to 1 if: A start condition followed by a matching address is detected. It is also set if a start byte (0x01) is received. If general calls are enabled and a general call code of (0x00) is received. This bit is cleared on receiving a stop condition.
13	I2CREPS	This bit is set to 1 if a repeated start condition is detected. This bit is cleared on receiving a stop condition. A read of the I2CxSSTA register also clears this bit.
12 to 11	I2CID[1:0]	I^2C address matching register. These bits indicate which I2CxIDx register matches the received address. [00] = received address matches I2CxID0. [01] = received address matches I2CxID1. [10] = received address matches I2CxID2. [11] = received address matches I2CxID3.
10	I2CSS	I^2C stop condition after start detected bit. This bit is set to 1 when a stop condition is detected after a previous start and matching address. When the I2CSSENI bit in I2CxSCON is set, an interrupt is generated. This bit is cleared by reading this register.
9 to 8	I2CGCID[1:0]	I^2C general call ID bits. [00] = no general call received. [01] = general call reset and program address. [10] = general program address. [11] = general call matching alternative ID. These bits are not cleared by a general call reset command. These bits are cleared by writing a 1 to the I2CGCCLR bit in I2CxSCON.
7	I2CGC	I^2C general call status bit. This bit is set to 1 if the slave receives a general call command of any type. If the command received is a reset command, then all registers return to their default state. If the command received is a hardware general call, the Rx FIFO holds the second byte of the command, and this can be compared with the I2CxALT register. This bit is cleared by writing a 1 to the I2CGCCLR bit in I2CxSCON.
6	I2CSBUSY	I^2C slave busy status bit. This bit is set to 1 when the slave receives a start condition. This bit is cleared by hardware if the received address does not match any of the I2CxIDx registers, the slave device receives a stop condition or if a repeated start address does not match any of the I2CxIDx registers.
5	I2CSNA	I^2C slave no acknowledge data bit. This bit is set to 1 when the slave responds to a bus address with a no acknowledge. This bit is asserted under the following conditions: if no acknowledge is returned because there is no data in the Tx FIFO or if the I2CNACKEN bit is set in the I2CxSCON register. This bit is cleared in all other conditions.
4	I2CSRxFO	Slave Rx FIFO overflow. This bit is set to 1 when a byte is written to the Rx FIFO when it is already full. This bit is cleared in all other conditions.
3	I2CSRXQ	I^2C slave receive request bit. This bit is set to 1 when the slave Rx FIFO is not empty. This bit causes an interrupt to occur if the I2CSRXENI bit in I2CxSCON is set. The Rx FIFO must be read or flushed to clear this bit.
2	I2CSTXQ	I^2C slave transmit request bit. This bit is set to 1 when the slave receives a matching address followed by a read. If the I2CSETEN bit in I2CxSCON is = 0, this bit goes high just after the negative edge of SCL during the read bit transmission. If the I2CSETEN bit in I2CxSCON is = 1, this bit goes high just after the positive edge of SCL during the read bit transmission. This bit causes an interrupt to occur if the I2CSTXENI bit in I2CxSCON is set. This bit is cleared in all other conditions.

PULSE-WIDTH MODULATOR

PULSE-WIDTH MODULATOR GENERAL OVERVIEW

The ADuC7023 integrates a 5-channel pulse-width modulator (PWM) interface. The PWM outputs can be configured to drive an H-bridge or can be used as standard PWM outputs. On power-up, the PWM outputs default to H-bridge mode. This ensures that the motor is turned off by default. In standard PWM mode, the outputs are arranged as three pairs of PWM pins. Users have control over the period of each pair of outputs and over the duty cycle of each individual output.

Table 84. PWM MMRs

MMR Name	Description
PWMCON1	PWM Control Register 1.
PWM0COM0	Compare Register 0 for PWM Output 0 and PWM Output 1.
PWM0COM1	Compare Register 1 for PWM Output 0 and PWM Output 1.
PWM0COM2	Compare Register 2 for PWM Output 0 and PWM Output 1.
PWM0LEN	Frequency control for PWM Output 0 and PWM Output 1.
PWM1COM0	Compare Register 0 for PWM Output 2 and PWM Output 3.
PWM1COM1	Compare Register 1 for PWM Output 2 and PWM Output 3.
PWM1COM2	Compare Register 2 for PWM Output 2 and PWM Output 3.
PWM1LEN	Frequency control for PWM Output 2 and PWM Output 3.
PWM2COM0	Compare Register 0 for PWM Output 4
PWM2COM1	Compare Register 1 for PWM Output 4
PWM2LEN	Frequency control for PWM Output 4.
PWMCLRI	PWM interrupt clear.

In all modes, the PWMxCOMx MMRs control the point at which the PWM outputs change state. An example of the first pair of PWM outputs (PWM0 and PWM1) is shown in Figure 40.

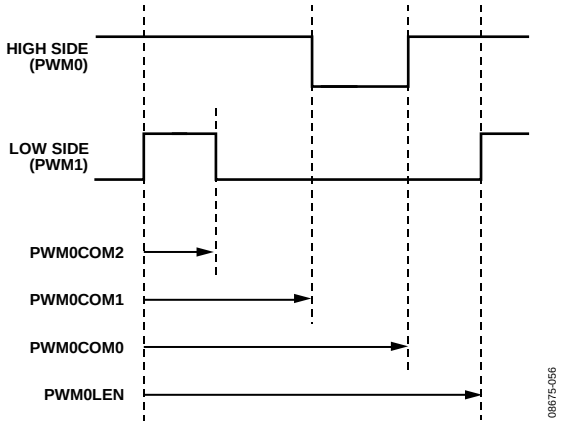

Figure 40. PWM Timing

The PWM clock is selectable via PWMCON1 with one of the following values: UCLK divided by 2, 4, 8, 16, 32, 64, 128, or 256. The length of a PWM period is defined by PWMxLEN.

The PWM waveforms are set by the count value of the 16-bit timer and the compare registers contents, as shown with the PWM0 and PWM1 waveforms in Figure 40.

The low-side waveform, PWM1, goes high when the timer count reaches PWM0LEN, and it goes low when the timer count reaches the value held in PWM0COM2 or when the high-side waveform (PWM0) goes low.

The high-side waveform, PWM0, goes high when the timer count reaches the value held in PWM0COM0, and it goes low when the timer count reaches the value held in PWM0COM1.

PWMCON1 Control Register

Name: PWMCON1

Address: 0xFFFF0F80

Default value: 0x0012

Access: Read and write

Function: This is a 16-bit MMR that configures the PWM outputs.

PWM2COM0 Compare Register

Name: PWM2COM0

Address: 0xFFFF0FA4

Default value: 0x0000

Access: Read/write

Function: PWM4 output pin goes high when the PWM timer reaches the count value stored in this register.

PWM2COM1 Compare Register

Name: PWM2COM1

Address: 0xFFFF0FA8

Default value: 0x0000

Access: Read/write

Function: PWM4 output pin goes low when the PWM timer reaches the count value stored in this register.

PWM2LEN Register

Name: PWM2LEN

Address: 0xFFFF0FB0

Default value: 0x0000

Access: Read/write

Function: PWM2LEN defines the period of PWM4.

PWMCLRI Register

Name: PWMCLRI

Address: 0xFFFF0FB8

Default value: 0x0000

Access: Write

Function: Write any value to this register to clear a PWM interrupt source. This register must be written to before exiting a PWM interrupt service routine; otherwise, multiple interrupts occur.

PROCESSOR REFERENCE PERIPHERALS

INTERRUPT SYSTEM

There are 22 interrupt sources on the ADuC7023 that are controlled by the interrupt controller. Most interrupts are generated from the on-chip peripherals, such as ADC. Four additional interrupt sources are generated from external interrupt request pins, IRQ0, IRQ1, IRQ2, and IRQ3. The ARM7TDMI CPU core only recognizes interrupts as one of two types, a normal interrupt request IRQ or a fast interrupt request FIQ. All the interrupts can be masked separately.

The control and configuration of the interrupt system is managed through nine interrupt related registers, four dedicated to IRQ, and four dedicated to FIQ. An additional MMR is used to select the programmed interrupt source. The bits in each IRQ and FIQ registers represent the same interrupt source as described in Table 88.

The ADuC7023 contains a vectored interrupt controller (VIC) that supports nested interrupts up to eight levels. The VIC also allows the programmer to assign priority levels to all interrupt sources. Interrupt nesting is enabled by setting the ENIRQN bit in the IRQCONN register. A number of extra MMRs are used when the full-vectored interrupt controller is enabled.

IRQSTA/FIQSTA should be saved immediately upon entering the interrupt service routine (ISR) to ensure that all valid interrupt sources are serviced.

Table 88. IRQ/FIQ MMRs Bit Description

Bit	Description
0	All interrupts OR'ed (FIQ only).
1	SWI.
2	Timer0.
3	Timer1.
4	Watchdog timer (Timer 2).
5	Flash control.
6	ADC channel.
7	PLL lock.
8	I^2C0 master.
9	I^2C0 slave.
10	I^2C1 master.
11	I^2C1 slave.
12	SPI.
13	External IRQ0.
14	Comparator.
15	PSM.
16	External IRQ1.
17	PLA IRQ0.
18	External IRQ2.
19	External IRQ3.
20	PLA IRQ1.
21	PWM.

IRQ

The interrupt request (IRQ) is the exception signal to enter the IRQ mode of the processor. It is used to service general-purpose interrupt handling of internal and external events.

The four 32-bit registers dedicated to IRQ are: IRQSTA, IRQSIG, IRQEN, and IRQCLR.

IRQSTA Register

Name: IRQSTA

Address: 0xFFFF0000

Default value: 0x00000000

Access: Read

Function: IRQSTA (read-only register) provides the current-enabled IRQ source status. When set to 1, that source generates an active IRQ request to the ARM7TDMI core. There is no priority encoder or interrupt vector generation. This function is implemented in software in a common interrupt handler routine. All 32 bits are logically OR'ed to create the IRQ signal to the ARM7TDMI core.

IRQSIG Register

Name: IRQSIG

Address: 0xFFFF0004

Default value: 0x00XXX000

Access: Read

Function: IRQSIG reflects the status of the different IRQ sources. If a peripheral generates an IRQ signal, the corresponding bit in the IRQSIG is set; otherwise, it is cleared. The IRQSIG bits are cleared when the interrupt in the particular peripheral is cleared. All IRQ sources can be masked in the IRQEN MMR. IRQSIG is read-only.

POWER-ON RESET OPERATION

An internal power-on reset (POR) is implemented on the ADuC7023. For LV_{DD} below 2.40 V typical, the internal POR holds the part in reset. As LV_{DD} rises above 2.40 V, an internal timer times out for typically 64 ms before the part is released from reset. The user must ensure that the power supply IOV_{DD} has reached a stable 2.7 V minimum level by this time. Likewise, on power-down, the internal POR holds the part in reset until LV_{DD} has dropped below 2.40 V.

Figure 53 illustrates the operation of the internal POR in detail.

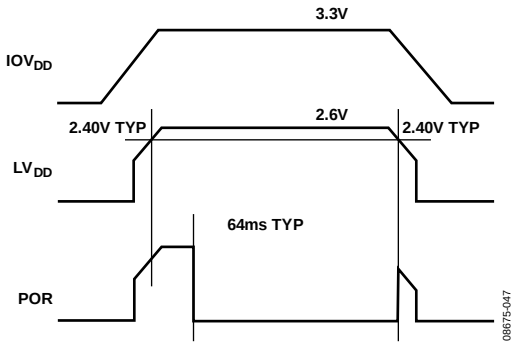

Figure 53. Internal Power-On Reset Operation

ORDERING GUIDE

Model[1]	ADC Channels	DAC Channels	FLASH/ RAM	GPIO	Downloader	Temperature Range	Package Description	Package Option	Ordering Quantity
ADuC7023BCP6Z62I	12	4	62 kB/8 kB	20	I^2C	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-10	490
ADuC7023BCP6Z62IRL	12	4	62 kB/8 kB	20	I^2C	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-10	2,500
ADuC7023BCP6Z62IR7	12	4	62 kB/8 kB	20	I^2C	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-10	750
ADuC7023BCPZ62I	6	4	62 kB/8 kB	12	I^2C	−40°C to +125°C	32-Lead LFCSP_WQ	CP-32-11	490
ADuC7023BCPZ62I-RL	6	4	62 kB/8 kB	12	I^2C	−40°C to +125°C	32-Lead LFCSP_WQ	CP-32-11	5,000
ADuC7023BCPZ62I-R7	6	4	62 kB/8 kB	12	I^2C	−40°C to +125°C	32-Lead LFCSP_WQ	CP-32-11	1,500
ADuC7023BCBZ62I-R7	10	4	62 kB/8 kB	16	I^2C	−40°C to +125°C	36-Ball WLCSP	CB-36-03	1,500
EVAL-ADuC7023QSPZ							ADuC7023 QuickStart Plus Development System Using 32-Pin ADuC7023		
EVAL-ADuC7023QSPZ1							ADuC7023 QuickStart Plus Development System Using 40-Pin ADuC7023		
EVAL-ADuC7023QSPZ2							ADuC7023 QuickStart Plus Development System Using 36-Ball ADuC7023		

[1] Z = RoHS Compliant Part.