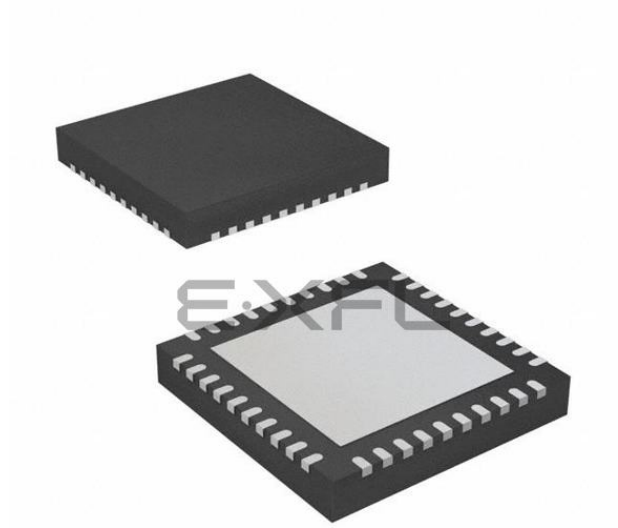

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Details	
Product Status	Active
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Core Size	16/32-Bit
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Connectivity	I²C, SPI
Peripherals	POR, PWM, WDT
Number of I/O	20
Program Memory Size	62KB (31K x16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 32
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 12x12b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	40-WFQFN Exposed Pad, CSP
Supplier Device Package	40-LFCSP-WQ (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc7023bcp6z62ir7

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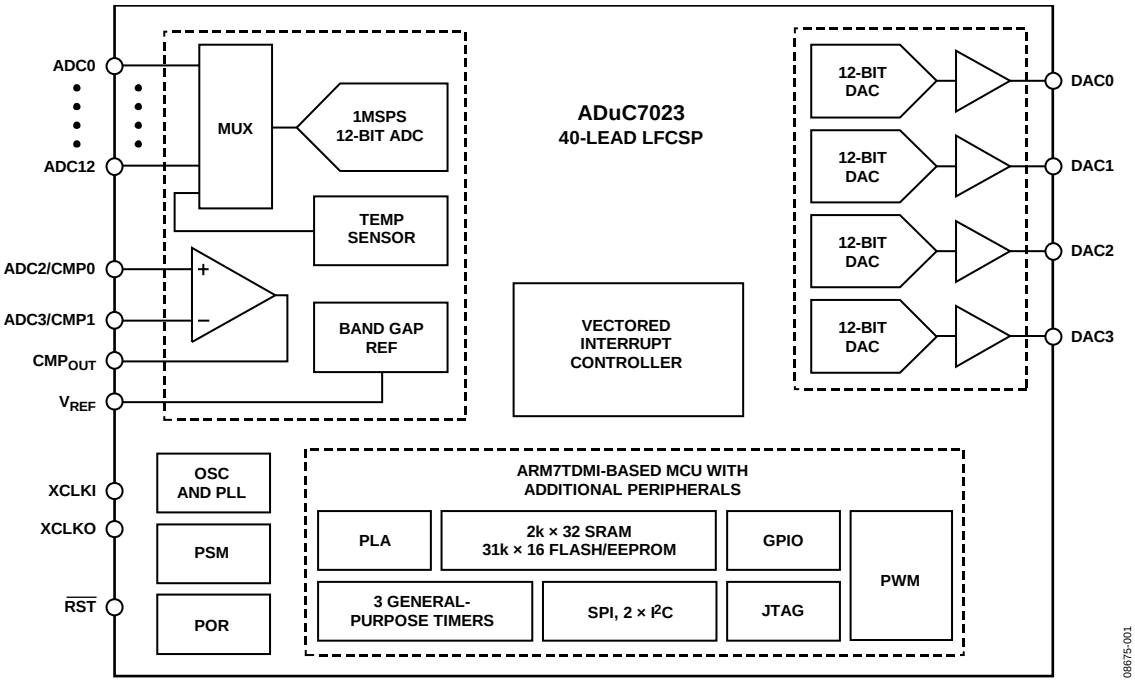


Figure 1.

SPECIFICATIONS

AV_{DD} = IOV_{DD} = 2.7 V to 3.6 V, V_{REF} = 2.5 V internal reference, f_{CORE} = 41.78 MHz, T_A = −40°C to +125°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ADC CHANNEL SPECIFICATIONS					Eight acquisition clocks and $f_{ADC}/2$
ADC Power-Up Time		5		µs	
DC Accuracy[1, 2]					
Resolution	12			Bits	
Integral Nonlinearity		±0.6	±1.5	LSB	2.5 V internal reference
		±1.0		LSB	1.0 V external reference
Differential Nonlinearity[3, 4]		±0.5	+1/−0.9	LSB	2.5 V internal reference
		+0.7/−0.6		LSB	1.0 V external reference
DC Code Distribution		1		LSB	ADC input is a dc voltage
ENDPOINT ERRORS[5]					
Offset Error		±1	±2	LSB	
Offset Error Match		±1		LSB	
Gain Error		±2		LSB	
Gain Error Match		±1		LSB	
DYNAMIC PERFORMANCE					f_{IN} = 10 kHz sine wave, f_{SAMPLE} = 1 MSPS
Signal-to-Noise Ratio (SNR)		69		dB	Includes distortion and noise components
Total Harmonic Distortion (THD)		−78		dB	
Peak Harmonic or Spurious Noise		−75		dB	
Channel-to-Channel Crosstalk		−80		dB	Measured on adjacent channels
ANALOG INPUT					
Input Voltage Ranges					
Differential Mode			$V_{CM} \pm V_{REF}/2$[6]	V	
Single-Ended Mode			0 to V_{REF}	V	
Leakage Current		±1	±6	µA	
Input Capacitance		20		pF	During ADC acquisition
ON-CHIP VOLTAGE REFERENCE					0.47 µF from V_{REF} to AGND
Output Voltage		2.5		V	
Accuracy			±4	mV	T_A = 25°C
Reference Temperature Coefficient		±15		ppm/°C	
Power Supply Rejection Ratio		75		dB	
Output Impedance		51		Ω	T_A = 25°C
Internal V_{REF} Power-On Time		1		ms	
EXTERNAL REFERENCE INPUT					
Input Voltage Range	0.625		AV_{DD}	V	
DAC CHANNEL SPECIFICATIONS					
DC Accuracy[7]					R_L = 5 kΩ, C_L = 100 pF
Resolution		12		Bits	
Relative Accuracy		±2		LSB	
Differential Nonlinearity			±1	LSB	Guaranteed monotonic
Offset Error			±15	mV	2.5 V internal reference
Gain Error[8]			±1	%	
Gain Error Mismatch		0.1		%	% of full scale on DAC0
DC Accuracy[9]					R_L = 1 kΩ, C_L = 100 pF
Resolution		12		Bits	
Relative Accuracy		±2.5		LSB	
Differential Nonlinearity		±1		LSB	Guaranteed monotonic
Offset Error		±15		mV	2.5 V internal reference
Gain Error[10]		±1		%	
Gain Error Mismatch		0.1		%	% of full scale on DAC0
ANALOG OUTPUTS					
Output Voltage Range 1		0 to 2.5		V	V_{REF} range: AGND to AV_{DD}
Output Voltage Range 2		0 to AV_{DD}		V	
Output Impedance		2		Ω	

Table 5. SPI Master Mode Timing (Phase Mode = 0)

Parameter	Description	Min	Typ	Max	Unit
t_{SL}	SCLK low pulse width[1]		(SPIDIV + 1) × t_{UCLK}		ns
t_{SH}	SCLK high pulse width[1]		(SPIDIV + 1) × t_{UCLK}		ns
t_{DAV}	Data output valid after SCLK edge			25	ns
t_{DOSU}	Data output setup before SCLK edge			75	ns
t_{DSU}	Data input setup time before SCLK edge[1]	1 × t_{UCLK}			ns
t_{DHD}	Data input hold time after SCLK edge[1]	2 × t_{UCLK}			ns
t_{DF}	Data output fall time		5	12.5	ns
t_{DR}	Data output rise time		5	12.5	ns
t_{SR}	SCLK rise time		5	12.5	ns
t_{SF}	SCLK fall time		5	12.5	ns

[1] t_{UCLK} = 23.9 ns. It corresponds to the 41.78 MHz internal clock from the PLL before the clock divider.

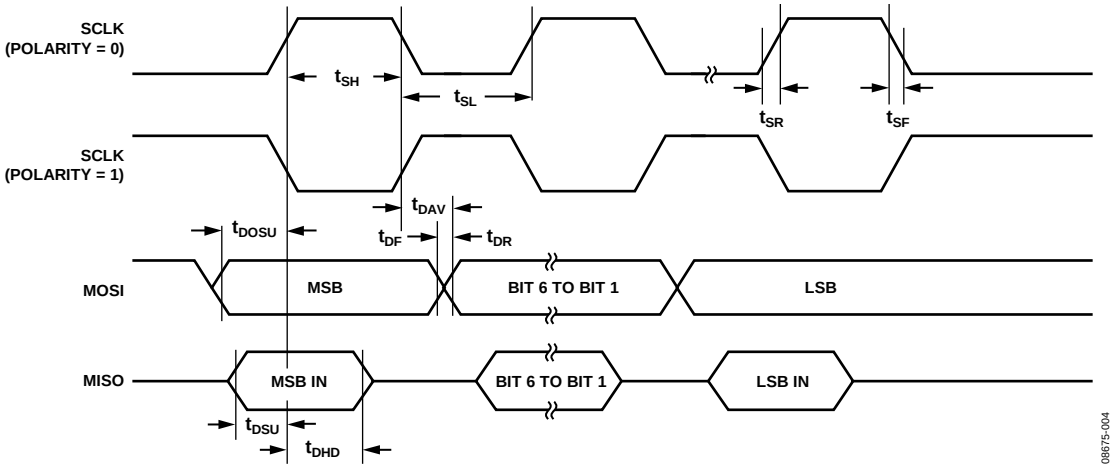


Figure 4. SPI Master Mode Timing (Phase Mode = 0)

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

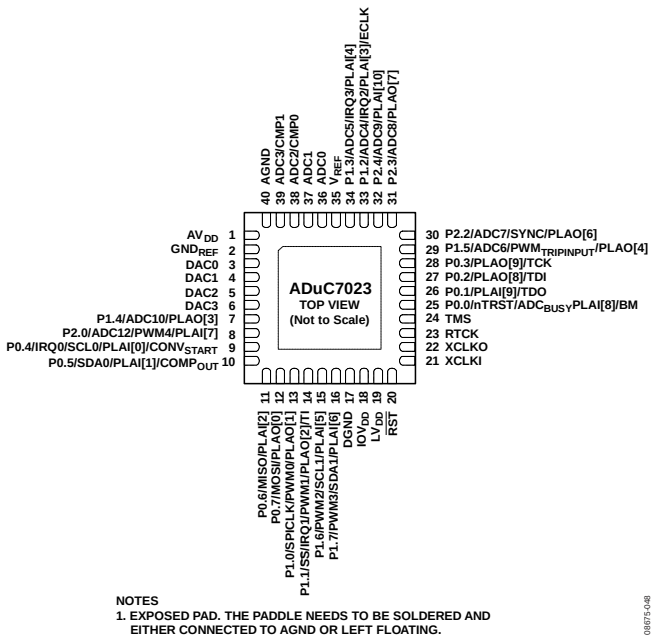


Figure 7. 40-Lead LFCSP Pin Configuration

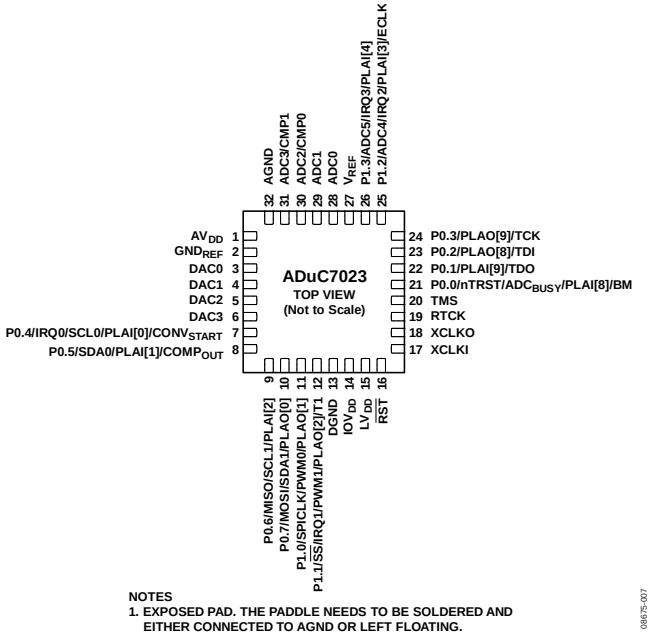


Figure 8. 32-Lead LFCSP Pin Configuration

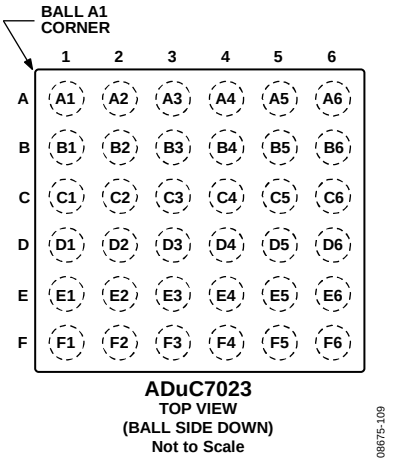


Figure 9. 36-Lead WLCSP Pin Configuration

Table 9. Pin Function Descriptions

Pin No.				
40-LFCSP	**32-LFCSP**	**36-WLCSP**	**Mnemonic**	**Description**
0	0	N/A	Exposed Paddle	Exposed Pad. The paddle needs to be soldered and either connected to AGND or left floating.
36	28	A4	ADC0	Single-Ended or Differential Analog Input 0.
37	29	B4	ADC1	Single-Ended or Differential Analog Input 1.
38	30	A5	ADC2/CMP0	Single-Ended or Differential Analog Input 2/Comparator Positive Input.
39	31	B5	ADC3/CMP1	Single-Ended or Differential Analog Input 3/Comparator Negative Input.
32	N/A	B2	P2.4/ADC9/PLAI[10]	General-Purpose Input and Output Port 2.4/ADC Single-Ended or Differential Analog Input/Programmable Logic Array Input Element 10. By default, this pin is configured as a digital input with a weak pull-up resistor enabled.

Pin No.				
40-LFCSP	32-LFCSP	36-WLCSP	Mnemonic	Description
34	26	A3	P1.3/ADC5/IRQ3/PLAI[4]	General-Purpose Input and Output Port 1.3/ADC Single-Ended or Differential Analog Input 5/External Interrupt Request 3/ Programmable Logic Array Input Element 4. By default, this pin is configured as a digital input with a weak pull-up resistor enabled. When used as ADC input, the pull-up resistor should be disabled manually.
33	25	A2	P1.2/ADC4/IRQ2/PLAI[3]/ECLK/	General-Purpose Input and Output Port 1.2/ADC Single-Ended or Differential Analog Input 4/External Interrupt Request 2/ Programmable Logic Array Input Element 3/Input-Output for External Clock. By default, this pin is configured as a digital input with a weak pull-up resistor enabled. When used as ADC input, the pull-up resistor should be disabled manually.
14	12	F4	P1.1/$\overline{SS}$/IRQ1/PWM1/PLAO[2]/T1	General-Purpose Input and Output Port 1.1/SPI Interface Slave Select (Active Low)/External Interrupt Request 1/PWM Output 1/ Programmable Logic Array Output Element 2/Timer 1 Input Clock. By default, this pin is configured as a digital input with a weak pull-up resistor enabled.
13	11	E4	P1.0/SCLK/PWM0/PLAO[1]	General-Purpose Input and Output Port 1.0/SPI Interface Clock Signal/ PWM Output 0/Programmable Logic Array Output Element 1. By default, this pin is configured as a digital input with a weak pull-up resistor enabled.
35	27	B3	V_{REF}	2.5 V Internal Voltage Reference. Must be connected to a 0.47 µF capacitor when using the internal reference.
40	32	A6	AGND	Analog Ground. Ground reference point for the analog circuitry.
1	1	B6	AV_{DD}	3.3 V Analog Power.

More information relative to the model of the programmer and the ARM7TDMI core architecture can be found in ARM7TDMI technical and ARM architecture manuals available directly from ARM Ltd.

INTERRUPT LATENCY

The worst-case latency for a fast interrupt request (FIQ) consists of the following: the longest time the request can take to pass through the synchronizer, the time for the longest instruction to complete (the longest instruction is an LDM) that loads all the registers including the PC, and the time for the data abort and FIQ entry.

At the end of this time, the ARM7TDMI executes the instruction at 0x1C (FIQ interrupt vector address). The maximum total time is 50 processor cycles, which is just under 1.2 μs in a system using a continuous 41.78 MHz processor clock.

The maximum interrupt request (IRQ) latency calculation is similar but must allow for the fact that FIQ has higher priority and could delay entry into the IRQ handling routine for an arbitrary length of time. This time can be reduced to 42 cycles if the LDM command is not used. Some compilers have an option to compile without using this command. Another option is to run the part in thumb mode where the time is reduced to 22 cycles.

The minimum latency for FIQ or IRQ interrupts is a total of five cycles, which consist of the shortest time the request can take through the synchronizer, plus the time to enter the exception mode.

The ARM7TDMI always runs in ARM (32-bit) mode when in privileged modes, for example, when executing interrupt service routines.

NONVOLATILE FLASH/EE MEMORY

The ADuC7023 incorporates Flash/EE memory technology on chip to provide the user with nonvolatile, in-circuit reprogrammable memory space.

Like EEPROM, flash memory can be programmed in-system at a byte level, although it must first be erased. The erase is performed in page blocks. As a result, flash memory is often and more correctly referred to as Flash/EE memory.

The Flash/EE memory represents a step closer to the ideal memory device that includes nonvolatility, in-circuit programmability, high density, and low cost. Incorporated in the ADuC7023, Flash/EE memory technology allows the user to update program code space in-circuit, without needing to replace one-time programmable (OTP) devices at remote operating nodes.

Each part contains a 64 kB array of Flash/EE memory. The lower 62 kB are available to the user, and the upper 2 kB contain permanently embedded firmware, allowing in-circuit serial download. These 2 kB of embedded firmware also contain a power-on configuration routine that downloads factory-calibrated coefficients to the various calibrated peripherals (such as ADC, temperature sensor, and band gap references). This 2 kB embedded firmware is hidden from user code.

Flash/EE Memory Reliability

The Flash/EE memory arrays on the parts are fully qualified for two key Flash/EE memory characteristics: Flash/EE memory cycling endurance and Flash/EE memory data retention.

Endurance quantifies the ability of the Flash/EE memory to be cycled through many program, read, and erase cycles. A single endurance cycle is composed of four independent, sequential events, defined as:

1. Initial page erase sequence.
2. Read/verify sequence (single Flash/EE).
3. Byte program sequence memory.
4. Second read/verify sequence (endurance cycle).

In reliability qualification, every half word (16-bit wide) location of the three pages (top, middle, and bottom) in the Flash/EE memory is cycled 10,000 times from 0x0000 to 0xFFFF. As indicated in Table 1, the Flash/EE memory endurance qualification is carried out in accordance with JEDEC Retention Lifetime Specification A117 over the industrial temperature range of −40° to +125°C. The results allow the specification of a minimum endurance figure over a supply temperature of 10,000 cycles.

Retention quantifies the ability of the Flash/EE memory to retain its programmed data over time. Again, the parts are qualified in accordance with the formal JEDEC Retention Lifetime Specification (A117) at a specific junction temperature (T_J = 85°C). As part of this qualification procedure, the Flash/EE memory is cycled to its specified endurance limit before data retention is characterized. This means that the Flash/EE memory is guaranteed to retain its data for its fully specified retention lifetime every time the Flash/EE memory is reprogrammed. In addition, note that retention lifetime, based on activation energy of 0.6 eV, derates with T_J as shown in Figure 30.

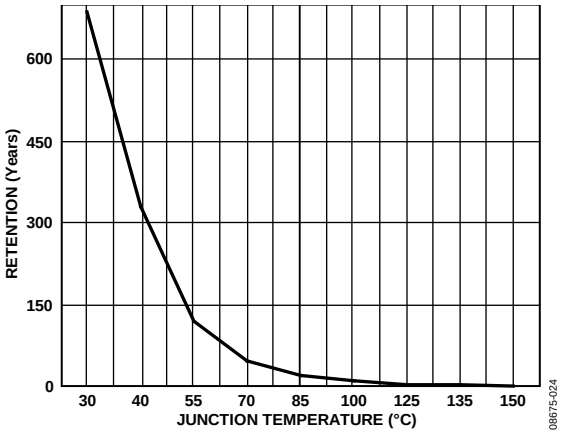


Figure 30. Flash/EE Memory Data Retention

PROGRAMMING

The 62 kB of Flash/EE memory can be programmed in circuit, using the serial download mode or the provided JTAG mode.

Downloading (In-Circuit Programming) via I²C

The ADuC7023 facilitates code download via the the I²C port. The parts enter download mode after a reset or power cycle if the BM pin is pulled low through an external 1 kΩ resistor and Flash Addess 0x80014 = 0xFFFFFFFF. Once in download mode, the user can download code to the full 62 kB of Flash/EE memory while the device is in-circuit in its target application hardware. An executable PC I²C download is provided as part of the development system for serial downloading via the I²C. A USB to I²C download dongle can be purchased from Analog Devices, Inc. This board connects to the USB port of a PC and to the I²C port of the ADuC7023. The part number is USB-I2C/LIN-CONV-Z.

The AN-806 Application Note describes the protocol for serial downloading via the I²C in more detail.

JTAG Access

The JTAG protocol uses the on-chip JTAG interface to facilitate code download and debug.

The JTAG interface is active as long as the part is not in download mode; that is, the P0.0/BM pin = 0 and Address 0x80014 = 0xFFFFFFFF at reset.

When debugging, user code must not write to the bits in GP0CON/GP0DAT corresponding to P0.0/P0.1/P0.2 and P0.3 pins. If user code changes the state of any of these pins, JTAG debug pods are not able to connect to the ADuC7023. In case this happens, the user should have a function in code that can be called externally to mass erase the part. Alternatively, the user should ensure that Flash Address 0x80014 is erased to allow erasing of the part through the I²C interface.

FEEMOD Register

Name: FEEMOD

Address: 0xFFFFF804

Default value: 0x0000

Access: Read/write

Function: FEEMOD sets the operating mode of the flash control interface. Table 32 shows FEEMOD MMR bit designations.

Table 32. FEEMOD MMR Bit Designations

Bit	Description
15 to 9	Reserved.
8	Reserved. Always set this bit to 0.
7 to 5	Reserved. Always set this bit to 0 except when writing keys. See the Sequence to Write the Key section.
4	Flash/EE interrupt enable. This bit is set by the user to enable the Flash/EE interrupt. The interrupt occurs when a command is complete. This bit is cleared by the user to disable the Flash/EE interrupt.
3	Erase/write command protection. This bit is set by the user to enable the erase and write commands. This bit is cleared to protect the Flash/EE against erase/write command.
2 to 0	Reserved. Always set this bit to 0.

FEECON Register

Name: FEECON

Address: 0xFFFFF808

Default value: 0x07

Access: Read/write

Function: FEECON is an 8-bit command register. The commands are described in Table 33.

Table 33. Command Codes in FEECON

Code	Command	Description
0x00[1]	Null	Idle state.
0x01[1]	Single read	Load FEEDAT with the 16-bit data. Indexed by FEEADR.
0x02[1]	Single write	Write FEEDAT at the address pointed by FEEADR. This operation takes 50 µs.
0x03[1]	Erase/write	Erase the page indexed by FEEADR, and write FEEDAT at the location pointed by FEEADR. This operation takes approximately 24 ms.
0x04[1]	Single verify	Compare the contents of the location pointed by FEEADR to the data in FEEDAT. The result of the comparison is returned in FEESTA Bit 1.
0x05[1]	Single erase	Erase the page indexed by FEEADR.
0x06[1]	Mass erase	Erase 62 kB of user space. The 2 kB of kernel are protected. This operation takes 2.48 sec. To prevent accidental execution, a command sequence is required to execute this instruction. See the Command Sequence for Executing a Mass Erase section.
0x07	Reserved	Reserved.
0x08	Reserved	Reserved.
0x09	Reserved	Reserved.
0x0A	Reserved	Reserved.
0x0B	Signature	Give a signature of the 64 kB of Flash/EE in the 24-bit FEESIGN MMR. This operation takes 32,778 clock cycles.
0x0C	Protect	This command can run one time only. The value of FEEPRO is saved and removed only with a mass erase (0x06) or the key (FEEADR/FEEDAT).

Table 63. SPISTA MMR Bit Designations

Bit	Name	Description
15 to 12		Reserved bits.
11	SPIREX	SPI Rx FIFO excess bytes present. This bit is set when there are more bytes in the Rx FIFO than indicated in the SPIMDE bits in SPICON. This bit is cleared when the number of bytes in the FIFO is equal or less than the number in SPIMDE.
10 to 8	SPIRXFSTA[2:0]	SPI Rx FIFO status bits. [000] = Rx FIFO is empty. [001] = 1 valid byte in the FIFO. [010] = 2 valid byte in the FIFO. [011] = 3 valid byte in the FIFO. [100] = 4 valid byte in the FIFO.
7	SPIFOF	SPI Rx FIFO overflow status bit. This bit is set when the Rx FIFO is full when new data is loaded to the FIFO. This bit generates an interrupt except when SPIRFLH is set in SPICON. This bit is cleared when the SPISTA register is read.
6	SPIRXIRQ	SPI Rx IRQ status bit. This bit is set when a receive interrupt occurs. This bit is set when SPITMDE in SPICON is cleared and the required number of bytes have been received. This bit is cleared when the SPISTA register is read.
5	SPITXIRQ	SPI Tx IRQ status bit. This bit is set when a transmit interrupt occurs. This bit is set when SPITMDE in SPICON is set and the required number of bytes have been transmitted. This bit is cleared when the SPISTA register is read.
4	SPITXUF	SPI Tx FIFO underflow. This bit is set when a transmit is initiated without any valid data in the Tx FIFO. This bit generates an interrupt except when SPITFLH is set in SPICON. This bit is cleared when the SPISTA register is read.
3 to 1	SPITXFSTA[2:0]	SPI Tx FIFO status bits. [000] = Tx FIFO is empty. [001] = 1 valid byte in the FIFO. [010] = 2 valid byte in the FIFO. [011] = 3 valid byte in the FIFO. [100] = 4 valid byte in the FIFO.
0	SPIISTA	SPI interrupt status bit. This bit is set to 1 when an SPI based interrupt occurs. This bit is cleared after reading SPISTA.

SPIRX Register

Name: SPIRX

Address: 0xFFFF0A04

Default value: 0x00

Access: Read

Function: This 8-bit MMR is the SPI receive register.

SPITX Register

Name: SPITX

Address: 0xFFFF0A08

Default value: 0xXX

Access: Write

Function: This 8-bit MMR is the SPI transmit register.

Table 77. PLAELMx MMR Bit Descriptions

Bit	Value	Description
31 to 11		Reserved.
10 to 9		Mux 0 control (see Table 81).
8 to 7		Mux 1 control (see Table 81).
6		Mux 2 control. This bit is set by the user to select the output of Mux 0. This bit is cleared by the user to select the bit value from the PLADIN register.
5		Mux 3 control. This bit is set by the user to select the input pin of the particular element. This bit is cleared by the user to select the output of Mux 1.
4 to 1		Look-up table control.
	0000	0.
	0001	NOR.
	0010	B and not A.
	0011	Not A.
	0100	A and not B.
	0101	Not B.
	0110	EXOR.
	0111	NAND.
	1000	AND.
	1001	EXNOR.
	1010	B.
	1011	Not A or B.
	1100	A.
	1101	A or not B.
	1110	OR.
	1111	1.
0		Mux 4 control. This bit is set by the user to bypass the flip-flop. This bit is cleared by the user to select the flip-flop (cleared by default).

PLACLK Register

Name: PLACLK

Address: 0xFFFF0B40

Default value: 0x00

Access: Read/write

Function: PLACLK is the clock selection for the flip-flops. The maximum frequency when using the GPIO pins as the clock input for the PLA blocks is 41.78 MHz.

Table 78. PLACLK MMR Bit Descriptions

Bit	Value	Description
31 to 7		Reserved.
6 to 4		Clock source selection.
	000	GPIO clock on P0.5.
	001	GPIO clock on P1.1.
	010	GPIO clock on P1.6.
	011	HCLK.
	100	External 32.768 kHz crystal.
	101	Timer1 overflow.
	110	UCLK.
	111	Internal 32,768 oscillator.
3		Reserved.
2 to 0		Clock source selection.
	000	GPIO clock on P0.5.
	001	GPIO clock on P1.1.
	010	GPIO clock on P1.6.
	011	HCLK.
	100	External 32.768 kHz crystal.
	101	Timer1 overflow.
	110	UCLK.
	111	Internal 32,768 oscillator.

PLAIRQ Register

Name: PLAIRQ

Address: 0xFFFF0B44

Default value: 0x00000000

Access: Read/write

Function: PLAIRQ enables IRQ0 and/or IRQ1 and selects the source of the IRQ.

Table 79. PLAIRQ MMR Bit Descriptions

Bit	Value	Description
31 to 13		Reserved.
12		PLA IRQ1 enable bit.
11 to 8	0000	PLA Element 0.
	0001	PLA Element 1.
	0010	PLA Element 2.
	0011	PLA Element 3.
	0100	PLA Element 4.
	0101	PLA Element 5.
	0110	PLA Element 6.
	0111	PLA Element 7.
	1000	PLA Element 8.
	1001	PLA Element 9.
	1010	PLA Element 10.
	1011	PLA Element 11.
	1100	PLA Element 12.
	1101	PLA Element 13.
	1110	PLA Element 14.
	1111	PLA Element 15.
7 to 5		Reserved.
4		PLA IRQ0 enable bit. This bit is set by the user to enable IRQ0 output from PLA. This bit is cleared by the user to disable IRQ0 output from PLA.
3 to 0		PLA IRQ0 source.
	0000	PLA Element 0.
	0001	PLA Element 1.
	0010	PLA Element 2.
	0011	PLA Element 3.
	0100	PLA Element 4.
	0101	PLA Element 5.
	0110	PLA Element 6.
	0111	PLA Element 7.
	1xxx	Reserved.

PULSE-WIDTH MODULATOR

PULSE-WIDTH MODULATOR GENERAL OVERVIEW

The ADuC7023 integrates a 5-channel pulse-width modulator (PWM) interface. The PWM outputs can be configured to drive an H-bridge or can be used as standard PWM outputs. On power-up, the PWM outputs default to H-bridge mode. This ensures that the motor is turned off by default. In standard PWM mode, the outputs are arranged as three pairs of PWM pins. Users have control over the period of each pair of outputs and over the duty cycle of each individual output.

Table 84. PWM MMRs

MMR Name	Description
PWMCON1	PWM Control Register 1.
PWM0COM0	Compare Register 0 for PWM Output 0 and PWM Output 1.
PWM0COM1	Compare Register 1 for PWM Output 0 and PWM Output 1.
PWM0COM2	Compare Register 2 for PWM Output 0 and PWM Output 1.
PWM0LEN	Frequency control for PWM Output 0 and PWM Output 1.
PWM1COM0	Compare Register 0 for PWM Output 2 and PWM Output 3.
PWM1COM1	Compare Register 1 for PWM Output 2 and PWM Output 3.
PWM1COM2	Compare Register 2 for PWM Output 2 and PWM Output 3.
PWM1LEN	Frequency control for PWM Output 2 and PWM Output 3.
PWM2COM0	Compare Register 0 for PWM Output 4
PWM2COM1	Compare Register 1 for PWM Output 4
PWM2LEN	Frequency control for PWM Output 4.
PWMCLRI	PWM interrupt clear.

In all modes, the PWMxCOMx MMRs control the point at which the PWM outputs change state. An example of the first pair of PWM outputs (PWM0 and PWM1) is shown in Figure 40.

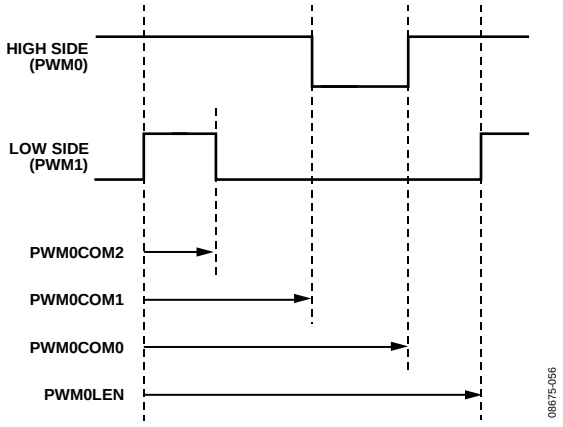


Figure 40. PWM Timing

The PWM clock is selectable via PWMCON1 with one of the following values: UCLK divided by 2, 4, 8, 16, 32, 64, 128, or 256. The length of a PWM period is defined by PWMxLEN.

The PWM waveforms are set by the count value of the 16-bit timer and the compare registers contents, as shown with the PWM0 and PWM1 waveforms in Figure 40.

The low-side waveform, PWM1, goes high when the timer count reaches PWM0LEN, and it goes low when the timer count reaches the value held in PWM0COM2 or when the high-side waveform (PWM0) goes low.

The high-side waveform, PWM0, goes high when the timer count reaches the value held in PWM0COM0, and it goes low when the timer count reaches the value held in PWM0COM1.

PWMCON1 Control Register

Name: PWMCON1

Address: 0xFFFF0F80

Default value: 0x0012

Access: Read and write

Function: This is a 16-bit MMR that configures the PWM outputs.

Table 85. PWMCON1 MMR Bit Designations

Bit	Name	Description
14	SYNC	Enables PWM synchronization. Set to 1 by the user so that all PWM counters are reset on the next clock edge after the detection of a high-to-low transition on the P2.2/SYNC pin. Cleared by the user to ignore transitions on the P2.2/SYNC pin.
13	Reserved	Set to 0 by the user.
12	PWM3INV	Set to 1 by the user to invert PWM3. Cleared by the user to use PWM3 in normal mode.
11	PWM1INV	Set to 1 by the user to invert PWM1. Cleared by the user to use PWM1 in normal mode.
10	PWMTRIP	Set to 1 by the user to enable PWM trip interrupt. When the PWM trip input (Pin P1.5/$PWM_{TRIPINPUT}$) is low, the PWMEN bit is cleared and an interrupt is generated. Cleared by the user to disable the PWMTRIP interrupt.
9	ENA	If HOFF = 0 and HMODE = 1. Note that, if not in H-bridge mode, this bit has no effect. Set to 1 by the user to enable PWM outputs. Cleared by the user to disable PWM outputs. If HOFF = 1 and HMODE = 1, see Table 86.
8 to 6	PWMCP[2:0]	PWM clock prescaler bits. Sets the UCLK divider. [000] = UCLK/2. [001] = UCLK/4. [010] = UCLK/8. [011] = UCLK/16. [100] = UCLK/32. [101] = UCLK/64. [110] = UCLK/128. [111] = UCLK/256.
5	POINV	Set to 1 by the user to invert all PWM outputs. Cleared by the user to use PWM outputs as normal.
4	HOFF	High side off. Set to 1 by the user to force PWM0 and PWM2 outputs high. This also forces PWM1 and PWM3 low. Cleared by the user to use the PWM outputs as normal.
3	LCOMP	Load compare registers. Set to 1 by the user to load the internal compare registers with the values in PWMxCOMx on the next transition of the PWM timer from 0x00 to 0x01. Cleared by the user to use the values previously stored in the internal compare registers.
2	DIR	Direction control. Set to 1 by the user to enable PWM0 and PWM1 as the output signals while PWM2 and PWM3 are held low. Cleared by the user to enable PWM2 and PWM3 as the output signals while PWM0 and PWM1 are held low.
1	HMODE	Enables H-bridge mode.[1] Set to 1 by the user to enable H-bridge mode. Cleared by the user to operate the PWMs in standard mode.
0	PWMEN	Set to 1 by the user to enable all PWM outputs. Cleared by the user to disable all PWM outputs.

[1] In H-bridge mode, HMODE = 1. See Table 86 to determine the PWM outputs.

PWM0COM0 Compare Register

Name: PWM0COM0

Address: 0xFFFF0F84

Default value: 0x0000

Access: Read and write

Function: PWM0 output pin goes high when the PWM timer reaches the count value stored in this register.

PWM0COM1 Compare Register

Name: PWM0COM1

Address: 0xFFFF0F88

Default value: 0x0000

Access: Read and write

Function: PWM0 output pin goes low when the PWM timer reaches the count value stored in this register.

PWM0COM2 Compare Register

Name: PWM0COM2

Address: 0xFFFF0F8C

Default value: 0x0000

Access: Read and write

Function: PWM1 output pin goes low when the PWM timer reaches the count value stored in this register.

PWM0LEN Register

Name: PWM0LEN

Address: 0xFFFF0F90

Default value: 0x0000

Access: Read and write

Function: PWM1 output pin goes high when the PWM timer reaches the value stored in this register.

PWM1COM0 Compare Register

Name: PWM1COM0

Address: 0xFFFF0F94

Default value: 0x0000

Access: Read and write

Function: PWM2 output pin goes high when the PWM timer reaches the count value stored in this register.

PWM1COM1 Compare Register

Name: PWM1COM1

Address: 0xFFFF0F98

Default value: 0x0000

Access: Read and write

Function: PWM2 output pin goes low when the PWM timer reaches the count value stored in this register.

PWM1COM2 Compare Register

Name: PWM1COM2

Address: 0xFFFF0F9C

Default value: 0x0000

Access: Read and write

Function: PWM3 output pin goes low when the PWM timer reaches the count value stored in this register.

PWM1LEN Register

Name: PWM1LEN

Address: 0xFFFF0FA0

Default value: 0x0000

Access: Read and write

Function: PWM3 output pin goes high when the PWM timer reaches the value stored in this register.

PROCESSOR REFERENCE PERIPHERALS

INTERRUPT SYSTEM

There are 22 interrupt sources on the ADuC7023 that are controlled by the interrupt controller. Most interrupts are generated from the on-chip peripherals, such as ADC. Four additional interrupt sources are generated from external interrupt request pins, IRQ0, IRQ1, IRQ2, and IRQ3. The ARM7TDMI CPU core only recognizes interrupts as one of two types, a normal interrupt request IRQ or a fast interrupt request FIQ. All the interrupts can be masked separately.

The control and configuration of the interrupt system is managed through nine interrupt related registers, four dedicated to IRQ, and four dedicated to FIQ. An additional MMR is used to select the programmed interrupt source. The bits in each IRQ and FIQ registers represent the same interrupt source as described in Table 88.

The ADuC7023 contains a vectored interrupt controller (VIC) that supports nested interrupts up to eight levels. The VIC also allows the programmer to assign priority levels to all interrupt sources. Interrupt nesting is enabled by setting the ENIRQN bit in the IRQCONN register. A number of extra MMRs are used when the full-vectored interrupt controller is enabled.

IRQSTA/FIQSTA should be saved immediately upon entering the interrupt service routine (ISR) to ensure that all valid interrupt sources are serviced.

Table 88. IRQ/FIQ MMRs Bit Description

Bit	Description
0	All interrupts OR'ed (FIQ only).
1	SWI.
2	Timer0.
3	Timer1.
4	Watchdog timer (Timer 2).
5	Flash control.
6	ADC channel.
7	PLL lock.
8	I^2C0 master.
9	I^2C0 slave.
10	I^2C1 master.
11	I^2C1 slave.
12	SPI.
13	External IRQ0.
14	Comparator.
15	PSM.
16	External IRQ1.
17	PLA IRQ0.
18	External IRQ2.
19	External IRQ3.
20	PLA IRQ1.
21	PWM.

IRQ

The interrupt request (IRQ) is the exception signal to enter the IRQ mode of the processor. It is used to service general-purpose interrupt handling of internal and external events.

The four 32-bit registers dedicated to IRQ are: IRQSTA, IRQSIG, IRQEN, and IRQCLR.

IRQSTA Register

Name: IRQSTA

Address: 0xFFFF0000

Default value: 0x00000000

Access: Read

Function: IRQSTA (read-only register) provides the current-enabled IRQ source status. When set to 1, that source generates an active IRQ request to the ARM7TDMI core. There is no priority encoder or interrupt vector generation. This function is implemented in software in a common interrupt handler routine. All 32 bits are logically OR'ed to create the IRQ signal to the ARM7TDMI core.

IRQSIG Register

Name: IRQSIG

Address: 0xFFFF0004

Default value: 0x00XXX000

Access: Read

Function: IRQSIG reflects the status of the different IRQ sources. If a peripheral generates an IRQ signal, the corresponding bit in the IRQSIG is set; otherwise, it is cleared. The IRQSIG bits are cleared when the interrupt in the particular peripheral is cleared. All IRQ sources can be masked in the IRQEN MMR. IRQSIG is read-only.

IRQCONN Register

The IRQCONN register is the IRQ and FIQ control register. It contains two active bits. The first to enable nesting and prioritization of IRQ interrupts and the other to enable nesting and prioritization of FIQ interrupts.

If these bits are cleared, then FIQs and IRQs may still be used, but it is not possible to nest IRQs or FIQs. Neither is it possible to set an interrupt source priority level. In this default state, an FIQ does have a higher priority than an IRQ.

Name: IRQCONN

Address: 0xFFFF0030

Default value: 0x00000000

Access: Read and write

Table 95. IRQCONN MMR Bit Designations

Bit	Name	Description
31 to 2	Reserved	These bits are reserved and should not be written to.
1	ENFIQN	This bit is set to 1 to enable nesting of FIQ interrupts. This bit is cleared to mean no nesting or prioritization of FIQs is allowed.
0	ENIRQN	This bit is set to 1 to enable nesting of IRQ interrupts. When this bit is cleared, it means no nesting or prioritization of IRQs is allowed.

IRQSTAN Register

If IRQCONN Bit 0 is asserted and IRQVEC is read then one of these bits is asserted. The bit that asserts depends on the priority of the IRQ. If the IRQ is of Priority 0, then Bit 0 asserts. If the IRQ is of Priority 1, then Bit 1 asserts, and so forth. When a bit is set in this register, all interrupts of that priority and lower are blocked.

To clear a bit in this register, all bits of a higher priority must be cleared first. It is only possible to clear one bit at a time. For example, if this register is set to 0x09, then writing 0xFF changes the register to 0x08, and writing 0xFF a second time changes the register to 0x00.

Name: IRQSTAN

Address: 0xFFFF003C

Default value: 0x00000000

Access: Read and write

Table 96. IRQSTAN MMR Bit Designations

Bit	Name	Description
31 to 8	Reserved	These bits are reserved and should not be written to.
7 to 0		This bit is set to 1 to enable nesting of FIQ interrupts. When this bit is cleared, it means no nesting or prioritization of FIQs is allowed.

FIQVEC Register

The FIQ interrupt vector register, FIQVEC, points to a memory address containing a pointer to the interrupt service routine of the currently active FIQ. This register should only be read when an FIQ occurs and FIQ interrupt nesting has been enabled by setting Bit 1 of the IRQCONN register.

Name: FIQVEC

Address: 0xFFFF011C

Default value: 0x00000000

Access: Read only

Table 97. FIQVEC MMR Bit Designations

Bit	Type	Initial Value	Description
31 to 23	Read only	0	Always read as 0.
22 to 7	R/W	0	IRQBASE register value.
6 to 2		0	Highest priority source. This is a value between 0 and 27 that represents the possible interrupt sources. For example, if the highest currently active FIQ is Timer 2, then these bits are [00100].
1 to 0	Reserved	0	Reserved bits.

Timer2 (Watchdog Time)

Timer2 has two modes of operation: normal mode and watchdog mode. The watchdog timer is used to recover from an illegal software state. When enabled, it requires periodic servicing to prevent it from forcing a processor reset.

Normal Mode

Timer2 in normal mode is identical to Timer0, except for the clock source and the count-up functionality. The clock source is 32 kHz from the PLL and can be scaled by a factor of 1, 16, or 256 (see Figure 44).

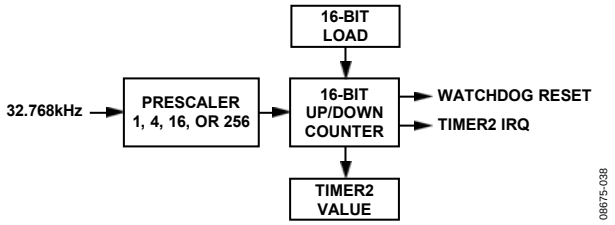


Figure 44. Timer2 Block Diagram

Watchdog Mode

Watchdog mode is entered by setting Bit 5 in the T2CON MMR. Timer2 decreases from the value present in the T2LD register until 0. T2LD is used as the timeout. The maximum timeout can be 512 sec using the prescaler/256, and full-scale in T2LD. Timer3 is clocked by the internal 32 kHz crystal when operating in the watchdog mode. To enter watchdog mode successfully, Bit 5 in the T2CON MMR must be set after writing to the T2LD MMR.

If the timer reaches 0, a reset or an interrupt occurs, depending on Bit 1 in the T2CON register. To avoid reset or interrupt, any value must be written to T2CLRI before the expiration period. This reloads the counter with T2LD and begins a new timeout period.

When watchdog mode is entered, T2LD and T2CON are write-protected. These two registers cannot be modified until a reset clears the watchdog enable bit, which causes Timer2 to exit watchdog mode.

The Timer2 interface consists of four MMRs: T2LD, T2VAL, T2CON, and T2CLRI.

T2LD Register

Name: T2LD

Address: 0xFFFF0360

Default value: 0x0000

Access: Read/write

T2LD is a 16-bit register load register that holds the 16-bit value that is loaded into the counter.

T2VAL Register

Name: T2VAL

Address: 0xFFFF0364

Default value: 0xFFFF

Access: Read

T2VAL is a 16-bit read-only register that represents the current state of the counter.

T2CON Register

Name: T2CON

Address: 0xFFFF0368

Default value: 0x0000

Access: Read/write

T2CON is the configuration MMR described in Table 104.

Table 104. T2CON MMR Bit Descriptions

Bit	Value	Description
15 to 9		Reserved.
8		Count up. This bit is set by the user for Timer2 to count up. This bit is cleared by the user for Timer2 to count down by default.
7		Timer2 enable bit. This bit is set by the user to enable Timer2. This bit is cleared by user to disable Timer2 by default.
6		Timer2 mode. This bit is set by user to operate in periodic mode. This bit is cleared by the user to operate in free-running mode. Default mode.
5		Watchdog mode enable bit. This bit is set by the user to enable watchdog mode. This bit is cleared by the user to disable watchdog mode by default.
4		Secure clear bit. This bit is set by the user to use the secure clear option. This bit is cleared by the user to disable the secure clear option by default.
3 to 2		Prescale.
	00	Source clock/1 by default.
	01	Source clock/16.
	10	Source clock/256.
	11	Undefined. Equivalent to 00.
1		Watchdog IRQ Option Bit. This bit is set by the user to produce an IRQ instead of a reset when the watchdog reaches 0. This bit is cleared by the user to disable the IRQ option.
0		Reserved.

POWER-ON RESET OPERATION

An internal power-on reset (POR) is implemented on the ADuC7023. For LV_{DD} below 2.40 V typical, the internal POR holds the part in reset. As LV_{DD} rises above 2.40 V, an internal timer times out for typically 64 ms before the part is released from reset. The user must ensure that the power supply IOV_{DD} has reached a stable 2.7 V minimum level by this time. Likewise, on power-down, the internal POR holds the part in reset until LV_{DD} has dropped below 2.40 V.

Figure 53 illustrates the operation of the internal POR in detail.

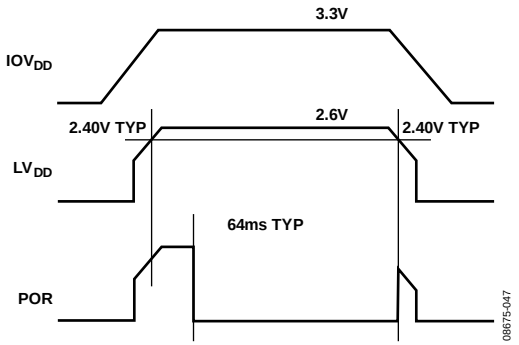
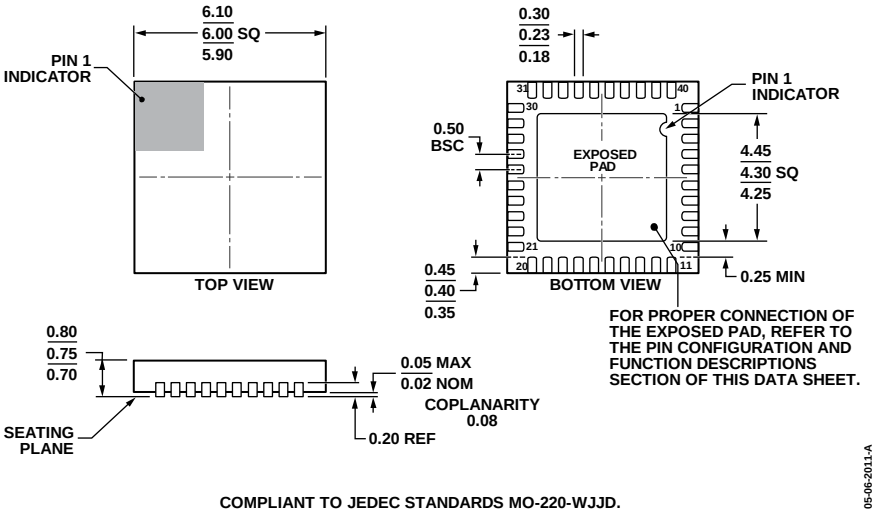


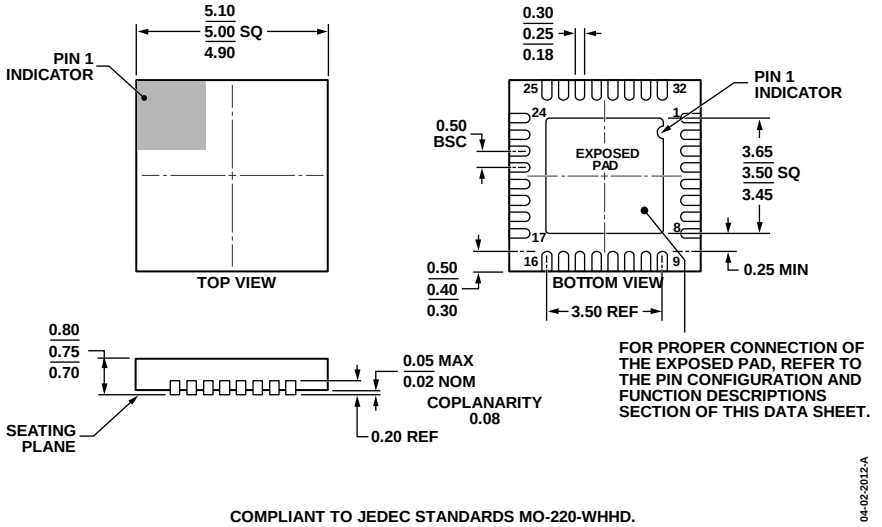
Figure 53. Internal Power-On Reset Operation

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WJJD.

Figure 55. 40-Lead Frame Chip Scale Package [LFCSP_WQ]
6 mm × 6 mm Body, Very Very Thin Quad
(CP-40-10)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WHHD.

Figure 56. 32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
5 mm × 5 mm Body, Very Very Thin Quad
(CP-32-11)
Dimensions shown in millimeters