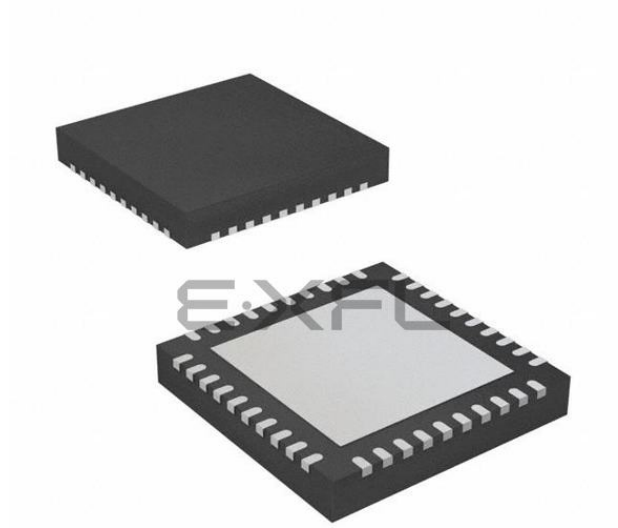


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	44MHz
Connectivity	I²C, SPI
Peripherals	POR, PWM, WDT
Number of I/O	20
Program Memory Size	62KB (31K x16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 32
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 12 x12b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	40-WFQFN Exposed Pad, CSP
Supplier Device Package	40-LFCSP-WQ (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc7023bcp6z62irl

REVISION HISTORY

1/15—Rev. F to Rev. G

Changes to Table 53 51
Changes to I²C Section 60
Changes to Table 65 61
Changes to Table 72 64
Changes to I2CREPS Bit Description, Table 73 66

5/14—Rev. E to Rev. F

Change $\overline{CONV}_{START}$ Pin to $CONV_{START}$ Pin ..... Throughout
Change to Layout, Power Requirements Parameter, Table 1 7
Change to Table 8 13
Changes to Figure 7 and Table 9 14
Change to Table 21 28
Change to Figure 23 30
Change to JTAG Access Section 37
Changes to Table 36 42
Changes to Table 55 51
Changes to I²C Bus Addresses Section 59
Change to Table 84 71
Added PWM2LEN Register Section 75

7/13—Rev. D to Rev. E

Changes to Ordering Guide 95

7/13—Rev. C to Rev. D

Added WLCSP (Throughout) 1
Changes to Features Section 1
Added Shared Analog/Digital Inputs to AGND Rating of −0.3 V to AV_{DD} + 0.3 V, Endnote 1, and Endnote 2; Table 8 13
Added Figure 9; Renumbered Sequentially; Added WLCSP Pin Numbers to Table 9 14
Changes to Pin P1.7/PWM3/SDA1/PLAI[6] and Pin P1.6/PWM2/SCL1/PLAI[5] Descriptions; Table 9 16
Changes to ADC Circuit Overview Section, Transfer Function Section, and Figure 20 Caption 29
Changes to Typical Operation Section, ADCCON Register Section, and ADCON[13] Description in Table 24 30
Changes to Bits[4:3] Value 10 Description; Table 24 31
Changes to Converter Operation Section and Deleted Pseudo Differential Mode Section 33
Changes to Figure 27 and Figure 28 Caption 34
Changes to Table 30 and Following Text 36
Changes to JTAG Access Section 37
Changes to References to ADC and the DACs Section 45
Changes to General-Purpose Input/Output Section 51
Changes to SPIDIV Register Section 56
Changes to Bits[1:0] Value 01 Description; Table 66 61
Changes to T0CLRI Register Section 84
Changes to Figure 53 90
Updated Outline Dimensions 93
Changes to Ordering Guide 95

5/12—Rev. B to Rev. C

Changed SDATA to SDA and SCLK to SCL, Table 2; SDATA to SDA and SCLK to SCL, Table 3; and SDATA to SDA and SCLK to SCL, Figure 2 8
Changes to Figure 7, Figure 8, and Table 9 14
Changed SCLK to SCL, Table 17 25
Changed SCLK to SCL, Table 18 26
Changes to Bit 6, Table 24 and 4 to 0, Description Column, Table 25 30
Changed Reference in REFCON Register Section from Table 22 to Table 30 35
Added Note 1 to Table 53 49
Changes to Note 1, Table 55 50
Changed SPICLK (Serial Clock I/O) Pin Section to SCLK (Serial Clock I/O) Pin Section 53
Changed SPICLK to SCLK in Serial Peripheral Interface Section and in SCLK (Serial Clock I/O) Pin Section 53
Changes to Table 79 68
Changes to Timers Section 82
Added Hours, Minutes, Seconds, and 1/128 Format Section and Table 101 82
Changes to T0LD Register Section and T1LD Register Section 83
Changes to T2LD Register Section 85
Updated Outline Dimensions 92
Changes to Ordering Guide 93

7/10—Rev. A to Rev. B

Changes to Temperature Sensor Parameter in Table 1 6
Change to Table 10 and changes to Table 11 23
Changes to Table 12 and Table 13 24
Changes to Table 16 and Table 17 25
Changes to Table 18 26
Change to Table 21 and changes to Table 22 27
Changes to Table 24 29
Changes to ADCGN Register and ADCOF Register Sections 32
Changes to Temperature Sensor Section 34
Changes to Table 29 35
Change to REMAP Register and RSTCLR Register Sections 41
Change to RSTKEY1 Register and RSTKEY2 Register Sections 42
Changes to Oscillator and PLL—Power Control Section 48
Changes to General-Purpose Input/Output Section 51
Changes to Serial Peripheral Interface Section 53
Changes to Table 75 67
Changes to Table 83 and Pulse-Width Modulator General Overview Section 70
Changes to Table 84 71
Change to Table 85 72
Change to FIQSTAN Register Section 81
Change to T2CLRI Register Section 85

FUNCTIONAL BLOCK DIAGRAM

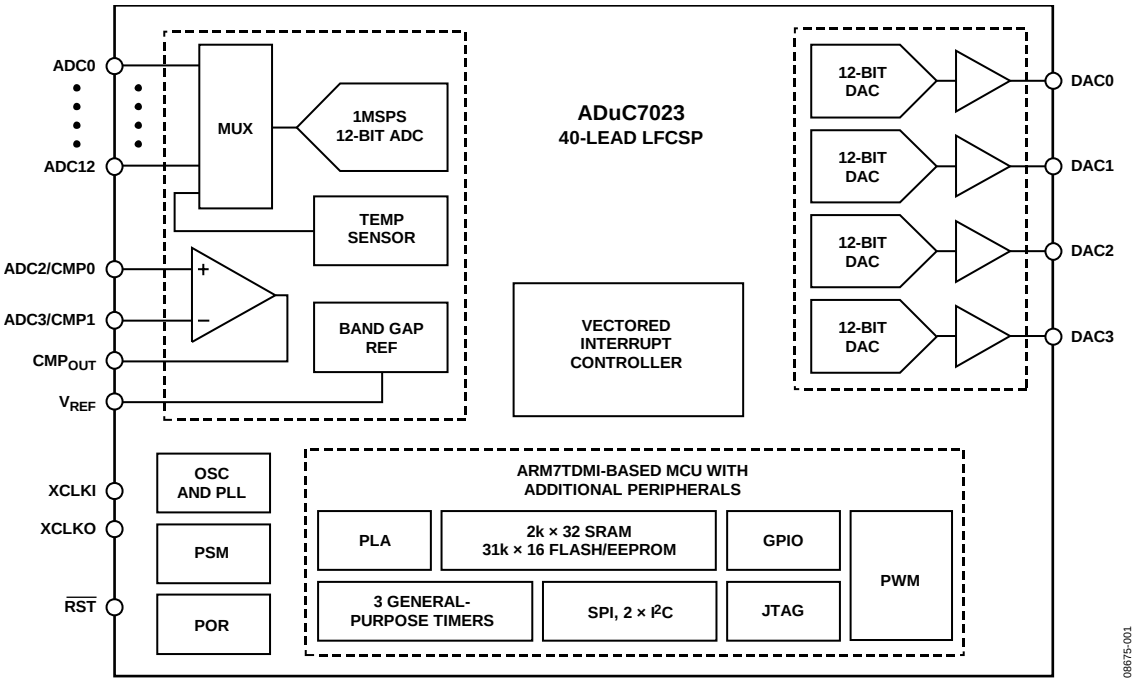


Figure 1.

Table 5. SPI Master Mode Timing (Phase Mode = 0)

Parameter	Description	Min	Typ	Max	Unit
t_{SL}	SCLK low pulse width[1]		(SPIDIV + 1) × t_{UCLK}		ns
t_{SH}	SCLK high pulse width[1]		(SPIDIV + 1) × t_{UCLK}		ns
t_{DAV}	Data output valid after SCLK edge			25	ns
t_{DOSU}	Data output setup before SCLK edge			75	ns
t_{DSU}	Data input setup time before SCLK edge[1]	1 × t_{UCLK}			ns
t_{DHD}	Data input hold time after SCLK edge[1]	2 × t_{UCLK}			ns
t_{DF}	Data output fall time		5	12.5	ns
t_{DR}	Data output rise time		5	12.5	ns
t_{SR}	SCLK rise time		5	12.5	ns
t_{SF}	SCLK fall time		5	12.5	ns

[1] t_{UCLK} = 23.9 ns. It corresponds to the 41.78 MHz internal clock from the PLL before the clock divider.

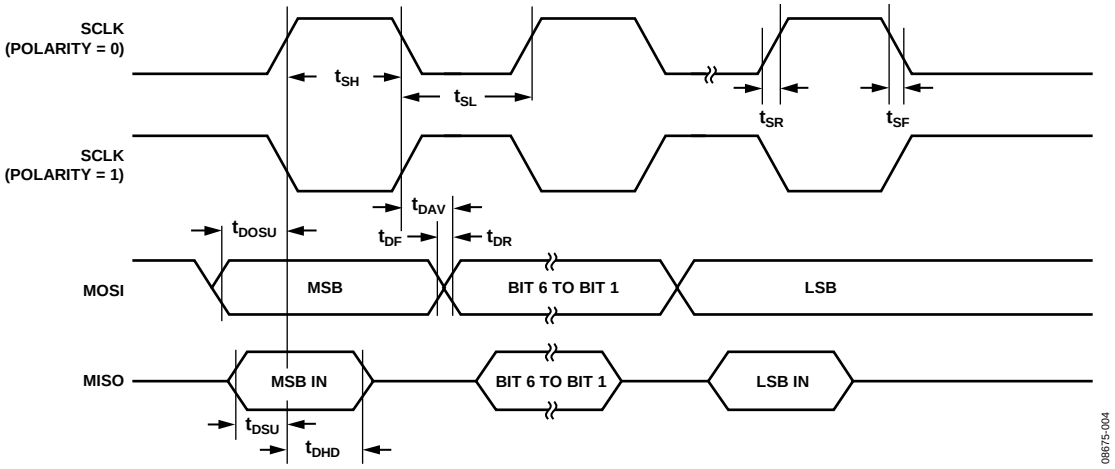


Figure 4. SPI Master Mode Timing (Phase Mode = 0)

Pin No.				
40-LFCSP	32-LFCSP	36-WLCSP	Mnemonic	Description
28	24	C3	P0.3/PLAO[9]/TCK	The default value of this pin depends on the level of P0.0/BM. If P0.0/BM = 0, this pin defaults to a general purpose input. If P0.0/BM = 1, this pin defaults to a JTAG test data clock pin. This is a multifunction pin as follows: General-Purpose Input and Output Port 0.3. Programmable Logic Array Output Element 9. Test Clock, JTAG Test Port Clock Input. Debug and download access. When debugging the part via JTAG, this pin must not be toggled by user code and the GP0CON/GP0DAT register bits affecting this pin must not be changed as doing so disables JTAG access.
17	13	E3	DGND	Digital Ground.
18	14	F3	IOV_{DD}	3.3 V Supply for GPIO and Input of the On-Chip Voltage Regulator.
19	15	D3	LV_{DD}	2.6 V Output of the On-Chip Voltage Regulator. This output must be connected to a 0.47 µF capacitor to DGND only.
20	16	F2	$\overline{RST}$	Reset Input, Active Low.
23	19	E1	RTCK	Return JTAG Clock Signal. This is not the standard JTAG clock signal. It is an output signal from the JTAG controller. If using a 20-lead JTAG header, connect to Pin 11.
9	7	F6	P0.4/IRQ0/SCL0/PLAI[0]/CONV	General-Purpose Input and Output Port 0.4/External Interrupt Request 0/ I^2C0 Clock Signal/Programmable Logic Array Input Element 0/ADC External Convert Start. By default, this pin is configured as a digital input with a weak pull-up resistor enabled.
10	8	E5	P0.5/SDA0/PLAI[1]/$COMP_{OUT}$	General-Purpose Input and Output Port 0.5/I^2C0 Data Signal/ Programmable Logic Array Input Element 1/Voltage Comparator Output. By default, this pin is configured as a digital input with a weak pull-up resistor enabled.
	9	F5	P0.6/MISO/SCL1/PLAI[2]	General-Purpose Input and Output Port 0.6/SPI MISO Signal/I^2C1 Clock On 32-Lead and 36-Ball Packages/Programmable Logic Array Input Element 2. By default, this pin is configured as a digital input with a weak pull-up resistor enabled.
	10	D4	P0.7/MOSI/SDA1/PLAO[0]	General-Purpose Input and Output Port 0.7/SPI MOSI Signal/I^2C1 Data Signal On 32-Lead and 36-Ball Packages/Programmable Logic Array Output Element 0. By default, this pin is configured as a digital input with a weak pull-up resistor enabled.
11			P0.6/MISO/PLAI[2]	General-Purpose Input and Output Port 0.6/SPI MISO Signal/Programmable Logic Array Input Element 2. By default, this pin is configured as a digital input with a weak pull-up resistor enabled.
12			P0.7/MOSI/PLAO[0]	General-Purpose Input and Output Port 0.7/SPI MOSI Signal/Programmable Logic Array Output Element 0. By default this pin is configured as a digital input with a weak pull-up reisistor enabled.
21	17	F1	XCLKI	Input to the Crystal Oscillator Inverter and Input to the Internal Clock Generator Circuits. Connect to DGND if unused.
22	18	E2	XCLKO	Output from the Crystal Oscillator Inverter. Leave unconnected if unused.
16	N/A	N/A	P1.7/PWM3/SDA1/PLAI[6]	General-Purpose Input and Output Port 1.7/PWM Output 3/I^2C1 Data Signal/Programmable Logic Array Input Element 6. By default, this pin is configured as a digital input with a weak pull-up resistor enabled.
15	N/A	N/A	P1.6/PWM2/SCL1/PLAI[5]	General-Purpose Input and Output Port 1.6/PWM Output 2/I^2C1 Clock Signal/Programmable Logic Array Input Element 5. By default, this pin is configured as a digital input with a weak pull-up resistor enabled.
29	N/A	N/A	P1.5/ADC6/$PWM_{TRIPINPUT}$/PLAO[4]	General-Purpose Input and Output Port 1.5/ADC Single-Ended or Differential Analog Input 6/$PWM_{TRIPINPUT}$/Programmable Logic Array Output Element 4. By default, this pin is configured as a digital input with a weak pull-up resistor enabled. When used as ADC input, the pull-up resistor should be disabled manually.
7	N/A	N/A	P1.4/ADC10/PLAO[3]	General-Purpose Input and Output Port 1.4/ADC Single-Ended or Differential Analog Input 10/Programmable Logic Array Output Element 3. By default, this pin is configured as a digital input with a weak pull-up resistor enabled. When used as ADC input, the pull-up resistor should be disabled manually.

Pin No.				
40-LFCSP	32-LFCSP	36-WLCSP	Mnemonic	Description
34	26	A3	P1.3/ADC5/IRQ3/PLAI[4]	General-Purpose Input and Output Port 1.3/ADC Single-Ended or Differential Analog Input 5/External Interrupt Request 3/ Programmable Logic Array Input Element 4. By default, this pin is configured as a digital input with a weak pull-up resistor enabled. When used as ADC input, the pull-up resistor should be disabled manually.
33	25	A2	P1.2/ADC4/IRQ2/PLAI[3]/ECLK/	General-Purpose Input and Output Port 1.2/ADC Single-Ended or Differential Analog Input 4/External Interrupt Request 2/ Programmable Logic Array Input Element 3/Input-Output for External Clock. By default, this pin is configured as a digital input with a weak pull-up resistor enabled. When used as ADC input, the pull-up resistor should be disabled manually.
14	12	F4	P1.1/$\overline{SS}$/IRQ1/PWM1/PLAO[2]/T1	General-Purpose Input and Output Port 1.1/SPI Interface Slave Select (Active Low)/External Interrupt Request 1/PWM Output 1/ Programmable Logic Array Output Element 2/Timer 1 Input Clock. By default, this pin is configured as a digital input with a weak pull-up resistor enabled.
13	11	E4	P1.0/SCLK/PWM0/PLAO[1]	General-Purpose Input and Output Port 1.0/SPI Interface Clock Signal/ PWM Output 0/Programmable Logic Array Output Element 1. By default, this pin is configured as a digital input with a weak pull-up resistor enabled.
35	27	B3	V_{REF}	2.5 V Internal Voltage Reference. Must be connected to a 0.47 µF capacitor when using the internal reference.
40	32	A6	AGND	Analog Ground. Ground reference point for the analog circuitry.
1	1	B6	AV_{DD}	3.3 V Analog Power.

TYPICAL PERFORMANCE CHARACTERISTICS

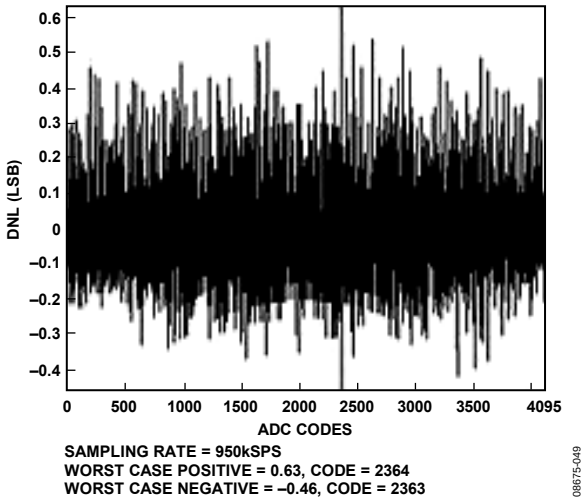


Figure 10. Typical DNL, f_{ADC} = 950 kSPS, Internal Reference Used

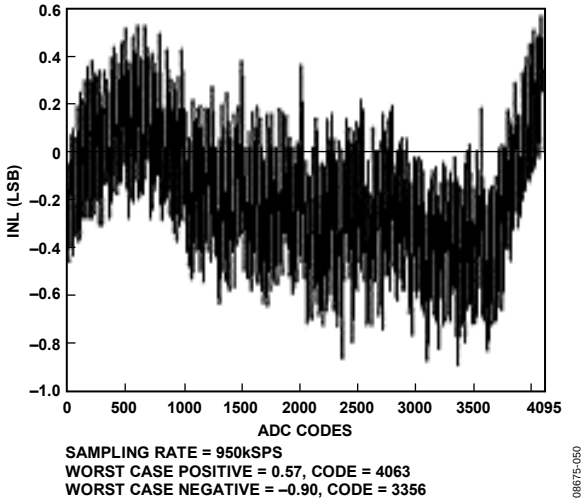


Figure 11. Typical INL, f_{ADC} = 950 kSPS, Internal Reference Used

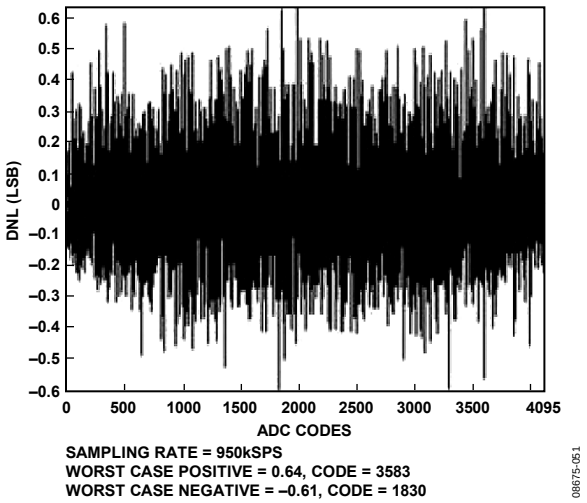


Figure 12. Typical DNL, f_{ADC} = 950 kSPS, External 1.0 V Reference Used

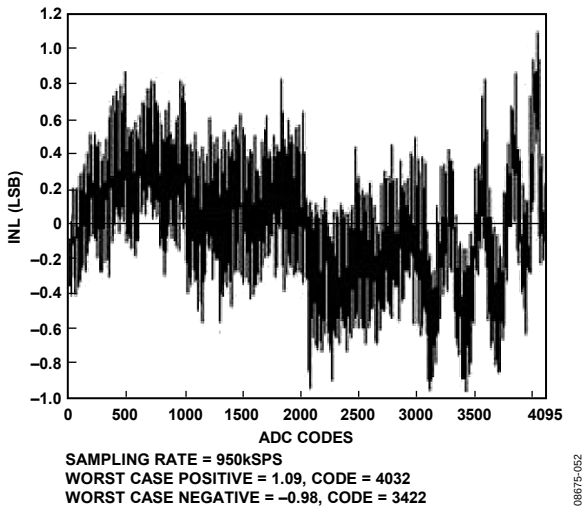


Figure 13. Typical INL, f_{ADC} = 950 kSPS, External 1.0 V Reference Used

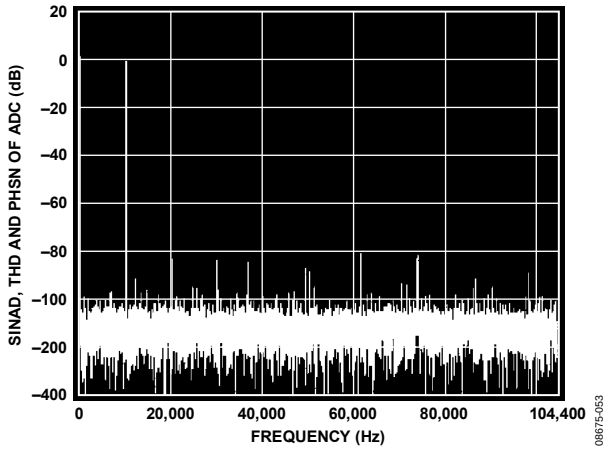


Figure 14. SINAD, THD, and PHSN of ADC , Internal 2.5 V Reference Used

OVERVIEW OF THE ARM7TDMI CORE

The ARM7® core is a 32-bit reduced instruction set computer (RISC). It uses a single 32-bit bus for instruction and data. The length of the data can be 8 bits, 16 bits, or 32 bits. The length of the instruction word is 32 bits.

The ARM7TDMI is an ARM7 core with four additional features: T support for the thumb (16-bit) instruction set, D support for debug, M support for long multiplications, and I includes the EmbeddedICE module to support embedded system debugging.

THUMB MODE (T)

An ARM instruction is 32 bits long. The ARM7TDMI processor supports a second instruction set that has been compressed into 16 bits, called the Thumb® instruction set. Faster execution from 16-bit memory and greater code density can usually be achieved by using the Thumb instruction set instead of the ARM instruction set, which makes the ARM7TDMI core particularly suitable for embedded applications.

However, the Thumb mode has two limitations. Thumb code typically requires more instructions for the same job. As a result, ARM code is usually best for maximizing the performance of time critical code. Also, the Thumb instruction set does not include some of the instructions needed for exception handling, which automatically switches the core to ARM code for exception handling.

See the ARM7TDMI user guide for details on the core architecture, the programming model, and both the ARM and ARM Thumb instruction sets.

LONG MULTIPLY (M)

The ARM7TDMI instruction set includes four extra instructions that perform 32-bit by 32-bit multiplication with a 64-bit result, and 32-bit by 32-bit multiplication-accumulation (MAC) with a 64-bit result. These results are achieved in fewer cycles than required on a standard ARM7 core.

EmbeddedICE (I)

EmbeddedICE provides integrated on-chip support for the core. The EmbeddedICE module contains the breakpoint and watchpoint registers that allow code to be halted for debugging purposes. These registers are controlled through the JTAG test port.

When a breakpoint or watchpoint is encountered, the processor halts and enters debug state. Once in a debug state, the processor registers can be inspected as well as the Flash/EE, SRAM, and memory mapped registers.

EXCEPTIONS

ARM supports five types of exceptions and a privileged processing mode for each type. The five types of exceptions are:

- Normal interrupt or IRQ. This is provided to service general-purpose interrupt handling of internal and external events.
- Fast interrupt or FIQ. This is provided to service data transfers or communication channels with low latency. FIQ has priority over IRQ.
- Memory abort.
- Attempted execution of an undefined instruction.
- Software interrupt instruction (SWI). This can be used to make a call to an operating system.

Typically, the programmer defines interrupt as IRQ, but for higher priority interrupt, that is, faster response time, the programmer can define interrupt as FIQ.

ARM REGISTERS

ARM7TDMI has a total of 37 registers: 31 general-purpose registers and six status registers. Each operating mode has dedicated banked registers.

When writing user-level programs, 15 general-purpose 32-bit registers (R0 to R14), the program counter (R15), and the current program status register (CPSR) are usable. The remaining registers are only used for system-level programming and exception handling.

When an exception occurs, some of the standard registers are replaced with registers specific to the exception mode. All exception modes have replacement banked registers for the stack pointer (R13) and the link register (R14) as represented in Figure 15. The fast interrupt mode has more registers (R8 to R12) for fast interrupt processing. This means the interrupt processing can begin without the need to save or restore these registers, and thus save critical time in the interrupt handling process.

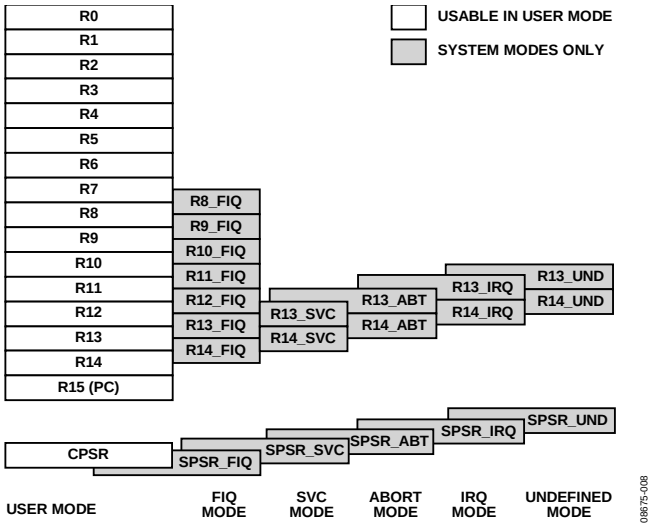


Figure 15. Register Organization

The ADCCON register must be configured to 0x37A3.

To calculate die temperature use the following formula:

$$T - T_{REF} = (V_{ADC} - V_{TREF}) \times K$$

where:
T is the temperature result.
T_{REF} is 25°C.
V_{ADC} is the average ADC result from two consecutive conversions.
V_{TREF} is 1369 mV, which corresponds to T_{REF} = 25°C as described in Table 1.
K is the gain of the ADC in temperature sensor mode as determined by characterization data, K = 0.2262°C/mV. This corresponds to 1/V TC specification as shown in Table 1.

Using the default values from Table 1 and without any calibration, this equation becomes

$$T - 25°C = (V_{ADC} - 1369) \times 0.2262$$

where:
V_{ADC} is in millivolts.

For increased accuracy, perform a single point calibration at a controlled temperature value.

For the calculation shown without calibration, (T_{REF}, V_{TREF}) = (25°C, 1369 mV). The idea of a single point calibration is to use other known (T_{REF}, V_{TREF}) values to replace the common (25°C, 1369 mV) for every part.

For some users, it is not possible to get such a known pair. For these cases, an ADuC7023 comes with a single point calibration value loaded in the TEMPREF register. For more details on this register, see the TEMPREF Register section.

During production testing of the ADuC7023, the TEMPREF register is loaded with an offset adjustment factor. Each part will have a different value in the TEMPREF register. Using this single point calibration, use the same formula as shown:

$$T - T_{REF} = (V_{ADC} - V_{TREF}) \times K$$

where:
T_{REF} is 27°C when using the TEMPREF register method, but is not guaranteed.
T_{TREF} can be calculated using the TEMPREF register.

TSCON Register

Name: TSCON

Address: 0xFFFF0544

Default value: 0x00

Access: Read/write

Table 28. TSCON MMR Bit Designations

Bit	Description
7 to 1	Reserved.
0	Temperature sensor chop enable bit. This bit is set to 1 to enable chopping of the internal amplifier to the ADC. This bit is cleared to disable chopping. This bit is cleared by default.

TEMPREF Register

Name: TEMPREF

Address: 0xFFFF0548

Default value: Factory configured

Access: Read/write

Table 29. TEMPREF MMR Bit Designations

Bit	Description
15 to 9	Reserved.
8	Temperature reference voltage sign.
7 to 0	Temperature sensor offset calibration voltage. To calculate the V_{TREF} from the TEMPREF register, perform the following calculation: If *TEMPREF* sign negative, subtract TEMPREF from 2292 $C_{TREF} = 2292 - TEMPREF[7:0]$ where *TEMREF*[8] = 1. or If *TEMREF* sign positive, add *TEMPREF* to 2292 $C_{TREF} = TEMPREF[7:0] + 2292$ where: TEMPREF[8] = 0. Then, $V_{TREF} = (C_{TREF} \times V_{REF})/4096 \times 1000$ where: C_{TREF} is calculated as above. V_{REF} is 2.5 V, internal reference voltage. Insert V_{TREF} into $T - T_{REF} = (V_{ADC} - V_{TREF}) \times K$ where: T_{REF} is 27°C, when using TEMREF register. V_{ADC} is the average ADC result from two consecutive conversions. V_{TREF} is calculated as above. Note that ADC code value 2292 is a default value when using the TEMREF register. It is not an exact value and must only be used with the TEMPREF register.

SECURITY

The 62 kB of Flash/EE memory available to the user can be read and write protected.

Bit 31 of the FEEPRO/FEEHIDE MMR (see Table 34) protects the 62 kB from being read through JTAG programming mode. The other 31 bits of this register protect writing to the flash memory. Each bit protects four pages, that is, 2 kB. Write protection is activated for all types of access.

Three Levels of Protection

Protection can be set and removed by writing directly into FEEHIDE MMR. This protection does not remain after reset.

Protection can be set by writing into FEEPRO MMR. It only takes effect after a save protection command (0x0C) and a reset. The FEEPRO MMR is protected by a key to avoid direct access. The key is saved once and must be entered again to modify FEEPRO. A mass erase sets the key back to 0xFFFF but also erases all the user code.

Flash can be permanently protected by using the FEEPRO MMR and a particular value of key: 0xDEADDEAD. Entering the key again to modify the FEEPRO register is not allowed.

Sequence to Write the Key

1. Write the bit in FEEPRO corresponding to the page to be protected.
2. Enable key protection by setting Bit 6 of FEEMOD (Bit 5 must equal 0).
3. Write a 32-bit key in FEEADR, FEEDAT.
4. Run the write key command 0x0C in FEECON; wait for the read to be successful by monitoring FEESTA.
5. Reset the part.

To remove or modify the protection, the same sequence is used with a modified value of FEEPRO. If the key chosen is the value 0xDEAD, the memory protection cannot be removed. Only a mass erase unprotects the part, but it also erases all user code.

The sequence to write the key is illustrated in the following example (this protects writing Page 4 to Page 7 of the Flash):

```
FEEPRO=0xFFFFFFFD;  //Protect Page 4 to
                     Page 7
FEEMOD=0x48; //Write key enable
FEEADR=0x1234;      //16 bit key value
FEEDAT=0x5678;      //16 bit key value
FEECON= 0x0C;       //Write key command
```

Follow the same sequence to protect the part permanently with FEEADR = 0xDEAD and FEEDAT = 0xDEAD.

FLASH/EE CONTROL INTERFACE

Serial and JTAG programming use the Flash/EE control interface, which includes the eight MMRs outlined in this section.

FEESTA Register

Name: FEESTA

Address: 0xFFFFF800

Default value: 0x20

Access: Read

Function: FEESTA is a read-only register that reflects the status of the flash control interface as described in Table 31.

Table 31. FEESTA MMR Bit Designations

Bit	Description
7 to 6	Reserved.
5	Reserved.
4	Reserved.
3	Flash interrupt status bit. This bit is set automatically when an interrupt occurs, that is, when a command is complete and the Flash/EE interrupt enable bit in the FEEMOD register is set. This bit is cleared when reading FEESTA register.
2	Flash/EE controller busy. This bit is set automatically when the controller is busy. This bit is cleared automatically when the controller is not busy.
1	Command fail. This bit is set automatically when a command is not completed. This bit is cleared automatically when reading FEESTA register.
0	Command pass. This bit is set by the MicroConverter when a command is completed. This bit is cleared automatically when reading the FEESTA register.

OTHER ANALOG PERIPHERALS

DAC

The ADuC7023 incorporates four, 12-bit voltage output DACs on chip. Each DAC has a rail-to-rail voltage output buffer capable of driving 5 kΩ/100 pF.

Each DAC has two selectable ranges: 0 V to V_{REF} (internal band gap 2.5 V reference) and 0 V to AV_{DD}.

The signal range is 0 V to AV_{DD}.

By setting RSTCFG Bit 2, the DAC output pins can retain their state during a watchdog or software reset.

MMRs Interface

Each DAC is independently configurable through a control register and a data register. These two registers are identical for the four DACs. Only DAC0CON (see Table 40) and DAC0DAT (see Table 41) are described in detail in this section.

DACxCON Registers

Name	Address	Default Value	Access
DAC0CON	0xFFFF0600	0x00	R/W
DAC1CON	0xFFFF0608	0x00	R/W
DAC2CON	0xFFFF0610	0x00	R/W
DAC3CON	0xFFFF0618	0x00	R/W

Table 40. DAC0CON MMR Bit Designations

Bit	Value	Name	Description
7			Reserved.
6		DACBY	This bit is set to bypass the DAC output buffer. This bit is cleared to enable the DAC output buffer.
5		DACCLK	DAC update rate. This bit is set by the user to update the DAC using Timer1. This bit is cleared by the user to update the DAC using HCLK (core clock).
4		DACCLR	DAC clear bit. This bit is set by the user to enable normal DAC operation. This bit is cleared by the user to reset data register of the DAC to 0.
3			Reserved. This bit remains at 0.
2			Reserved. This bit remains at 0.
1 to 0			DAC range bits.
	00		Power-down mode. The DAC output is in tristate.
	01		Reserved.
	10		0 V to V_{REF} (2.5 V) range.
	11		0 V to AV_{DD} range.

DACxDAT Registers

Name	Address	Default Value	Access
DAC0DAT	0xFFFF0604	0x00000000	R/W
DAC1DAT	0xFFFF060C	0x00000000	R/W
DAC2DAT	0xFFFF0614	0x00000000	R/W
DAC3DAT	0xFFFF061C	0x00000000	R/W

Table 41. DAC0DAT MMR Bit Designations

Bit	Description
31 to 28	Reserved.
27 to 16	12-bit data for DAC0.
15 to 0	Reserved.

Using the DACs

The on-chip DAC architecture consists of a resistor string DAC followed by an output buffer amplifier. The functional equivalent is shown in Figure 32.

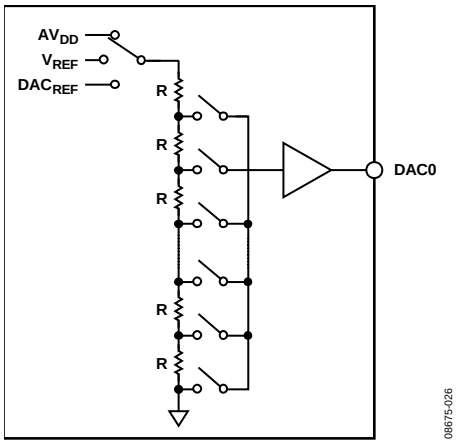


Figure 32. DAC Structure

As illustrated in Figure 32, the reference source for each DAC is user-selectable in software. It can be either AV_{DD} or V_{REF}. In 0-to-AV_{DD} mode, the DAC output transfer function spans from 0 V to the voltage at the AV_{DD} pin. In 0-to-V_{REF} mode, the DAC output transfer function spans from 0 V to the internal 2.5 V reference, V_{REF}.

The DAC output buffer amplifier features a true, rail-to-rail output stage implementation. This means that when unloaded, each output is capable of swinging to within less than 5 mV of both AV_{DD} and ground. Moreover, the DAC linearity specification (when driving a 5 kΩ resistive load to ground) is guaranteed through the full transfer function except Code 0 to Code 100, and, in 0-to-AV_{DD} mode only, Code 3995 to Code 4095.

Linearity degradation near ground and V_{DD} is caused by saturation of the output amplifier, and a general representation of its effects (neglecting offset and gain error) is illustrated in Figure 33. The dotted line in Figure 33 indicates the ideal transfer function, and the solid line represents what the transfer function may look like with endpoint nonlinearities due to saturation of the output amplifier. Figure 33 represents a transfer function in 0-to-AV_{DD}

MMRs and Keys

The operating mode, clocking mode, and programmable clock divider are controlled via three MMRs, PLLCON (see Table 49) and POWCONx. PLLCON controls the operating mode of the clock system, POWCON0 controls the core clock frequency and the power-down mode, POWCON1 controls the clock frequency to I^2C and SPI.

To prevent accidental programming, a certain sequence has to be followed to write to the PLLCON and POWCONx registers.

PLLKEY1 Register

Name: PLLKEY1

Address: 0xFFFF0410

Default value: 0xXXXX

Access: Write

PLLKEY2 Register

Name: PLLKEY2

Address: 0xFFFF0418

Default value: 0xXXXX

Access: Write

PLLCON Register

Name: PLLCON

Address: 0xFFFF0414

Default value: 0x21

Access: Read/write

Table 49. PLLCON MMR Bit Designations

Bit	Value	Name	Description
7 to 6			Reserved.
5		OSEL	32 kHz PLL input selection. This bit is set by the user to select the internal 32 kHz oscillator. This bit is set by default. This bit is cleared by the user to select the external 32 kHz crystal.
4 to 2			Reserved.
1 to 0		MDCLK	Clocking modes.
	00		Reserved.
	01		PLL default configuration.
	10		Reserved.
	11		External clock on Pin 33 (40-lead LFCSP)/Pin 25 (32-lead LFCSP).

Table 50. PLLCON Write Sequence

Name	Code
PLLKEY1	0xAA
PLLCON	User value
PLLKEY2	0x55

POWKEY1 Register

Name: POWKEY1

Address: 0xFFFF0404

Default value: 0xXXXX

Access: Write

Function: POWKEY1 prevents accidental programming to POWCON0.

POWKEY2 Register

Name POWKEY2

Address 0xFFFF040C

Default value 0xXXXX

Access Write

Function: POWKEY2 prevents accidental programming to POWCON0.

POWCON0 Register

Name: POWCON0

Address: 0xFFFF0408

Default value: 0x00

Access: Read/write

Table 51. POWCON0 MMR Bit Designations

Bit	Value	Name	Description
7			Reserved.
6 to 4		PC	Operating modes.
	000		Active mode.
	001		Pause mode.
	010		Nap.
	011		Sleep mode. IRQ0 to IRQ3 can wake up the part.
	100		Stop mode. IRQ0 to IRQ3 can wake up the part.
	Others		Reserved.
3			Reserved.
2 to 0		CD	CPU clock divider bits.
	000		41.78 MHz.
	001		20.89 MHz.
	010		10.44 MHz.
	011		5.22 MHz.
	100		2.61 MHz.
	101		1.31 MHz.
	110		653 kHz.
	111		326 kHz.

GP2PAR Register

Name	GP2PAR
Address	0xFFFFF44C
Default value	0x00000000
Access	Read/write
Function	GP2PAR programs the parameters for Port 0, Port 1, and Port 2. Note that the GP2DAT MMR must always be written after changing the GP2PAR MMR.

Table 57. GPxPAR MMR Bit Descriptions

Bit	Description
31	Reserved.
30 to 29	Drive strength Px.7.
28	Pull-up disable Px.7.
27	Reserved.
26 to 26	Drive strength Px.6.
24	Pull-up disable Px.6.
23	Reserved.
22 to 21	Drive strength Px.5.
20	Pull-up disable Px.5.
19	Reserved.
18 to 17	Drive strength Px.4.
16	Pull-up disable Px.4.
15	Reserved.
14 to 13	Drive strength Px.3.
12	Pull-up disable Px.3.
11	Reserved.
10 to 9	Drive strength Px.2.
8	Pull-up disable Px.2.
7	Reserved.
6 to 5	Drive strength Px.1.
4	Pull-up disable Px.1.
3	Reserved.
2 to 1	Drive strength Px.0.
0	Pull-up disable Px.0.

Table 58. GPIO Drive Strength Control Bits Descriptions

Control Bits Value	Description
00	Medium drive strength.
01	Low drive strength.
1x	High drive strength.

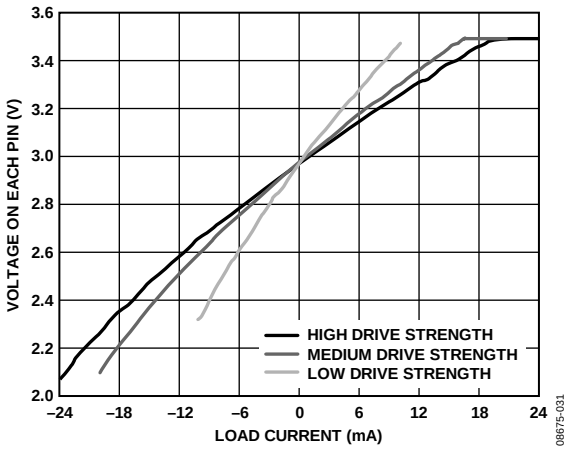


Figure 37. Programmable Strength for High Level

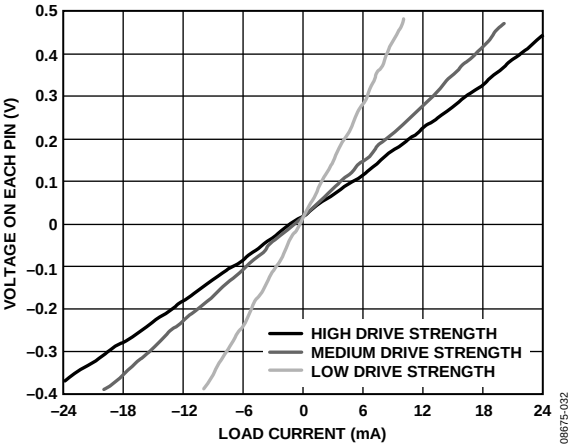


Figure 38. Programmable Strength for Low Level

The drive strength bits can be written one time only after reset. More writing to related bits has no effect on changing drive strength. The GPIO drive strength and pull-up disable is not always adjustable for the GPIO port. Some control bits cannot be changed (see Table 59).

Table 59. GPxPAR Control Bits Access Descriptions[1]

Bit	GP0PAR	GP1PAR	GP2PAR
31	Reserved	Reserved	Reserved
30 to 29	R/W	R/W	Reserved
28	R/W	R/W	Reserved
27	Reserved	Reserved	Reserved
26 to 26	R/W	R/W	Reserved
24	R/W	R/W	Reserved
23	Reserved	Reserved	Reserved
22 to 21	R/W	R (b00)	Reserved
20	R/W	R/W	Reserved
19	Reserved	Reserved	Reserved
18 to 17	R (b00)	R (b00)	R (b00)
16	R/W	R/W	R/W
15	Reserved	Reserved	Reserved
14 to 13	R (b00)	R (b00)	R (b00)
12	R/W	R/W	R/W
11	Reserved	Reserved	Reserved

Bit	GP0PAR	GP1PAR	GP2PAR
10 to 9	R (b00)	R (b00)	R (b00)
8	R/W	R/W	R/W
7	Reserved	Reserved	Reserved
6 to 5	R (b00)	R (b00)	Reserved
4	R/W	R/W	Reserved
3	Reserved	Reserved	Reserved
2 to 1	R (b00)	R (b00)	R (b00)
0	R/W	R/W	R (b0)

[1] When P2.0 is configured as AIN12, the internal pull-up resistor cannot be disabled.

GP0DAT Register

Name	Address	Default Value	Access
GP0DAT	0xFFFFF420	0x000000XX	R/W
GP1DAT	0xFFFFF430	0x000000XX	R/W
GP2DAT	0xFFFFF440	0x000000XX	R/W

GPxDAT are Port x configuration and data registers. They configure the direction of the GPIO pins of Port x, set the output value for the pins configured as output, and store the input value of the pins configured as input.

Table 60. GPxDAT MMR Bit Descriptions

Bit	Description
31 to 24	Direction of the data. This bit is set to 1 by the user to configure the GPIO pin as an output. This bit is cleared to 0 by the user to configure the GPIO pin as an input.
23 to 16	Port x data output.
15 to 8	Reflect the state of Port x pins at reset (read only).
7 to 0	Port x data input (read only).

GP0SET Register

Name: GP0SET

Address: 0xFFFFF424

Default value: 0x000000XX

Access: Write

Function: GP0SET is a data set Port x register.

GP1SET Register

Name: GP1SET

Address: 0xFFFFF434

Default value: 0x000000XX

Access: Write

Function: GP1SET is a data set Port x register.

GP2SET Register

Name: GP2SET

Address: 0xFFFFF444

Default value: 0x000000XX

Access: Write

Function: GP2SET is a data set Port x register.

Table 61. GPxSET MMR Bit Descriptions

Bit	Description
31 to 24	Reserved.
23 to 16	Data port x. This bit is set to 1 by the user to set bit on Port x; this bit also sets the corresponding bit in the GPxDAT MMR. This bit is cleared to 0 by the user; this bit does not affect the data out.
15 to 0	Reserved.

GP0CLR Registers

Name: GP0CLR

Address: 0xFFFFF428

Default value: 0x000000XX

Access: Write

Function: GP0CLR is a data clear Port x register.

GP1CLR Registers

Name: GP1CLR

Address: 0xFFFFF438

Default value: 0x000000XX

Access: Write

Function: GP1CLR is a data clear Port x register.

GP2CLR Registers

Name: GP2CLR

Address: 0xFFFFF448

Default value: 0x000000XX

Access: Write

Function: GP2CLR is a data clear Port x register.

Table 62. GPxCLR MMR Bit Descriptions

Bit	Description
31 to 24	Reserved.
23 to 16	Data port x clear bit. This bit is set to 1 by the user to clear the bit on Port x; this bit also clears the corresponding bit in the GPxDAT MMR. This bit is cleared to 0 by the user; this bit does not affect the data out.
15 to 0	Reserved.

SERIAL PERIPHERAL INTERFACE

The ADuC7023 integrates a complete hardware serial peripheral interface (SPI) on chip. SPI is an industry standard, synchronous serial interface that allows eight bits of data to be synchronously transmitted and simultaneously received, that is, full duplex up to a maximum bit rate of 20 Mbps.

The SPI port can be configured for master or slave operation and typically consists of four pins: MISO, MOSI, SCLK, and SPI$\overline{SS}$.

MISO (Master In, Slave Out) Pin

The MISO pin is configured as an input line in master mode and an output line in slave mode. The MISO line on the master (data in) should be connected to the MISO line in the slave device (data out). The data is transferred as byte wide (8-bit) serial data, MSB first.

MOSI (Master Out, Slave In) Pin

The MOSI pin is configured as an output line in master mode and an input line in slave mode. The MOSI line on the master (data out) should be connected to the MOSI line in the slave device (data in). The data is transferred as byte wide (8-bit) serial data, MSB first.

SCLK (Serial Clock I/O) Pin

The master serial clock (SCLK) synchronizes the data being transmitted and received through the MOSI SCLK period. Therefore, a byte is transmitted/received after eight SCLK periods. The SCLK pin is configured as an output in master mode and as an input in slave mode.

In master mode, polarity and phase of the clock are controlled by the SPICON register, and the bit rate is defined in the SPIDIV register as follows:

$$f_{SERIAL\ CLOCK} = \frac{f_{UCLK}}{2 \times (1 + SPIDIV)}$$

where:

f_{UCLK} is the clock selected by POWCON1 Bit 7 to Bit 6.

The maximum speed of the SPI clock is independent on the clock divider bits.

In slave mode, the SPICON register must be configured with the phase and polarity of the expected input clock. The slave accepts data from an external master up to 10 Mbps.

In both master and slave modes, data is transmitted on one edge of the SCLK signal and sampled on the other. Therefore, it is important that the polarity and phase are configured the same for the master and slave devices.

SPI Chip Select ($\overline{SS}$ Input) Pin

In SPI slave mode, a transfer is initiated by the assertion of $\overline{SS}$, which is an active low input signal. The SPI port then transmits and receives 8-bit data until the transfer is concluded by deassertion of $\overline{SS}$. In slave mode, $\overline{SS}$ is always an input.

In SPI master mode, the $\overline{SS}$ is an active low output signal. It asserts itself automatically at the beginning of a transfer and deasserts itself upon completion.

Configuring External Pins for SPI Functionality

P1.1 is the slave chip select pin. In slave mode, this pin is an input and must be driven low by the master. In master mode, this pin is an output and goes low at the beginning of a transfer and high at the end of a transfer.

P1.0 is the SCLK pin.

P0.6 is the master in, slave out (MISO) pin.

P0.7 is the master out, slave in (MOSI) pin.

To configure these pins for SPI mode, see the General-Purpose Input/Output section.

SPI Registers

The following MMR registers control the SPI interface: SPISTA, SPIRX, SPITX, SPIDIV, and SPICON.

SPI Status Register

Name: SPISTA

Address: 0xFFFF0A00

Default value: 0x0000

Access: Read

Function: This 32-bit MMR contains the status of the SPI interface in both master and slave modes.

I²C Address 1 Registers, I2CxADR1

Name: I2C0ADR1, I2C1ADR1

Address: 0xFFFF081C , 0xFFFF091C

Default value: 0x00

Access: Read/write

Function: These 8-bit MMRs are used in 10-bit addressing mode only. These registers contain the least significant byte of the address.

Table 70. I2CxADR1 MMR in 10-Bit Address Mode

Bit	Name	Description
7 to 0	I2CLADR	These bits contain ADDR[7:0] in 10-bit address mode.

I²C Master Clock Control Register, I2CxDIV

Name: I2C0DIV, I2C1DIV

Address: 0xFFFF0824, 0xFFFF0924

Default value: 0x1F1F

Access: Read/write

Function: These MMRs control the frequency of the I²C clock generated by the master on to the SCL pin. For further details, see the I²C initial section.

Table 71. I2CxDIV MMR

Bit	Name	Description
15 to 8	DIVH	These bits control the duration of the high period of SCL.
7 to 0	DIVL	These bits control the duration of the low period of SCL.

I²C Slave Registers

I²C Slave Control Registers, I2CxSCON

Name: I2C0SCON, I2C1SCON

Address: 0xFFFF0828, 0xFFFF0928

Default value: 0x0000

Access: Read/write

Function: These 16-bit MMRs configure the I²C peripheral in slave mode.

Table 72. I2CxSCON MMR Bit Designations

Bit	Name	Description
15 to 11		Reserved bits.
10	I2CSTXENI	Slave transmit interrupt enable bit. This bit is set to enable an interrupt after a slave transmits a byte. This bit clears this interrupt source.
9	I2CSRXENI	Slave receive interrupt enable bit. This bit is set to enable an interrupt after the slave receives data. This bit clears this interrupt source.
8	I2CSSENI	I²C stop condition detected interrupt enable bit. This bit is set to enable an interrupt on detecting a stop condition on the I²C bus. This bit clears this interrupt source.
7	I2CNACKEN	I²C no acknowledge enable bit. This bit is set to no acknowledge the next byte in the transmission sequence. This bit is cleared to let the hardware control the acknowledge/no acknowledge sequence.
6		Reserved. Write a value of 0 to this bit.
5	I2CSETEN	I²C early transmit interrupt enable bit. This bit is set to enable a transmit request interrupt just after the positive edge of SCL during the read bit transmission. This bit is cleared to enable a transmit request interrupt just after the negative edge of SCL during the read bit transmission.

PWM2COM0 Compare Register

Name: PWM2COM0

Address: 0xFFFF0FA4

Default value: 0x0000

Access: Read/write

Function: PWM4 output pin goes high when the PWM timer reaches the count value stored in this register.

PWM2COM1 Compare Register

Name: PWM2COM1

Address: 0xFFFF0FA8

Default value: 0x0000

Access: Read/write

Function: PWM4 output pin goes low when the PWM timer reaches the count value stored in this register.

PWM2LEN Register

Name: PWM2LEN

Address: 0xFFFF0FB0

Default value: 0x0000

Access: Read/write

Function: PWM2LEN defines the period of PWM4.

PWMCLRI Register

Name: PWMCLRI

Address: 0xFFFF0FB8

Default value: 0x0000

Access: Write

Function: Write any value to this register to clear a PWM interrupt source. This register must be written to before exiting a PWM interrupt service routine; otherwise, multiple interrupts occur.

PROCESSOR REFERENCE PERIPHERALS

INTERRUPT SYSTEM

There are 22 interrupt sources on the ADuC7023 that are controlled by the interrupt controller. Most interrupts are generated from the on-chip peripherals, such as ADC. Four additional interrupt sources are generated from external interrupt request pins, IRQ0, IRQ1, IRQ2, and IRQ3. The ARM7TDMI CPU core only recognizes interrupts as one of two types, a normal interrupt request IRQ or a fast interrupt request FIQ. All the interrupts can be masked separately.

The control and configuration of the interrupt system is managed through nine interrupt related registers, four dedicated to IRQ, and four dedicated to FIQ. An additional MMR is used to select the programmed interrupt source. The bits in each IRQ and FIQ registers represent the same interrupt source as described in Table 88.

The ADuC7023 contains a vectored interrupt controller (VIC) that supports nested interrupts up to eight levels. The VIC also allows the programmer to assign priority levels to all interrupt sources. Interrupt nesting is enabled by setting the ENIRQN bit in the IRQCONN register. A number of extra MMRs are used when the full-vectored interrupt controller is enabled.

IRQSTA/FIQSTA should be saved immediately upon entering the interrupt service routine (ISR) to ensure that all valid interrupt sources are serviced.

Table 88. IRQ/FIQ MMRs Bit Description

Bit	Description
0	All interrupts OR'ed (FIQ only).
1	SWI.
2	Timer0.
3	Timer1.
4	Watchdog timer (Timer 2).
5	Flash control.
6	ADC channel.
7	PLL lock.
8	I^2C0 master.
9	I^2C0 slave.
10	I^2C1 master.
11	I^2C1 slave.
12	SPI.
13	External IRQ0.
14	Comparator.
15	PSM.
16	External IRQ1.
17	PLA IRQ0.
18	External IRQ2.
19	External IRQ3.
20	PLA IRQ1.
21	PWM.

IRQ

The interrupt request (IRQ) is the exception signal to enter the IRQ mode of the processor. It is used to service general-purpose interrupt handling of internal and external events.

The four 32-bit registers dedicated to IRQ are: IRQSTA, IRQSIG, IRQEN, and IRQCLR.

IRQSTA Register

Name: IRQSTA

Address: 0xFFFF0000

Default value: 0x00000000

Access: Read

Function: IRQSTA (read-only register) provides the current-enabled IRQ source status. When set to 1, that source generates an active IRQ request to the ARM7TDMI core. There is no priority encoder or interrupt vector generation. This function is implemented in software in a common interrupt handler routine. All 32 bits are logically OR'ed to create the IRQ signal to the ARM7TDMI core.

IRQSIG Register

Name: IRQSIG

Address: 0xFFFF0004

Default value: 0x00XXX000

Access: Read

Function: IRQSIG reflects the status of the different IRQ sources. If a peripheral generates an IRQ signal, the corresponding bit in the IRQSIG is set; otherwise, it is cleared. The IRQSIG bits are cleared when the interrupt in the particular peripheral is cleared. All IRQ sources can be masked in the IRQEN MMR. IRQSIG is read-only.

FIQSTAN Register

If IRQCONN Bit 1 is asserted and FIQVEC is read, then one of these bits assert. The bit that asserts depends on the priority of the FIQ. If the FIQ is of Priority 0, then Bit 0 asserts. If the FIQ is of Priority 1, then Bit 1 asserts, and so forth.

When a bit is set in this register, all interrupts of that priority and lower are blocked.

To clear a bit in this register, all bits of a higher priority must be cleared first. It is only possible to clear one bit at a time. For example, if this register is set to 0x09, then writing 0xFF changes the register to 0x08 and writing 0xFF a second time changes the register to 0x00.

Name: FIQSTAN

Address: 0xFFFF013C

Default value: 0x00000000

Access: Read/write

Table 98. FIQSTAN MMR Bit Designations

Bit	Name	Description
31 to 8	Reserved	These bits are reserved and should not be written to.
7 to 0		This bit is set to 1 to enables nesting of FIQ interrupts. When this bit is cleared, it means no nesting or prioritization of FIQs is allowed.

External Interrupts and PLA interrupts

The ADuC7023 provides up to four external interrupt sources and two PLA interrupt sources. These external interrupts can be individually configured as level or rising/falling edge triggered.

To enable the external interrupt source or the PLA interrupt source, the appropriate bit must be set in the FIQEN or IRQEN register. To select the required edge or level to trigger on, the IRQCONE register must be appropriately configured.

To properly clear an edge-based external IRQ interrupt or an edge-based PLA interrupt, set the appropriate bit in the IRQCLRE register.

IRQCONE Register

Name: IRQCONE

Address: 0xFFFF0034

Default value: 0x00000000

Access: Read and write

Table 99. IRQCONE MMR Bit Designations

Bit	Value	Name	Description
31 to 12		Reserved	These bits are reserved and should not be written to.
11 to 10	11	PLA1SRC[1:0]	PLA IRQ1 triggers on falling edge.
	10		PLA IRQ1 triggers on rising edge.
	01		PLA IRQ1 triggers on low level.
	00		PLA IRQ1 triggers on high level.
9 to 8	11	IRQ3SRC[1:0]	External IRQ3 triggers on falling edge.
	10		External IRQ3 triggers on rising edge.
	01		External IRQ3 triggers on low level.
	00		External IRQ3 triggers on high level.
7 to 6	11	IRQ2SRC[1:0]	External IRQ2 triggers on falling edge.
	10		External IRQ2 triggers on rising edge.
	01		External IRQ2 triggers on low level.
	00		External IRQ2 triggers on high level.
5 to 4	11	PLA0SRC[1:0]	PLA IRQ0 triggers on falling edge.
	10		PLA IRQ0 triggers on rising edge.
	01		PLA IRQ0 triggers on low level.
	00		PLA IRQ0 triggers on high level.
3 to 2	11	IRQ1SRC[1:0]	External IRQ1 triggers on falling edge.
	10		External IRQ1 triggers on rising edge.
	01		External IRQ1 triggers on low level.
	00		External IRQ1 triggers on high level.
1 to 0	11	IRQ0SRC[1:0]	External IRQ0 triggers on falling edge.
	10		External IRQ0 triggers on rising edge.
	01		External IRQ0 triggers on low level.
	00		External IRQ0 triggers on high level.

T1LD Register

Name: T1LD

Address: 0xFFFF0320

Default value: 0x00000000

Access: Read/write

T1LD is a 32-bit load register that holds the 32-bit value that is loaded into the counter.

T1VAL Register

Name: T1VAL

Address: 0xFFFF0324

Default value: 0xFFFFFFFF

Access: Read

T1VAL is a 32-bit read-only register that represents the current state of the counter.

T1CON Register

Name: T1CON

Address: 0xFFFF0328

Default value: 0x00000000

Access: Read/write

T1CON is the configuration MMR described in Table 103.

Table 103. T1CON MMR Bit Descriptions

Bit	Value	Description
31 to 18		Reserved.
17		Event select bit. This bit is set by the user to enable time capture of an event. This bit is cleared by the user to disable time capture of an event.
16 to 12		Event select range, 0 to 31. These events are as described in Table 88. All events are offset by two, that is, Event 2 in Table 88 becomes Event 0 for the purposes of Timer1.
11 to 9		Clock select.
	000	Core clock (HCLK).
	001	Internal 32.768 kHz crystal
	010	UCLK
	011	P1.1 raising edge triggered.
8		Count up. This bit is set by the user for Timer1 to count up. This bit is cleared by the user for Timer1 to count down by default.
7		Timer1 enable bit. This bit is set by the user to enable Timer1. This bit is cleared by the user to disable Timer1 by default.
6		Timer1 mode. This bit is set by the user to operate in periodic mode. This bit is cleared by the user to operate in free-running mode. Default mode.
5 to 4		Format.
	00	Binary.
	01	Reserved.
	10	Hours, minutes, seconds, hundredths (23 hours to 0 hour).
	11	Hours, minutes, seconds, hundredths (255 hours to 0 hour).
3 to 0		Prescale.
	0000	Source clock/1.
	0100	Source clock/16.
	1000	Source clock/256.
	1111	Source clock/32,768.

T1CLRI Register

Name: T1CLRI

Address: 0xFFFF032C

Default value: 0xXX

Access: Write

T1CLRI is an 8-bit register. Writing any value to this register clears the Timer1 interrupt.

T1CAP Register

Name: T1CAP

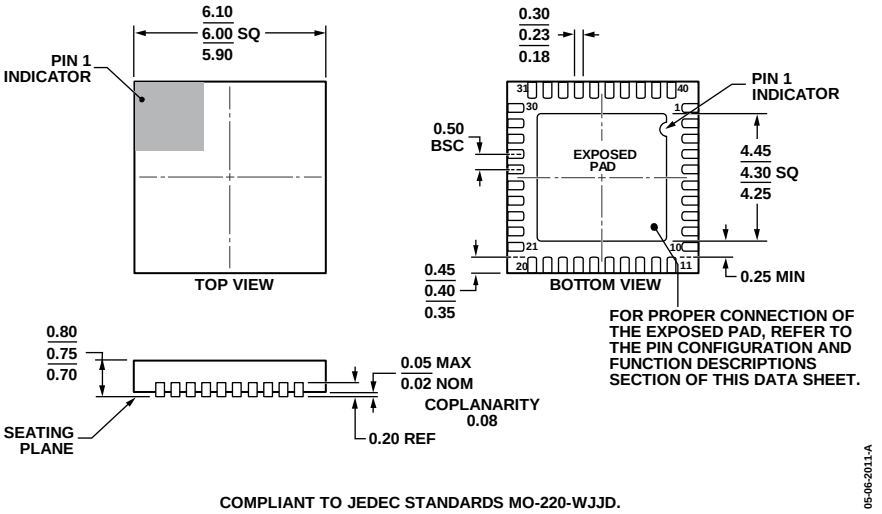
Address: 0xFFFF0330

Default value: 0x00000000

Access: Read

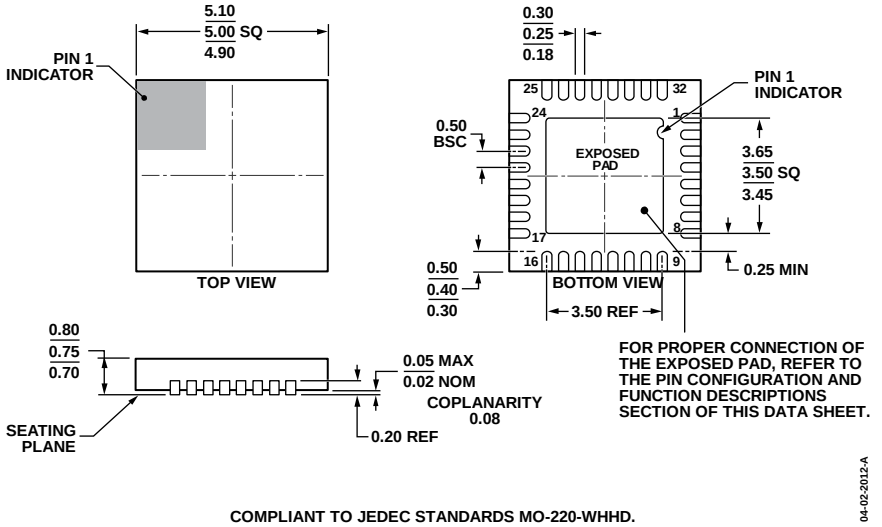
T1CAP is a 32-bit register. It holds the value contained in T1VAL when a particular event occurrs. This event must be selected in T1CON.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WJJD.

Figure 55. 40-Lead Frame Chip Scale Package [LFCSP_WQ]
6 mm × 6 mm Body, Very Very Thin Quad
(CP-40-10)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WHHD.

Figure 56. 32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
5 mm × 5 mm Body, Very Very Thin Quad
(CP-32-11)
Dimensions shown in millimeters