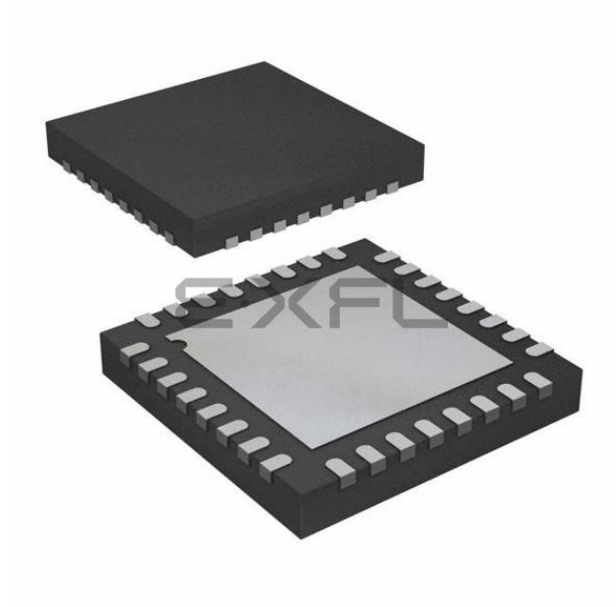

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	44MHz
Connectivity	I²C, SPI
Peripherals	POR, PWM, WDT
Number of I/O	12
Program Memory Size	62KB (31K x16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 32
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x12b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-WFQFN Exposed Pad, CSP
Supplier Device Package	32-LFCSP-WQ (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc7023bcpz62i-r7

6/10—Rev. 0 to Rev. A

Changes to Temperature Sensor Parameter in Table 1 6
Changes to Table 24 29
Changes to Temperature Sensor Section 34
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Changes to Ordering Guide 93

1/10—Revision 0: Initial Version

TIMING SPECIFICATIONS

Table 2. I²C Timing in Fast Mode (400 kHz)

Parameter	Description	Slave		Master	Unit
		Min	Max	Typ	
t_L	SCL low pulse width	200		1360	ns
t_H	SCL high pulse width	100		1140	ns
t_{SHD}	Start condition hold time	300			ns
t_{DSU}	Data setup time	100		740	ns
t_{DHD}	Data hold time	0		400	ns
t_{RSU}	Setup time for repeated start	100			ns
t_{PSU}	Stop condition setup time	100		800	ns
t_{BUF}	Bus-free time between a stop condition and a start condition	1.3			µs
t_R	Rise time for both SCL and SDA		300	200	ns
t_F	Fall time for both SCL and SDA		300		ns

Table 3. I²C Timing in Standard Mode (100 kHz)

Parameter	Description	Slave		Unit
		Min	Max	
t_L	SCL low pulse width	4.7		µs
t_H	SCL high pulse width	4.0		ns
t_{SHD}	Start condition hold time	4.0		µs
t_{DSU}	Data setup time	250		ns
t_{DHD}	Data hold time	0	3.45	µs
t_{RSU}	Setup time for repeated start	4.7		µs
t_{PSU}	Stop condition setup time	4.0		µs
t_{BUF}	Bus-free time between a stop condition and a start condition	4.7		µs
t_R	Rise time for both SCL and SDA		1	µs
t_F	Fall time for both SCL and SDA		300	ns

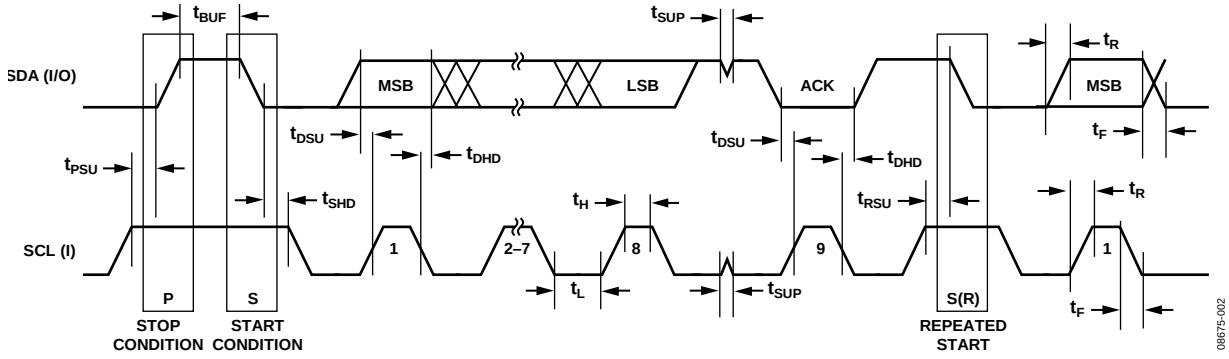

Figure 2. I²C-Compatible Interface Timing

Pin No.				
40-LFCSP	32-LFCSP	36-WLCSP	Mnemonic	Description
31	N/A	A1	P2.3/ADC8/PLAO[7]	General-Purpose Input and Output Port 2.3/ADC Single-Ended or Differential Analog Input 8/Programmable Logic Array Output Element 7. By default, this pin is configured as a digital input with a weak pull-up resistor enabled. When used as ADC input, pull-up resistor should be disabled manually.
30	N/A	B1	P2.2/ADC7/SYNC/PLAO[6]	General-Purpose Input and Output Port 2.2/ADC Single-Ended or Differential Analog Input 7/PWM Sync/Programmable Logic Array Output Element 6. By default, this pin is configured as a digital input with a weak pull-up resistor enabled. When used as ADC input, pull-up resistor should be disabled manually.
8	N/A	E6	P2.0/ADC12/PWM4/PLAI[7]	General-Purpose Input and Output Port 2.0/ADC Single-Ended or Differential Analog Input 12/PWM Output 4/Programmable Logic Array Input Element 7. By default, this pin is configured as a digital input with a weak pull-up resistor enabled. When used as an ADC input, it is not possible to disable the internal pull-up resister. This means that this pin has a higher leakage current value than other analog input pins.
2	2	C4	GND_{REF}	Ground Voltage Reference for the ADC. For optimal performance, the analog power supply should be separated from DGND.
3	3	C5	DAC0	DAC0 Voltage Output or ADC Input.
4	4	C6	DAC1	DAC1 Voltage Output or ADC Input.
5	5	D5	DAC2	DAC2 Voltage Output
6	6	D6	DAC3	DAC3 Voltage Output
24	20	D2	TMS	Test Mode Select, JTAG Test Port Input. Debug and download access. This pin has an internal pull-up resistor to IOV_{DD}. In some cases an external pull-up resistor is also required to ensure the part does not enter an erroneous state.
25	21	D1	P0.0/nTRST/ADC_{BUSY}/PLAI[8]/BM	This is a multifunction pin as follows: General-Purpose Input and Output Port 0.0. By default, this pin is configured as GPIO. JTAG Reset Input. Debug and download access. If this pin is held low, JTAG access is not possible because the JTAG interface is held in reset and P0.1/P0.2/P0.3 are configured as GPIO pins. ADC Busy Signal. Programmable Logic Array Input Element 8. Boot Mode Entry Pin. The ADuC7023 enters I^2C download mode if BM is low at reset with a flash address 0x80014 = 0xFFFFFFFF. The ADuC7023 executes code if BM is pulled high at reset or if BM is low at reset with a flash address 0x80014 not equal to 0xFFFFFFFF.
26	22	C1	P0.1/PLAI[9]/TDO	The default value of this pin depends on the level of P0.0/BM. If P0.0/BM = 0, this pin defaults to a general purpose input. If P0.0/BM = 1, this pin defaults to a JTAG test data output pin and does not work as a GPIO. This is a multifunction pin as follows: General-Purpose Input and Output Port 0.1. Programmable Logic Array Input Element 9. Test Data Out, JTAG Test Port Output. Debug and download access. When debugging the part via JTAG, this pin must not be toggled by user code, and the GP0CON/GP0DAT register bits affecting this pin must not be changed as doing so disables JTAG access.
27	23	C2	P0.2/PLAO[8]/TDI	The default value of this pin depends on the level of P0.0/BM. If P0.0/BM = 0, this pin defaults to a general purpose input. If P0.0/BM = 1, this pin defaults to a JTAG test data input pin and does not work as a GPIO. This is a multifunction pin as follows: General-Purpose Input and Output Port 0.2. Programmable Logic Array Output Element 8. Test Data In, JTAG Test Port Input. Debug and download access. When debugging the part via JTAG, this pin must not be toggled by user code, and the GP0CON/GP0DAT register bits affecting this pin must not be changed as doing so disables JTAG access.

Pin No.				
40-LFCSP	32-LFCSP	36-WLCSP	Mnemonic	Description
28	24	C3	P0.3/PLAO[9]/TCK	The default value of this pin depends on the level of P0.0/BM. If P0.0/BM = 0, this pin defaults to a general purpose input. If P0.0/BM = 1, this pin defaults to a JTAG test data clock pin. This is a multifunction pin as follows: General-Purpose Input and Output Port 0.3. Programmable Logic Array Output Element 9. Test Clock, JTAG Test Port Clock Input. Debug and download access. When debugging the part via JTAG, this pin must not be toggled by user code and the GP0CON/GP0DAT register bits affecting this pin must not be changed as doing so disables JTAG access.
17	13	E3	DGND	Digital Ground.
18	14	F3	IOV_{DD}	3.3 V Supply for GPIO and Input of the On-Chip Voltage Regulator.
19	15	D3	LV_{DD}	2.6 V Output of the On-Chip Voltage Regulator. This output must be connected to a 0.47 µF capacitor to DGND only.
20	16	F2	$\overline{RST}$	Reset Input, Active Low.
23	19	E1	RTCK	Return JTAG Clock Signal. This is not the standard JTAG clock signal. It is an output signal from the JTAG controller. If using a 20-lead JTAG header, connect to Pin 11.
9	7	F6	P0.4/IRQ0/SCL0/PLAI[0]/CONV	General-Purpose Input and Output Port 0.4/External Interrupt Request 0/ I^2C0 Clock Signal/Programmable Logic Array Input Element 0/ADC External Convert Start. By default, this pin is configured as a digital input with a weak pull-up resistor enabled.
10	8	E5	P0.5/SDA0/PLAI[1]/$COMP_{OUT}$	General-Purpose Input and Output Port 0.5/I^2C0 Data Signal/ Programmable Logic Array Input Element 1/Voltage Comparator Output. By default, this pin is configured as a digital input with a weak pull-up resistor enabled.
	9	F5	P0.6/MISO/SCL1/PLAI[2]	General-Purpose Input and Output Port 0.6/SPI MISO Signal/I^2C1 Clock On 32-Lead and 36-Ball Packages/Programmable Logic Array Input Element 2. By default, this pin is configured as a digital input with a weak pull-up resistor enabled.
	10	D4	P0.7/MOSI/SDA1/PLAO[0]	General-Purpose Input and Output Port 0.7/SPI MOSI Signal/I^2C1 Data Signal On 32-Lead and 36-Ball Packages/Programmable Logic Array Output Element 0. By default, this pin is configured as a digital input with a weak pull-up resistor enabled.
11			P0.6/MISO/PLAI[2]	General-Purpose Input and Output Port 0.6/SPI MISO Signal/Programmable Logic Array Input Element 2. By default, this pin is configured as a digital input with a weak pull-up resistor enabled.
12			P0.7/MOSI/PLAO[0]	General-Purpose Input and Output Port 0.7/SPI MOSI Signal/Programmable Logic Array Output Element 0. By default this pin is configured as a digital input with a weak pull-up reisistor enabled.
21	17	F1	XCLKI	Input to the Crystal Oscillator Inverter and Input to the Internal Clock Generator Circuits. Connect to DGND if unused.
22	18	E2	XCLKO	Output from the Crystal Oscillator Inverter. Leave unconnected if unused.
16	N/A	N/A	P1.7/PWM3/SDA1/PLAI[6]	General-Purpose Input and Output Port 1.7/PWM Output 3/I^2C1 Data Signal/Programmable Logic Array Input Element 6. By default, this pin is configured as a digital input with a weak pull-up resistor enabled.
15	N/A	N/A	P1.6/PWM2/SCL1/PLAI[5]	General-Purpose Input and Output Port 1.6/PWM Output 2/I^2C1 Clock Signal/Programmable Logic Array Input Element 5. By default, this pin is configured as a digital input with a weak pull-up resistor enabled.
29	N/A	N/A	P1.5/ADC6/$PWM_{TRIPINPUT}$/PLAO[4]	General-Purpose Input and Output Port 1.5/ADC Single-Ended or Differential Analog Input 6/$PWM_{TRIPINPUT}$/Programmable Logic Array Output Element 4. By default, this pin is configured as a digital input with a weak pull-up resistor enabled. When used as ADC input, the pull-up resistor should be disabled manually.
7	N/A	N/A	P1.4/ADC10/PLAO[3]	General-Purpose Input and Output Port 1.4/ADC Single-Ended or Differential Analog Input 10/Programmable Logic Array Output Element 3. By default, this pin is configured as a digital input with a weak pull-up resistor enabled. When used as ADC input, the pull-up resistor should be disabled manually.

Pin No.				
40-LFCSP	32-LFCSP	36-WLCSP	Mnemonic	Description
34	26	A3	P1.3/ADC5/IRQ3/PLAI[4]	General-Purpose Input and Output Port 1.3/ADC Single-Ended or Differential Analog Input 5/External Interrupt Request 3/ Programmable Logic Array Input Element 4. By default, this pin is configured as a digital input with a weak pull-up resistor enabled. When used as ADC input, the pull-up resistor should be disabled manually.
33	25	A2	P1.2/ADC4/IRQ2/PLAI[3]/ECLK/	General-Purpose Input and Output Port 1.2/ADC Single-Ended or Differential Analog Input 4/External Interrupt Request 2/ Programmable Logic Array Input Element 3/Input-Output for External Clock. By default, this pin is configured as a digital input with a weak pull-up resistor enabled. When used as ADC input, the pull-up resistor should be disabled manually.
14	12	F4	P1.1/$\overline{SS}$/IRQ1/PWM1/PLAO[2]/T1	General-Purpose Input and Output Port 1.1/SPI Interface Slave Select (Active Low)/External Interrupt Request 1/PWM Output 1/ Programmable Logic Array Output Element 2/Timer 1 Input Clock. By default, this pin is configured as a digital input with a weak pull-up resistor enabled.
13	11	E4	P1.0/SCLK/PWM0/PLAO[1]	General-Purpose Input and Output Port 1.0/SPI Interface Clock Signal/ PWM Output 0/Programmable Logic Array Output Element 1. By default, this pin is configured as a digital input with a weak pull-up resistor enabled.
35	27	B3	V_{REF}	2.5 V Internal Voltage Reference. Must be connected to a 0.47 µF capacitor when using the internal reference.
40	32	A6	AGND	Analog Ground. Ground reference point for the analog circuitry.
1	1	B6	AV_{DD}	3.3 V Analog Power.

TYPICAL PERFORMANCE CHARACTERISTICS

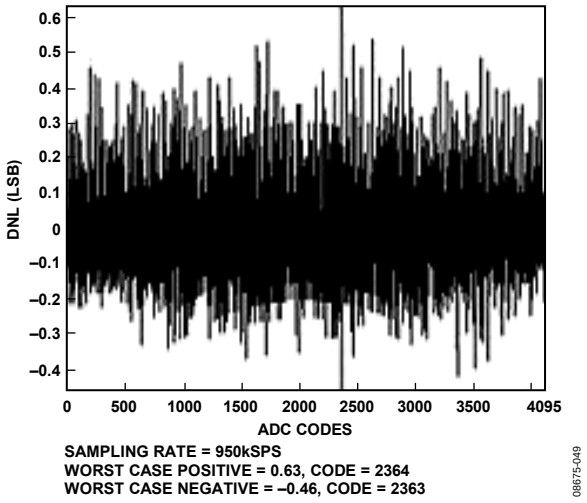

Figure 10. Typical DNL, f_{ADC} = 950 kSPS, Internal Reference Used

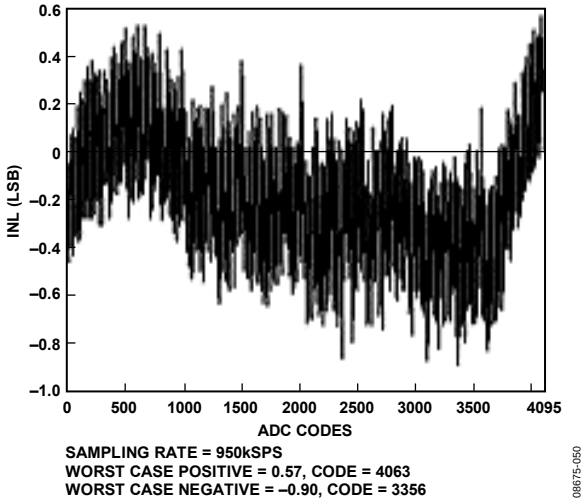

Figure 11. Typical INL, f_{ADC} = 950 kSPS, Internal Reference Used

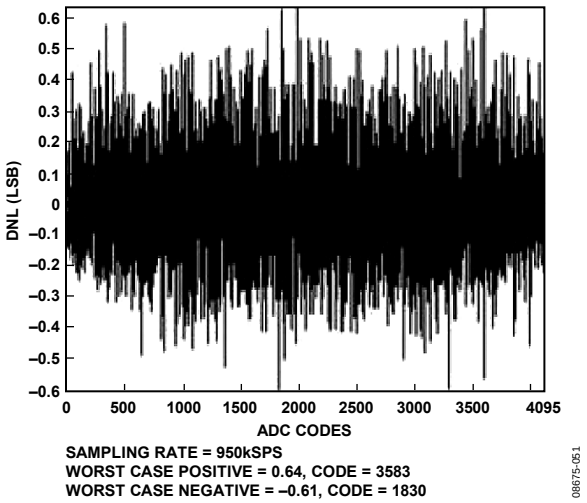

Figure 12. Typical DNL, f_{ADC} = 950 kSPS, External 1.0 V Reference Used

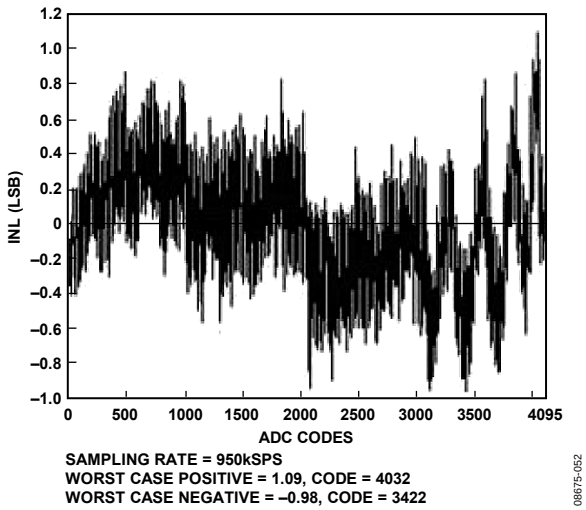

Figure 13. Typical INL, f_{ADC} = 950 kSPS, External 1.0 V Reference Used

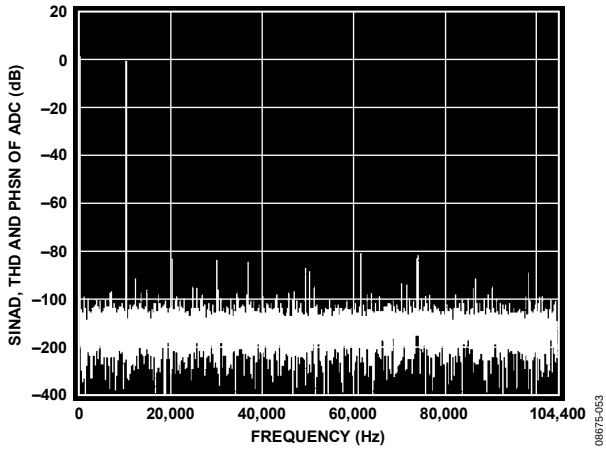

Figure 14. SINAD, THD, and PHSN of ADC , Internal 2.5 V Reference Used

More information relative to the model of the programmer and the ARM7TDMI core architecture can be found in ARM7TDMI technical and ARM architecture manuals available directly from ARM Ltd.

INTERRUPT LATENCY

The worst-case latency for a fast interrupt request (FIQ) consists of the following: the longest time the request can take to pass through the synchronizer, the time for the longest instruction to complete (the longest instruction is an LDM) that loads all the registers including the PC, and the time for the data abort and FIQ entry.

At the end of this time, the ARM7TDMI executes the instruction at 0x1C (FIQ interrupt vector address). The maximum total time is 50 processor cycles, which is just under 1.2 μs in a system using a continuous 41.78 MHz processor clock.

The maximum interrupt request (IRQ) latency calculation is similar but must allow for the fact that FIQ has higher priority and could delay entry into the IRQ handling routine for an arbitrary length of time. This time can be reduced to 42 cycles if the LDM command is not used. Some compilers have an option to compile without using this command. Another option is to run the part in thumb mode where the time is reduced to 22 cycles.

The minimum latency for FIQ or IRQ interrupts is a total of five cycles, which consist of the shortest time the request can take through the synchronizer, plus the time to enter the exception mode.

The ARM7TDMI always runs in ARM (32-bit) mode when in privileged modes, for example, when executing interrupt service routines.

MEMORY ORGANIZATION

The ADuC7023 incorporates two separate blocks of memory: 8 kB of SRAM and 64 kB of on-chip Flash/EE memory; 62 kB of on-chip Flash/EE memory is available to the user, and the remaining 2 kB are reserved for the factory configured boot page. These two blocks are mapped as shown in Figure 16.

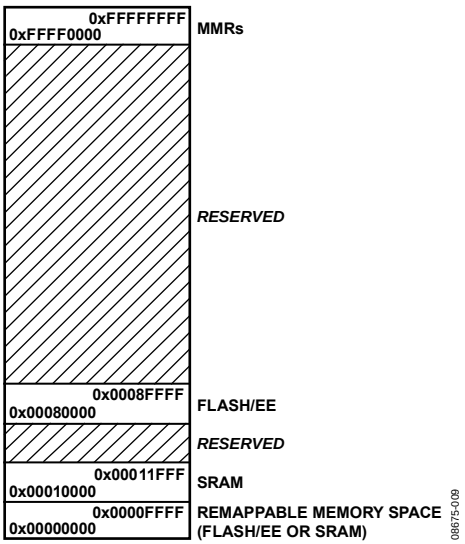

Figure 16. Physical Memory Map

By default, after a reset, the Flash/EE memory is mirrored at Address 0x00000000. It is possible to remap the SRAM at Address 0x00000000 by clearing Bit 0 of the Remap MMR. This remap function is described in more detail in the Flash/EE Memory section.

MEMORY ACCESS

The ARM7 core sees memory as a linear array of the 2^{32} byte location where the different blocks of memory are mapped as outlined in Figure 16.

The ADuC7023 memory organizations are configured in little endian format, which means that the least significant byte is located in the lowest byte address, and the most significant byte is in the highest byte address.

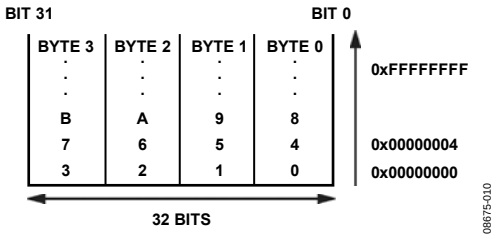

Figure 17. Little Endian Format

FLASH/EE MEMORY

The total 64 kB of Flash/EE memory is organized as 32k × 16 bits; 31k × 16 bits is user space and 1 k × 16 bits is reserved for the on-chip kernel. The page size of this Flash/EE memory is 512 bytes.

62 kilobytes of Flash/EE memory are available to the user as code and nonvolatile data memory. There is no distinction between data and program because ARM code shares the same space. The real width of the Flash/EE memory is 16 bits, which means that in ARM mode (32-bit instruction), two accesses to the Flash/EE are necessary for each instruction fetch. It is, therefore, recommended to use Thumb mode when executing from Flash/EE memory for optimum access speed. The maximum access speed for the Flash/EE memory is 41.78 MHz in Thumb mode and 20.89 MHz in full ARM mode. More details about Flash/EE access time are outlined later in the Execution Time from SRAM and Flash/EE section.

SRAM

Eight kilobytes of SRAM are available to the user, organized as 2k × 32 bits, that is, two words. ARM code can run directly from SRAM at 41.78 MHz, given that the SRAM array is configured as a 32-bit wide memory array. More details about SRAM access time are outlined later in the Execution Time from SRAM and Flash/EE section.

MEMORY MAPPED REGISTERS

The memory mapped register (MMR) space is mapped into the upper two pages of the memory array and accessed by indirect addressing through the ARM7 banked registers.

The MMR space provides an interface between the CPU and all on-chip peripherals. All registers, except the core registers, reside in the MMR area. All shaded locations shown in Figure 18 are unoccupied or reserved locations and should not be accessed by user software. Table 10 to Table 23 show the full MMR memory map.

The access time for reading from or writing to an MMR depends on the advanced microcontroller bus architecture (AMBA) bus used to access the peripheral. The processor has two AMBA buses: advanced high performance bus (AHB) used for system modules and advanced peripheral bus (APB) used for lower performance peripheral. Access to the AHB is one cycle, and access to the APB is two cycles. All peripherals on the ADuC7023 are on the APB except the Flash/EE memory and the GPIOs.

ADCCN Register

Name: ADCCN

Address: 0xFFFF0508

Default value: 0x01

Access: Read/write

Function: ADCCN is an ADC negative channel selection register. This MMR is described in Table 26.

Table 26. ADCCN MMR Bit Designation

Bit	Value	Description
7 to 5		Reserved.
4 to 0		Negative channel selection bits.
	00000	ADC0.
	00001	ADC1.
	00010	ADC2.
	00011	ADC3.
	00100	ADC4.
	00101	ADC5.
	00110	ADC6.
	00111	ADC7.
	01000	ADC8.
	01001	ADC9.
	01010	ADC10.
	01011	Reserved
	01100	ADC12.
	01101	Reserved
	01110	Reserved
	01111	DAC1.
	10000	Temperature sensor.
	10001	AGND (self-diagnostic feature).
	10010	Internal reference (self-diagnostic feature).
	10011	Reserved
	Others	Reserved.

ADCSTA Register

Name: ADCSTA

Address: 0xFFFF050C

Default Value: 0x00

Access: Read

Function: ADCSTA is an ADC status register that indicates when an ADC conversion result is ready. The ADCSTA register contains only one bit, ADCReady (Bit 0), representing the status of the ADC. This bit is set at the end of an ADC conversion, generating an ADC interrupt. It is cleared automatically by reading the ADCDAT MMR. When the ADC is performing a conversion, the status of the ADC can be read externally via the ADC_{BUSY} pin. This pin is high during a conversion. When the conversion is finished, ADC_{BUSY} goes back low. This information can be available on P0.0 (see the General-Purpose Input/Output section) if enabled in the ADCCON register.

ADCDAT Register

Name: ADCDAT

Address: 0xFFFF0510

Default value: 0x00000000

Access: Read

Function: ADCDAT is an ADC data result register. Hold the 12-bit ADC result as shown in Figure 22.

ADCRST Register

Name: ADCRST

Address: 0xFFFF0514

Default Value: 0x00

Access: Read/write

Function: ADCRST resets the digital interface of the ADC. Writing any value to this register resets all the ADC registers to their default value.

EXECUTION TIME FROM SRAM AND FLASH/EE

Execution from SRAM

Fetching instructions from SRAM takes one clock cycle because the access time of the SRAM is 2 ns, and a clock cycle is 22 ns minimum. However, if the instruction involves reading or writing data to memory, one extra cycle must be added if the data is in SRAM (or three cycles if the data is in Flash/EE); one cycle to execute the instruction and two cycles to obtain the 32-bit data from Flash/EE. A control flow instruction (a branch instruction, for example) takes one cycle to fetch but also takes two cycles to fill the pipeline with the new instructions.

Execution from Flash/EE

Because the Flash/EE width is 16 bits and the access time for 16-bit words is 22 ns, execution from Flash/EE cannot be completed in one cycle (as can be done from SRAM when the CD bit = 0). Also, some dead times are needed before accessing data for any value of CD bits.

In ARM mode, where instructions are 32 bits, two cycles are needed to fetch any instruction when CD = 0. In thumb mode, where instructions are 16 bits, one cycle is needed to fetch any instruction.

Timing is identical in both modes when executing instructions that involve using the Flash/EE for data memory. If the instruction to be executed is a control flow instruction, an extra cycle is needed to decode the new address of the program counter, and then four cycles are needed to fill the pipeline. A data processing instruction involving only the core register does not require any extra clock cycles. However, if it involves data in Flash/EE, an extra clock cycle is needed to decode the address of the data, and two cycles are needed to get the 32-bit data from Flash/EE. An extra cycle must also be added before fetching another instruction. Data transfer instructions are more complex and are summarized in Table 35.

Table 35. Execution Cycles in ARM/Thumb Mode

Instructions	Fetch Cycles	Dead Time	Data Access	Dead Time
LD[1]	2/1	1	2	1
LDH	2/1	1	1	1
LDM/PUSH	2/1	N[2]	2 × N[2]	N[1]
STR[1]	2/1	1	2 × 20 ns	1
STRH	2/1	1	20 ns	1
STRM/POP	2/1	N[1]	2 × N × 20 ns[1]	N[1]

[1] The SWAP instruction combines an LD and STR instruction with only one fetch, giving a total of eight cycles + 40 ns.
[2] N is the number of data to load or store in the multiple load/store instruction (1 < N ≤ 16).

RESET AND REMAP

The ARM exception vectors are all situated at the bottom of the memory array, from Address 0x00000000 to Address 0x00000020 as shown in Figure 31.

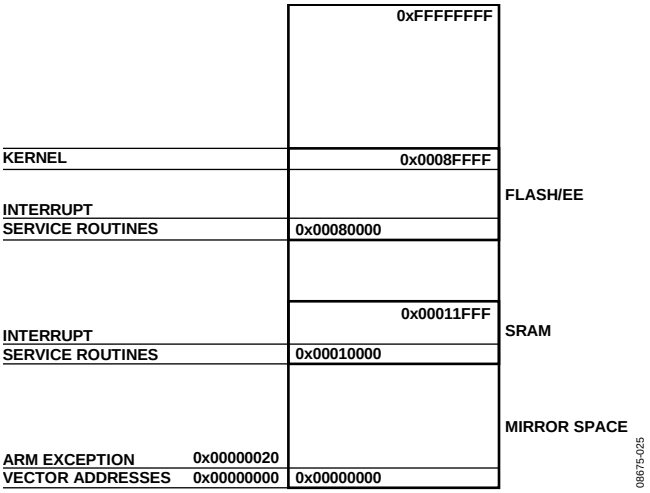

Figure 31. Remap for Exception Execution

By default, and after any reset, the Flash/EE is mirrored at the bottom of the memory array. The remap function allows the programmer to mirror the SRAM at the bottom of the memory array, which facilitates execution of exception routines from SRAM instead of from Flash/EE. This means exceptions are executed twice as fast, being executed in 32-bit ARM mode with 32-bit wide SRAM instead of 16-bit wide Flash/EE memory.

Remap Operation

When a reset occurs on the ADuC7023, execution automatically starts in factory programmed, internal configuration code. This kernel is hidden and cannot be accessed by user code. If the part is in normal mode (BM pin is high), it executes the power-on configuration routine of the kernel and then jumps to the reset vector address, 0x00000000, to execute the reset exception routine of the user.

Because the Flash/EE is mirrored at the bottom of the memory array at reset, the reset interrupt routine must always be written in Flash/EE.

The remap is done from Flash/EE by setting Bit 0 of the Remap register. Caution must be taken to execute this command from Flash/EE above Address 0x00080020, and not from the bottom of the array because this is replaced by the SRAM.

This operation is reversible. The Flash/EE can be remapped at Address 0x00000000 by clearing Bit 0 of the Remap MMR. Caution must again be taken to execute the remap function from outside the mirrored area. Any type of reset remaps the Flash/EE memory at the bottom of the array.

OTHER ANALOG PERIPHERALS

DAC

The ADuC7023 incorporates four, 12-bit voltage output DACs on chip. Each DAC has a rail-to-rail voltage output buffer capable of driving 5 kΩ/100 pF.

Each DAC has two selectable ranges: 0 V to V_{REF} (internal band gap 2.5 V reference) and 0 V to AV_{DD}.

The signal range is 0 V to AV_{DD}.

By setting RSTCFG Bit 2, the DAC output pins can retain their state during a watchdog or software reset.

MMRs Interface

Each DAC is independently configurable through a control register and a data register. These two registers are identical for the four DACs. Only DAC0CON (see Table 40) and DAC0DAT (see Table 41) are described in detail in this section.

DACxCON Registers

Name	Address	Default Value	Access
DAC0CON	0xFFFF0600	0x00	R/W
DAC1CON	0xFFFF0608	0x00	R/W
DAC2CON	0xFFFF0610	0x00	R/W
DAC3CON	0xFFFF0618	0x00	R/W

Table 40. DAC0CON MMR Bit Designations

Bit	Value	Name	Description
7			Reserved.
6		DACBY	This bit is set to bypass the DAC output buffer. This bit is cleared to enable the DAC output buffer.
5		DACCLK	DAC update rate. This bit is set by the user to update the DAC using Timer1. This bit is cleared by the user to update the DAC using HCLK (core clock).
4		DACCLR	DAC clear bit. This bit is set by the user to enable normal DAC operation. This bit is cleared by the user to reset data register of the DAC to 0.
3			Reserved. This bit remains at 0.
2			Reserved. This bit remains at 0.
1 to 0			DAC range bits.
	00		Power-down mode. The DAC output is in tristate.
	01		Reserved.
	10		0 V to V_{REF} (2.5 V) range.
	11		0 V to AV_{DD} range.

DACxDAT Registers

Name	Address	Default Value	Access
DAC0DAT	0xFFFF0604	0x00000000	R/W
DAC1DAT	0xFFFF060C	0x00000000	R/W
DAC2DAT	0xFFFF0614	0x00000000	R/W
DAC3DAT	0xFFFF061C	0x00000000	R/W

Table 41. DAC0DAT MMR Bit Designations

Bit	Description
31 to 28	Reserved.
27 to 16	12-bit data for DAC0.
15 to 0	Reserved.

Using the DACs

The on-chip DAC architecture consists of a resistor string DAC followed by an output buffer amplifier. The functional equivalent is shown in Figure 32.

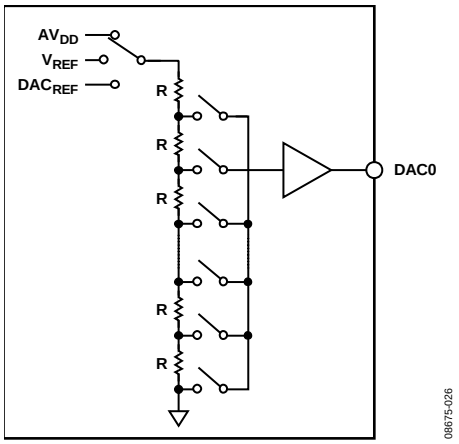

Figure 32. DAC Structure

As illustrated in Figure 32, the reference source for each DAC is user-selectable in software. It can be either AV_{DD} or V_{REF}. In 0-to-AV_{DD} mode, the DAC output transfer function spans from 0 V to the voltage at the AV_{DD} pin. In 0-to-V_{REF} mode, the DAC output transfer function spans from 0 V to the internal 2.5 V reference, V_{REF}.

The DAC output buffer amplifier features a true, rail-to-rail output stage implementation. This means that when unloaded, each output is capable of swinging to within less than 5 mV of both AV_{DD} and ground. Moreover, the DAC linearity specification (when driving a 5 kΩ resistive load to ground) is guaranteed through the full transfer function except Code 0 to Code 100, and, in 0-to-AV_{DD} mode only, Code 3995 to Code 4095.

Linearity degradation near ground and V_{DD} is caused by saturation of the output amplifier, and a general representation of its effects (neglecting offset and gain error) is illustrated in Figure 33. The dotted line in Figure 33 indicates the ideal transfer function, and the solid line represents what the transfer function may look like with endpoint nonlinearities due to saturation of the output amplifier. Figure 33 represents a transfer function in 0-to-AV_{DD}

Bit	GP0PAR	GP1PAR	GP2PAR
10 to 9	R (b00)	R (b00)	R (b00)
8	R/W	R/W	R/W
7	Reserved	Reserved	Reserved
6 to 5	R (b00)	R (b00)	Reserved
4	R/W	R/W	Reserved
3	Reserved	Reserved	Reserved
2 to 1	R (b00)	R (b00)	R (b00)
0	R/W	R/W	R (b0)

[1] When P2.0 is configured as AIN12, the internal pull-up resistor cannot be disabled.

GP0DAT Register

Name	Address	Default Value	Access
GP0DAT	0xFFFFF420	0x000000XX	R/W
GP1DAT	0xFFFFF430	0x000000XX	R/W
GP2DAT	0xFFFFF440	0x000000XX	R/W

GPxDAT are Port x configuration and data registers. They configure the direction of the GPIO pins of Port x, set the output value for the pins configured as output, and store the input value of the pins configured as input.

Table 60. GPxDAT MMR Bit Descriptions

Bit	Description
31 to 24	Direction of the data. This bit is set to 1 by the user to configure the GPIO pin as an output. This bit is cleared to 0 by the user to configure the GPIO pin as an input.
23 to 16	Port x data output.
15 to 8	Reflect the state of Port x pins at reset (read only).
7 to 0	Port x data input (read only).

GP0SET Register

Name: GP0SET

Address: 0xFFFFF424

Default value: 0x000000XX

Access: Write

Function: GP0SET is a data set Port x register.

GP1SET Register

Name: GP1SET

Address: 0xFFFFF434

Default value: 0x000000XX

Access: Write

Function: GP1SET is a data set Port x register.

GP2SET Register

Name: GP2SET

Address: 0xFFFFF444

Default value: 0x000000XX

Access: Write

Function: GP2SET is a data set Port x register.

Table 61. GPxSET MMR Bit Descriptions

Bit	Description
31 to 24	Reserved.
23 to 16	Data port x. This bit is set to 1 by the user to set bit on Port x; this bit also sets the corresponding bit in the GPxDAT MMR. This bit is cleared to 0 by the user; this bit does not affect the data out.
15 to 0	Reserved.

GP0CLR Registers

Name: GP0CLR

Address: 0xFFFFF428

Default value: 0x000000XX

Access: Write

Function: GP0CLR is a data clear Port x register.

GP1CLR Registers

Name: GP1CLR

Address: 0xFFFFF438

Default value: 0x000000XX

Access: Write

Function: GP1CLR is a data clear Port x register.

GP2CLR Registers

Name: GP2CLR

Address: 0xFFFFF448

Default value: 0x000000XX

Access: Write

Function: GP2CLR is a data clear Port x register.

Table 64. SPICON MMR Bit Designations

Bit	Name	Description
15 to 14	SPIMDE	SPI IRQ mode bits. These bits configure when the Tx/Rx interrupts occur in a transfer. [00] = Tx interrupt occurs when one byte has been transferred. Rx interrupt occurs when one or more bytes have been received into the FIFO. [01] = Tx interrupt occurs when two bytes has been transferred. Rx interrupt occurs when two or more bytes have been received into the FIFO. [10] = Tx interrupt occurs when three bytes has been transferred. Rx interrupt occurs when three or more bytes have been received into the FIFO. [11] = Tx interrupt occurs when four bytes has been transferred. Rx interrupt occurs when the Rx FIFO is full or four bytes present.
13	SPITFLH	SPI Tx FIFO flush enable bit. This bit is set to flush the Tx FIFO. This bit does not clear itself and should be toggled if a single flush is required. If this bit is left high, then either the last transmitted value or 0x00 is transmitted depending on the SPIZEN bit. Any writes to the Tx FIFO are ignored while this bit is set. This bit is cleared to disable Tx FIFO flushing.
12	SPIRFLH	SPI Rx FIFO flush enable bit. This bit is set to flush the Rx FIFO. This bit does not clear itself and should be toggled if a single flush is required. If this bit is set, all incoming data is ignored and no interrupts are generated. If set and SPITMDE = 0, a read of the Rx FIFO initiates a transfer. This bit is cleared to disable Rx FIFO flushing.
11	SPICONT	Continuous transfer enable. This bit is set by the user to enable continuous transfer. In master mode, the transfer continues until no valid data is available in the Tx register. $\overline{SS}$ is asserted and remains asserted for the duration of each 8-bit serial transfer until Tx is empty. This bit is cleared by the user to disable continuous transfer. Each transfer consists of a single 8-bit serial transfer. If valid data exists in the SPITX register, then a new transfer is initiated after a stall period of 1 serial clock cycle.
10	SPILP	Loop back enable bit. This bit is set by the user to connect MISO to MOSI and test software. This bit is cleared by the user to be in normal mode.
9	SPIOEN	Slave MISO output enable bit. This bit is set for MISO to operate as normal. This bit is cleared to disable the output driver on the MISO pin. The MISO pin is open-drain when this bit is clear.
8	SPIROW	SPIRX overflow overwrite enable. This bit is set by the user; the valid data in the Rx register is overwritten by the new serial byte received. This bit is cleared by the user; the new serial byte received is discarded.
7	SPIZEN	SPI transmit zeros when Tx FIFO is empty. This bit is set to transmit 0x00 when there is no valid data in the Tx FIFO. This bit is cleared to transmit the last transmitted value when there is no valid data in the Tx FIFO.
6	SPITMDE	SPI transfer and interrupt mode. This bit is set by the user to initiate transfer with a write to the SPITX register. Interrupt only occurs when Tx is empty. This bit is cleared by the user to initiate transfer with a read of the SPIRX register. Interrupt only occurs when Rx is full.
5	SPILF	LSB first transfer enable bit. This bit is set by the user; the LSB is transmitted first. This bit is cleared by the user; the MSB is transmitted first.
4	SPIWOM	SPI wired or mode enable bit. This bit is set to 1 enable open-drain data output. External pull-ups are required on data out pins. This bit is cleared for normal output levels.
3	SPICPO	Serial clock polarity mode bit. This bit is set by the user; the serial clock idles high. This bit is cleared by the user; the serial clock idles low.
2	SPICPH	Serial clock phase mode bit. This bit is set by the user; the serial clock pulses at the beginning of each serial bit transfer. This bit is cleared by the user; the serial clock pulses at the end of each serial bit transfer.

I²C Master Status Registers, I2CxMSTA

Name: I2C0MSTA , I2C1MSTA

Address: 0xFFFF0804, 0xFFFF0904

Default value: 0x0000, 0x0000

Access: Read

Function: These 16-bit MMRs are the I²C status registers in master mode.

Table 66. I2CxMSTA MMR Bit Designations

Bit	Name	Description
15 to 11		Reserved. These bits are reserved.
10	I2CBBUSY	I²C bus busy status bit. This bit is set to 1 when a start condition is detected on the I²C bus. This bit is cleared when a stop condition is detected on the bus.
9	I2CMRxFO	Master Rx FIFO overflow. This bit is set to 1 when a byte is written to the Rx FIFO when it is already full. This bit is cleared in all other conditions.
8	I2CMTC	I²C transmission complete status bit. This bit is set to 1 when a transmission is complete between the master and the slave with which it was communicating. If the I2CMCENI bit in I2CxMCON is set, an interrupt is generated when this bit is set. This bit clears this interrupt source.
7	I2CMNA	I²C master no acknowledge data bit. This bit is set to 1 when a no acknowledge condition is received by the master in response to a data write transfer. If the I2CNACKENI bit in I2CxMCON is set, an interrupt is generated when this bit is set. This bit is cleared in all other conditions.
6	I2CMBUSY	I²C master busy status bit. This bit is set to 1 when the master is busy processing a transaction. This bit is cleared if the master is ready or if another master device has control of the bus.
5	I2CAL	I²C arbitration lost status bit. This bit is set to 1 when the I²C master has lost in trying to gain control of the I²C bus. If the I2CALENI bit in I2C1MCON is set, an interrupt is generated when this bit is set. This bit is cleared in all other conditions.
4	I2CMNA	I²C master no acknowledge address bit. This bit is set to 1 when a no acknowledge condition is received by the master in response to an address. If the I2CNACKENI bit in I2C1MCON is set, an interrupt is generated when this bit is set. This bit is cleared in all other conditions.
3	I2CMRXQ	I²C master receive request bit. This bit is set to 1 when data enters the Rx FIFO. If the I2CMRENI in I2C1MCON is set, an interrupt is generated. This bit is cleared in all other conditions.
2	I2CMTXQ	I²C master transmit request bit. This bit becomes high if the Tx FIFO is empty or only contains one byte and the master has transmitted an address and write. If the I2CMTENI bit in I2C1MCON is set, an interrupt is generated when this bit is set. This bit is cleared in all other conditions.
1 to 0	I2CMTFSTA	I²C master Tx FIFO status bits. 00 = I²C master Tx FIFO empty. 01 = Reserved. 10 = 1 byte in master Tx FIFO. 11 = I²C master Tx FIFO full.

Table 77. PLAELMx MMR Bit Descriptions

Bit	Value	Description
31 to 11		Reserved.
10 to 9		Mux 0 control (see Table 81).
8 to 7		Mux 1 control (see Table 81).
6		Mux 2 control. This bit is set by the user to select the output of Mux 0. This bit is cleared by the user to select the bit value from the PLADIN register.
5		Mux 3 control. This bit is set by the user to select the input pin of the particular element. This bit is cleared by the user to select the output of Mux 1.
4 to 1		Look-up table control.
	0000	0.
	0001	NOR.
	0010	B and not A.
	0011	Not A.
	0100	A and not B.
	0101	Not B.
	0110	EXOR.
	0111	NAND.
	1000	AND.
	1001	EXNOR.
	1010	B.
	1011	Not A or B.
	1100	A.
	1101	A or not B.
	1110	OR.
	1111	1.
0		Mux 4 control. This bit is set by the user to bypass the flip-flop. This bit is cleared by the user to select the flip-flop (cleared by default).

PLACLK Register

Name: PLACLK

Address: 0xFFFF0B40

Default value: 0x00

Access: Read/write

Function: PLACLK is the clock selection for the flip-flops. The maximum frequency when using the GPIO pins as the clock input for the PLA blocks is 41.78 MHz.

Table 78. PLACLK MMR Bit Descriptions

Bit	Value	Description
31 to 7		Reserved.
6 to 4		Clock source selection.
	000	GPIO clock on P0.5.
	001	GPIO clock on P1.1.
	010	GPIO clock on P1.6.
	011	HCLK.
	100	External 32.768 kHz crystal.
	101	Timer1 overflow.
	110	UCLK.
	111	Internal 32,768 oscillator.
3		Reserved.
2 to 0		Clock source selection.
	000	GPIO clock on P0.5.
	001	GPIO clock on P1.1.
	010	GPIO clock on P1.6.
	011	HCLK.
	100	External 32.768 kHz crystal.
	101	Timer1 overflow.
	110	UCLK.
	111	Internal 32,768 oscillator.

Table 85. PWMCON1 MMR Bit Designations

Bit	Name	Description
14	SYNC	Enables PWM synchronization. Set to 1 by the user so that all PWM counters are reset on the next clock edge after the detection of a high-to-low transition on the P2.2/SYNC pin. Cleared by the user to ignore transitions on the P2.2/SYNC pin.
13	Reserved	Set to 0 by the user.
12	PWM3INV	Set to 1 by the user to invert PWM3. Cleared by the user to use PWM3 in normal mode.
11	PWM1INV	Set to 1 by the user to invert PWM1. Cleared by the user to use PWM1 in normal mode.
10	PWMTRIP	Set to 1 by the user to enable PWM trip interrupt. When the PWM trip input (Pin P1.5/$PWM_{TRIPINPUT}$) is low, the PWMEN bit is cleared and an interrupt is generated. Cleared by the user to disable the PWMTRIP interrupt.
9	ENA	If HOFF = 0 and HMODE = 1. Note that, if not in H-bridge mode, this bit has no effect. Set to 1 by the user to enable PWM outputs. Cleared by the user to disable PWM outputs. If HOFF = 1 and HMODE = 1, see Table 86.
8 to 6	PWMCP[2:0]	PWM clock prescaler bits. Sets the UCLK divider. [000] = UCLK/2. [001] = UCLK/4. [010] = UCLK/8. [011] = UCLK/16. [100] = UCLK/32. [101] = UCLK/64. [110] = UCLK/128. [111] = UCLK/256.
5	POINV	Set to 1 by the user to invert all PWM outputs. Cleared by the user to use PWM outputs as normal.
4	HOFF	High side off. Set to 1 by the user to force PWM0 and PWM2 outputs high. This also forces PWM1 and PWM3 low. Cleared by the user to use the PWM outputs as normal.
3	LCOMP	Load compare registers. Set to 1 by the user to load the internal compare registers with the values in PWMxCOMx on the next transition of the PWM timer from 0x00 to 0x01. Cleared by the user to use the values previously stored in the internal compare registers.
2	DIR	Direction control. Set to 1 by the user to enable PWM0 and PWM1 as the output signals while PWM2 and PWM3 are held low. Cleared by the user to enable PWM2 and PWM3 as the output signals while PWM0 and PWM1 are held low.
1	HMODE	Enables H-bridge mode.[1] Set to 1 by the user to enable H-bridge mode. Cleared by the user to operate the PWMs in standard mode.
0	PWMEN	Set to 1 by the user to enable all PWM outputs. Cleared by the user to disable all PWM outputs.

[1] In H-bridge mode, HMODE = 1. See Table 86 to determine the PWM outputs.

On power-up, PWMCON1 defaults to 0x0012 (HOFF = 1 and HMODE = 1). All GPIO pins associated with the PWM are configured in PWM mode by default (see Table 86). Clear the PWM trip interrupt by writing any value to the PWMCLRI MMR. Note that when using the PWM trip interrupt, clear the PWM interrupt before exiting the ISR. This prevents generation of multiple interrupts.

Table 86. PWM Output Selection

PWMCON1 MMR[1]				PWM Outputs[2]			
ENA	**HOFF**	**POINV**	**DIR**	**PWM0**	**PWM1**	**PWM2**	**PWM3**
0	0	X	X	1	1	1	1
X	1	X	X	1	0	1	0
1	0	0	0	0	0	HS1	LS1
1	0	0	1	HS1	LS1	0	0
1	0	1	0	HS1	LS1	1	1
1	0	1	1	1	1	HS1	LS1

[1] X is don't care.
[2] HS = high side, LS = low side.

Table 87. Compare Registers

Name	Address	Default Value	Access
PWM0COM0	0xFFFF0F84	0x0000	R/W
PWM0COM1	0xFFFF0F88	0x0000	R/W
PWM0COM2	0xFFFF0F8C	0x0000	R/W
PWM1COM0	0xFFFF0F94	0x0000	R/W
PWM1COM1	0xFFFF0F98	0x0000	R/W
PWM1COM2	0xFFFF0F9C	0x0000	R/W
PWM2COM0	0xFFFF0FA4	0x0000	R/W
PWM2COM1	0xFFFF0FA8	0x0000	R/W

POWER-ON RESET OPERATION

An internal power-on reset (POR) is implemented on the ADuC7023. For LV_{DD} below 2.40 V typical, the internal POR holds the part in reset. As LV_{DD} rises above 2.40 V, an internal timer times out for typically 64 ms before the part is released from reset. The user must ensure that the power supply IOV_{DD} has reached a stable 2.7 V minimum level by this time. Likewise, on power-down, the internal POR holds the part in reset until LV_{DD} has dropped below 2.40 V.

Figure 53 illustrates the operation of the internal POR in detail.

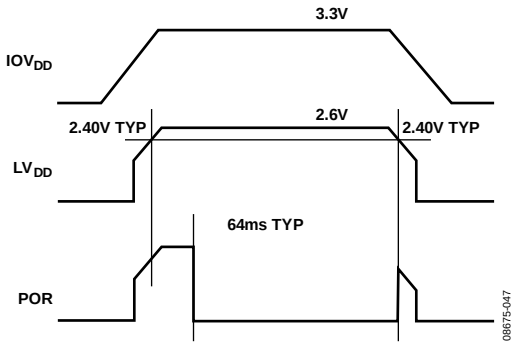

Figure 53. Internal Power-On Reset Operation

TYPICAL SYSTEM CONFIGURATION

A typical ADuC7023 configuration is shown in Figure 54. It summarizes some of the hardware considerations. The bottom of the LFCSP package has an exposed pad that needs to be soldered to a metal plate on the board for mechanical reasons. The metal plate of the board can be connected to ground.

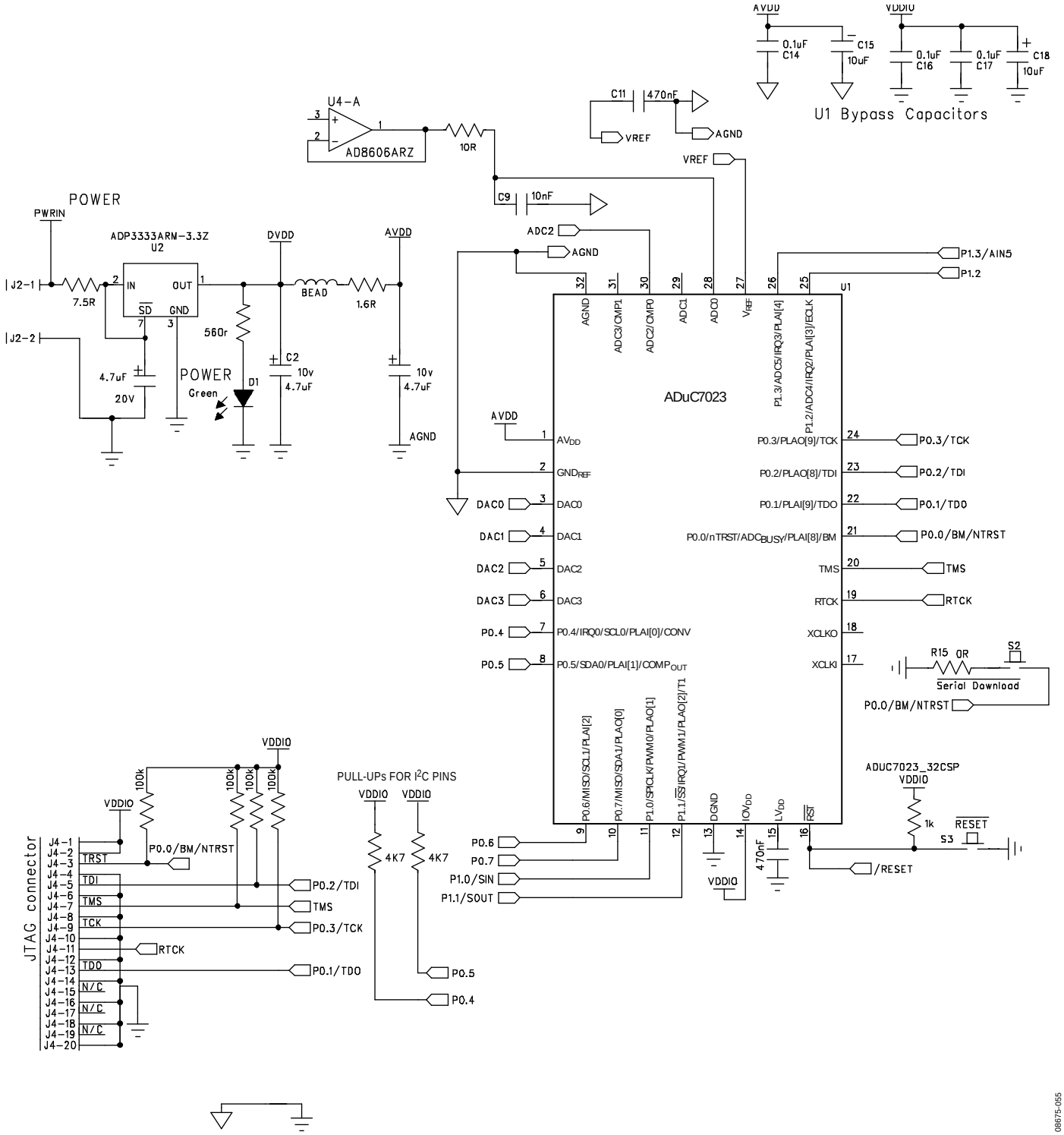

Figure 54. Typical System Configuration

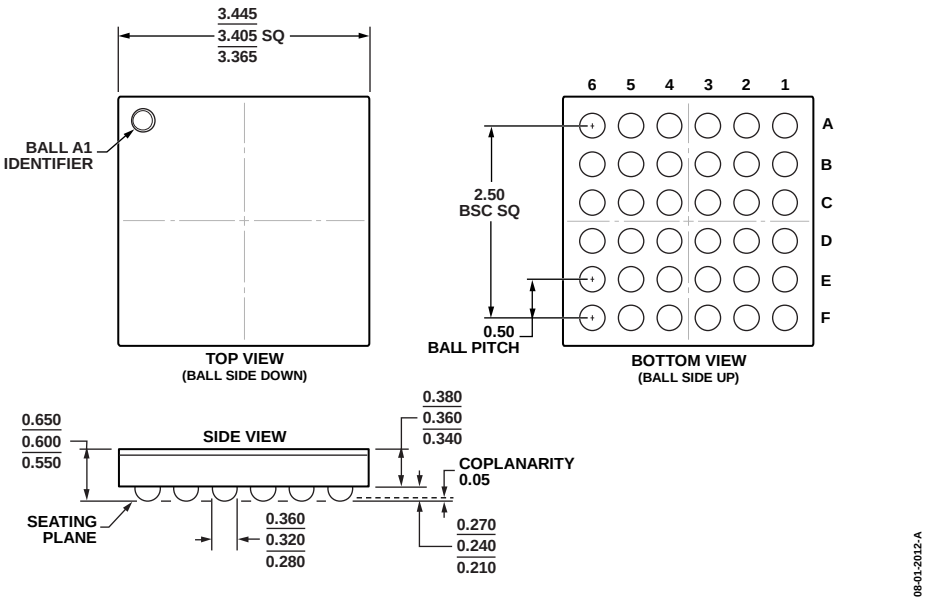

Figure 57. 36-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-36-3)
Dimensions shown in millimeters