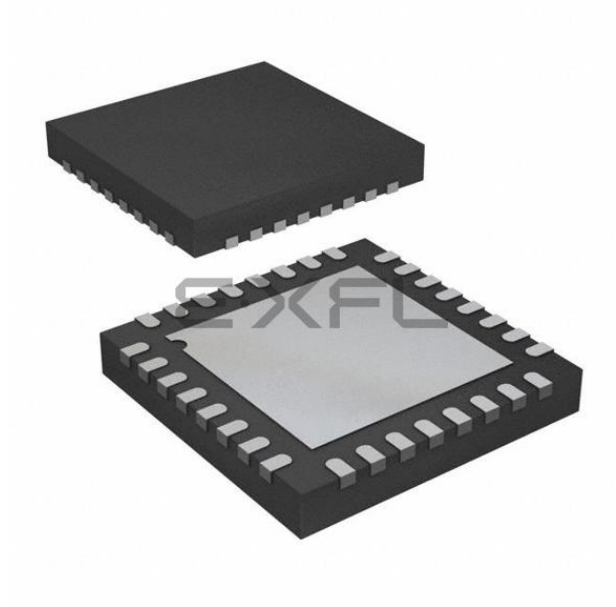

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Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 32
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Data Converters	A/D 8x12b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
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6/10—Rev. 0 to Rev. A

Changes to Temperature Sensor Parameter in Table 1 6
Changes to Table 24 29
Changes to Temperature Sensor Section 34
Changes to DACBKEY0 Register Section and to Table 43 47
Changes to Ordering Guide 93

1/10—Revision 0: Initial Version

Table 6. SPI Slave Mode Timing (Phase Mode = 1)

Parameter	Description	Min	Typ	Max	Unit
$t_{\overline{SS}}$	$\overline{SS}$ to SCLK edge	200			ns
t_{SL}	SCLK low pulse width[1]		(SPIDIV + 1) × t_{UCLK}		ns
t_{SH}	SCLK high pulse width[1]		(SPIDIV + 1) × t_{UCLK}		ns
t_{DAV}	Data output valid after SCLK edge			25	ns
t_{DSU}	Data input setup time before SCLK edge[1]	1 × t_{UCLK}			ns
t_{DHD}	Data input hold time after SCLK edge[1]	2 × t_{UCLK}			ns
t_{DF}	Data output fall time		5	12.5	ns
t_{DR}	Data output rise time		5	12.5	ns
t_{SR}	SCLK rise time		5	12.5	ns
t_{SF}	SCLK fall time		5	12.5	ns
t_{SFS}	$\overline{SS}$ high after SCLK edge	0			ns

[1] t_{UCLK} = 23.9 ns. It corresponds to the 41.78 MHz internal clock from the PLL before the clock divider.

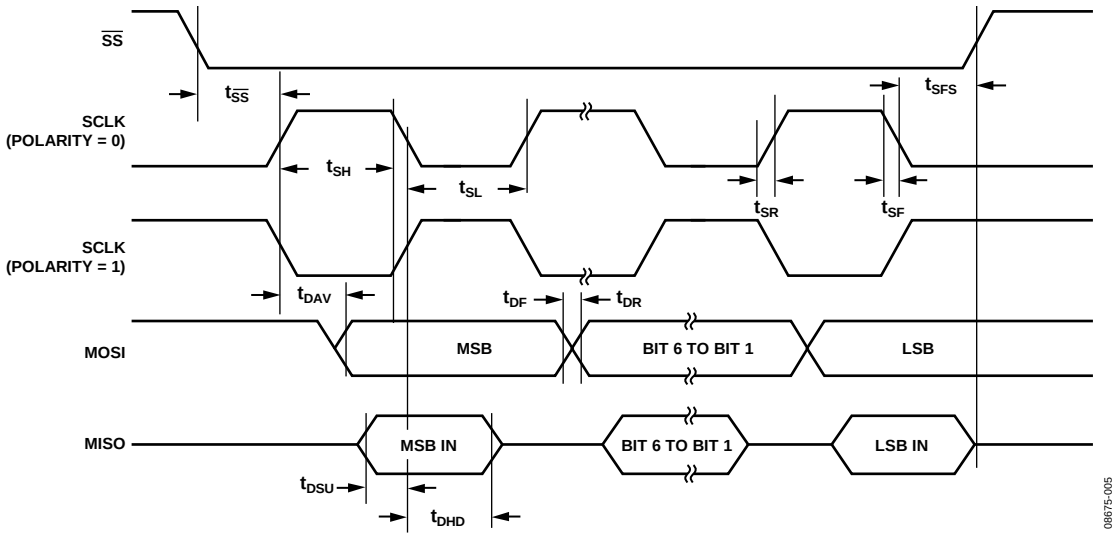

Figure 5. SPI Slave Mode Timing (Phase Mode = 1)

ABSOLUTE MAXIMUM RATINGS

AGND = GND_{REF}, T_A = 25°C, unless otherwise noted.

Table 8.

Parameter	Rating
AV_{DD} to IOV_{DD}	−0.3 V to +0.3 V
AGND to DGND	−0.3 V to +0.3 V
IOV_{DD} to DGND, AV_{DD} to AGND	−0.3 V to +6 V
Digital Input Voltage to DGND[1]	−0.3 V to +5.3 V
Digital Output Voltage to DGND[1]	−0.3 V to IOV_{DD} + 0.3 V
Shared Analog/Digital Inputs to AGND[2]	−0.3 V to AV_{DD} + 0.3 V
V_{REF} to AGND	−0.3 V to AV_{DD} + 0.3 V
Analog Inputs to AGND	−0.3 V to AV_{DD} + 0.3 V
Analog Outputs to AGND	−0.3 V to AV_{DD} + 0.3 V
Operating Temperature Range, Industrial	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance	
40-Lead LFCSP	26°C/W
32-Lead LFCSP	32.5°C/W
36-Lead WLCSP	50°C/W
Peak Solder Reflow Temperature	
SnPb Assemblies (10 sec to 30 sec)	240°C
RoHS Compliant Assemblies (20 sec to 40 sec)	260°C

[1] These limits apply to the P0.0, P0.1, P0.2, P0.3, P0.4, P0.5, P0.6, P0.7, P1.0, P1.1, P1.6, and P1.7 pins.
[2] These limits apply to the P1.2, P1.3, P1.4, P1.5, P2.0, P2.2, P2.3, and P2.4 pins.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Pin No.				
40-LFCSP	32-LFCSP	36-WLCSP	Mnemonic	Description
34	26	A3	P1.3/ADC5/IRQ3/PLAI[4]	General-Purpose Input and Output Port 1.3/ADC Single-Ended or Differential Analog Input 5/External Interrupt Request 3/ Programmable Logic Array Input Element 4. By default, this pin is configured as a digital input with a weak pull-up resistor enabled. When used as ADC input, the pull-up resistor should be disabled manually.
33	25	A2	P1.2/ADC4/IRQ2/PLAI[3]/ECLK/	General-Purpose Input and Output Port 1.2/ADC Single-Ended or Differential Analog Input 4/External Interrupt Request 2/ Programmable Logic Array Input Element 3/Input-Output for External Clock. By default, this pin is configured as a digital input with a weak pull-up resistor enabled. When used as ADC input, the pull-up resistor should be disabled manually.
14	12	F4	P1.1/$\overline{SS}$/IRQ1/PWM1/PLAO[2]/T1	General-Purpose Input and Output Port 1.1/SPI Interface Slave Select (Active Low)/External Interrupt Request 1/PWM Output 1/ Programmable Logic Array Output Element 2/Timer 1 Input Clock. By default, this pin is configured as a digital input with a weak pull-up resistor enabled.
13	11	E4	P1.0/SCLK/PWM0/PLAO[1]	General-Purpose Input and Output Port 1.0/SPI Interface Clock Signal/ PWM Output 0/Programmable Logic Array Output Element 1. By default, this pin is configured as a digital input with a weak pull-up resistor enabled.
35	27	B3	V_{REF}	2.5 V Internal Voltage Reference. Must be connected to a 0.47 µF capacitor when using the internal reference.
40	32	A6	AGND	Analog Ground. Ground reference point for the analog circuitry.
1	1	B6	AV_{DD}	3.3 V Analog Power.

Table 21. PWM Base Address = 0xFFFF0F80

Address	Name	Byte	Access Type	Default Value	Description
0x0F80	PWMCON1	2	R/W	0x0012	PWM Control Register 1. See the Pulse-Width Modulator section for full details.
0x0F84	PWM0COM0	2	R/W	0x0000	Compare Register 0 for PWM Output 0 and PWM Output 1.
0x0F88	PWM0COM1	2	R/W	0x0000	Compare Register 1 for PWM Output 0 and PWM Output 1.
0x0F8C	PWM0COM2	2	R/W	0x0000	Compare Register 2 for PWM Output 0 and PWM Output 1.
0x0F90	PWM0LEN	2	R/W	0x0000	Frequency control for PWM Output 0 and PWM Output 1.
0x0F94	PWM1COM0	2	R/W	0x0000	Compare Register 0 for PWM Output 2 and PWM Output 3.
0x0F98	PWM1COM1	2	R/W	0x0000	Compare Register 1 for PWM Output 2 and PWM Output 3.
0x0F9C	PWM1COM2	2	R/W	0x0000	Compare Register 2 for PWM Output 2 and PWM Output 3.
0x0FA0	PWM1LEN	2	R/W	0x0000	Frequency control for PWM Output 2 and PWM Output 3.
0x0FA4	PWM2COM0	2	R/W	0x0000	Compare Register 0 for PWM Output 4.
0x0FA8	PWM2COM1	2	R/W	0x0000	Compare Register 1 for PWM Output 4.
0x0FB0	PWM2LEN	2	R/W	0x0000	Frequency control for PWM Output 4.
0x0FB8	PWMCLRI	2	W	0x0000	PWM interrupt clear register. Writing any value to this register clears a PWM interrupt source.

Table 22. GPIO Base Address = 0xFFFFF400

Address	Name	Byte	Access Type	Default Value	Description
0xF400	GP0CON	4	R/W	0x00001111	GPIO Port0 control MMR.
0xF404	GP1CON	4	R/W	0x00000000	GPIO Port1 control MMR.
0xF408	GP2CON	4	R/W	0x00000000	GPIO Port2 control MMR.
0xF420	GP0DAT	4	R/W	0x000000XX	GPIO Port0 data control MMR.
0xF424	GP0SET	4	W	0x000000XX	GPIO Port0 data set MMR.
0xF428	GP0CLR	4	W	0x000000XX	GPIO Port0 data clear MMR.
0xF42C	GP0PAR	4	R/W	0x22220000	GPIO Port0 pull-up disable MMR.
0xF430	GP1DAT	4	R/W	0x000000XX	GPIO Port1 data control MMR.
0xF434	GP1SET	4	W	0x000000XX	GPIO Port1 data set MMR.
0xF438	GP1CLR	4	W	0x000000XX	GPIO Port1 data clear MMR.
0xF43C	GP1PAR	4	R/W	0x22000022	GPIO Port1 pull-up disable MMR.
0xF440	GP2DAT	4	R/W	0x000000XX	GPIO Port2 data control MMR.
0xF444	GP2SET	4	W	0x000000XX	GPIO Port2 data set MMR.
0xF448	GP2CLR	4	W	0x000000XX	GPIO Port2 data clear MMR.
0xF44C	GP2PAR	4	R/W	0x00000000	GPIO Port2 pull-up disable MMR.

Table 23. Flash/EE Base Address = 0xFFFFF800

Address	Name	Byte	Access Type	Default Value	Description
0xF800	FEESTA	1	R	0x20	Flash/EE status MMR.
0xF804	FEEMOD	2	R/W	0x0000	Flash/EE control MMR.
0xF808	FEECON	1	R/W	0x07	Flash/EE control MMR.
0xF80C	FEEDAT	2	R/W	0xXXXX	Flash/EE data MMR.
0xF810	FEEADR	2	R/W	0x0000	Flash/EE address MMR.
0xF818	FEESIGN	3	R	0xFFFFFF	Flash/EE LFSR MMR.
0xF81C	FEEPRO	4	R/W	0x00000000	Flash/EE protection MMR.
0xF820	FEEHIDE	4	R/W	0xFFFFFFFF	Flash/EE protection MMR.

The C1 capacitors in Figure 27 are typically 4 pF and can be primarily attributed to pin capacitance. The resistors are lumped components made up of the on resistance of the switches. The value of these resistors is typically about 100 Ω. The C2 capacitors are the ADC sampling capacitors and typically have a capacitance of 16 pF.

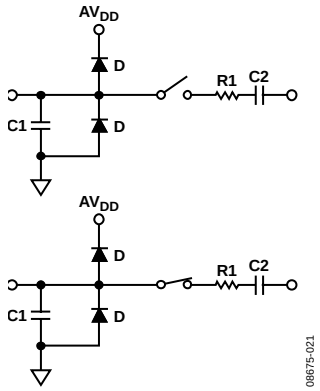

Figure 27. Equivalent Analog Input Circuit Conversion Phase: Switches Open, Track Phase: Switches Closed

For ac applications, removing high frequency components from the analog input signal is recommended by using an RC low-pass filter on the relevant analog input pins. In applications where harmonic distortion and signal-to-noise ratio are critical, the analog input should be driven from a low impedance source. Large source impedances significantly affect the ac performance of the ADC. This can necessitate the use of an input buffer amplifier. The choice of the op amp is a function of the particular application. Figure 28 and Figure 29 give an example of an ADC front end.

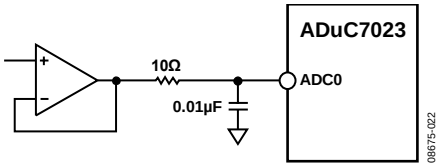

Figure 28. Buffering Single-Ended Differential Input

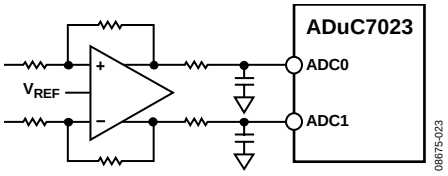

Figure 29. Buffering Differential Inputs

When no amplifier is used to drive the analog input, limit the source impedance to values lower than 1 kΩ. The maximum source impedance depends on the amount of total harmonic distortion (THD) that can be tolerated. The THD increases as the source impedance increases and the performance degrades.

DRIVING THE ANALOG INPUTS

Internal or external references can be used for the ADC. When operating in differential mode, there are restrictions on the common-mode input signal (V_{CM}), which is dependent upon the reference value and supply voltage used to ensure that the signal remains within the supply rails. Table 27 gives some calculated V_{CM} minimum and V_{CM} maximum values.

Table 27. V_{CM} Ranges

AV_{DD}	V_{REF}	V_{CM} Min	V_{CM} Max	Signal Peak-to-Peak
3.3 V	2.5 V	1.25 V	2.05 V	2.5 V
	2.048 V	1.024 V	2.276 V	2.048 V
	1.25 V	0.75 V	2.55 V	1.25 V
3.0 V	2.5 V	1.25 V	1.75 V	2.5 V
	2.048 V	1.024 V	1.976 V	2.048 V
	1.25 V	0.75 V	2.25 V	1.25 V

CALIBRATION

By default, the factory-set values written to the ADC offset (ADCOF) and gain coefficient registers (ADCGN) yield optimum performance in terms of endpoint errors and linearity for standalone operation of the part (see the Specifications section). If system calibration is required, it is possible to modify the default offset and gain coefficients to improve endpoint errors, but note that any modification to the factory-set ADCOF and ADCGN values can degrade ADC linearity performance.

For system offset error correction, the ADC channel input stage must be tied to AGND. A continuous software ADC conversion loop must be implemented by modifying the value in ADCOF until the ADC result (ADCDAT) reads Code 0 to Code 1. If the ADCDAT value is greater than 1, ADCOF should be decremented until ADCDAT reads Code 0 to Code 1. Offset error correction is done digitally and has a resolution of 0.25 LSB and a range of ±3.125% of V_{REF}.

For system gain error correction, the ADC channel input stage must be tied to V_{REF}. A continuous software ADC conversion loop must be implemented to modify the value in ADCGN until the ADCDAT reads Code 4094 to Code 4095. If the ADCDAT value is less than 4094, ADCGN should be incremented until ADCDAT reads Code 4094 to Code 4095. Similar to the offset calibration, the gain calibration resolution is 0.25 LSB with a range of ±3% of V_{REF}.

TEMPERATURE SENSOR

The ADuC7023 provides a voltage output from an on-chip band gap reference that is proportional to absolute temperature. This voltage output can also be routed through the front-end ADC multiplexer (effectively an additional ADC channel input), facilitating an internal temperature sensor channel, measuring die temperature.

An ADC temperature sensor conversion differs from a standard ADC voltage. The ADC performance specifications do not apply to the temperature sensor.

Chopping of the internal amplifier should be enabled using the TSCON register. To enable this mode, the user must set Bit 0 of TSCON. The user must also take two consecutive ADC readings and average them in this mode.

Comparator Interface

The comparator interface consists of a 16-bit MMR, CMPCON, which is described in Table 46.

CMPCON Register

Name: CMPCON

Address: 0xFFFF0444

Default value: 0x0000

Access: Read/write

Table 46. CMPCON MMR Bit Descriptions

Bit	Value	Name	Description
15 to 11			Reserved.
10		CMPEN	Comparator enable bit. This bit is set by the user to enable the comparator. This bit is cleared by the user to disable the comparator.
9 to 8		CMPIN	Comparator negative input select bits.
	00		$AV_{DD}/2$.
	01		ADC3 input.
	10		DAC0 output.
	11		Reserved.
7 to 6		CMPOC	Comparator output configuration bits.
	00		Reserved.
	01		Reserved.
	10		Output on $COMP_{OUT}$.
	11		IRQ.
5		CMPOL	Comparator output logic state bit. When low, the comparator output is high if the positive input (CMP0) is above the negative input (CMP1). When high, the comparator output is high if the positive input is below the negative input.
4 to 3		CMPRES	Response time.
	00		5 µs response time typical for large signals (2.5 V differential). 17 µs response time typical for small signals (0.65 mV differential).
	11		3 µs typical.
	01/10		Reserved.
2		CMPHYST	Comparator hysteresis bit. This bit is set by the user to have a hysteresis of about 7.5 mV. This bit is cleared by the user to have no hysteresis.
1		CMPORI	Comparator output rising edge interrupt. This bit is set automatically when a rising edge occurs on the monitored voltage (CMP0). This bit is cleared by the user by writing a 1 to this bit.
0		CMPOFI	Comparator output rallying edge interrupt. This bit is set automatically when a falling edge occurs on the monitored voltage (CMP0). This bit is cleared by user.

SPIDIV Register

Name:	SPIDIV
Address:	0xFFFF0A0C
Default value:	0x00
Access:	Read/write
Function:	This 6-bit MMR is the SPI baud rate selection register. (Note that the maximum value of this MMR is 0x3F.)

SPI Control Register

Name:	SPICON
Address:	0xFFFF0A10
Default value:	0x0000
Access:	Read/write
Function:	This 16-bit MMR configures the SPI peripheral in both master and slave modes.

Bit	Name	Description
1	SPIMEN	Master mode enable bit. This bit is set by the user to enable master mode. This bit is cleared by the user to enable slave mode.
0	SPIEN	SPI enable bit. This bit is set by the user to enable the SPI. This bit is cleared by the user to disable the SPI.

I²C Address 1 Registers, I2CxADR1

Name: I2C0ADR1, I2C1ADR1

Address: 0xFFFF081C , 0xFFFF091C

Default value: 0x00

Access: Read/write

Function: These 8-bit MMRs are used in 10-bit addressing mode only. These registers contain the least significant byte of the address.

Table 70. I2CxADR1 MMR in 10-Bit Address Mode

Bit	Name	Description
7 to 0	I2CLADR	These bits contain ADDR[7:0] in 10-bit address mode.

I²C Master Clock Control Register, I2CxDIV

Name: I2C0DIV, I2C1DIV

Address: 0xFFFF0824, 0xFFFF0924

Default value: 0x1F1F

Access: Read/write

Function: These MMRs control the frequency of the I²C clock generated by the master on to the SCL pin. For further details, see the I²C initial section.

Table 71. I2CxDIV MMR

Bit	Name	Description
15 to 8	DIVH	These bits control the duration of the high period of SCL.
7 to 0	DIVL	These bits control the duration of the low period of SCL.

I²C Slave Registers

I²C Slave Control Registers, I2CxSCON

Name: I2C0SCON, I2C1SCON

Address: 0xFFFF0828, 0xFFFF0928

Default value: 0x0000

Access: Read/write

Function: These 16-bit MMRs configure the I²C peripheral in slave mode.

Table 72. I2CxSCON MMR Bit Designations

Bit	Name	Description
15 to 11		Reserved bits.
10	I2CSTXENI	Slave transmit interrupt enable bit. This bit is set to enable an interrupt after a slave transmits a byte. This bit clears this interrupt source.
9	I2CSRXENI	Slave receive interrupt enable bit. This bit is set to enable an interrupt after the slave receives data. This bit clears this interrupt source.
8	I2CSSENI	I²C stop condition detected interrupt enable bit. This bit is set to enable an interrupt on detecting a stop condition on the I²C bus. This bit clears this interrupt source.
7	I2CNACKEN	I²C no acknowledge enable bit. This bit is set to no acknowledge the next byte in the transmission sequence. This bit is cleared to let the hardware control the acknowledge/no acknowledge sequence.
6		Reserved. Write a value of 0 to this bit.
5	I2CSETEN	I²C early transmit interrupt enable bit. This bit is set to enable a transmit request interrupt just after the positive edge of SCL during the read bit transmission. This bit is cleared to enable a transmit request interrupt just after the negative edge of SCL during the read bit transmission.

FIQSTA

FIQSTA is a read-only register that provides the current enabled FIQ source status (effectively a logic AND of the FIQSIG and FIQEN bits). When set to 1, that source generates an active FIQ request to the ARM7TDMI core. There is no priority encoder or interrupt vector generation. This function is implemented in software in a common interrupt handler routine.

FIQSTA Register

Name: FIQSTA

Address: 0xFFFF0100

Default value: 0x00000000

Access: Read only

Programmed Interrupts

Because the programmed interrupts are not maskable, they are controlled by another register (SWICFG) that writes into both IRQSTA and IRQSIG registers and/or the FIQSTA and FIQSIG registers at the same time.

The 32-bit register dedicated to software interrupt is SWICFG described in Table 89. This MMR allows the control of a programmed source interrupt.

Table 89. SWICFG MMR Bit Designations

Bit	Description
31 to 3	Reserved.
2	Programmed interrupt FIQ. Setting/clearing this bit corresponds to setting/clearing Bit 1 of FIQSTA and FIQSIG.
1	Programmed interrupt IRQ. Setting/clearing this bit corresponds to setting/clearing Bit 1 of IRQSTA and IRQSIG.
0	Reserved.

Any interrupt signal must be active for at least the minimum interrupt latency time, to be detected by the interrupt controller and to be detected by the user in the IRQSTA and FIQSTA registers.

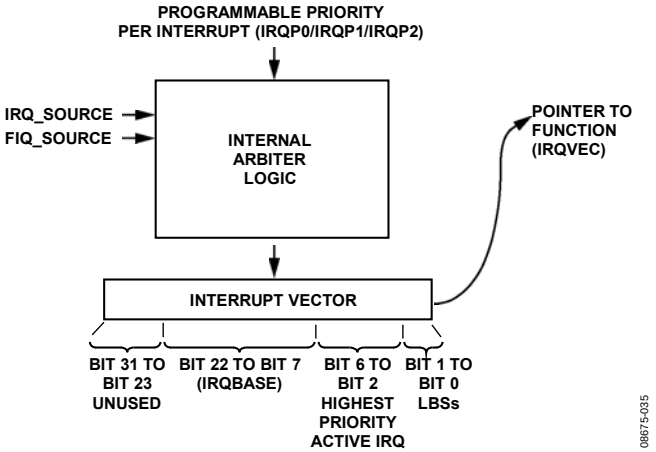

Figure 41. Interrupt Structure

VECTORED INTERRUPT CONTROLLER (VIC)

The ADuC7023 incorporates an enhanced interrupt control system or vectored interrupt controller. The vectored interrupt controller for IRQ interrupt sources is enabled by setting Bit 0 of the IRQCONN register. Similarly, Bit 1 of IRQCONN enables the vectored interrupt controller for the FIQ interrupt sources. The vectored interrupt controller provides the following enhancements to the standard IRQ/FIQ interrupts:

- Vectored interrupts allow a user to define separate interrupt service routine addresses for every interrupt source. This is achieved by using the IRQBASE and IRQVEC registers.
- IRQ/FIQ interrupts can be nested up to eight levels depending on the priority settings. An FIQ still has a higher priority than an IRQ. Therefore, if the VIC is enabled for both the FIQ and IRQ and prioritization is maximized, then it is possible to have 16 separate interrupt levels.
- Programmable interrupt priorities, using the IRQP0 to IRQP2 registers, can be assigned an interrupt priority level value between 0 and 7.

VIC MMRs

IRQBASE Register

The vector base register, IRQBASE, is used to point to the start address of memory used to store 32 pointer addresses. These pointer addresses are the addresses of the individual interrupt service routines.

Name: IRQBASE

Address: 0xFFFF0014

Default value: 0x00000000

Access: Read and write

Table 90. IRQBASE MMR Bit Designations

Bit	Type	Initial Value	Description
31:16	Read only	Reserved	Always read as 0.
15:0	R/W	0	Vector base address.

IRQP0 Register

Name: IRQP0

Address: 0xFFFF0020

Default value: 0x00000000

Access: Read and write

Table 92. IRQP0 MMR Bit Designations

Bit	Name	Description
31	Reserved	Reserved bit
30 to 28	PLLPI	A priority level of 0 to 7 can be set for PLL lock interrupt.
27	Reserved	Reserved bit
26 to 24	ADCPI	A priority level of 0 to 7 can be set for the ADC interrupt source.
23	Reserved	Reserved bit
22 to 20	FlashPI	A priority level of 0 to 7 can be set for the Flash controller interrupt source.
19	Reserved	Reserved bit.
18 to 16	T2PI	A priority level of 0 to 7 can be set for Timer2.
15	Reserved	Reserved bit.
14 to 12	T1PI	A priority level of 0 to 7 can be set for Timer1.
11	Reserved	Reserved bit.
10 to 8	T0PI	A priority level of 0 to 7 can be set for Timer0.
7	Reserved	Reserved bit
6 to 4	SWINTP	A priority level of 0 to 7 can be set for the software interrupt source.
3 to 0	Reserved	Interrupt 0 cannot be prioritized.

IRQP1 Register

Name: IRQP1

Address: 0xFFFF0024

Default value: 0x00000000

Access: Read and write

Table 93. IRQP1 MMR Bit Designations

Bit	Name	Description
31	Reserved	Reserved bit.
30 to 28	PSMPI	A priority level of 0 to 7 can be set for the power supply monitor interrupt source.
27	Reserved	Reserved bit.
26 to 24	COMPI	A priority level of 0 to 7 can be set for comparator.
23	Reserved	Reserved bit.
22 to 20	IRQ0PI	A priority level of 0 to 7 can be set for IRQ0.
19	Reserved	Reserved bit.
18 to 16	SPIPI	A priority level of 0 to 7 can be set for SPI.
15	Reserved	Reserved bit.
14 to 12	I2C1SPI	A priority level of 0 to 7 can be set for I^2C1 slave.
11	Reserved	Reserved bit.
10 to 8	I2C1MPI	A priority level of 0 to 7 can be set for I^2C1 master.
7	Reserved	Reserved bits.
6 to 4	I2C0SPI	A priority level of 0 to 7 can be set for I^2C0 slave.
3	Reserved	Reserved bits.
2 to 0	I2C0MPI	A priority level of 0 to 7 can be set for I^2C0 master.

IRQP2 Register

Name: IRQP2

Address: 0xFFFF0028

Default value: 0x00000000

Access: Read and write

Table 94. IRQP2 MMR Bit Designations

Bit	Name	Description
31 to 23	Reserved	Reserved bit.
22 to 20	PWMPI	A priority level of 0 to 7 can be set for PWM.
19	Reserved	Reserved bit.
18 to 16	PLA1PI	A priority level of 0 to 7 can be set for PLA IRQ1.
15	Reserved	Reserved bit.
14 to 12	IRQ3PI	A priority level of 0 to 7 can be set for IRQ3.
11	Reserved	Reserved bit.
10 to 8	IRQ2PI	A priority level of 0 to 7 can be set for IRQ2.
7	Reserved	Reserved bit.
6 to 4	PLA0PI	A priority level of 0 to 7 can be set for PLA IRQ0.
3	Reserved	Reserved bit.
2 to 0	IRQ1PI	A priority level of 0 to 7 can be set for IRQ1.

IRQCLRE Register

Name: IRQCLRE

Address: 0xFFFF0038

Default value: 0x00000000

Access: Read and write

Table 100. IRQCLRE MMR Bit Designations

Bit	Name	Description
31 to 21	Reserved	These bits are reserved and should not be written to.
20	PLA1CLRI	A 1 must be written to this bit in the PLA IRQ1 interrupt service routine to clear an edge triggered PLA IRQ1 interrupt.
19	IRQ3CLRI	A 1 must be written to this bit in the external IRQ3 interrupt service routine to clear an edge triggered IRQ3 interrupt.
18	IRQ2CLRI	A 1 must be written to this bit in the external IRQ2 interrupt service routine to clear an edge triggered IRQ2 interrupt.
17	PLA0CLRI	A 1 must be written to this bit in the PLA IRQ0 interrupt service routine to clear an edge triggered PLA IRQ0 interrupt.
16	IRQ1CLRI	A 1 must be written to this bit in the external IRQ1 interrupt service routine to clear an edge triggered IRQ1 interrupt.
15 to 14	Reserved	These bits are reserved and should not be written to.
13	IRQ0CLRI	A 1 must be written to this bit in the external IRQ0 interrupt service routine to clear an edge triggered IRQ0 interrupt.
12 to 0	Reserved	These bits are reserved and should not be written to.

TIMERS

The ADuC7023 has three general-purpose timer/counters: Timer0, Timer1, and Timer2 or Watchdog Timer.

These three timers in their normal mode of operation can be either free-running or periodic.

In free-running mode, the counter decreases from the maximum value until zero scale and starts again at the minimum value. (It also increases from the minimum value until full scale and starts again at the maximum value.)

In periodic mode, the counter decrements/increments from the value in the load register (TxLD MMR) until zero/full scale and starts again at the value stored in the load register.

The timer interval is calculated as follows.

If the timer is set to count down,

$$Interval = \frac{(TxLD) \times Prescaler}{Source\,Clock}$$

If the timer is set to count up,

$$Interval = \frac{(FullScale - TxLD) \times Prescaler}{Source\,Clock}$$

The value of a counter can be read at any time by accessing its value register (TxVAL). When a timer is being clocked from a clock other than core clock, an incorrect value may be read (due to asynchronous clock system). In this configuration, TxVAL should always be read twice. If the two readings are different, it should be read a third time to get the correct value.

Timers are started by writing in the control register of the corresponding timer (TxCON).

In normal mode, an IRQ is generated each time the value of the counter reaches zero when counting down. It is also generated each time the counter value reaches full scale when counting up. An IRQ can be cleared by writing any value to clear the register of that particular timer (TxCLRI).

When using an asynchronous clock-to-clock timer, the interrupt in the timer block can take more time to clear than the time it takes for the code in the interrupt routine to execute. Ensure that the interrupt signal is cleared before leaving the interrupt service routine. This can be done by checking the IRQSTA MMR.

Hours, Minutes, Seconds, and 1/128 Format

To use the timer in hours, minutes, seconds,and hundreds format, select the 32768 kHz clock and a prescaler of 256. The hundreds field does not represent milliseconds but 1/128 of a seconds (256/32,768). The bits representing the hour, minute, and second are not consecutive in the register. This arrangement applies to T1LD and T1VAL when using the Hr:Min:Sec:hundreds format as set in T1CON[5:4]. See Table 101 for more details.

Table 101. Hours, Minutes, Seconds, and Hundreds Format

Bit	Value	Description
31:24	0 to 23 or 0 to 255	Hours
23:22	0	Reserved
21:16	0 to 59	Minutes
15:14	0	Reserved
13:8	0 to 59	Seconds
7	0	Reserved
6:0	0 to 127	1/128 of second

Timer0 (RTOS Timer)

Timer0 is a general-purpose, 16-bit timer (count-down) with a programmable prescaler (see Figure 42). The prescaler source is the core clock frequency (HCLK) and can be scaled by factors of 1, 16, or 256.

Timer0 can be used to start ADC conversions as shown in the block diagram in Figure 42.

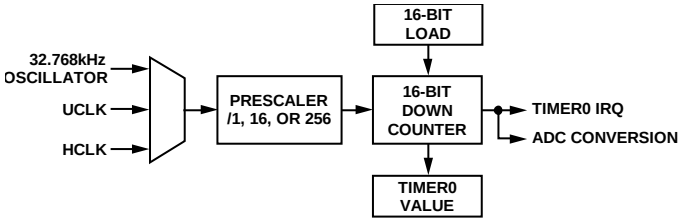

Figure 42. Timer0 Block Diagram

HARDWARE DESIGN CONSIDERATIONS

POWER SUPPLIES

The ADuC7023 operational power supply voltage range is 2.7 V to 3.6 V. Separate analog and digital power supply pins (AV_{DD} and IOV_{DD}, respectively) allow AV_{DD} to be kept relatively free of noisy digital signals often present on the system IOV_{DD} line. In this mode, the part can also operate with split supplies, that is, it can use different voltage levels for each supply. For example, the system can be designed to operate with an IOV_{DD} voltage level of 3.3 V while the AV_{DD} level can be at 3 V, or vice versa. A typical split supply configuration is shown in Figure 46.

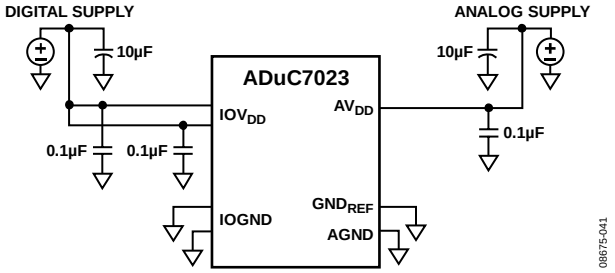

Figure 46. External Dual Supply Connections

As an alternative to providing two separate power supplies, the user can reduce noise on AV_{DD} by placing a small series resistor and/or ferrite bead between AV_{DD} and IOV_{DD}, and then decoupling AV_{DD} separately to ground. An example of this configuration is shown in Figure 47. With this configuration, other analog circuitry (such as op amps, voltage reference, and others) can be powered from the AV_{DD} supply line as well.

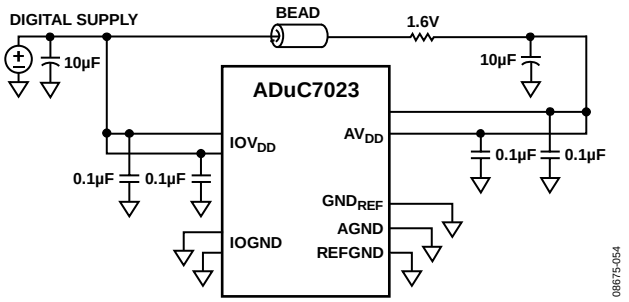

Figure 47. External Single Supply Connections

In both Figure 46 and Figure 47, a large value (10 µF) reservoir capacitor sits on IOV_{DD}, and a separate 10 µF capacitor sits on AV_{DD}. In addition, local small-value (0.1 µF) capacitors are located at each AV_{DD} and IOV_{DD} pin of the chip. As per standard design practice, include all of these capacitors and ensure the smaller capacitors are close to each AV_{DD} pin with trace lengths as short as possible. Connect the ground terminal of each of these capacitors directly to the underlying ground plane.

Finally, the analog and digital ground pins on the ADuC7023 must be referenced to the same system ground reference point at all times.

IOV_{DD} Supply Sensitivity

The IOV_{DD} supply is sensitive to high frequency noise because it is the supply source for the internal oscillator and PLL circuits. When the internal PLL loses lock, the clock source is removed by a gating circuit from the CPU, and the ARM7TDMI core stops executing code until the PLL regains lock. This feature is to ensure that no flash interface timings or ARM7TDMI timings are violated.

Typically, frequency noise greater than 50 kHz and 50 mV p-p on top of the supply causes the core to stop working.

If decoupling values recommended in the Power Supplies section do not sufficiently dampen all noise soures below 50 mV on IOV_{DD}, a filter such as the one shown in Figure 48 is recommended.

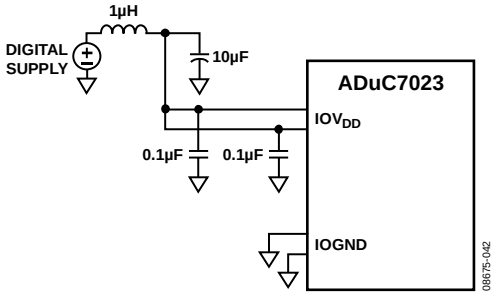

Figure 48. Recommended IOV_{DD} Supply Filter

Linear Voltage Regulator

Each ADuC7023 requires a single 3.3 V supply, but the core logic requires a 2.6 V supply. An on-chip linear regulator generates the 2.6 V from IOV_{DD} for the core logic. The LV_{DD} pin is the 2.6 V supply for the core logic. An external compensation capacitor of 0.47 µF must be connected between LV_{DD} and DGND (as close as possible to these pins) to act as a tank of charge, as shown in Figure 49.

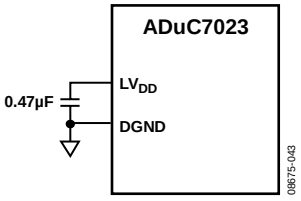

Figure 49. Voltage Regulator Connections

The LV_{DD} pin should not be used for any other chip. It is also recommended to use excellent power supply decoupling on IOV_{DD} to help improve line regulation performance of the on-chip voltage regulator.

GROUNDING AND BOARD LAYOUT RECOMMENDATIONS

As with all high resolution data converters, special attention must be paid to grounding and PC board layout of the ADuC7023-based designs to achieve optimum performance from the ADCs and DACs.

Although the parts have separate pins for analog and digital ground (AGND and DGND), the user must not tie these to two separate ground planes unless the two ground planes are connected very close to the part. This is illustrated in the simplified example shown in Figure 50a. In systems where digital and analog ground planes are connected together somewhere else (at the system power supply, for example), the planes cannot be reconnected near the part because a ground loop would result. In these cases, tie all the ADuC7023 AGND and DGND pins to the analog ground plane, as illustrated in Figure 50b. In systems with only one ground plane, ensure that the digital and analog components are physically separated onto separate halves of the board so that digital return currents do not flow near analog circuitry (and vice versa).

The ADuC7023 can then be placed between the digital and analog sections, as illustrated in Figure 50c.

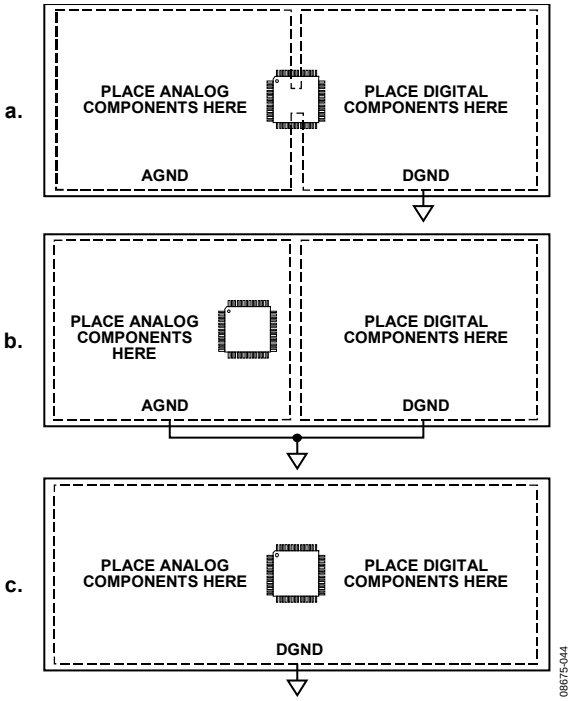

Figure 50. System Grounding Schemes

In all of these scenarios, and in more complicated real-life applications, users should pay particular attention to the flow of current from the supplies and back to ground. Make sure the return paths for all currents are as close as possible to the paths the currents took to reach their destinations.

For example, do not power components on the analog side (as seen in Figure 50b) with IOV_{DD} because that would force return currents from IOV_{DD} to flow through AGND. Avoid digital currents flowing under analog circuitry, which can occur if a noisy digital chip is placed on the left half of the board (shown in Figure 50c). If possible, avoid large discontinuities in the ground plane(s) such as those formed by a long trace on the same layer, because they force return signals to travel a longer path. In addition, make all connections to the ground plane directly, with little or no trace separating the pin from its via to ground.

When connecting fast logic signals (rise/fall time < 5 ns) to any of the ADuC7023 digital inputs, add a series resistor to each relevant line to keep rise and fall times longer than 5 ns at the input pins of the part. A value of 100 Ω or 200 Ω is usually sufficient enough to prevent high speed signals from coupling capacitively into the part and affecting the accuracy of ADC conversions.

CLOCK OSCILLATOR

The clock source for the ADuC7023 can be generated by the internal PLL or by an external clock input. To use the internal PLL, connect a 32.768 kHz parallel resonant crystal between XCLKI and XCLKO, and connect a capacitor from each pin to ground, as shown in Figure 51. The crystal allows the PLL to lock correctly to give a frequency of 41.78 MHz. If no external crystal is present, the internal oscillator is used to give a typical frequency of 41.78 MHz ± 3%.

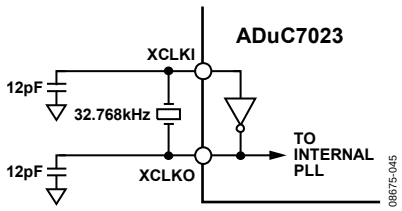

Figure 51. External Parallel Resonant Crystal Connections

To use an external source clock input instead of the PLL (see Figure 52), Bit 1 and Bit 0 of PLLCON must be modified. The external clock uses P1.1 and XCLK.

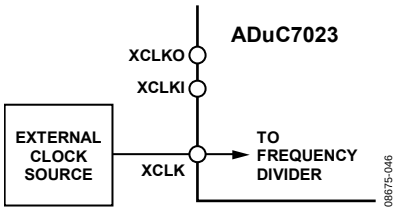

Figure 52. Connecting an External Clock Source

Using an external clock source, the ADuC7023 specified operational clock speed range is 50 kHz to 44 MHz ± 1%, which ensures correct operation of the analog peripherals and Flash/EE.

POWER-ON RESET OPERATION

An internal power-on reset (POR) is implemented on the ADuC7023. For LV_{DD} below 2.40 V typical, the internal POR holds the part in reset. As LV_{DD} rises above 2.40 V, an internal timer times out for typically 64 ms before the part is released from reset. The user must ensure that the power supply IOV_{DD} has reached a stable 2.7 V minimum level by this time. Likewise, on power-down, the internal POR holds the part in reset until LV_{DD} has dropped below 2.40 V.

Figure 53 illustrates the operation of the internal POR in detail.

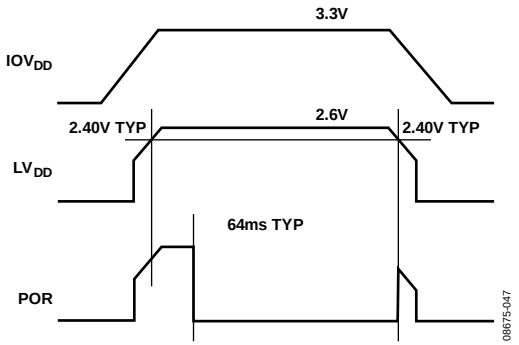

Figure 53. Internal Power-On Reset Operation

TYPICAL SYSTEM CONFIGURATION

A typical ADuC7023 configuration is shown in Figure 54. It summarizes some of the hardware considerations. The bottom of the LFCSP package has an exposed pad that needs to be soldered to a metal plate on the board for mechanical reasons. The metal plate of the board can be connected to ground.

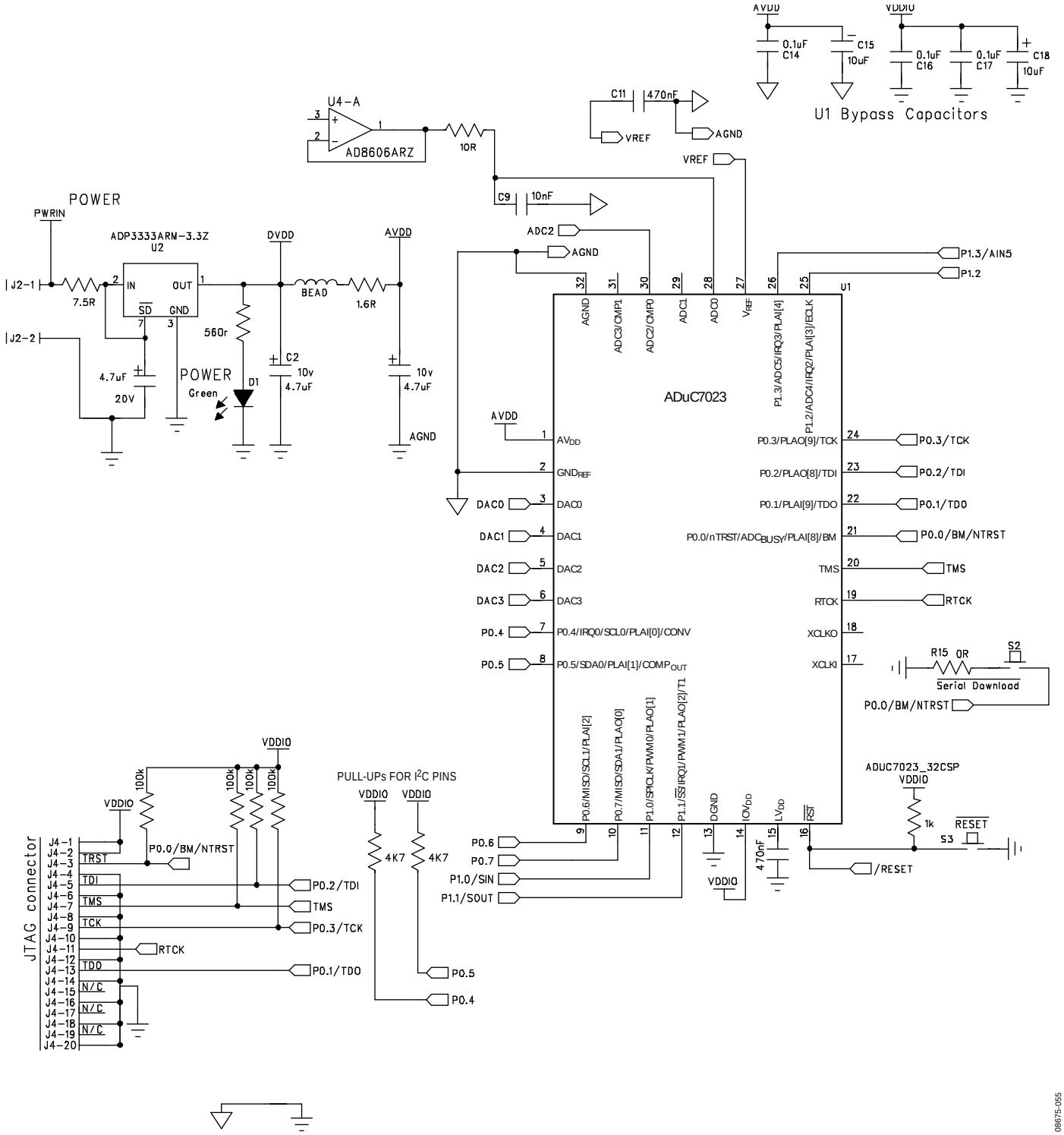

Figure 54. Typical System Configuration

DEVELOPMENT TOOLS

PC-BASED TOOLS

Four types of development systems are available for the ADuC7023 family. The ADuC7023 QuickStart Plus is intended for new users who want to have a comprehensive hardware development environment.

These systems consist of the following PC-based (Windows® compatible) hardware and software development tools.

Hardware

The hardware system uses the ADuC7023 evaluation board, a serial port programming cable, and a RDI-compliant JTAG emulator (included in the ADuC7023 QuickStart Plus only).

Software

The software system has an integrated development environment, incorporating an assembler, compiler, and nonintrusive JTAG-based debugger. The software sytem uses a serial downloader software and example code.

Miscellaneous

The miscellaneous systems use CD-ROM documentation.

IN-CIRCUIT I²C DOWNLOADER

An I²C-based serial downloader is available at www.analog.com. This software requires an USB-to-I²C adaptor board available from Analog Devices. The part number for this USB-to-I²C adapter is USB-I2C/LIN-CONV-Z.

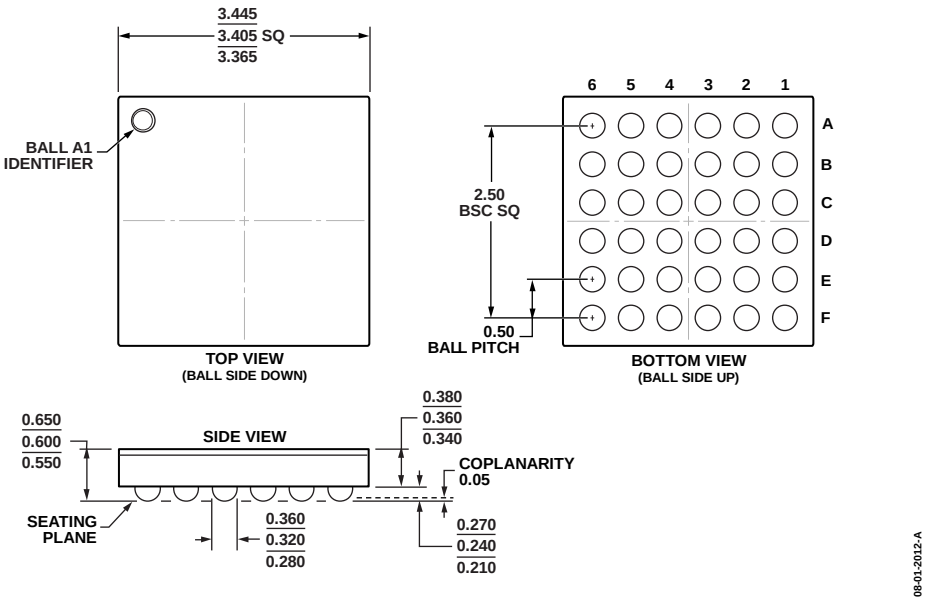

Figure 57. 36-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-36-3)
Dimensions shown in millimeters