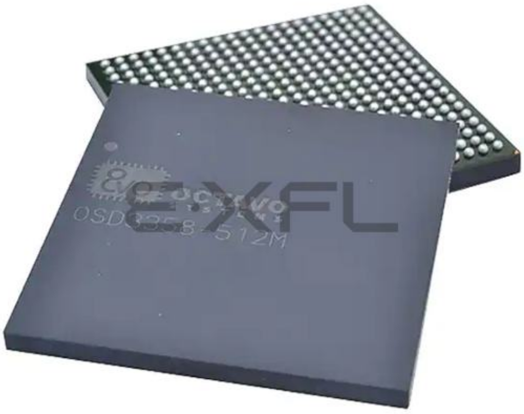
Octavo Systems LLC - OSD3358-512M-BAS Datasheet



Understanding Embedded - Microcontroller, Microprocessor, FPGA Modules

Embedded - Microcontroller, Microprocessor, and FPGA Modules are fundamental components in modern electronic systems, offering a wide range of functionalities and capabilities. Microcontrollers are compact integrated circuits designed to execute specific control tasks within an embedded system. They typically include a processor, memory, and input/output peripherals on a single chip. Microprocessors, on the other hand, are more powerful processing units used in complex computing tasks, often requiring external memory and peripherals. FPGAs (Field Programmable Gate Arrays) are highly flexible devices that can be configured by the user to perform specific logic functions, making them invaluable in applications requiring customization and adaptability.

Applications of Embedded - Microcontroller,

Details	
Product Status	Active
Module/Board Type	MPU Core
Core Processor	ARM® Cortex®-A8, AM3358
Co-Processor	NEON™ SIMD
Speed	1GHz
Flash Size	-
RAM Size	512MB
Connector Type	400-BGA
Size / Dimension	1.06" x 1.06" (27.0mm x 27.0mm)
Operating Temperature	0°C ~ 85°C
Purchase URL	https://www.e-xfl.com/product-detail/octavo-systems/osd3358-512m-bas

Table of Contents

1 Revision History

Revision Number	Revision Date	Changes	Author
1	5/6/2016	Initial Release	Greg Sheridan, Kevin Troy
2	5/15/2016	Updated Misprint on ADC Specs on first page	Greg Sheridan
3	5/19/2016	Added Information on the MSL Rating	Greg Sheridan
4	6/12/16	Added reference to TI Handling Recommendations to Handling Section. Fixed Link	Greg Sheridan
5	12/5/16	Updated Electrical Characteristics add Thermal information. Also changed operating temperature from junction to case	Neeraj Dantu, Greg Sheridan
6	2/15/17	Updated Max Current and Voltage in Output Power and Electrical & Thermal Characterization Sections	Neeraj Dantu

2 Block Diagram

The OSD335x family of devices consist of 4 main components serving 3 different functions. The main processor is a Texas Instruments Sitara™ AM335x ARM® Cortex®-A8. The power system has 2 devices from Texas Instruments, the TPS65217C Power Management IC (PMIC) and the TL5209 LDO. The last main component is the DDR3 system memory. Figure 2.1 shows a detailed block diagram of the OSD335x and breaks out the key functions of the AM335x processor.

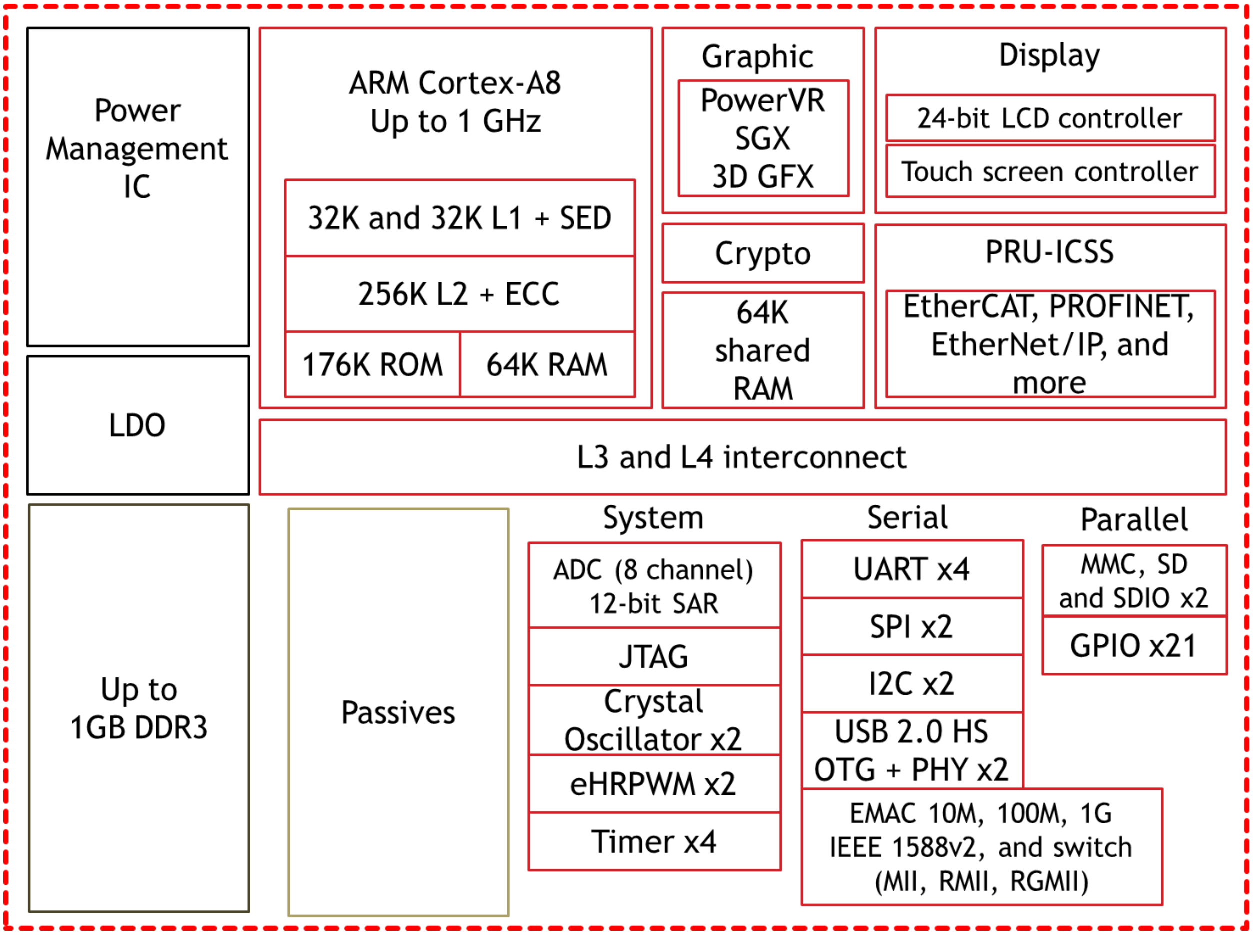


Figure 2.1. OSD335x Detailed Block Diagram

2.1 Passives

Besides the four major components, the OSD335x also integrates over 140 capacitors, resistors, inductors, and ferrite beads (Passives). Table 2.1 lists the location, value, quantity of the input, and output of these passives to externally accessible signals on the OSD335x.

Table 2.1. OSD335x Passives

From	To	Device	Pin	Type	Value	Qty
CAP_VBB_MPU	VSS	AM335x	CAP_VBB_MPU	C	1uF	1
CAP_VDD_RTC	VSS	AM335x	CAP_VDD_RTC	C	1uF	1
CAP_VDD_SRAM_CORE	VSS	AM335x	CAP_VDD_SRAM_CORE	C	1uF	1
CAP_VDD_SRAM_MPU	VSS	AM335x	CAP_VDD_SRAM_MPU	C	1uF	1
SYS_RTC_1P8V	VSS	AM335x	VDDS	C	10uF	1
SYS_RTC_1P8V	VSS	AM335x	VDDS	C	0.01uF	4
SYS_RTC_1P8V	VSS	AM335x	VDDS_RTC	C	0.01uF	1
SYS_VDD_1P8V	VSS	AM335x	VDDA1P8V_USB0	C	0.01uF	1
SYS_VDD_1P8V	VSS	AM335x	VDDA1P8V_USB1	C	0.01uF	1
SYS_VDD_1P8V	VSS	AM335x	VDDS_SRAM_CORE_BG	C	10uF	1
SYS_VDD_1P8V	VSS	AM335x	VDDS_SRAM_CORE_BG	C	0.01uF	1
SYS_VDD_1P8V	VSS	AM335x	VDDS_SRAM_MPU_BB	C	10uF	1
SYS_VDD_1P8V	VSS	AM335x	VDDS_SRAM_MPU_BB	C	0.01uF	1
VDDSHV_3P3V	VSS	AM335x	VDDA3P3V_USB0	C	0.01uF	1
VDDSHV_3P3V	VSS	AM335x	VDDA3P3V_USB1	C	0.01uF	1
VDDSHV_3P3V	VSS	AM335x	VDDSHV1-VDDSHV6	C	10uF	6
VDDSHV_3P3V	VSS	AM335x	VDDSHV1-VDDSHV6	C	0.01uF	16
VDD_CORE	VSS	AM335x	VDD_CORE	C	10uF	1
VDD_CORE	VSS	AM335x	VDD_CORE	C	0.01uF	8
VDD_MPU	VSS	AM335x	VDD_MPU	C	10uF	1
VDD_MPU	VSS	AM335x	VDD_MPU	C	0.01uF	5
VDDA_ADC	VSS	AM335x	VDDA_ADC	C	0.01uF	1
VDDS_DDR	VSS	AM335x	VDDS_DDR	C	10uF	2
VDDS_DDR	VSS	AM335x	VDDS_DDR	C	0.047uF	22
VDDS_PLL	VSS	AM335x	VDDS_OSC	C	0.01uF	1
VDDS_PLL	VSS	AM335x	VDDS_PLL_CORE_LCD	C	0.01uF	1
VDDS_PLL	VSS	AM335x	VDDS_PLL_DDR	C	0.01uF	1
VDDS_PLL	VSS	AM335x	VDDS_PLL_MPU	C	0.01uF	1
SYS_VDD_1P8V	VDDA_ADC	AM335x	VDDA_ADC	FB	150 Ohm	1
SYS_VDD_1P8V	VDDS_PLL	AM335x	VDDS_PLL	FB	150 Ohm	1
VSS	VSSA_ADC	AM335x	VSSA_ADC	FB	150 Ohm	1
VDDS_DDR	VSS	OSD335x	DDR3 Memory Device	C	10uF	2
VDDS_DDR	VSS	OSD335x	DDR3 Memory Device	C	0.1uF	12
VDDSHV_3P3V	VSS	TL5209	OUT	C	2.2uF	1
SYS_VOUT	VSS	TL5209	IN	C	2.2uF	1
SYS_RTC_1P8V	VSS	TPS65217C	VLDO1	C	2.2uF	1
SYS_VDD_1P8V	VSS	TPS65217C	LS1_OUT	C	10uF	1
SYS_VDD2_3P3V	VSS	TPS65217C	VLDO2	C	2.2uF	1
VDDSHV_3P3V	VSS	TPS65217C	LS2_OUT	C	10uF	1
SYS_VOUT	VSS	TPS65217C	SYS	C	10uF	2
SYS_VOUT	VSS	TPS65217C	VIN_DCDC1	C	10uF	1
SYS_VOUT	VSS	TPS65217C	VIN_DCDC2	C	10uF	1
SYS_VOUT	VSS	TPS65217C	VIN_DCDC3	C	10uF	1
SYS_VOUT	VSS	TPS65217C	VIN_LDO	C	10uF	1
VDD_CORE	VSS	TPS65217C	VDCDC3	C	10uF	1
VDD_MPU	VSS	TPS65217C	VDCDC2	C	10uF	1
VDDS_DDR	VSS	TPS65217C	VDCDC1	C	10uF	1
VIN_5V	VSS	TPS65217C	AC	C	10uF	1
VIN_BAT	VSS	TPS65217C	BAT	C	10uF	1
VIN_USB	VSS	TPS65217C	USB	C	10uF	1

VDD_CORE	L3	TPS65217C	L3	L	2.2uH	1
VDD_MPU	L2	TPS65217C	L2	L	2.2uH	1
VDDS_DDR	L1	TPS65217C	L1	L	2.2uH	1
SYS_RTC_1P8V	PMIC_OUT_PWR_EN	TPS65217C	PWR_EN pull-up	R	10K Ohm	1
SYS_RTC_1P8V	PMIC_OUT_NWAKEUP	TPS65217C	WAKEUPN pull-up	R	10K Ohm	1
VDDSHV_3P3V	PMIC_OUT_NINT	TPS65217C	INTN pull-up	R	10K Ohm	1
VDDSHV_3P3V	PMIC_IN_I2C_SCL	TPS65217C	SCL pull-up	R	4.7K Ohm	1
VDDSHV_3P3V	PMIC_IN_I2C_SDA	TPS65217C	SDA pull-up	R	4.7K Ohm	1

Trim Designator – A set of letters and numbers that designate a set additional features in the device. Table 3.3 shows the valid values for the Trim Designator.

Table 3.3. Trim Designator

Trim Designator	Device Options
BAS	Base Model containing the Processer, DDR Memory, PMIC, and LDO

Revision Designator – One or two letters that designate the revision of the device. An **X** in the first position of the designator shows that this device is a preproduction device.

4 Reference Documents

4.1 Data Sheets

Below are links to the data sheets for the key devices used in the OSD335X. Please refer to them for specifics on that device. The remainder of this document will describe how the devices are used in the OSD335X system. It will also highlight any differences between the performance stated in the device specific datasheet and what should be expected from its operation in the OSD335X.

- Processor – AM335X – http://www.ti.com/product/AM3358/datasheet
- PMIC – TPS62517C – http://www.ti.com/product/TPS65217/datasheet
- LDO – TL509 – http://www.ti.com/product/TL5209/datasheet

4.2 Other Reference

This section contains links to other reference documents that could be helpful when using the OSD335x device. Some are referenced in this document.

- TI AN-2029 – Handling & Process recommendations – http://www.ti.com/lit/snoa550
- AN1002 – Pin Assignments and Application Differences From TI AM3358 – http://octavosystems.com/docs/AN1002.pdf
- AM335x DR PHY register configuration for DDR3 using Software Leveling – http://processors.wiki.ti.com/index.php/AM335x_DDR_PHY_register_configuration_for_DDR3_using_Software_Leveling
- AM335x Power Estimation Tool – http://processors.wiki.ti.com/index.php/AM335x_Power_Estimation_Tool
- Powering the AM335x with the TPS65217x – http://www.ti.com/lit/slvu551

5 Ball Map

The balls on the OSD335x are mainly the signals of the AM335x along with extra rows and columns for the power supplies. With a few exceptions, the ball assignments for the OSD335x are a superset of the ball assignments for the AM335x. *Table 5.1* through Table 5.5 show the ball map for the OSD335x.

Table 5.1. OSD335X Ball Map Top View (Columns A-D)

	A	B	C	D
20	PMIC_OUT_PGOOD	PMIC_OUT_LDO_PGOOD	PMIC_IN_I2C_SCL	PMIC_IN_PB_IN
19	PMIC_OUT_NWAKEUP	PMIC_OUT_NINT	PMIC_IN_I2C_SDA	PMIC_IN_PWR_EN
18	VSS	EXTINTN	ECAP0_IN_PWM0_OUT	UART1_CTSN
17	SPI0_SCLK	SPI0_D0	I2C0_SDA	UART1_RTSN
16	SPI0_CS0	SPI0_D1	I2C0_SCL	UART1_RXD
15	XDMA_EVENT_INTR0	PWRONRSTN	SPI0_CS1	UART1_TXD
14	MCASP0_AHCLKX	EMU1	EMU0	XDMA_EVENT_INTR1
13	MCASP0_ACLKX	MCASP0_FSX	MCASP0_FSR	MCASP0_AXR1
12	TCK	MCASP0_ACLKR	MCASP0_AHCLKR	MCASP0_AXR0
11	TDO	TDI	TMS	CAP_VDD_SRAM_MPU
10	WARMRSTN	TRSTN	CAP_VBB_MPU	SYS_VDD_1P8V
9	VSSA_ADC	VREFP	AIN7	CAP_VDD_SRAM_CORE
8	AIN6	AIN5	AIN4	SYS_ADC_1P8V
7	AIN3	AIN2	AIN1	SYS_RTC_1P8V
6	VSSA_ADC	AIN0	PMIC_POWER_EN	CAP_VDD_RTC
5	SYS_ADC_1P8V	RTC_PWRONRSTN	EXT_WAKEUP	NC
4	SYS_ADC_1P8V	RTC_KALDO_ENN	NC	NC
3	TESTOUT	NC	NC	NC
2	VDD_MPU_MON	NC	NC	NC
1	VSS	NC	NC	NC

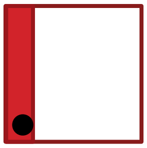


Table 5.3. OSD335X Ball Map Top View (Columns J-M)

	J	K	L	M
20	VSS	OSC0_OUT	OSC0_GND	OSC0_IN
19	VSS	VSS	VSS	VSS
18	MII1_TXD3	MII1_TX_CLK	MII1_RX_CLK	MDC
17	MII1_RX_DV	MII1_TXD0	MII1_RXD3	MDIO
16	MII1_TX_EN	MII1_TXD1	MII1_RXD2	MII1_RXD0
15	MII1_RX_ER	MII1_TXD2	MII1_RXD1	USB0_CE
14	VDDSHV_3P3V	VDDSHV_3P3V	VDDSHV_3P3V	VSS
13	VDD_MPU	SYS_RTC_1P8V	VSS	VDD_CORE
12	VDD_CORE	VDD_CORE	VSS	VSS
11	VSS	VSS	VSS	VDD_CORE
10	VSS	VSS	VSS	VSS
9	VSS	VSS	VDD_CORE	VSS
8	VSS	VDD_CORE	VDD_CORE	VSS
7	VSS	VSS	VDD_CORE	VSS
6	VSS	VDD_CORE	VDD_CORE	VSS
5	VDDS_DDR	VDDS_DDR	VDDS_DDR	VPP
4	NC	NC	NC	NC
3	NC	NC	NC	NC
2	NC	NC	NC	NC
1	NC	NC	NC	NC

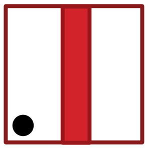


Table 5.4. OSD335X Ball Map Top View (Columns N-T)

	N	**P**	**R**	**T**
20	VSS	VSS	VSS	VSS
19	VSS	VSS	VSS	VSS
18	USB0_DM	USB1_CE	USB1_DM	USB1_VBUS
17	USB0_DP	USB1_ID	USB1_DP	GPMC_WAIT0
16	SYS_VDD_1P8V	USB0_ID	SYS_VDD_1P8V	GPMC_A10
15	VDDSHV_3P3V	USB0_VBUS	VDDSHV_3P3V	GPMC_A07
14	VSS	SYS_RTC_1P8V	GPMC_A04	GPMC_A03
13	VDD_CORE	VDDSHV_3P3V	GPMC_A00	GPMC_CSN3
12	VDD_CORE	VDDSHV_3P3V	GPMC_AD13	GPMC_AD12
11	VSS	VDDSHV_3P3V	VDDS_PLL	GPMC_AD10
10	VSS	VDDSHV_3P3V	VDDS_PLL	GPMC_AD09
9	VDD_CORE	SYS_RTC_1P8V	GPMC_AD06	GPMC_AD07
8	VDD_CORE	VDDSHV_3P3V	GPMC_AD02	GPMC_AD03
7	VSS	VDDSHV_3P3V	GPMC_ADVN_ALE	GPMC_OEN_REN
6	SYS_RTC_1P8V	VDDSHV_3P3V	LCD_AC_BIAS_EN	GPMC_BEN0_CLE
5	VDDSHV_3P3V	VDDSHV_3P3V	LCD_HSYNC	LCD_DATA15
4	NC	NC	LCD_DATA03	LCD_DATA07
3	NC	NC	LCD_DATA02	LCD_DATA06
2	NC	NC	LCD_DATA01	LCD_DATA05
1	NC	NC	LCD_DATA00	LCD_DATA04

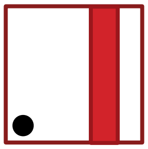
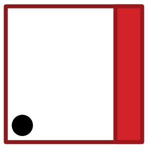


Table 5.5. OSD335X Ball Map Top View (Columns U-Y)

	U	**V**	**W**	**Y**
20	SYS_VDD1_3P3V	SYS_VDD1_3P3V	VSS	EXTL3B
19	VSS	VSS	VSS	EXTL3A
18	GPMC_BEN1	VSS	VSS	VSS
17	GPMC_WPN	GPMC_A11	VSS	EXTL2B
16	GPMC_A09	GPMC_A08	VSS	EXTL2A
15	GPMC_A06	GPMC_A05	VSS	VSS
14	GPMC_A02	GPMC_A01	VSS	EXTL1B
13	GPMC_AD15	GPMC_AD14	VSS	EXTL1A
12	GPMC_AD11	GPMC_CLK	VSS	VSS
11	NC	NC	VSS	SYS_VDD2_3P3V
10	GPMC_AD08	NC	VSS	VSS
9	GPMC_CSN1	GPMC_CSN2	VSS	VIN_USB
8	GPMC_AD04	GPMC_AD05	VSS	VIN_USB
7	GPMC_AD00	GPMC_AD01	VSS	VSS
6	GPMC_WEN	GPMC_CSN0	VSS	VIN_AC
5	LCD_VSYNC	LCD_PCLK	VSS	VIN_AC
4	LCD_DATA11	LCD_DATA14	SYS_VOUT	SYS_VOUT
3	LCD_DATA10	LCD_DATA13	VSS	VIN_BAT
2	LCD_DATA09	LCD_DATA12	VSS	VIN_BAT
1	LCD_DATA08	VSS	BAT_TEMP	BAT_VOLT



5.1 Ball Description

Table 5.6 lists all of the unique balls of the OSD335x and gives a brief explanation of their function. For more detail please refer to the datasheet in section 4.1 for the individual device that ball is associated with.

Table 5.6 OSD335x Ball Descriptions

Pin Name	Description
AIN0	Analog Input / Output
AIN1	Analog Input / Output
AIN2	Analog Input / Output
AIN3	Analog Input / Output
AIN4	Analog Input / Output
AIN5	Analog Input
AIN6	Analog Input
AIN7	Analog Input
BAT_TEMP	TPS65217C TS Input
BAT_VOLT	TPS65217C BAT_SENSE Input
CAP_VBB_MPU	Internal Voltage Test Point
CAP_VDD_RTC	Internal Voltage Test Point, RTC Supply Voltage Input
CAP_VDD_SRAM_CORE	Internal Voltage Test Point
CAP_VDD_SRAM_MPU	Internal Voltage Test Point
ECAP0_IN_PWM0_OUT	Enhanced Capture 0 Input or PWM0 Output
EMU0	Miscellaneous Emulation Pin
EMU1	Miscellaneous Emulation Pin
EXT_WAKEUP	AM335x EXT_WAKEUP Input
EXTINTN	AM335x External Interrupt to ARM Cortex-A8
EXTL1A	RESERVED
EXTL1B	RESERVED
EXTL2A	RESERVED
EXTL2B	RESERVED
EXTL3A	RESERVED
EXTL3B	RESERVED
GPMC_A00	GPMC Address
GPMC_A01	GPMC Address
GPMC_A02	GPMC Address
GPMC_A03	GPMC Address
GPMC_A04	GPMC Address
GPMC_A05	GPMC Address
GPMC_A06	GPMC Address
GPMC_A07	GPMC Address
GPMC_A08	GPMC Address
GPMC_A09	GPMC Address
GPMC_A10	GPMC Address
GPMC_A11	GPMC Address
GPMC_AD00	GPMC Address and Data
GPMC_AD01	GPMC Address and Data
GPMC_AD02	GPMC Address and Data
GPMC_AD03	GPMC Address and Data
GPMC_AD04	GPMC Address and Data
GPMC_AD05	GPMC Address and Data
GPMC_AD06	GPMC Address and Data
GPMC_AD07	GPMC Address and Data
GPMC_AD08	GPMC Address and Data
GPMC_AD09	GPMC Address and Data
GPMC_AD10	GPMC Address and Data
GPMC_AD11	GPMC Address and Data
GPMC_AD12	GPMC Address and Data
GPMC_AD13	GPMC Address and Data
GPMC_AD14	GPMC Address and Data

MMC0_DAT1	MMC/SD/SDIO Data
MMC0_DAT2	MMC/SD/SDIO Data
MMC0_DAT3	MMC/SD/SDIO Data
NC	No Connect
OSC0_GND	High Frequency Oscillator Ground
OSC0_IN	High Frequency Oscillator Input
OSC0_OUT	High Frequency Oscillator Output
OSC1_GND	Real Time Clock Oscillator Ground
OSC1_IN	Real Time Clock Oscillator Input
OSC1_OUT	Real Time Clock Oscillator Output
PMIC_IN_I2C_SCL	TPS65217C SCL Input
PMIC_IN_I2C_SDA	TPS65217C SDA Input / Output
PMIC_IN_PB_IN	TPS65217C PB_IN Input
PMIC_IN_PWR_EN	TPS65217C PWR_EN Input
PMIC_OUT_LDO_PGOOD	TPS65217C LDO_PGOOD Output
PMIC_OUT_NINT	TPS65217C NINT Output
PMIC_OUT_NWAKEUP	TPS65217C NWAKEUP Output
PMIC_OUT_PGOOD	TPS65217C PGOOD Output
PMIC_POWER_EN	AM335x PMIC_POWER_EN Output
PWRONRSTN	Power On Reset Input (Active Low)
RMII1_REF_CLK	RMII Reference Clock
RTC_KALDO_ENN	Enable input for internal CAP_VDD_RTC voltage regulator (Active Low)
RTC_PWRONRSTN	RTC Reset Input (Active Low)
SPI0_CS0	SPI Chip Select
SPI0_CS1	SPI Chip Select
SPI0_D0	SPI Data
SPI0_D1	SPI Data
SPI0_SCLK	SPI Clock
SYS_ADC_1P8V	Output Power Supply, Analog, 1.8VDC
SYS_RTC_1P8V	Output Power Supply, RTC Voltage Domain, 1.8VDC
SYS_VDD_1P8V	Output Power Supply, Digital, 1.8VDC
SYS_VDD1_3P3V	Output Power Supply, Primary, 3.3VDC
SYS_VDD2_3P3V	Output Power Supply, Secondary, 3.3VDC
SYS_VOUT	TPS65217C SYS Output
TCK	JTAG Test Clock
TDI	JTAG Test Data Input
TDO	JTAG Test Data Output
TESTOUT	RESERVED
TMS	JTAG Test Mode Select
TRSTN	JTAG Test Reset
UART0_CTSN	UART Clear to Send
UART0_RTSN	UART Request to Send
UART0_RXD	UART Receive Data
UART0_TXD	UART Transmit Data
UART1_CTSN	UART Clear to Send
UART1_RTSN	UART Request to Send
UART1_RXD	UART Receive Data
UART1_TXD	UART Transmit Data
USB0_CE	USB0 Charger Enable Output
USB0_DM	USB0 Data (-)
USB0_DP	USB0 Data (+)
USB0_DRVVBUS	USB0 VBUS Control Output
USB0_ID	USB0 OTG ID
USB0_VBUS	USB0 VBUS
USB1_CE	USB1 Data (-)
USB1_DM	USB1 Data (+)
USB1_DP	USB1 VBUS Control Output
USB1_DRVVBUS	USB1 OTG ID
USB1_ID	USB1 VBUS
USB1_VBUS	USB1 Data (-)
VDD_CORE	Internal Power Supply Test Point
VDD_MPU	Internal Power Supply Test Point
VDD_MPU_MON	AM335x VDD_MPU_MON Signal

VDDS_DDR	Internal Power Supply Test Point
VDDS_PLL	Internal Power Supply Test Point
VDDSHV_3P3V	Internal Power Supply Test Point
VIN_AC	TPS65217C AC Input
VIN_BAT	TPS65217C BAT Input / Output
VIN_USB	TPS65217C USB Input
VPP	RESERVED
VREFP	Analog Positive Reference Input
VSS	Digital Ground
VSSA_ADC	Analog Ground, Analog Negative Reference Input
WARMRSTN	Warm Reset (Active Low)
XDMA_EVENT_INTR0	External DMA Event or Interrupt 0
XDMA_EVENT_INTR1	External DMA Event or Interrupt 1

5.2 AM335x Relocated Signals

A small number of signals from the AM335x have been moved to a different location on the OSD335x. For more information on these signals please refer to AN1002. A link to it is provided in the Reference Documents section of this document.

5.3 Not Connected Balls

The OSD335x ball map contains a number of balls which are marked NC (No Connect). These balls must be left unconnected on the system PCB since they may be used for other purposes in future versions of the OSD335x.

Most of these balls are from the AM335x pins associated with the DDR3 interface. They are not brought out because they are exclusively used internally to connect the AM335x with the DDR Memory. Several other balls in the ball map are also NC due to other functions handled internal to the OSD335x.

7 Power Management

The power management portion of the OSD335x consists of two devices, the TPS65217C (PMIC) and the TL5209 (LDO). These devices are used to provide the necessary power rails to the AM335x and the DDR3. They also provide power supply outputs that may be used to power circuitry external to the OSD335x. This section describes how to power the OSD335x in a system and the outputs that can be used. The OSD335x has a complicated power distribution network and care must be taken to read and understand the proper use of the external connections to the power supplies.

7.1 Input Power

The OSD335x may be powered by any combination of the following input power supplies. Please refer to the TPS65217C datasheet for details.

7.1.1 VIN_AC

The OSD335x may be powered by an external AC Adaptor at 5.0 VDC.

7.1.2 VIN_USB

The OSD335x may be powered by a USB port at 5.0 VDC.

7.1.3 VIN_BAT

The OSD335x may be powered by a Li-Ion or Li-Polymer Battery.

7.2 Output Power

The OSD335x produces the following output power supplies.

7.2.1 SYS_VOUT: Switched VIN_AC, VIN_USB, or VIN_BAT

The OSD335x contains a shared supply to power the AM335x, DDR3, and TL5209 which is also used to power external circuitry. This is supplied by the TPS65217C SYS output. The SYS output is a switched connection to one of the input power supplies selected by the TPS65217C as described in the datasheet for that device.

7.2.2 SYS_VDD1_3P3V

The OSD335x contains a dedicated 3.3 VDC supply[1] to power external circuitry. This is supplied by the TL5209, powered by the TPS65217C SYS output, and enabled by the TPS65217C LDO4.

7.2.3 SYS_VDD2_3P3V

The OSD335x contains a dedicated 3.3 VDC supply to power external circuitry. This is supplied by the TPS65217C LDO2.

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[1] The nominal output voltage of the LDO has been set to 3.33V using 1% tolerance resistors. This implies a nominal voltage range of 3.29V – 3.37V. The LDO has an accuracy of 1 – 2% depending on the ambient temperature which will also affect the nominal voltage. See the TL5209 datasheet for more information.

7.2.4 SYS_RTC_1P8V

The OSD335x contains a shared 1.8 VDC supply to power the AM335x RTC which may also be used to power external circuitry. This is supplied by the TPS65217C LDO1.

Please note that the AM335x in the OSD335x is powered by TPS65217 PMIC **version C** which does not support RTC only mode.

7.2.5 SYS_VDD_1P8V

The OSD335x contains a shared 1.8 VDC supply to power the AM335x SRAM, PLLs, and USB which may also be used to power external circuitry. This is supplied by the TPS65217C LDO3.

7.2.6 SYS_ADC_1P8V

The OSD335x contains a shared 1.8 VDC supply to power the AM335x ADC which may also be used to power external analog circuitry. This is supplied by the TPS65217C LDO3 and filtered for analog applications.

7.3 Internal Power

The OSD335x has internal power supplies that are not available to power external circuitry. To do so will prevent the OSD335x from functioning properly. The power supplies are accessible externally for monitoring purposes only.

7.3.1 VDDSHV_3P3V

The OSD335x contains a dedicated 3.3 VDC supply to power the AM335x I/O domain. This is supplied by the TPS65217C LDO4.

7.3.2 VDDS_DDR

The OSD335x contains a dedicated 1.5 VDC supply to power the AM335x DDR3 interface and the DDR3 device.

7.3.3 VDD_MPU

The OSD335x contains a dedicated 1.1 VDC supply to power the AM335x MPU domain.

7.3.4 VDD_CORE

The OSD335x contains a dedicated 1.1 VDC supply to power the AM335x CORE domain.

7.3.5 VDDS_PLL

The OSD335x contains a filtered 1.8 VDC supply to power the AM335x PLLs and oscillators.

7.5 Control and Status

Table 7.1 lists the signals required to coordinate the operation of the AM335x and TPS65217C. Figure 7.1 illustrates the required connections between the required signals. This is the minimum requirement. The accessibility of these signals enables other uses of the reset, power control, power status, interrupt, wakeup, and serial communication signals.

Table 7.1. AM335x and TPS65217C Signal Descriptions

Signal	Description	Notes
PMIC_POWER_EN	PMIC Power Enable from AM335x	
PMIC_IN_PWR_EN	PMIC Power Enable to TPS65217C	1
I2C0_SCL	I2C0 SCL from AM335x	
PMIC_IN_I2C_SCL	I2C SCL to TPS65217C	1
I2C0_SDA	I2C0 SDA from AM335x	
PMIC_IN_I2C_SDA	I2C SDA to TPS65217C	1
PMIC_OUT_PGOOD	PGOOD from TPS65217C	
PWRONRSTN	PWRONRSTN to AM335x	
PMIC_OUT_LDO_PGOOD	LDO_PGOOD from TPS65217C	
RTC_PWRONRSTN	RTC_ PWRONRSTN to AM335x	
PMIC_OUT_NINT	NINT from TPS65217C	
EXTINTN	EXTINTN to AM335x	1
PMIC_OUT_NWAKEUP	NWAKEUP from TPS65217C	
EXT_WAKEUP	EXT_WAKEUP to AM335x	1

1. See Table 2.1 for pull up on this signal

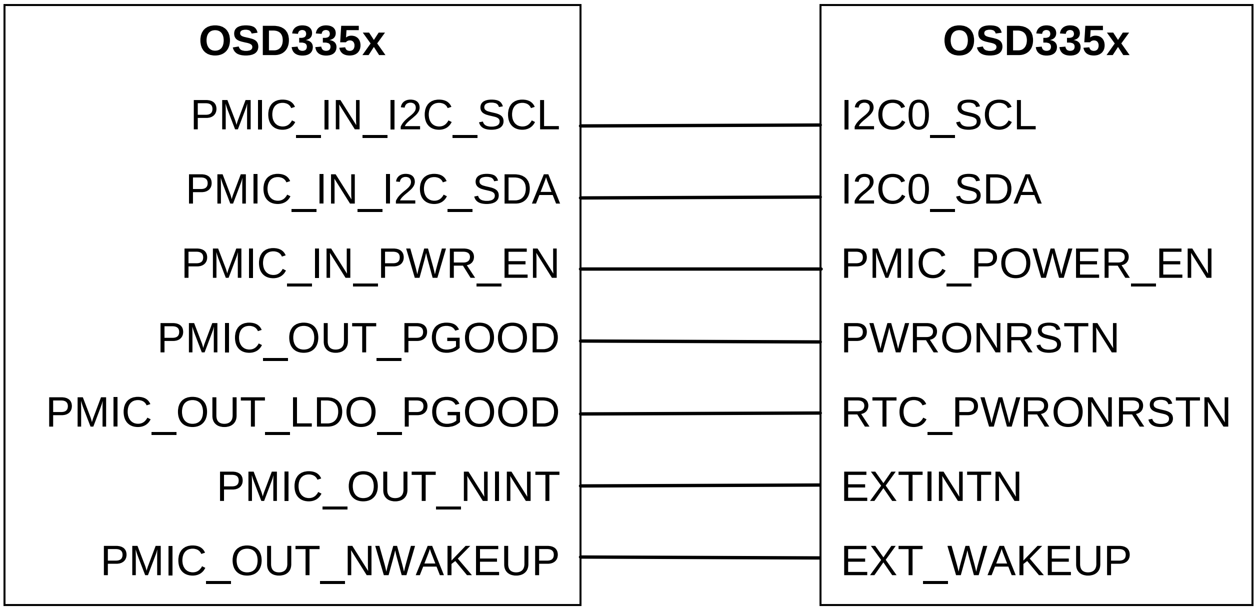


Figure 7.1. OSD335x Minimum Signal Connections

8 Electrical & Thermal Characteristics

Table 8.1 lists electrical and thermal characteristic parameters of OSD3358.

Table 8.1. OSD335x Absolute Maximum Ratings over operating free-air temperature range (unless otherwise noted) (1) (2)

		Value	Unit
Supply voltage range (with respect to VSS)	VIN_BAT	-0.3 to 7	V
	VIN_USB, VIN_AC	-0.3 to 7	
Input/Output voltage range (with respect to VSS)	All pins unless specified separately	-0.3 to 3.6	V
Terminal current	SYS_VOUT, VIN_USB, VIN_BAT	3000	mA
T_C	Operating case temperature	0 to 85	°C
T_{stg}	Storage temperature	-40 to 125	°C
ESD rating	(HBM) Human body model	±2000	V
	(CDM) Charged device model	±500	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Thermal characteristic values were measured using the OSD3358 SBC Reference Design.

Table 8.2. Recommended Operating Conditions over operating free-air temperature range (unless otherwise noted)

	Min	Nom	Max	Unit
Supply voltage, VIN_USB, VIN_AC	4.3		5.8	V
Supply voltage, VIN_BAT	2.75		5.5	V
Input current from VIN_AC			2.0	A
Input current from VIN_USB			1.3	A
VIN_BAT current			2.0	A
Output voltage range for SYS_VDD1_3P3V		3.33		V
Output voltage range for SYS_VDD2_3P3V		3.3		V
Output voltage range for SYS_RTC_1P8V		1.8		V
Output voltage range for SYS_VDD_1P8V		1.8		V
Output voltage range for SYS_ADC_1P8V		1.8		V
Output voltage range for VDDS_DDR[1]		1.5		V
Output voltage range for VDD_MPU[1]		1.1		V
Output voltage range for VDD_CORE[1]		1.1		V
Output voltage range for VDDS_PLL[1]		1.8		V
Output voltage range for VDDSHV_3P3V[1]		3.3		V
Output current for SYS_VOUT[2]	0		500	mA
Output current for SYS_VDD1_3P3V[2]	0		500	mA
Output current for SYS_VDD2_3P3V[2]	0		150	mA
Output current for SYS_RTC_1P8V[2]	0		100	mA
Output current for SYS_VDD_1P8V[2]	0		250	mA
Output current for SYS_ADC_1P8V[2]	0		25	mA

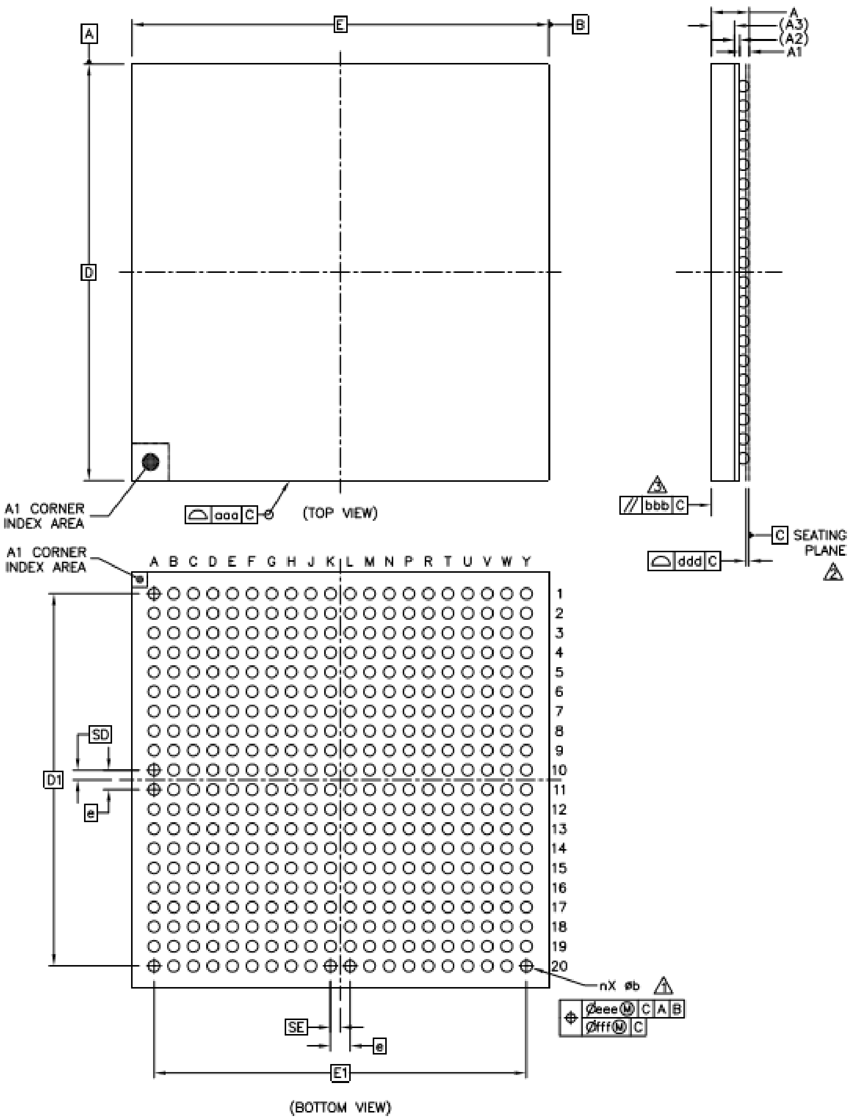
(1) *These voltage rails are for reference only and should not be used to power anything on the PCB.*
(2) *Please note that the total input current on VIN_AC, VIN_USB or VIN_BAT must not exceed the recommended maximum value even if individual currents drawn from these power supply outputs are less than or equal to the maximum recommended operating output currents. See section 7.4 for more details.*

9 Packaging Information

The OSD335x is packaged in a 400 ball, Ball Grid Array (BGA). The package size is 27 X 27 millimeters with a ball pitch of 1.27mm. This section will give you the specifics on the package.

9.1 Mechanical Dimensions

The mechanical drawings of the OSD335x show pin A1 in the lower left hand corner when looking at the top view of the device. Pin A1 is in the upper left hand corner if looking at the balls from the bottom view of the package. The PCB layout should have pin A1 in the lower left hand corner when looking at the top side of the PCB where the OSD335x will be attached.



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	2.6
STAND OFF	A1	0.5	---	0.7
SUBSTRATE THICKNESS	A2		0.35	REF
MOLD THICKNESS	A3		1.5	REF
BODY SIZE	D		27	BSC
	E		27	BSC
BALL DIAMETER			0.75	
BALL OPENING			0.6	
BALL WIDTH	b	0.6	---	0.9
BALL PITCH	e		1.27	BSC
BALL COUNT	n		400	
EDGE BALL CENTER TO CENTER	D1		24.13	BSC
	E1		24.13	BSC
BODY CENTER TO CONTACT BALL	SD		0.635	BSC
	SE		0.635	BSC
PACKAGE EDGE TOLERANCE	aaa		0.2	
MOLD FLATNESS	bbb		0.35	
COPLANARITY	ddd		0.2	
BALL OFFSET (PACKAGE)	eee		0.3	
BALL OFFSET (BALL)	fff		0.15	

NOTES:

1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.
2. DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.