Octavo Systems LLC - OSD3358-512M-ISM Datasheet

Welcome to E-XFL.COM

Understanding Embedded - Microcontroller, Microprocessor, FPGA Modules

Embedded - Microcontroller, Microprocessor, and FPGA Modules are fundamental components in modern electronic systems, offering a wide range of functionalities and capabilities. Microcontrollers are compact integrated circuits designed to execute specific control tasks within an embedded system. They typically include a processor, memory, and input/output peripherals on a single chip. Microprocessors, on the other hand, are more powerful processing units used in complex computing tasks, often requiring external memory and peripherals. FPGAs (Field Programmable Gate Arrays) are highly flexible devices that can be configured by the user to perform specific logic functions, making them invaluable in applications requiring customization and adaptability.

Applications of Embedded - Microcontroller,

Details	
Product Status	Active
Module/Board Type	MPU Core
Core Processor	ARM® Cortex®-A8, AM3358
Co-Processor	NEON™ SIMD
Speed	1GHz
Flash Size	-
RAM Size	512MB
Connector Type	256-BGA
Size / Dimension	0.83" x 0.83" (21mm x 21mm)
Operating Temperature	-40°C ~ 85°C
Purchase URL	https://www.e-xfl.com/product-detail/octavo-systems/osd3358-512m-ism

Table of Contents

1 Revision History

Revision Number	Revision Date	Changes	Author
1	5/6/2016	Initial Release	Greg Sheridan, Kevin Troy
2	5/15/2016	Updated Misprint on ADC Specs on first page	Greg Sheridan
3	5/19/2016	Added Information on the MSL Rating	Greg Sheridan
4	6/12/16	Added reference to TI Handling Recommendations to Handling Section. Fixed Link	Greg Sheridan
5	12/5/16	Updated Electrical Characteristics add Thermal information. Also changed operating temperature from junction to case	Neeraj Dantu, Greg Sheridan
6	2/15/17	Updated Max Current and Voltage in Output Power and Electrical & Thermal Characterization Sections	Neeraj Dantu

2 Block Diagram

The OSD335x family of devices consist of 4 main components serving 3 different functions. The main processor is a Texas Instruments Sitara™ AM335x ARM® Cortex®-A8. The power system has 2 devices from Texas Instruments, the TPS65217C Power Management IC (PMIC) and the TL5209 LDO. The last main component is the DDR3 system memory. Figure 2.1 shows a detailed block diagram of the OSD335x and breaks out the key functions of the AM335x processor.

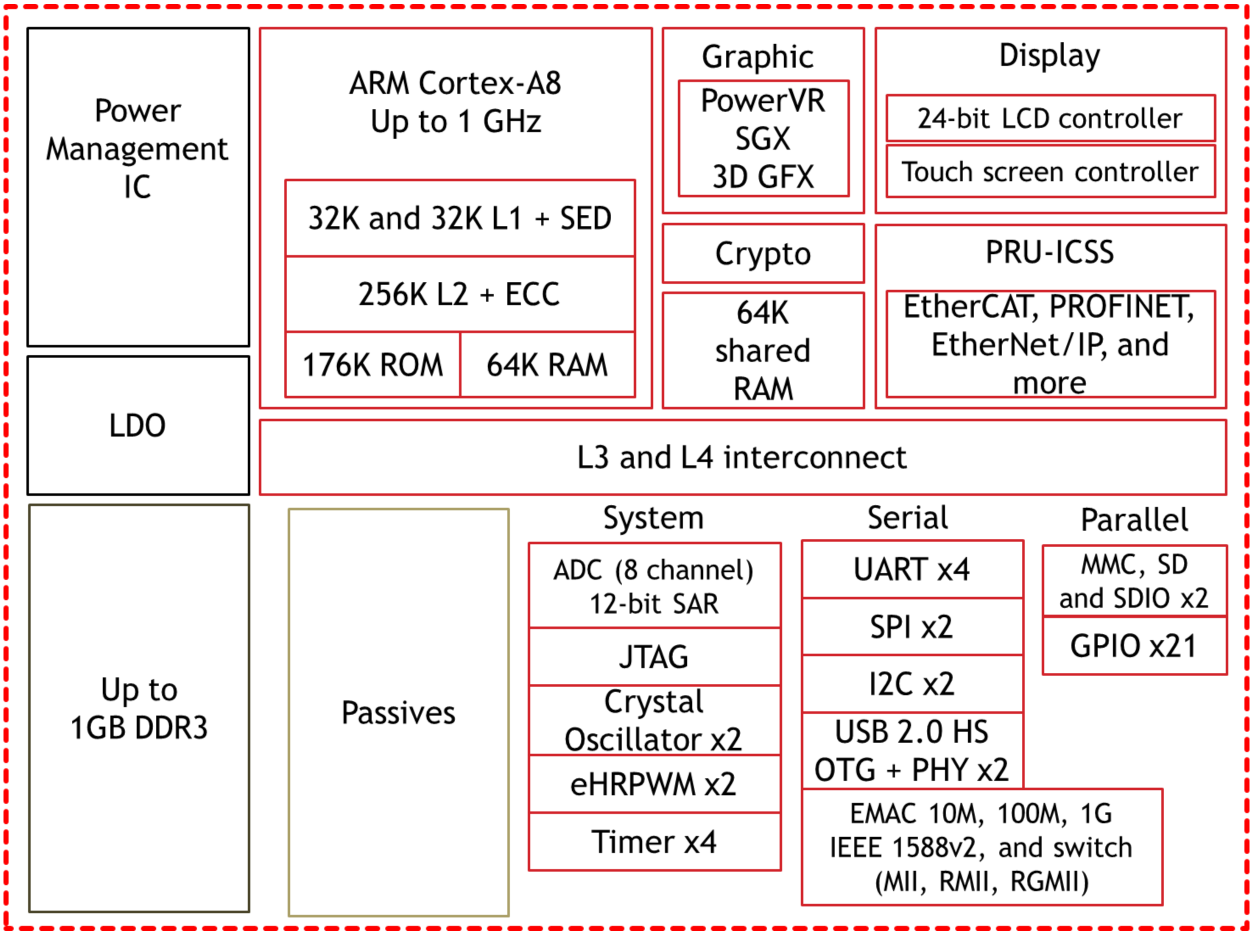


Figure 2.1. OSD335x Detailed Block Diagram

2.1 Passives

Besides the four major components, the OSD335x also integrates over 140 capacitors, resistors, inductors, and ferrite beads (Passives). Table 2.1 lists the location, value, quantity of the input, and output of these passives to externally accessible signals on the OSD335x.

Table 2.1. OSD335x Passives

From	To	Device	Pin	Type	Value	Qty
CAP_VBB_MPU	VSS	AM335x	CAP_VBB_MPU	C	1uF	1
CAP_VDD_RTC	VSS	AM335x	CAP_VDD_RTC	C	1uF	1
CAP_VDD_SRAM_CORE	VSS	AM335x	CAP_VDD_SRAM_CORE	C	1uF	1
CAP_VDD_SRAM_MPU	VSS	AM335x	CAP_VDD_SRAM_MPU	C	1uF	1
SYS_RTC_1P8V	VSS	AM335x	VDDS	C	10uF	1
SYS_RTC_1P8V	VSS	AM335x	VDDS	C	0.01uF	4
SYS_RTC_1P8V	VSS	AM335x	VDDS_RTC	C	0.01uF	1
SYS_VDD_1P8V	VSS	AM335x	VDDA1P8V_USB0	C	0.01uF	1
SYS_VDD_1P8V	VSS	AM335x	VDDA1P8V_USB1	C	0.01uF	1
SYS_VDD_1P8V	VSS	AM335x	VDDS_SRAM_CORE_BG	C	10uF	1
SYS_VDD_1P8V	VSS	AM335x	VDDS_SRAM_CORE_BG	C	0.01uF	1
SYS_VDD_1P8V	VSS	AM335x	VDDS_SRAM_MPU_BB	C	10uF	1
SYS_VDD_1P8V	VSS	AM335x	VDDS_SRAM_MPU_BB	C	0.01uF	1
VDDSHV_3P3V	VSS	AM335x	VDDA3P3V_USB0	C	0.01uF	1
VDDSHV_3P3V	VSS	AM335x	VDDA3P3V_USB1	C	0.01uF	1
VDDSHV_3P3V	VSS	AM335x	VDDSHV1-VDDSHV6	C	10uF	6
VDDSHV_3P3V	VSS	AM335x	VDDSHV1-VDDSHV6	C	0.01uF	16
VDD_CORE	VSS	AM335x	VDD_CORE	C	10uF	1
VDD_CORE	VSS	AM335x	VDD_CORE	C	0.01uF	8
VDD_MPU	VSS	AM335x	VDD_MPU	C	10uF	1
VDD_MPU	VSS	AM335x	VDD_MPU	C	0.01uF	5
VDDA_ADC	VSS	AM335x	VDDA_ADC	C	0.01uF	1
VDDS_DDR	VSS	AM335x	VDDS_DDR	C	10uF	2
VDDS_DDR	VSS	AM335x	VDDS_DDR	C	0.047uF	22
VDDS_PLL	VSS	AM335x	VDDS_OSC	C	0.01uF	1
VDDS_PLL	VSS	AM335x	VDDS_PLL_CORE_LCD	C	0.01uF	1
VDDS_PLL	VSS	AM335x	VDDS_PLL_DDR	C	0.01uF	1
VDDS_PLL	VSS	AM335x	VDDS_PLL_MPU	C	0.01uF	1
SYS_VDD_1P8V	VDDA_ADC	AM335x	VDDA_ADC	FB	150 Ohm	1
SYS_VDD_1P8V	VDDS_PLL	AM335x	VDDS_PLL	FB	150 Ohm	1
VSS	VSSA_ADC	AM335x	VSSA_ADC	FB	150 Ohm	1
VDDS_DDR	VSS	OSD335x	DDR3 Memory Device	C	10uF	2
VDDS_DDR	VSS	OSD335x	DDR3 Memory Device	C	0.1uF	12
VDDSHV_3P3V	VSS	TL5209	OUT	C	2.2uF	1
SYS_VOUT	VSS	TL5209	IN	C	2.2uF	1
SYS_RTC_1P8V	VSS	TPS65217C	VLDO1	C	2.2uF	1
SYS_VDD_1P8V	VSS	TPS65217C	LS1_OUT	C	10uF	1
SYS_VDD2_3P3V	VSS	TPS65217C	VLDO2	C	2.2uF	1
VDDSHV_3P3V	VSS	TPS65217C	LS2_OUT	C	10uF	1
SYS_VOUT	VSS	TPS65217C	SYS	C	10uF	2
SYS_VOUT	VSS	TPS65217C	VIN_DCDC1	C	10uF	1
SYS_VOUT	VSS	TPS65217C	VIN_DCDC2	C	10uF	1
SYS_VOUT	VSS	TPS65217C	VIN_DCDC3	C	10uF	1
SYS_VOUT	VSS	TPS65217C	VIN_LDO	C	10uF	1
VDD_CORE	VSS	TPS65217C	VDCDC3	C	10uF	1
VDD_MPU	VSS	TPS65217C	VDCDC2	C	10uF	1
VDDS_DDR	VSS	TPS65217C	VDCDC1	C	10uF	1
VIN_5V	VSS	TPS65217C	AC	C	10uF	1
VIN_BAT	VSS	TPS65217C	BAT	C	10uF	1
VIN_USB	VSS	TPS65217C	USB	C	10uF	1

VDD_CORE	L3	TPS65217C	L3	L	2.2uH	1
VDD_MPU	L2	TPS65217C	L2	L	2.2uH	1
VDDS_DDR	L1	TPS65217C	L1	L	2.2uH	1
SYS_RTC_1P8V	PMIC_OUT_PWR_EN	TPS65217C	PWR_EN pull-up	R	10K Ohm	1
SYS_RTC_1P8V	PMIC_OUT_NWAKEUP	TPS65217C	WAKEUPN pull-up	R	10K Ohm	1
VDDSHV_3P3V	PMIC_OUT_NINT	TPS65217C	INTN pull-up	R	10K Ohm	1
VDDSHV_3P3V	PMIC_IN_I2C_SCL	TPS65217C	SCL pull-up	R	4.7K Ohm	1
VDDSHV_3P3V	PMIC_IN_I2C_SDA	TPS65217C	SDA pull-up	R	4.7K Ohm	1

3 Product Number Information

Figure 3.1 shows an example of an orderable product number for the OSD335X family. This section explains the different sections of the product number. It will also list the valid entries and their meaning for each designator.

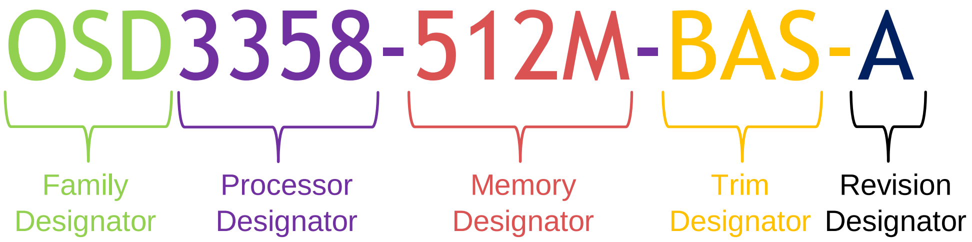


Figure 3.1. Example Product Number

Family Designator – Three letters that designate the family of device.

Processor Designator – A set of letters and numbers that designate the specific processor in the device. Table 3.1 shows the valid values for the Processor Designator.

Table 3.1. Processor Designators

Processor Designator	Processor
3358	Texas Instruments AM3358
3352	Texas Instruments AM3352

Memory Designator – A set of letters and numbers that designate the DDR3 memory size in the device. Table 3.2 shows the valid values for the Memory Designator.

Table 3.2. Memory Designator

Memory Designator	DDR Memory Size
1G	1GB DDR3
512M	512 MB DDR3
256M	256 MB DDR3

Trim Designator – A set of letters and numbers that designate a set additional features in the device. Table 3.3 shows the valid values for the Trim Designator.

Table 3.3. Trim Designator

Trim Designator	Device Options
BAS	Base Model containing the Processer, DDR Memory, PMIC, and LDO

Revision Designator – One or two letters that designate the revision of the device. An **X** in the first position of the designator shows that this device is a preproduction device.

4 Reference Documents

4.1 Data Sheets

Below are links to the data sheets for the key devices used in the OSD335X. Please refer to them for specifics on that device. The remainder of this document will describe how the devices are used in the OSD335X system. It will also highlight any differences between the performance stated in the device specific datasheet and what should be expected from its operation in the OSD335X.

- Processor – AM335X – http://www.ti.com/product/AM3358/datasheet
- PMIC – TPS62517C – http://www.ti.com/product/TPS65217/datasheet
- LDO – TL509 – http://www.ti.com/product/TL5209/datasheet

4.2 Other Reference

This section contains links to other reference documents that could be helpful when using the OSD335x device. Some are referenced in this document.

- TI AN-2029 – Handling & Process recommendations – http://www.ti.com/lit/snoa550
- AN1002 – Pin Assignments and Application Differences From TI AM3358 – http://octavosystems.com/docs/AN1002.pdf
- AM335x DR PHY register configuration for DDR3 using Software Leveling – http://processors.wiki.ti.com/index.php/AM335x_DDR_PHY_register_configuration_for_DDR3_using_Software_Leveling
- AM335x Power Estimation Tool – http://processors.wiki.ti.com/index.php/AM335x_Power_Estimation_Tool
- Powering the AM335x with the TPS65217x – http://www.ti.com/lit/slvu551

5 Ball Map

The balls on the OSD335x are mainly the signals of the AM335x along with extra rows and columns for the power supplies. With a few exceptions, the ball assignments for the OSD335x are a superset of the ball assignments for the AM335x. Table 5.1 through Table 5.5 show the ball map for the OSD335x.

Table 5.1. OSD335X Ball Map Top View (Columns A-D)

	A	B	C	D
20	PMIC_OUT_PGOOD	PMIC_OUT_LDO_PGOOD	PMIC_IN_I2C_SCL	PMIC_IN_PB_IN
19	PMIC_OUT_NWAKEUP	PMIC_OUT_NINT	PMIC_IN_I2C_SDA	PMIC_IN_PWR_EN
18	VSS	EXTINTN	ECAP0_IN_PWM0_OUT	UART1_CTSN
17	SPI0_SCLK	SPI0_D0	I2C0_SDA	UART1_RTSN
16	SPI0_CS0	SPI0_D1	I2C0_SCL	UART1_RXD
15	XDMA_EVENT_INTR0	PWRONRSTN	SPI0_CS1	UART1_TXD
14	MCASP0_AHCLKX	EMU1	EMU0	XDMA_EVENT_INTR1
13	MCASP0_ACLKX	MCASP0_FSX	MCASP0_FSR	MCASP0_AXR1
12	TCK	MCASP0_ACLKR	MCASP0_AHCLKR	MCASP0_AXR0
11	TDO	TDI	TMS	CAP_VDD_SRAM_MPU
10	WARMRSTN	TRSTN	CAP_VBB_MPU	SYS_VDD_1P8V
9	VSSA_ADC	VREFP	AIN7	CAP_VDD_SRAM_CORE
8	AIN6	AIN5	AIN4	SYS_ADC_1P8V
7	AIN3	AIN2	AIN1	SYS_RTC_1P8V
6	VSSA_ADC	AIN0	PMIC_POWER_EN	CAP_VDD_RTC
5	SYS_ADC_1P8V	RTC_PWRONRSTN	EXT_WAKEUP	NC
4	SYS_ADC_1P8V	RTC_KALDO_ENN	NC	NC
3	TESTOUT	NC	NC	NC
2	VDD_MPU_MON	NC	NC	NC
1	VSS	NC	NC	NC

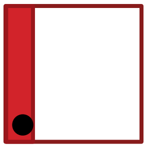


Table 5.2. OSD335X Ball Map Top View (Columns E-H)

	E	**F**	**G**	**H**
20	VSS	OSC1_OUT	OSC1_GND	OSC1_IN
19	VSS	VSS	VSS	VSS
18	UART0_CTSN	MMC0_DAT2	MMC0_CMD	RMII1_REF_CLK
17	UART0_RTSN	MMC0_DAT3	MMC0_CLK	MII1_CRS
16	UART0_TXD	USB0_DRVVBUS	MMC0_DAT0	MII1_COL
15	UART0_RXD	USB1_DRVVBUS	MMC0_DAT1	VDDS_PLL
14	SYS_RTC_1P8V	VDDSHV_3P3V	VDDSHV_3P3V	VDDSHV_3P3V
13	VDDSHV_3P3V	VDD_MPU	VDD_MPU	VDD_MPU
12	VDDSHV_3P3V	VDD_MPU	VSS	VSS
11	VDDSHV_3P3V	VDD_MPU	VSS	VDD_CORE
10	VDDSHV_3P3V	VDD_MPU	VDD_CORE	VSS
9	SYS_VDD_1P8V	SYS_RTC_1P8V	VSS	VSS
8	VSSA_ADC	VSS	VSS	VSS
7	VDDS_PLL	VDD_CORE	VDD_CORE	VSS
6	SYS_RTC_1P8V	VDD_CORE	VDD_CORE	VSS
5	VDDS_DDR	VDDS_DDR	VDDS_DDR	VDDS_DDR
4	NC	NC	NC	NC
3	NC	NC	NC	NC
2	NC	NC	NC	NC
1	NC	NC	NC	NC

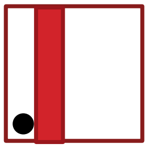
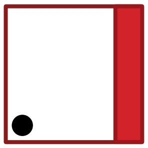


Table 5.5. OSD335X Ball Map Top View (Columns U-Y)

	U	V	W	Y
20	SYS_VDD1_3P3V	SYS_VDD1_3P3V	VSS	EXTL3B
19	VSS	VSS	VSS	EXTL3A
18	GPMC_BEN1	VSS	VSS	VSS
17	GPMC_WPN	GPMC_A11	VSS	EXTL2B
16	GPMC_A09	GPMC_A08	VSS	EXTL2A
15	GPMC_A06	GPMC_A05	VSS	VSS
14	GPMC_A02	GPMC_A01	VSS	EXTL1B
13	GPMC_AD15	GPMC_AD14	VSS	EXTL1A
12	GPMC_AD11	GPMC_CLK	VSS	VSS
11	NC	NC	VSS	SYS_VDD2_3P3V
10	GPMC_AD08	NC	VSS	VSS
9	GPMC_CSN1	GPMC_CSN2	VSS	VIN_USB
8	GPMC_AD04	GPMC_AD05	VSS	VIN_USB
7	GPMC_AD00	GPMC_AD01	VSS	VSS
6	GPMC_WEN	GPMC_CSN0	VSS	VIN_AC
5	LCD_VSYNC	LCD_PCLK	VSS	VIN_AC
4	LCD_DATA11	LCD_DATA14	SYS_VOUT	SYS_VOUT
3	LCD_DATA10	LCD_DATA13	VSS	VIN_BAT
2	LCD_DATA09	LCD_DATA12	VSS	VIN_BAT
1	LCD_DATA08	VSS	BAT_TEMP	BAT_VOLT



GPMC_AD15	GPMC Address and Data
GPMC_ADVN_ALE	GPMC Address Valid / Address Latch Enable
GPMC_BEN0_CLE	GPMC Byte Enable 0 / Command Latch Enable
GPMC_BEN1	GPMC Byte Enable 1
GPMC_CLK	GPMC Clock
GPMC_CSN0	GPMC Chip Select
GPMC_CSN1	GPMC Chip Select
GPMC_CSN2	GPMC Chip Select
GPMC_CSN3	GPMC Chip Select
GPMC_OEN_REN	GPMC Output Enable / Read Enable
GPMC_WAIT0	GPMC Wait 0
GPMC_WEN	GPMC Write Enable
GPMC_WPN	GPMC Write Protect
I2C0_SCL	I2C Clock
I2C0_SDA	I2C Data
LCD_AC_BIAS_EN	LCD AC Bias Enable Chip Select
LCD_DATA00	LCD Data Bus
LCD_DATA01	LCD Data Bus
LCD_DATA02	LCD Data Bus
LCD_DATA03	LCD Data Bus
LCD_DATA04	LCD Data Bus
LCD_DATA05	LCD Data Bus
LCD_DATA06	LCD Data Bus
LCD_DATA07	LCD Data Bus
LCD_DATA08	LCD Data Bus
LCD_DATA09	LCD Data Bus
LCD_DATA10	LCD Data Bus
LCD_DATA11	LCD Data Bus
LCD_DATA12	LCD Data Bus
LCD_DATA13	LCD Data Bus
LCD_DATA14	LCD Data Bus
LCD_DATA15	LCD Data Bus
LCD_HSYNC	LCD Horizontal Sync
LCD_PCLK	LCD Pixel Clock
LCD_VSYNC	LCD Vertical Sync
MCASP0_ACLKR	McASP0 Receive Bit Clock
MCASP0_ACLKX	McASP0 Transmit Bit Clock
MCASP0_AHCLKR	McASP0 Receive Master Clock
MCASP0_AHCLKX	McASP0 Transmit Master Clock
MCASP0_AXR0	McASP0 Serial Data
MCASP0_AXR1	McASP0 Serial Data
MCASP0_FSR	McASP0 Receive Frame Sync
MCASP0_FSX	McASP0 Transmit Frame Sync
MDC	MDIO Clock
MDIO	MDIO Data
MII1_COL	MII Collision
MII1_CRS	MII Carrier Sense
MII1_RX_CLK	MII Receive Clock
MII1_RX_DV	MII Receive Data Valid
MII1_RX_ER	MII Receive Data Error
MII1_RXD0	MII Receive Data
MII1_RXD1	MII Receive Data
MII1_RXD2	MII Receive Data
MII1_RXD3	MII Receive Data
MII1_TX_CLK	MII Transmit Clock
MII1_TX_EN	MII Transmit Enable
MII1_TXD0	MII Transmit Data
MII1_TXD1	MII Transmit Data
MII1_TXD2	MII Transmit Data
MII1_TXD3	MII Transmit Data
MMC0_CLK	MMC/SD/SDIO Clock
MMC0_CMD	MMC/SD/SDIO Command
MMC0_DAT0	MMC/SD/SDIO Data

MMC0_DAT1	MMC/SD/SDIO Data
MMC0_DAT2	MMC/SD/SDIO Data
MMC0_DAT3	MMC/SD/SDIO Data
NC	No Connect
OSC0_GND	High Frequency Oscillator Ground
OSC0_IN	High Frequency Oscillator Input
OSC0_OUT	High Frequency Oscillator Output
OSC1_GND	Real Time Clock Oscillator Ground
OSC1_IN	Real Time Clock Oscillator Input
OSC1_OUT	Real Time Clock Oscillator Output
PMIC_IN_I2C_SCL	TPS65217C SCL Input
PMIC_IN_I2C_SDA	TPS65217C SDA Input / Output
PMIC_IN_PB_IN	TPS65217C PB_IN Input
PMIC_IN_PWR_EN	TPS65217C PWR_EN Input
PMIC_OUT_LDO_PGOOD	TPS65217C LDO_PGOOD Output
PMIC_OUT_NINT	TPS65217C NINT Output
PMIC_OUT_NWAKEUP	TPS65217C NWAKEUP Output
PMIC_OUT_PGOOD	TPS65217C PGOOD Output
PMIC_POWER_EN	AM335x PMIC_POWER_EN Output
PWRONRSTN	Power On Reset Input (Active Low)
RMII1_REF_CLK	RMII Reference Clock
RTC_KALDO_ENN	Enable input for internal CAP_VDD_RTC voltage regulator (Active Low)
RTC_PWRONRSTN	RTC Reset Input (Active Low)
SPI0_CS0	SPI Chip Select
SPI0_CS1	SPI Chip Select
SPI0_D0	SPI Data
SPI0_D1	SPI Data
SPI0_SCLK	SPI Clock
SYS_ADC_1P8V	Output Power Supply, Analog, 1.8VDC
SYS_RTC_1P8V	Output Power Supply, RTC Voltage Domain, 1.8VDC
SYS_VDD_1P8V	Output Power Supply, Digital, 1.8VDC
SYS_VDD1_3P3V	Output Power Supply, Primary, 3.3VDC
SYS_VDD2_3P3V	Output Power Supply, Secondary, 3.3VDC
SYS_VOUT	TPS65217C SYS Output
TCK	JTAG Test Clock
TDI	JTAG Test Data Input
TDO	JTAG Test Data Output
TESTOUT	RESERVED
TMS	JTAG Test Mode Select
TRSTN	JTAG Test Reset
UART0_CTSN	UART Clear to Send
UART0_RTSN	UART Request to Send
UART0_RXD	UART Receive Data
UART0_TXD	UART Transmit Data
UART1_CTSN	UART Clear to Send
UART1_RTSN	UART Request to Send
UART1_RXD	UART Receive Data
UART1_TXD	UART Transmit Data
USB0_CE	USB0 Charger Enable Output
USB0_DM	USB0 Data (-)
USB0_DP	USB0 Data (+)
USB0_DRVVBUS	USB0 VBUS Control Output
USB0_ID	USB0 OTG ID
USB0_VBUS	USB0 VBUS
USB1_CE	USB1 Data (-)
USB1_DM	USB1 Data (+)
USB1_DP	USB1 VBUS Control Output
USB1_DRVVBUS	USB1 OTG ID
USB1_ID	USB1 VBUS
USB1_VBUS	USB1 Data (-)
VDD_CORE	Internal Power Supply Test Point
VDD_MPU	Internal Power Supply Test Point
VDD_MPU_MON	AM335x VDD_MPU_MON Signal

VDDS_DDR	Internal Power Supply Test Point
VDDS_PLL	Internal Power Supply Test Point
VDDSHV_3P3V	Internal Power Supply Test Point
VIN_AC	TPS65217C AC Input
VIN_BAT	TPS65217C BAT Input / Output
VIN_USB	TPS65217C USB Input
VPP	RESERVED
VREFP	Analog Positive Reference Input
VSS	Digital Ground
VSSA_ADC	Analog Ground, Analog Negative Reference Input
WARMRSTN	Warm Reset (Active Low)
XDMA_EVENT_INTR0	External DMA Event or Interrupt 0
XDMA_EVENT_INTR1	External DMA Event or Interrupt 1

5.2 AM335x Relocated Signals

A small number of signals from the AM335x have been moved to a different location on the OSD335x. For more information on these signals please refer to AN1002. A link to it is provided in the Reference Documents section of this document.

5.3 Not Connected Balls

The OSD335x ball map contains a number of balls which are marked NC (No Connect). These balls must be left unconnected on the system PCB since they may be used for other purposes in future versions of the OSD335x.

Most of these balls are from the AM335x pins associated with the DDR3 interface. They are not brought out because they are exclusively used internally to connect the AM335x with the DDR Memory. Several other balls in the ball map are also NC due to other functions handled internal to the OSD335x.

5.4 Reserved Signals

There is a subset of signals that are available on the OSD335x ball map but ***should not be*** used externally to the device. These signals are used internally to the OSD335x and using them could significantly affect the performance of the device. They are provided for test purposes only. The list of signals that should not be used can be found in Table 5.7.

Table 5.7. Reserved Signals

Reserved Signals
TESTOUT
CAP_VBB_MPU
CAP_VDD_SRAM_CORE
CAP_VDD_SRAM_MPU
VPP
EXTL1A
EXTL1B
EXTL2A
EXTL2B
EXTL3A
EXTL3B

7 Power Management

The power management portion of the OSD335x consists of two devices, the TPS65217C (PMIC) and the TL5209 (LDO). These devices are used to provide the necessary power rails to the AM335x and the DDR3. They also provide power supply outputs that may be used to power circuitry external to the OSD335x. This section describes how to power the OSD335x in a system and the outputs that can be used. The OSD335x has a complicated power distribution network and care must be taken to read and understand the proper use of the external connections to the power supplies.

7.1 Input Power

The OSD335x may be powered by any combination of the following input power supplies. Please refer to the TPS65217C datasheet for details.

7.1.1 VIN_AC

The OSD335x may be powered by an external AC Adaptor at 5.0 VDC.

7.1.2 VIN_USB

The OSD335x may be powered by a USB port at 5.0 VDC.

7.1.3 VIN_BAT

The OSD335x may be powered by a Li-Ion or Li-Polymer Battery.

7.2 Output Power

The OSD335x produces the following output power supplies.

7.2.1 SYS_VOUT: Switched VIN_AC, VIN_USB, or VIN_BAT

The OSD335x contains a shared supply to power the AM335x, DDR3, and TL5209 which is also used to power external circuitry. This is supplied by the TPS65217C SYS output. The SYS output is a switched connection to one of the input power supplies selected by the TPS65217C as described in the datasheet for that device.

7.2.2 SYS_VDD1_3P3V

The OSD335x contains a dedicated 3.3 VDC supply[1] to power external circuitry. This is supplied by the TL5209, powered by the TPS65217C SYS output, and enabled by the TPS65217C LDO4.

7.2.3 SYS_VDD2_3P3V

The OSD335x contains a dedicated 3.3 VDC supply to power external circuitry. This is supplied by the TPS65217C LDO2.

---

[1] The nominal output voltage of the LDO has been set to 3.33V using 1% tolerance resistors. This implies a nominal voltage range of 3.29V – 3.37V. The LDO has an accuracy of 1 – 2% depending on the ambient temperature which will also affect the nominal voltage. See the TL5209 datasheet for more information.

7.4 Total Current Consideration

The total current consumption of all power rails must not exceed the recommended input currents described in Table 8.2. This includes power consumption within the SiP from the AM335x and the DDR3, as well as all external loads on the output power rails from Section 7.2.

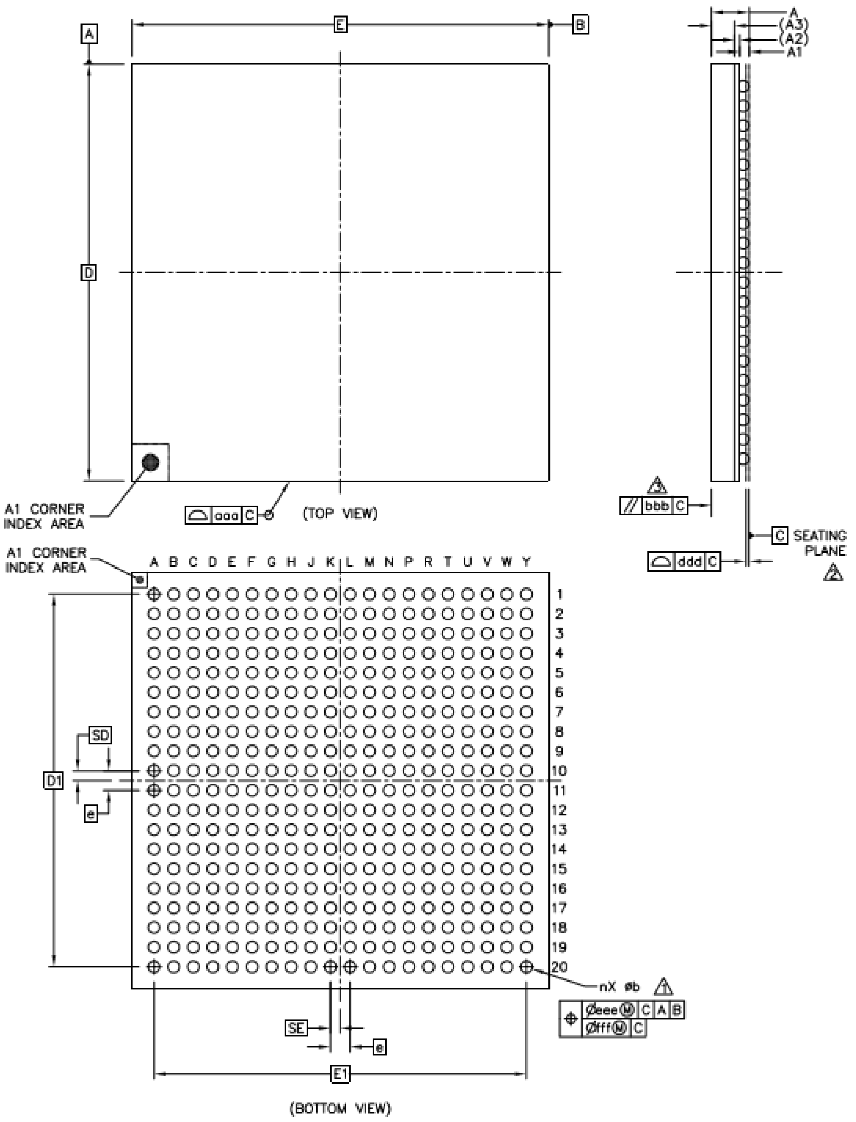
The power consumed by the AM335x can be estimated using the *AM335x Power Estimation Tool* found in the Reference Documents section of this document. When estimating power consumption, the efficiencies and types of the OSD335x internal power supplies must be considered. Refer to the "*Connections Diagram for TPS65217C and AM335x*" section of *Powering the AM335x with the TPS65217x* found in the Reference Documents section of this document for more information on the power supplies providing power to the AM335x.

9 Packaging Information

The OSD335x is packaged in a 400 ball, Ball Grid Array (BGA). The package size is 27 X 27 millimeters with a ball pitch of 1.27mm. This section will give you the specifics on the package.

9.1 Mechanical Dimensions

The mechanical drawings of the OSD335x show pin A1 in the lower left hand corner when looking at the top view of the device. Pin A1 is in the upper left hand corner if looking at the balls from the bottom view of the package. The PCB layout should have pin A1 in the lower left hand corner when looking at the top side of the PCB where the OSD335x will be attached.



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	2.6
STAND OFF	A1	0.5	---	0.7
SUBSTRATE THICKNESS	A2		0.35	REF
MOLD THICKNESS	A3		1.5	REF
BODY SIZE	D		27	BSC
	E		27	BSC
BALL DIAMETER			0.75	
BALL OPENING			0.6	
BALL WIDTH	b	0.6	---	0.9
BALL PITCH	e		1.27	BSC
BALL COUNT	n		400	
EDGE BALL CENTER TO CENTER	D1		24.13	BSC
	E1		24.13	BSC
BODY CENTER TO CONTACT BALL	SD		0.635	BSC
	SE		0.635	BSC
PACKAGE EDGE TOLERANCE	aaa		0.2	
MOLD FLATNESS	bbb		0.35	
COPLANARITY	ddd		0.2	
BALL OFFSET (PACKAGE)	eee		0.3	
BALL OFFSET (BALL)	fff		0.15	

NOTES:

1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.
2. DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

9.2 Reflow Instructions

The reflow profile for this package should be in accordance with the Lead-free process for BGA. A peak reflow temperature is recommended to be 245°C.

Texas Instruments provides a good overview of Handling & Process Recommendations in AN-2029 for this type of device. A link to the document can be found in the Reference Documents section of this document.

9.3 Storage Recommendations

The OSD335x Family of devices are sensitive to moisture and need to be handled in specific ways to make sure they function properly during and after the manufacturing process. The OSD335x Family of devices are rated with a Moisture Sensitivity Level (MSL) of 4. This means that they are typically stored in a sealed Dry Pack.

⚠ Once the sealed Dry Pack is opened the OSD335x needs to be used within 72 hours to avoid further processing. If the OSD335x has been exposed for more than 72 hours, then it is required that you bake the device for 24 hours at 125°C before using.

Alternatively, the devices could be stored in a dry cabinet with humidity <10% to avoid the baking requirement.

For more information, please refer to the Texas Instruments AN-2029 which can be found in the Reference Documents section of this document.