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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

2 0 0 0 0 0	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	792
Total RAM Bits	-
Number of I/O	101
Number of Gates	30000
Voltage - Supply	1.14V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	128-TQFP
Supplier Device Package	128-VTQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/aglp030v2-vq128i

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong







Note: *Not supported by AGLP030 devices

Figure 1-1 • IGLOO PLUS Device Architecture Overview with Four I/O Banks (AGLP030, AGLP060, and AGLP125)

Flash*Freeze Technology

The IGLOO PLUS device has an ultra-low power static mode, called Flash*Freeze mode, which retains all SRAM and register information and can still quickly return to normal operation. Flash*Freeze technology enables the user to quickly (within 1 μ s) enter and exit Flash*Freeze mode by activating the Flash*Freeze pin while all power supplies are kept at their original values. In addition, I/Os and global I/Os can still be driven and can be toggling without impact on power consumption, clocks can still be driven or can be toggling without impact on power consumption, and the device retains all core registers, SRAM information, and I/O states. I/Os can be individually configured to either hold their previous state or be tristated during Flash*Freeze mode. Alternatively, they can be set to a certain state using weak pull-up or pull-down I/O attribute configuration. No power is consumed by the I/O banks, clocks, JTAG pins, or PLL, and the device consumes as little as 5 μ W in this mode.

Flash*Freeze technology allows the user to switch to Active mode on demand, thus simplifying the power management of the device.

The Flash*Freeze pin (active low) can be routed internally to the core to allow the user's logic to decide when it is safe to transition to this mode. Refer to Figure 1-2 for an illustration of entering/exiting Flash*Freeze mode. It is also possible to use the Flash*Freeze pin as a regular I/O if Flash*Freeze mode usage is not planned.



Figure 1-2 • IGLOO PLUS Flash*Freeze Mode

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IGLOO PLUS DC and Switching Characteristics

Symbol	Pa	rameter	Commercial	Industrial	Units
TJ	Junction temperature ²	0 to + 85	-40 to +100	°C	
VCC ³	1.5 V DC core supply voltage	4	1.425 to 1.575	1.425 to 1.575	V
	1.2 V–1.5 V wide range core	voltage ^{5,6}	1.14 to 1.575	1.14 to 1.575	V
VJTAG	JTAG DC voltage		1.4 to 3.6	1.4 to 3.6	V
VPUMP ⁷	Programming voltage	3.15 to 3.45	3.15 to 3.45	V	
		Operation	0 to 3.6	0 to 3.6	V
VCCPLL ⁸	Analog power supply (PLL)	1.5 V DC core supply voltage ⁴	1.425 to 1.575	1.425 to 1.575	V
		1.2 V-1.5 V wide range core voltage ⁵	1.14 to 1.575	1.14 to 1.575	V
VCCI	1.2 V DC supply voltage ⁵		1.14 to 1.26	1.14 to 1.26	V
	1.2 V DC wide range supply	1.14 to 1.575	1.14 to 1.575	V	
	1.5 V DC supply voltage		1.425 to 1.575	1.425 to 1.575	V
	1.8 V DC supply voltage		1.7 to 1.9	1.7 to 1.9	V
	2.5 V DC supply voltage	2.3 to 2.7	2.3 to 2.7	V	
	3.3 V wide range DC supply	voltage ⁹	2.7 to 3.6	2.7 to 3.6	V
	3.3 V DC supply voltage		3.0 to 3.6	3.0 to 3.6	V

Table 2-2 • Recommended Operating Conditions^{1,2}

Notes:

- 1. All parameters representing voltages are measured with respect to GND unless otherwise specified.
- 2. To ensure targeted reliability standards are met across ambient and junction operating temperatures, Microsemi recommends that the user follow best design practices using Microsemi's timing and power simulation tools.
- 3. The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-21 on page 2-19. VCCI should be at the same voltage within a given I/O bank.
- 4. For IGLOO[®] PLUS V5 devices
- 5. For IGLOO PLUS V2 devices only, operating at VCCI \geq VCC.
- 6. All IGLOO PLUS devices (V5 and V2) must be programmed with the VCC core voltage at 1.5 V. Applications using V2 devices powered by a 1.2 V supply must switch the core supply to 1.5 V for in-system programming.
- 7. VPUMP can be left floating during operation (not programming mode).
- 8. VCCPLL pins should be tied to VCC pins. See the Pin Descriptions chapter of the IGLOO PLUS FPGA Fabric User's Guide for further information.
- 9. 3.3 V wide range is compliant to the JDEC8b specification and supports 3.0 V VCCI operation.
- 10. VMV pins must be connected to the corresponding VCCI pins. See the "Pin Descriptions" chapter of the IGLOO FPGA Fabric User's Guide for further information.
- 11. Software Default Junction Temperature Range in the Libero SoC software is set to 0°C to +70°C for commercial, and -40°C to +85°C for industrial. To ensure targeted reliability standards are met across the full range of junction temperatures, Microsemi recommends using custom settings for temperature range before running timing and power analysis tools. For more information regarding custom settings, refer to the New Project Dialog Box in the Libero SoC Online Help.

Parameter	Parameter Definition
t _{DP}	Data to Pad delay through the Output Buffer
t _{PY}	Pad to Data delay through the Input Buffer
t _{DOUT}	Data to Output Buffer delay through the I/O interface
t _{EOUT}	Enable to Output Buffer Tristate Control delay through the I/O interface
t _{DIN}	Input Buffer to Data delay through the I/O interface
t _{HZ}	Enable to Pad delay through the Output Buffer—High to Z
t _{ZH}	Enable to Pad delay through the Output Buffer—Z to High
t _{LZ}	Enable to Pad delay through the Output Buffer—Low to Z
t _{ZL}	Enable to Pad delay through the Output Buffer—Z to Low
t _{ZHS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to High
t _{ZLS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to Low

Table 2-24 • I/O AC Parameter Definitions

Micros IGLOO PLUS Low Power Flash FPGAs

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IGLOO PLUS DC and Switching Characteristics

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

2.5 V LVCMOS	v	IL	v	н	VOL	VOH	IOL	юн	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	-0.3	0.7	1.7	3.6	0.7	1.7	2	2	16	18	10	10
4 mA	-0.3	0.7	1.7	3.6	0.7	1.7	4	4	16	18	10	10
6 mA	-0.3	0.7	1.7	3.6	0.7	1.7	6	6	32	37	10	10
8 mA	-0.3	0.7	1.7	3.6	0.7	1.7	8	8	32	37	10	10
12 mA	-0.3	0.7	1.7	3.6	0.7	1.7	12	12	65	74	10	10

Table 2-46 • Minimum and Maximum DC Input and Output Levels

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.

2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

4. Currents are measured at 85°C junction temperature.

5. Software default selection highlighted in gray.

Test Point
$$rac{1}{1}$$
 $rac{1}{1}$ $rac{1$

Figure 2-8 • AC Loading

Table 2-47 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	2.5	1.2	5

Note: *Measuring point = Vtrip. See Table 2-23 on page 2-20 for a complete table of trip points.



1.5 V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for generalpurpose 1.5 V applications. It uses a 1.5 V input buffer and a push-pull output buffer.

Table 2-58 •	Minimum and	Maximum DC	Input and Out	put Levels
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1.5 V LVCMOS		VIL	VIH		VOL	VOH	IOL	юн	IOSL	IOSH	IIL¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	µA⁴
2 mA	-0.3	0.35 * VCCI	0.7 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	13	16	10	10
4 mA	-0.3	0.35 * VCCI	0.7 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	4	4	25	33	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.

2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

4. Currents are measured at 85°C junction temperature.

5. Software default selection highlighted in gray.



Figure 2-10 • AC Loading

Table 2-59 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	1.5	0.75	5

Note: *Measuring point = Vtrip. See Table 2-23 on page 2-20 for a complete table of trip points.





Timing Characteristics 1.5 V DC Core Voltage

Table 2-82 • Register Delays

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
t _{CLKQ}	Clock-to-Q of the Core Register	0.89	ns
t _{SUD}	Data Setup Time for the Core Register	0.81	ns
t _{HD}	Data Hold Time for the Core Register	0.00	ns
t _{SUE}	Enable Setup Time for the Core Register	0.73	ns
t _{HE}	Enable Hold Time for the Core Register	0.00	ns
t _{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.60	ns
t _{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.62	ns
t _{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	ns
t _{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.24	ns
t _{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	ns
t _{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.23	ns
t _{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.30	ns
t _{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.30	ns
t _{CKMPWH}	Clock Minimum Pulse Width High for the Core Register	0.56	ns
t _{CKMPWL}	Clock Minimum Pulse Width Low for the Core Register	0.56	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

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IGLOO PLUS DC and Switching Characteristics

1.2 V DC Core Voltage

Table 2-83 • Register Delays

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V

Parameter	Description	Std.	Units
t _{CLKQ}	Clock-to-Q of the Core Register	1.61	ns
t _{SUD}	Data Setup Time for the Core Register	1.17	ns
t _{HD}	Data Hold Time for the Core Register	0.00	ns
t _{SUE}	Enable Setup Time for the Core Register	1.29	ns
t _{HE}	Enable Hold Time for the Core Register	0.00	ns
t _{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.87	ns
t _{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.89	ns
t _{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	ns
t _{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.24	ns
t _{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	ns
t _{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.24	ns
t _{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.46	ns
t _{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.46	ns
t _{CKMPWH}	Clock Minimum Pulse Width High for the Core Register	0.95	ns
t _{CKMPWL}	Clock Minimum Pulse Width Low for the Core Register	0.95	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.



Global Tree Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard–dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the "Clock Conditioning Circuits" section on page 2-61. Table 2-84 to Table 2-89 on page 2-60 present minimum and maximum global clock delays within each device. Minimum and maximum delays are measured with minimum and maximum loading.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-84 • AGLP030 Global Resource

Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

		Std.		
Parameter	Description	Min. ¹	Max. ²	Units
t _{RCKL}	Input Low Delay for Global Clock	1.21	1.42	ns
t _{RCKH}	Input High Delay for Global Clock	1.23	1.49	ns
t _{RCKMPWH}	Minimum Pulse Width High for Global Clock	1.18		ns
t _{RCKMPWL}	Minimum Pulse Width Low for Global Clock	1.15		ns
t _{RCKSW}	Maximum Skew for Global Clock		0.27	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-85 • AGLP060 Global Resource Commercial-Case Conditions: T₁ = 70°C, VCC = 1.425 V

		Std.		
Parameter	Description	Min. ¹	Max. ²	Units
t _{RCKL}	Input Low Delay for Global Clock	1.32	1.62	ns
^t _{RCKH}	Input High Delay for Global Clock	1.34	1.72	ns
t _{RCKMPWH}	Minimum Pulse Width High for Global Clock	1.18		ns
t _{RCKMPWL}	Minimum Pulse Width Low for Global Clock	1.15		ns
t _{RCKSW}	Maximum Skew for Global Clock		0.38	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.



Table 2-88 • AGLP060 Global Resource Commercial-Case Conditions: T_J = 70°C, VCC = 1.14 V

		Std.		
Parameter	Description	Min. ¹	Max. ²	Units
t _{RCKL}	Input Low Delay for Global Clock	2.02	2.43	ns
t _{RCKH}	Input High Delay for Global Clock	2.09	2.65	ns
t _{RCKMPWH}	Minimum Pulse Width High for Global Clock	1.40		ns
t _{RCKMPWL}	Minimum Pulse Width Low for Global Clock	1.65		ns
t _{RCKSW}	Maximum Skew for Global Clock		0.56	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3. For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

Table 2-89 • AGLP125 Global Resource

Commercial-Case Conditions: T_J = 70°C, VCC = 1.14 V

		S	td.	
Parameter	Description	Min. ¹	Max. ²	Units
t _{RCKL}	Input Low Delay for Global Clock	2.08	2.54	ns
t _{RCKH}	Input High Delay for Global Clock	2.15	2.77	ns
t _{RCKMPWH}	Minimum Pulse Width High for Global Clock	1.40		ns
t _{RCKMPWL}	Minimum Pulse Width Low for Global Clock	1.65		ns
t _{RCKSW}	Maximum Skew for Global Clock		0.62	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3. For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

Clock Conditioning Circuits

CCC Electrical Specifications

Timing Characteristics

Table 2-90 • IGLOO PLUS CCC/PLL Specification

For IGLOO PLUS V2 or V5 devices, 1.5 V DC Core Supply Voltage

Parameter	Min.	Тур.	Max.	Units
Clock Conditioning Circuitry Input Frequency fIN_CCC	1.5		250	MHz
Clock Conditioning Circuitry Output Frequency f _{OUT_CCC}	0.75		250	MHz
Delay Increments in Programmable Delay Blocks ^{1, 2}		360 ³		ps
Number of Programmable Values in Each Programmable Delay Block			32	
Serial Clock (SCLK) for Dynamic PLL ^{4,5}			100	MHz
Input Cycle-to-Cycle Jitter (peak magnitude)			1	ns
Acquisition Time				
LockControl = 0			300	μs
LockControl = 1			6.0	ms
Tracking Jitter ⁶				
LockControl = 0			2.5	ns
LockControl = 1			1.5	ns
Output Duty Cycle	48.5		51.5	%
Delay Range in Block: Programmable Delay 1 ^{1, 2}	1.25		15.65	ns
Delay Range in Block: Programmable Delay 2 ^{1, 2}	0.469		15.65	ns
Delay Range in Block: Fixed Delay ^{1, 2}		3.5		ns
VCO Output Peak-to-Peak Period Jitter F _{CCC_OUT} ⁷	Maximum Peak-to-Peak Period Jitter ^{7,8}		l Jitter ^{7,8,9}	
	$SSO \leq 2$	$SSO \leq 4$	$SSO \leq 8$	$\text{SSO} \leq 16$
0.75 MHz to 50 MHz	0.50%	0.60%	0.80%	1.20%
50 MHz to 250 MHz	2.50%	4.00%	6.00%	12.00%

Notes:

1. This delay is a function of voltage and temperature. See Table 2-6 on page 2-6 and Table 2-7 on page 2-6 for deratings.

2. $T_J = 25^{\circ}C$, VCC = 1.5 V

- 3. When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help associated with the core for more information.
- 4. Maximum value obtained for a STD speed grade device in Worst Case Commercial Conditions. For specific junction temperature and voltage supply, refer to Table 2-6 on page 2-6 and Table 2-7 on page 2-6 for derating values.
- 5. The AGLP030 device does not support a PLL.
- 6. Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.
- 7. VCO output jitter is calculated as a percentage of the VCO frequency. The jitter (in ps) can be calculated by multiplying the VCO period by the per cent jitter. The VCO jitter (in ps) applies to CCC_OUT regardless of the output divider settings. For example, if the jitter on VCO is 300 ps, the jitter on CCC_OUT is also 300 ps, regardless of the output divider settings.
- 8. Measurements done with LVTTL 3.3 V 8 mA I/O drive strength and high slew rate, VCC/VCCPLL = 1.425 V, VCCI = 3.3 V, VQ/PQ/TQ type of packages, 20 pF load.
- 9. SSO are outputs that are synchronous to a single clock domain and have clock-to-out times that are within ±200 ps of each other. Switching I/Os are placed outside of the PLL bank. Refer to the "Simultaneously Switching Outputs (SSOs) and Printed Circuit Board Layout" section in the IGLOO PLUS FPGA Fabric User's Guide.

Timing Waveforms











Figure 2-32 • FIFO Reset







Pin Descriptions and Packaging

JTAG Pins

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the part must be supplied to allow JTAG signals to transition the device. Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND.

тск

Test Clock

Test clock input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pullup/-down resistor. If JTAG is not used, Microsemi recommends tying off TCK to GND through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.

Note that to operate at all VJTAG voltages, 500 Ω to 1 k Ω will satisfy the requirements. Refer to Table 3-2 for more information.

Table 3-2 • Recommended	I Tie-Off Values	for the T	CK and TRST	Pins
-------------------------	------------------	-----------	-------------	------

VJTAG	Tie-Off Resistance	
VJTAG at 3.3 V	200 Ω to 1 k Ω	
VJTAG at 2.5 V	200 Ω to 1 k Ω	
VJTAG at 1.8 V	500 Ω to 1 k Ω	
VJTAG at 1.5 V	500 Ω to 1 k Ω	

Notes:

- 1. Equivalent parallel resistance if more than one device is on the JTAG chain
- 2. The TCK pin can be pulled up/down.
- 3. The TRST pin is pulled down.

TDI

Test Data Input

Test Data Output

Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.

TDO

Serial output for JTAG boundary scan, ISP, and UJTAG usage.

TMS

Test Mode Select

The TMS pin controls the use of the IEEE 1532 boundary scan pins (TCK, TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin.

TRST

Boundary Scan Reset Pin

The TRST pin functions as an active-low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor could be included to ensure the test access port (TAP) is held in reset mode. The resistor values must be chosen from Table 3-2 and must satisfy the parallel resistance value requirement. The values in Table 3-2 correspond to the resistor recommended when a single device is used, and the equivalent parallel resistor when multiple devices are connected via a JTAG chain.

In critical applications, an upset in the JTAG circuit could allow entrance to an undesired JTAG state. In such cases, Microsemi recommends tying off TRST to GND through a resistor placed close to the FPGA pin.

Note that to operate at all VJTAG voltages, 500 Ω to 1 k Ω will satisfy the requirements.

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IGLOO PLUS Low Power Flash FPGAs

CS281		CS281		
Pin Number	AGLP125 Function	Pin Number	AGLP125 Function	
R15	IO109RSB2	V10	IO133RSB2	
R16	GDA1/IO103RSB1	V11	IO127RSB2	
R18	GDB0/IO102RSB1	V12	IO123RSB2	
R19	GDC0/IO100RSB1	V13	IO120RSB2	
T1	IO171RSB3	V14	GND	
T2	GEC0/IO169RSB3	V15	IO113RSB2	
T4	GEB0/IO167RSB3	V16	GDA2/IO105RSB2	
T5	IO157RSB2	V17	TDI	
T6	IO158RSB2	V18	VCCIB2	
Τ7	IO148RSB2	V19	TDO	
Т8	IO145RSB2	W1	GND	
Т9	IO143RSB2	W2	FF/GEB2/IO163RSB	
T10	GND		2	
T11	IO129RSB2	W3	IO155RSB2	
T12	IO126RSB2	W4	IO152RSB2	
T13	IO125RSB2	W5	IO150RSB2	
T14	IO116RSB2	W6	IO147RSB2	
T15	GDC2/IO107RSB2	W7	IO142RSB2	
T16	TMS	W8	IO139RSB2	
T18	VJTAG	W9	IO136RSB2	
T19	GDB1/IO101RSB1	W10	VCCIB2	
U1	IO160RSB2	W11	IO128RSB2	
U2	GEA1/IO166RSB3	W12	IO124RSB2	
U6	IO151RSB2	W13	IO119RSB2	
U14	IO121RSB2	W14	IO115RSB2	
U18	TRST	W15	IO114RSB2	
U19	GDA0/IO104RSB1	W16	IO110RSB2	
V1	IO159RSB2	W17	GDB2/IO106RSB2	
V2	VCCIB3	W18	ТСК	
V3	GEC2/IO162RSB2	W19	GND	
V4	IO156RSB2			
V5	IO153RSB2			
V6	GND			
V7	IO144RSB2			
V8	IO141RSB2			

V9

IO140RSB2