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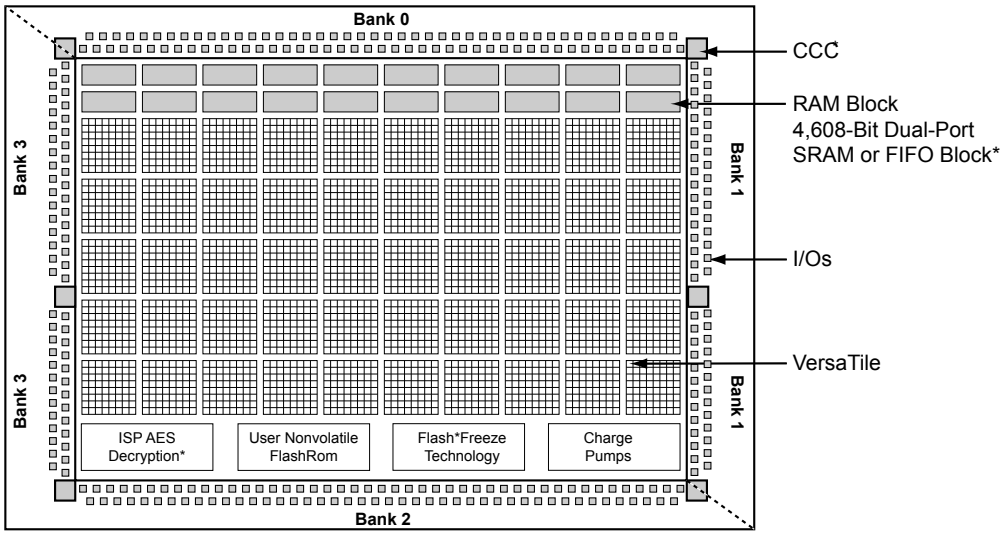
Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	792
Total RAM Bits	-
Number of I/O	101
Number of Gates	30000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	128-TQFP
Supplier Device Package	128-VTQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/aglp030v5-vq128



*Note: *Not supported by AGLP030 devices*

Figure 1-1 • **IGLOO PLUS Device Architecture Overview with Four I/O Banks (AGLP030, AGLP060, and AGLP125)**

*Flash*Freeze Technology*

The IGLOO PLUS device has an ultra-low power static mode, called Flash*Freeze mode, which retains all SRAM and register information and can still quickly return to normal operation. Flash*Freeze technology enables the user to quickly (within 1 µs) enter and exit Flash*Freeze mode by activating the Flash*Freeze pin while all power supplies are kept at their original values. In addition, I/Os and global I/Os can still be driven and can be toggling without impact on power consumption, clocks can still be driven or can be toggling without impact on power consumption, and the device retains all core registers, SRAM information, and I/O states. I/Os can be individually configured to either hold their previous state or be tristated during Flash*Freeze mode. Alternatively, they can be set to a certain state using weak pull-up or pull-down I/O attribute configuration. No power is consumed by the I/O banks, clocks, JTAG pins, or PLL, and the device consumes as little as 5 µW in this mode.

Flash*Freeze technology allows the user to switch to Active mode on demand, thus simplifying the power management of the device.

The Flash*Freeze pin (active low) can be routed internally to the core to allow the user's logic to decide when it is safe to transition to this mode. Refer to Figure 1-2 for an illustration of entering/exiting Flash*Freeze mode. It is also possible to use the Flash*Freeze pin as a regular I/O if Flash*Freeze mode usage is not planned.

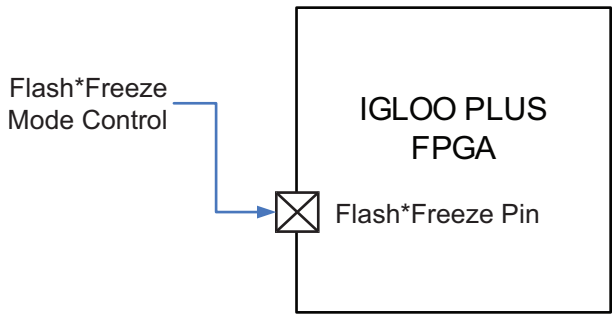


Figure 1-2 • **IGLOO PLUS Flash*Freeze Mode**

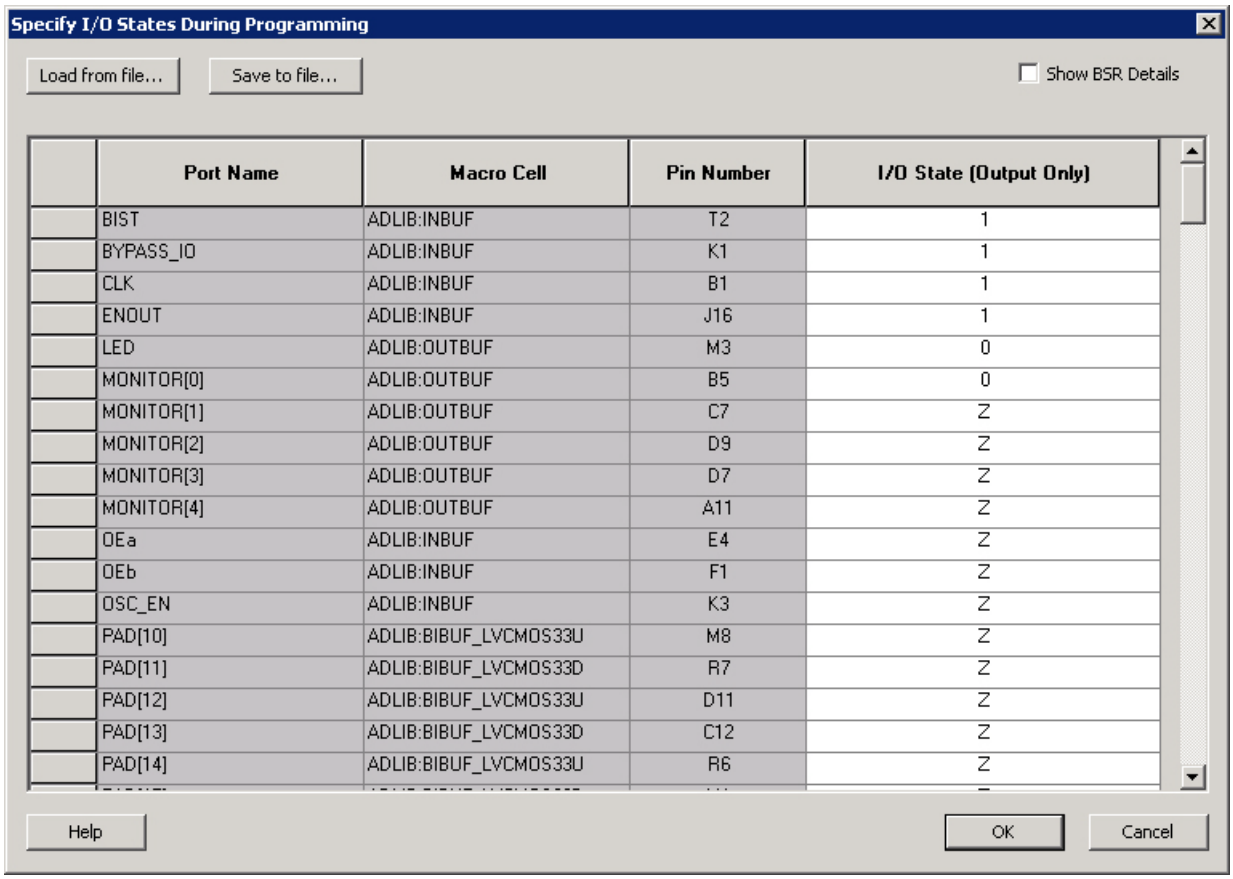


Figure 1-4 • **I/O States During Programming Window**

6. Click OK to return to the FlashPoint – Programming File Generator window.

Note: I/O States During programming are saved to the ADB and resulting programming files after completing programming file generation.

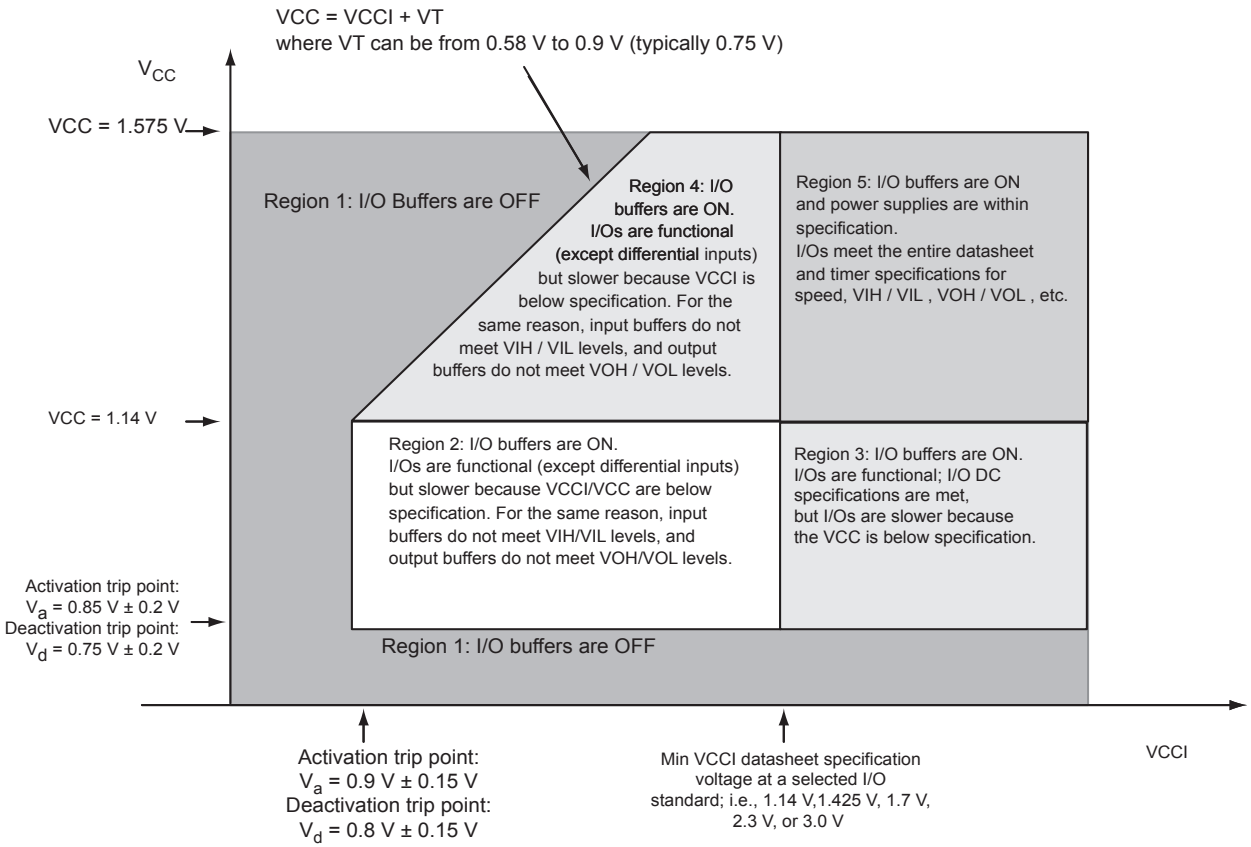


Figure 2-2 • **V2 Devices – I/O State as a Function of VCCI and VCC Voltage Levels**

Thermal Characteristics

Introduction

The temperature variable in the Microsemi Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction temperature to be higher than the ambient temperature.

EQ 1 can be used to calculate junction temperature.

$$T_J = \text{Junction Temperature} = \Delta T + T_A \qquad \textit{EQ 1}$$

where:

T_A = Ambient temperature

ΔT = Temperature gradient between junction (silicon) and ambient $\Delta T = \theta_{ja} * P$

θ_{ja} = Junction-to-ambient of the package. θ_{ja} numbers are located in Figure 2-5.

P = Power dissipation

Power Consumption of Various Internal Resources

***Table 2-15* • Different Components Contributing to Dynamic Power Consumption in IGLOO PLUS Devices For IGLOO PLUS V2 or V5 Devices, 1.5 V Core Supply Voltage**

Parameter	Definition	Device Specific Dynamic Power (µW/MHz)		
		AGLP125	AGLP060	AGLP030
PAC1	Clock contribution of a Global Rib	4.489	2.696	0.000[1]
PAC2	Clock contribution of a Global Spine	1.991	1.962	3.499
PAC3	Clock contribution of a VersaTile row	1.510	1.523	1.537
PAC4	Clock contribution of a VersaTile used as a sequential module	0.153	0.151	0.151
PAC5	First contribution of a VersaTile used as a sequential module	0.029	0.029	0.029
PAC6	Second contribution of a VersaTile used as a sequential module	0.323	0.323	0.323
PAC7	Contribution of a VersaTile used as a combinatorial module	0.280	0.300	0.278
PAC8	Average contribution of a routing net	1.097	1.081	1.130
PAC9	Contribution of an I/O input pin (standard-dependent)	See Table 2-13 on page 2-9.		
PAC10	Contribution of an I/O output pin (standard-dependent)	See Table 2-14 on page 2-9.		
PAC11	Average contribution of a RAM block during a read operation	25.00		
PAC12	Average contribution of a RAM block during a write operation	30.00		
PAC13	Dynamic contribution for PLL	2.70		

Note: 1. There is no Center Global Rib present in AGLP030, and thus it starts directly at the spine resulting in 0µW/MHz.

***Table 2-16* • Different Components Contributing to the Static Power Consumption in IGLOO PLUS Devices For IGLOO PLUS V2 or V5 Devices, 1.5 V Core Supply Voltage**

Parameter	Definition	Device-Specific Static Power (mW)		
		AGLP125	AGLP060	AGLP030
PDC1	Array static power in Active mode	See Table 2-12 on page 2-8		
PDC2	Array static power in Static (Idle) mode	See Table 2-11 on page 2-7		
PDC3	Array static power in Flash*Freeze mode	See Table 2-9 on page 2-7		
PDC4	Static PLL contribution	1.84[1]		
PDC5	Bank quiescent power (VCCI-dependent)	See Table 2-12 on page 2-8		

Notes:

1. *This is the minimum contribution of the PLL when operating at lowest frequency.*
2. *For a different output load, drive strength, or slew rate, Microsemi recommends using the Microsemi power spreadsheet calculator or the SmartPower tool in Libero SoC software.*

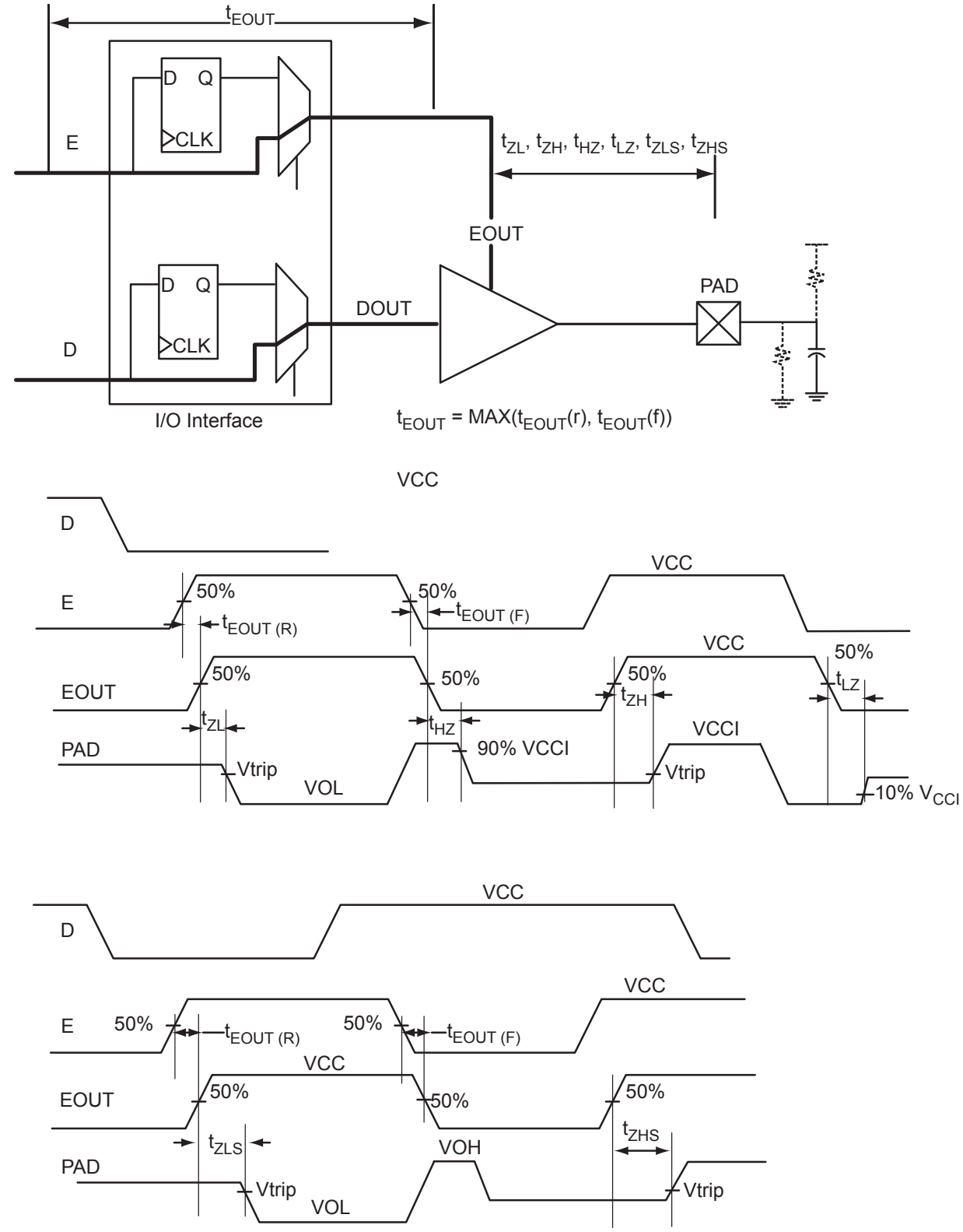


Figure 2-6 • **Tristate Output Buffer Timing Model and Delays (example)**

1.5 V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5 V applications. It uses a 1.5 V input buffer and a push-pull output buffer.

Table 2-58 • Minimum and Maximum DC Input and Output Levels

1.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
2 mA	–0.3	0.35 * VCCI	0.7 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	13	16	10	10
4 mA	–0.3	0.35 * VCCI	0.7 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	4	4	25	33	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

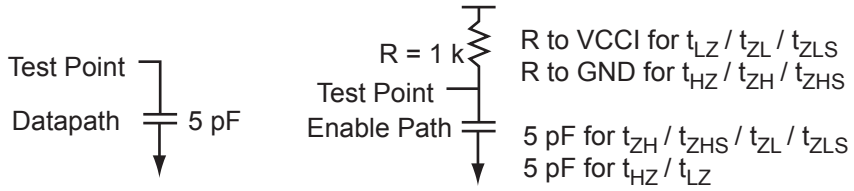


Figure 2-10 • AC Loading

Table 2-59 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	1.5	0.75	5

*Note: *Measuring point = Vtrip. See Table 2-23 on page 2-20 for a complete table of trip points.*

Timing Characteristics

Applies to 1.2 V DC Core Voltage

Table 2-70 • 1.2 V LVCMOS Wide Range Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 µA	2 mA	STD	0.98	8.27	0.19	1.57	2.34	0.67	7.94	6.77	3.00	3.11	ns

Notes:

1. *The minimum drive strength for any LVCMOS 1.2 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-71 • 1.2 V LVCMOS Wide Range High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 µA	2 mA	STD	0.98	3.38	0.19	1.57	2.34	0.67	3.26	2.78	2.99	3.24	ns

Notes:

1. *The minimum drive strength for any LVCMOS 1.2 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*
3. *Software default selection highlighted in gray.*

Timing Waveforms

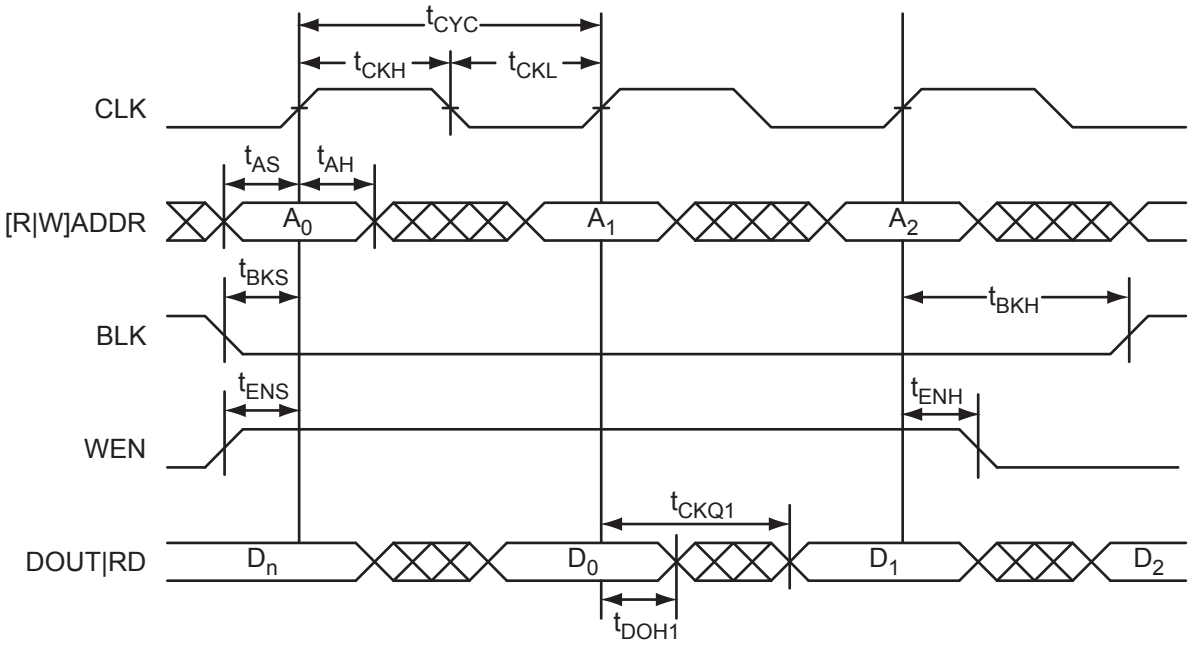


Figure 2-24 • **RAM Read for Pass-Through Output. Applicable to Both RAM4K9 and RAM512x18.**

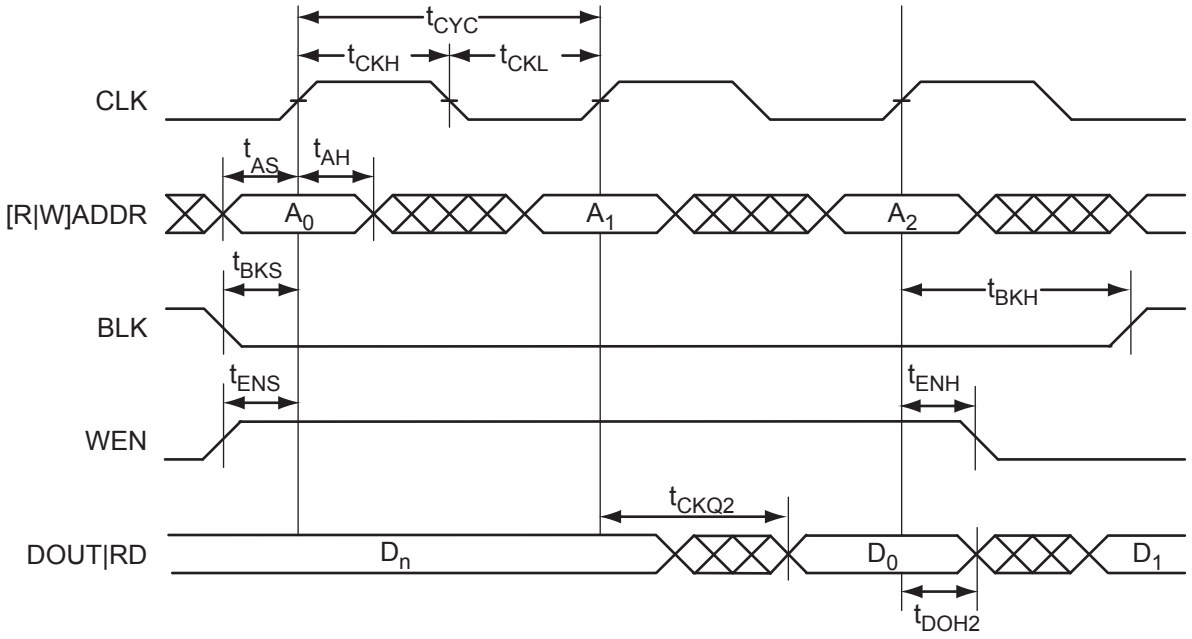


Figure 2-25 • **RAM Read for Pipelined Output. Applicable to Both RAM4K9 and RAM512x18.**

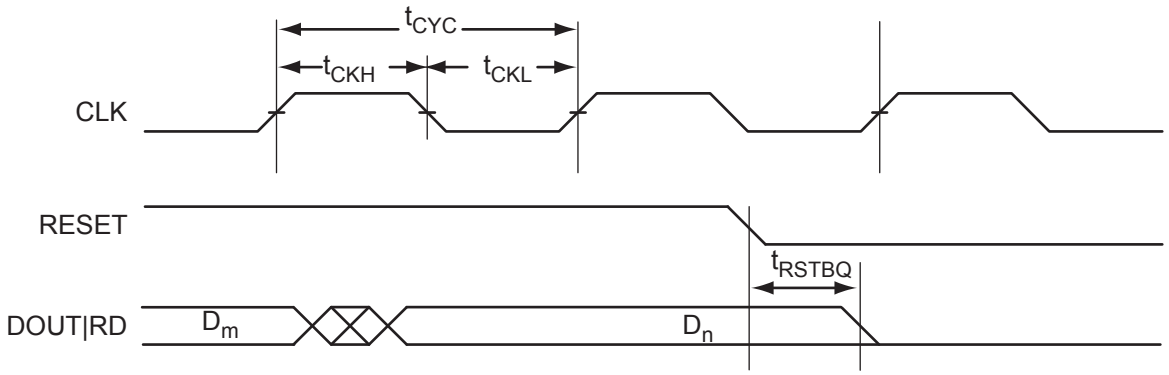


Figure 2-28 • **RAM Reset**

Timing Waveforms

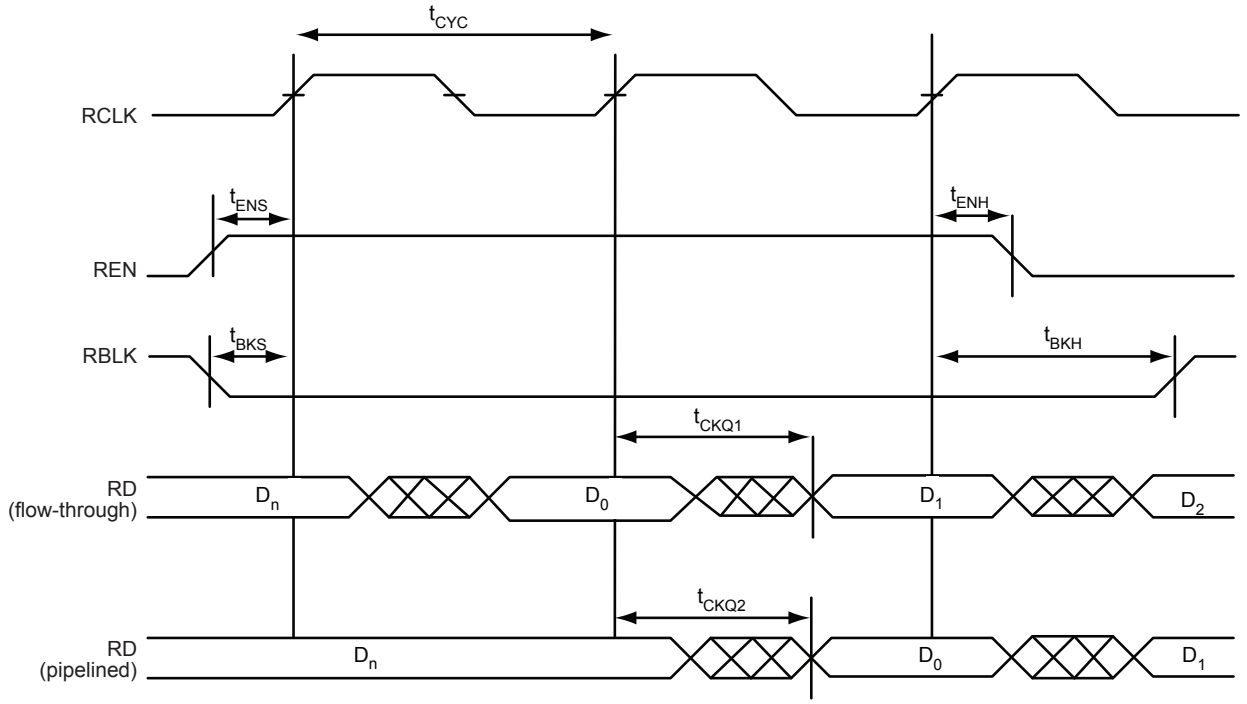


Figure 2-30 • **FIFO Read**

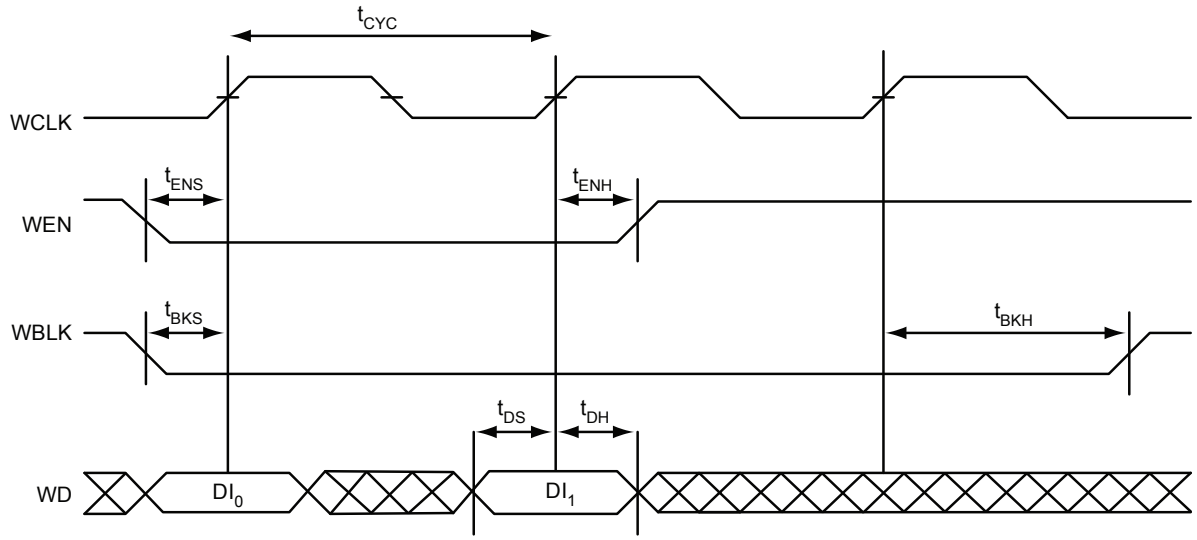


Figure 2-31 • **FIFO Write**

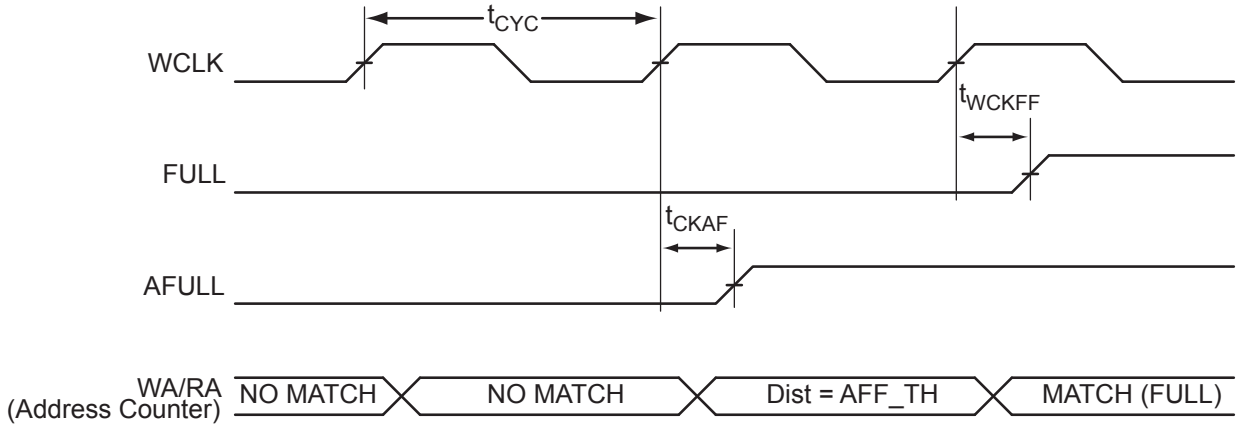


Figure 2-34 • **FIFO FULL Flag and AFULL Flag Assertion**

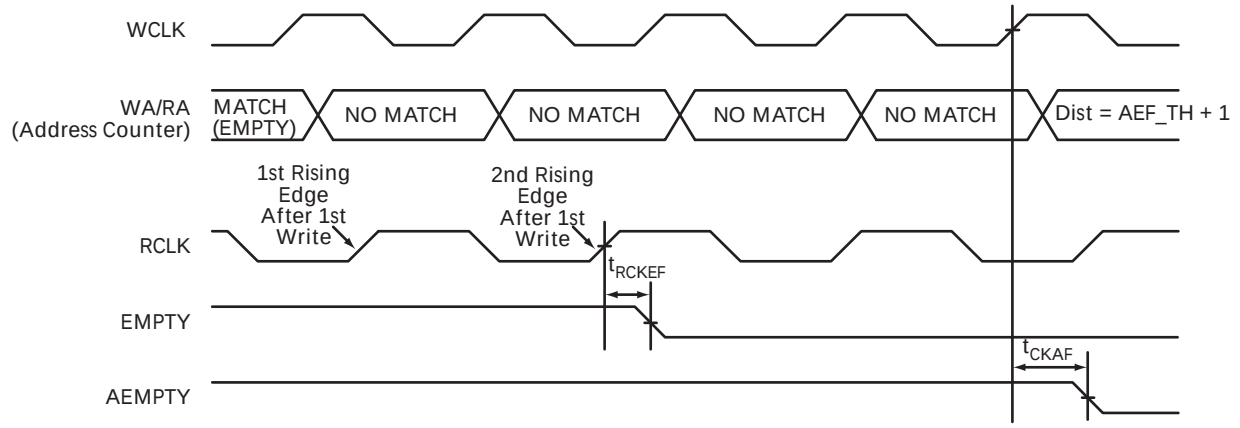


Figure 2-35 • **FIFO EMPTY Flag and AEMPTY Flag Deassertion**

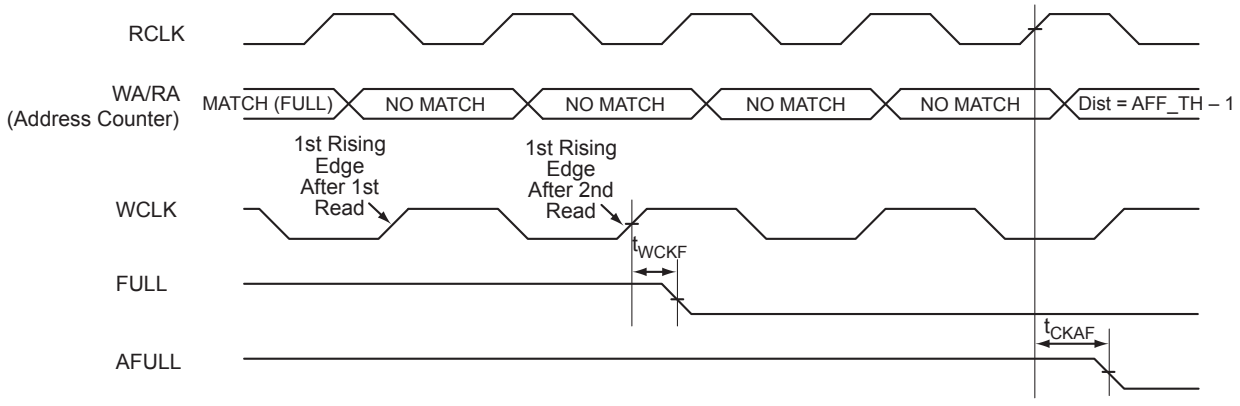


Figure 2-36 • **FIFO FULL Flag and AFULL Flag Deassertion**

JTAG Pins

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the part must be supplied to allow JTAG signals to transition the device. Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND.

TCK Test Clock

Test clock input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/-down resistor. If JTAG is not used, Microsemi recommends tying off TCK to GND through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.

Note that to operate at all VJTAG voltages, 500 Ω to 1 kΩ will satisfy the requirements. Refer to Table 3-2 for more information.

***Table 3-2* • Recommended Tie-Off Values for the TCK and TRST Pins**

VJTAG	Tie-Off Resistance
VJTAG at 3.3 V	200 Ω to 1 kΩ
VJTAG at 2.5 V	200 Ω to 1 kΩ
VJTAG at 1.8 V	500 Ω to 1 kΩ
VJTAG at 1.5 V	500 Ω to 1 kΩ

Notes:

1. *Equivalent parallel resistance if more than one device is on the JTAG chain*
2. *The TCK pin can be pulled up/down.*
3. *The TRST pin is pulled down.*

TDI Test Data Input

Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.

TDO Test Data Output

Serial output for JTAG boundary scan, ISP, and UJTAG usage.

TMS Test Mode Select

The TMS pin controls the use of the IEEE 1532 boundary scan pins (TCK, TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin.

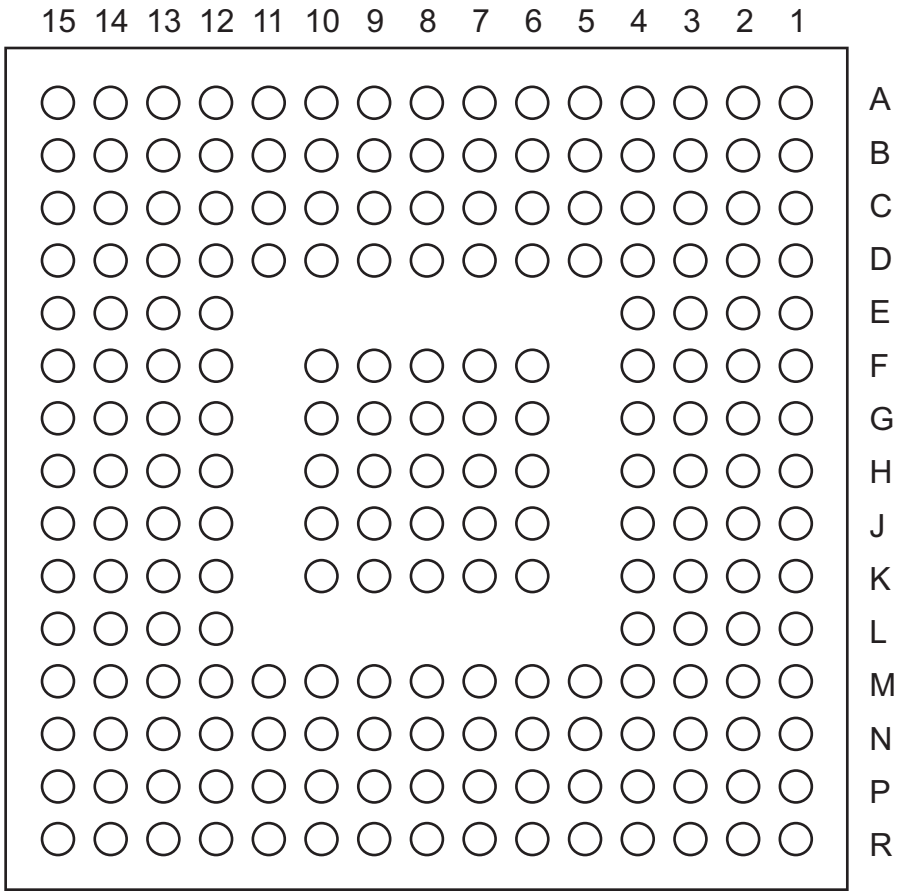
TRST Boundary Scan Reset Pin

The TRST pin functions as an active-low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor could be included to ensure the test access port (TAP) is held in reset mode. The resistor values must be chosen from Table 3-2 and must satisfy the parallel resistance value requirement. The values in Table 3-2 correspond to the resistor recommended when a single device is used, and the equivalent parallel resistor when multiple devices are connected via a JTAG chain.

In critical applications, an upset in the JTAG circuit could allow entrance to an undesired JTAG state. In such cases, Microsemi recommends tying off TRST to GND through a resistor placed close to the FPGA pin.

Note that to operate at all VJTAG voltages, 500 Ω to 1 kΩ will satisfy the requirements.

CS201



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

CS289	
Pin Number	AGLP060 Function
A1	GAB1/IO03RSB0
A2	NC
A3	NC
A4	GND
A5	IO10RSB0
A6	IO14RSB0
A7	IO16RSB0
A8	IO18RSB0
A9	GND
A10	IO23RSB0
A11	IO27RSB0
A12	NC
A13	NC
A14	GND
A15	NC
A16	NC
A17	GBC0/IO30RSB0
B1	GAA1/IO01RSB0
B2	GND
B3	NC
B4	NC
B5	IO07RSB0
B6	NC
B7	VCCIB0
B8	IO17RSB0
B9	IO19RSB0
B10	IO24RSB0
B11	IO28RSB0
B12	VCCIB0
B13	NC
B14	NC
B15	NC
B16	GBC1/IO31RSB0
B17	GND
C1	IO155RSB3
C2	GAA0/IO00RSB0
C3	GAC0/IO04RSB0
C4	NC

CS289	
Pin Number	AGLP060 Function
C5	VCCIB0
C6	IO09RSB0
C7	IO13RSB0
C8	IO15RSB0
C9	IO21RSB0
C10	GND
C11	IO29RSB0
C12	NC
C13	NC
C14	NC
C15	GND
C16	GBA0/IO34RSB0
C17	IO39RSB1
D1	IO150RSB3
D2	IO151RSB3
D3	GND
D4	GAB0/IO02RSB0
D5	NC
D6	NC
D7	NC
D8	GND
D9	IO20RSB0
D10	IO25RSB0
D11	NC
D12	NC
D13	GND
D14	GBB0/IO32RSB0
D15	GBA1/IO35RSB0
D16	IO37RSB1
D17	IO42RSB1
E1	VCCIB3
E2	IO147RSB3
E3	GAC2/IO152RSB3
E4	GAA2/IO156RSB3
E5	GAC1/IO05RSB0
E6	NC
E7	IO06RSB0
E8	IO11RSB0

CS289	
Pin Number	AGLP060 Function
E9	IO22RSB0
E10	IO26RSB0
E11	VCCIB0
E12	NC
E13	GBB1/IO33RSB0
E14	GBA2/IO36RSB1
E15	GBB2/IO38RSB1
E16	VCCIB1
E17	IO44RSB1
F1	GFC1/IO140RSB3
F2	IO142RSB3
F3	IO149RSB3
F4	VCCIB3
F5	GAB2/IO154RSB3
F6	IO153RSB3
F7	NC
F8	IO08RSB0
F9	IO12RSB0
F10	NC
F11	NC
F12	NC
F13	GBC2/IO40RSB1
F14	GND
F15	IO43RSB1
F16	IO46RSB1
F17	IO45RSB1
G1	GFC0/IO139RSB3
G2	GND
G3	IO144RSB3
G4	IO145RSB3
G5	IO146RSB3
G6	IO148RSB3
G7	GND
G8	GND
G9	VCC
G10	GND
G11	GND
G12	IO48RSB1

CS289	
Pin Number	AGLP125 Function
G13	IO64RSB1
G14	IO69RSB1
G15	IO78RSB1
G16	IO76RSB1
G17	GND
H1	VCOMPLF
H2	GFB0/IO191RSB3
H3	IO195RSB3
H4	IO197RSB3
H5	IO199RSB3
H6	GFB1/IO192RSB3
H7	GND
H8	GND
H9	GND
H10	GND
H11	GND
H12	GCC1/IO79RSB1
H13	IO74RSB1
H14	GCA0/IO84RSB1
H15	VCCIB1
H16	GCA2/IO85RSB1
H17	GCC0/IO80RSB1
J1	VCCPLF
J2	GFA1/IO190RSB3
J3	VCCIB3
J4	IO185RSB3
J5	IO183RSB3
J6	IO181RSB3
J7	VCC
J8	GND
J9	GND
J10	GND
J11	VCC
J12	GCB2/IO86RSB1
J13	GCB1/IO81RSB1
J14	IO90RSB1
J15	IO89RSB1
J16	GCB0/IO82RSB1

CS289	
Pin Number	AGLP125 Function
J17	GCA1/IO83RSB1
K1	GND
K2	GFA0/IO189RSB3
K3	GFB2/IO187RSB3
K4	IO179RSB3
K5	IO175RSB3
K6	IO177RSB3
K7	GND
K8	GND
K9	GND
K10	GND
K11	GND
K12	IO88RSB1
K13	IO94RSB1
K14	IO95RSB1
K15	IO93RSB1
K16	GND
K17	GCC2/IO87RSB1
L1	GFA2/IO188RSB3
L2	GFC2/IO186RSB3
L3	IO182RSB3
L4	GND
L5	IO173RSB3
L6	GEC1/IO170RSB3
L7	GND
L8	GND
L9	VCC
L10	GND
L11	GND
L12	GDC1/IO99RSB1
L13	GDB1/IO101RSB1
L14	VCCIB1
L15	IO98RSB1
L16	IO92RSB1
L17	IO91RSB1
M1	IO184RSB3
M2	VCCIB3
M3	IO176RSB3

CS289	
Pin Number	AGLP125 Function
M4	IO172RSB3
M5	GEB0/IO167RSB3
M6	GEB1/IO168RSB3
M7	IO159RSB2
M8	IO161RSB2
M9	IO135RSB2
M10	IO128RSB2
M11	IO121RSB2
M12	IO113RSB2
M13	GDA1/IO103RSB1
M14	GDA0/IO104RSB1
M15	IO97RSB1
M16	IO96RSB1
M17	VCCIB1
N1	IO180RSB3
N2	IO178RSB3
N3	GEC0/IO169RSB3
N4	GEA0/IO165RSB3
N5	GND
N6	IO156RSB2
N7	IO148RSB2
N8	IO144RSB2
N9	IO137RSB2
N10	VCCIB2
N11	IO119RSB2
N12	IO111RSB2
N13	GDB2/IO106RSB2
N14	IO109RSB2
N15	GND
N16	GDB0/IO102RSB1
N17	GDC0/IO100RSB1
P1	IO174RSB3
P2	IO171RSB3
P3	GND
P4	IO160RSB2
P5	IO157RSB2
P6	IO154RSB2
P7	IO152RSB2

Revision	Changes	Page
Revision 13 (June 2012)	Figure 2-30 • FIFO Read and Figure 2-31 • FIFO Write have been added (SAR 34843).	2-73
	Updated the terminology used in Timing Characteristics in the following tables: Table 2-96 • FIFO and Table 2-97 • FIFO (SAR 38236).	2-76
	The following sentence was removed from the "VMVx I/O Supply Voltage (quiet)" section in the "Pin Descriptions and Packaging" section: "Within the package, the VMV plane is decoupled from the simultaneous switching noise originating from the output buffer VCCI domain" and replaced with “Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks” (SAR 38320). The datasheet mentions that "VMV pins must be connected to the corresponding VCCI pins" for an ESD enhancement.	3-1
Revision 12 (March 2012)	The "In-System Programming (ISP) and Security" section and "Security" section were revised to clarify that although no existing security measures can give an absolute guarantee, Microsemi FPGAs implement the best security available in the industry (SAR 34664).	I, 1-2
	The Y security option and Licensed DPA Logo were added to the "IGLOO PLUS Ordering Information" section. The trademarked Licensed DPA Logo identifies that a product is covered by a DPA counter-measures license from Cryptography Research (SAR 34724).	III
	The "Specifying I/O States During Programming" section is new (SAR 34695).	1-7
	The following sentence was removed from the "Advanced Architecture" section: "In addition, extensive on-chip programming circuitry allows for rapid, single-voltage (3.3 V) programming of IGLOO PLUS devices via an IEEE 1532 JTAG interface" (SAR 34684).	1-3

Revision	Changes	Page
Revision 12 (continued)	The reference to guidelines for global spines and VersaTile rows, given in the "Global Clock Contribution—P_{CLOCK}" section, was corrected to the "Spine Architecture" section of the Global Resources chapter in the *IGLOO PLUS FPGA Fabric User's Guide* (SAR 34733).	2-12
	t_{DOUT} was corrected to t_{DIN} in Figure 2-4 • Input Buffer Timing Model and Delays (example) (SAR 37107).	2-16
	The AC Loading figures in the "Single-Ended I/O Characteristics" section were updated to match tables in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section (SAR 34887).	2-27
	Minimum pulse width High and Low values were added to the tables in the "Global Tree Timing Characteristics" section. The maximum frequency for global clock parameter was removed from these tables because a frequency on the global is only an indication of what the global network can do. There are other limiters such as the SRAM, I/Os, and PLL. SmartTime software should be used to determine the design frequency (SAR 36963).	2-58
	Table 2-90 • IGLOO PLUS CCC/PLL Specification and Table 2-91 • IGLOO PLUS CCC/PLL Specification were updated. A note was added to both tables indicating that when the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available (SAR 34820). The value for serial clock was missing from these tables and has been restored. The value and units for input cycle-to-cycle jitter were incorrect and have been restored. The note to Table 2-90 • IGLOO PLUS CCC/PLL Specification giving specifications for which measurements done was corrected from VCC/VCCPLL = 1.14 V to VCC/VCCPLL = 1.425 V. The Delay Range in Block: Programmable Delay 2 value in Table 2-91 • IGLOO PLUS CCC/PLL Specification was corrected from 0.025 to 0.863 (SAR 37058).	2-61, 2-62
	Figure 2-28 • Write Access after Read onto Same Address was deleted. Reference was made to a new application note, *Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs*, which covers these cases in detail (SAR 34868). The port names in the SRAM "Timing Waveforms", SRAM "Timing Characteristics" tables, Figure 2-32 • FIFO Reset, and the FIFO "Timing Characteristics" tables were revised to ensure consistency with the software names (SAR 35748).	2-65, 2-68, 2-74, 2-76
	The "Pin Descriptions and Packaging" chapter has been added (SAR 34769).	3-1
	Package names used in the "Package Pin Assignments" section were revised to match standards given in *Package Mechanical Drawings* (SAR 34769).	4-1
Revision 11 (July 2010)	The versioning system for datasheets has been changed. Datasheets are assigned a revision number that increments each time the datasheet is revised. The "IGLOO PLUS Device Status" table indicates the status for each device in the family.	N/A
	The "Reprogrammable Flash Technology" section was revised to add "250 MHz (1.5 V systems) and 160 MHz (1.2 V systems) System Performance."	I
	The "I/Os with Advanced I/O Standards" section was revised to add definitions for hot-swap and cold-sparing.	1-6
	Conditional statements regarding hot insertion were removed from the description of VI in Table 2-1 • Absolute Maximum Ratings, since all IGLOO PLUS devices are hot insertion enabled.	2-1

Revision	Changes	Page
Revision 11 (continued)	The tables in the "Single-Ended I/O Characteristics" section were updated. Notes clarifying IIL and IIH were added. Tables for 3.3 V LVCMOS and 1.2 V LVCMOS wide range were added (SAR 79370, SAR 79353, and SAR 79366). Notes in the wide range tables state that the minimum drive strength for any LVCMOS 3.3 V (or LVCMOS 1.2 V) software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models (SAR 25700).	2-27
	The following sentence was deleted from the "2.5 V LVCMOS" section: It uses a 5 V–tolerant input buffer and push-pull output buffer (SAR 24916).	2-32
	The tables in the "Input Register" section, "Output Register" section, and "Output Enable Register" section were updated. The tables in the "VersaTile Characteristics" section were updated.	2-45 through 2-56
	The following tables were updated in the "Global Tree Timing Characteristics" section: Table 2-85 • AGLP060 Global Resource (1.5 V) Table 2-86 • AGLP125 Global Resource (1.5 V) Table 2-88 • AGLP060 Global Resource (1.2 V)	2-58
	Table 2-90 • IGLOO PLUS CCC/PLL Specification and Table 2-91 • IGLOO PLUS CCC/PLL Specification were revised (SAR 79388). VCO output jitter and maximum peak-to-peak jitter data were changed. Three notes were added to the table in connection with these changes.	2-61
	Figure 2-28 • Write Access after Write onto Same Address and Figure 2-29 • Write Access after Read onto Same Address were deleted.	N/A
	The tables in the "SRAM", "FIFO" and "Embedded FlashROM Characteristics" sections were updated.	2-68, 2-78

Revision	Changes	Page
Revision 10 (Apr 2009) Product Brief v1.5 DC and Switching Characteristics Advance v0.5	The –F speed grade is no longer offered for IGLOO PLUS devices. References to it have been removed from the document. The speed grade column and note regarding –F speed grade were removed from "IGLOO PLUS Ordering Information". The "Speed Grade and Temperature Grade Matrix" section was removed.	III, IV
Revision 9 (Feb 2009) Product Brief v1.4	The "Advanced I/O" section was revised to add two bullets regarding support of wide range power supply voltage.	I
	The "I/Os with Advanced I/O Standards" section was revised to add 3.0 V wide range to the list of supported voltages. The "Wide Range I/O Support" section is new.	1-7
Revision 8 (Jan 2009) Packaging v1.5	The "CS201" pin table was revised to add a note regarding pins G1 and H1.	4-8
Revision 7 (Dec 2008) Product Brief v1.3	A note was added to IGLOO PLUS Devices: "AGLP060 in CS201 does not support the PLL."	I
	Table 2 • IGLOO PLUS FPGAs Package Size Dimensions was updated to change the nominal size of VQ176 from 100 to 400 mm^2.	II
Revision 6 (Oct 2008) DC and Switching Characteristics Advance v0.4	Data was revised significantly in the following tables: Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings, STD Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V Table 2-26 • Summary of I/O Timing Characteristics—Software Default Settings, STD Speed Grade Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V Table 2-50 • 2.5 LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage Table 2-51 • 2.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage	2-22, 2-33
Revision 5 (Aug 2008) Product Brief v1.2	The VQ128 and VQ176 packages were added to Table 1 • IGLOO PLUS Product Family, the "I/Os Per Package [1]" table, Table 2 • IGLOO PLUS FPGAs Package Size Dimensions, "IGLOO PLUS Ordering Information", and the "Temperature Grade Offerings" table.	I to IV
Packaging v1.4	The "VQ128" package drawing and pin table are new.	4-2
	The "VQ176" package drawing and pin table are new.	4-5
Revision 4 (Jul 2008) Product Brief v1.1 DC and Switching Characteristics Advance v0.3	As a result of the Libero IDE v8.4 release, Actel now offers a wide range of core voltage support. The document was updated to change 1.2 V / 1.5 V to 1.2 V to 1.5 V.	N/A
Revision 3 (Jun 2008) DC and Switching Characteristics Advance v0.2	Tables have been updated to reflect default values in the software. The default I/O capacitance is 5 pF. Tables have been updated to include the LVCMOS 1.2 V I/O set.	N/A
	Table note 3 was updated in Table 2-2 • Recommended Operating Conditions[1,2] to add the sentence, "VCCI should be at the same voltage within a given I/O bank." References to table notes 5, 6, 7, and 8 were added. Reference to table note 3 was removed from VPUMP Operation and placed next to VCC.	2-2
	Table 2-4 • Overshoot and Undershoot Limits [1] was revised to remove "as measured on quiet I/Os" from the title. Table note 2 was revised to remove "estimated SSO density over cycles." Table note 3 was deleted.	2-3

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in the "IGLOO PLUS Device" table on page II, is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Production

This version contains information that is considered to be final.

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