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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

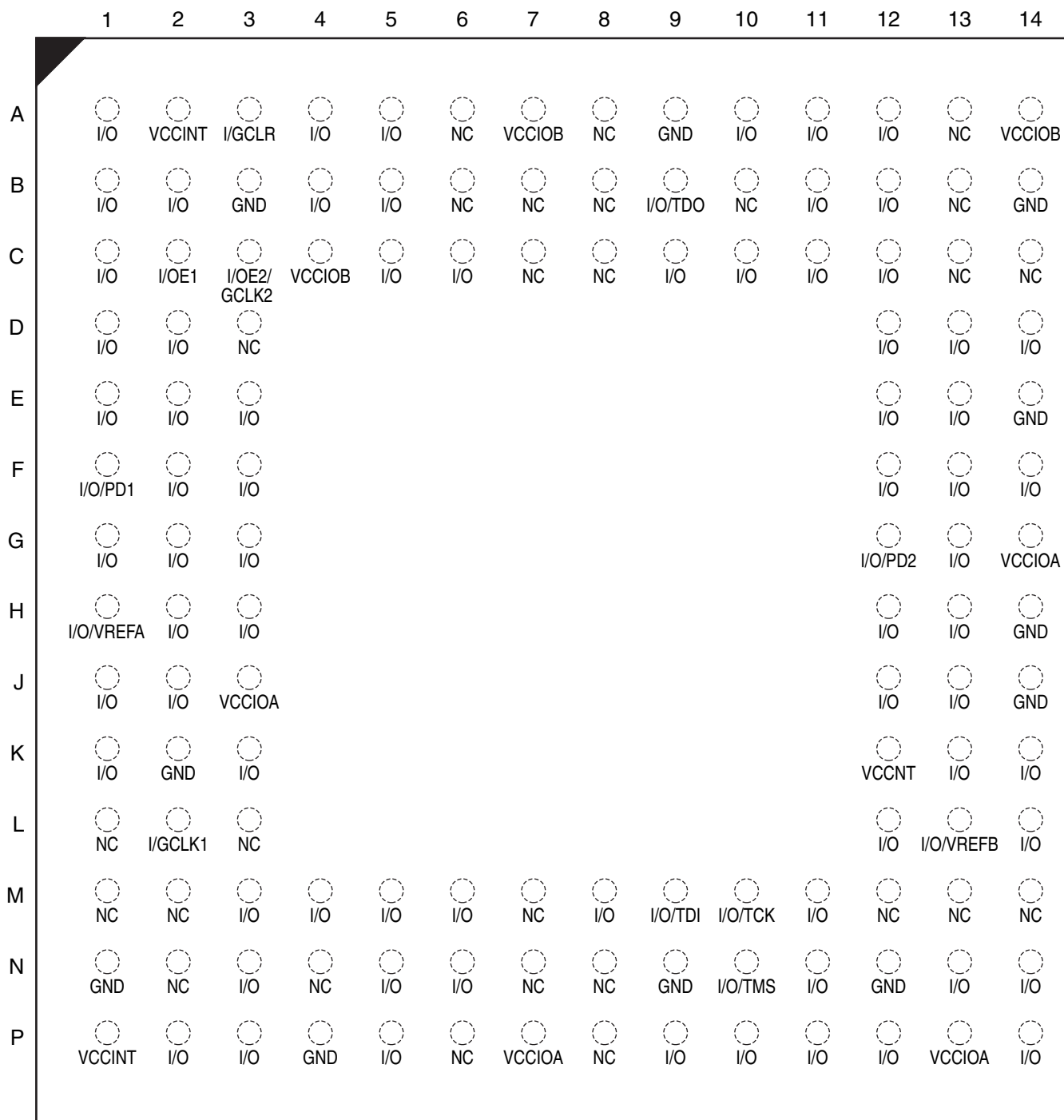
Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable (min 10K program/erase cycles)
Delay Time tpd(1) Max	5 ns
Voltage Supply - Internal	1.7V ~ 1.9V
Number of Logic Elements/Blocks	-
Number of Macrocells	128
Number of Gates	-
Number of I/O	80
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atf1508be-5ax100

Figure 1-2. 132-CBGA Top View



Note: 1. The 132-ball CBGA package is 8 x 8 x 1.2 mm in size with 0.5 mm ball spacing.

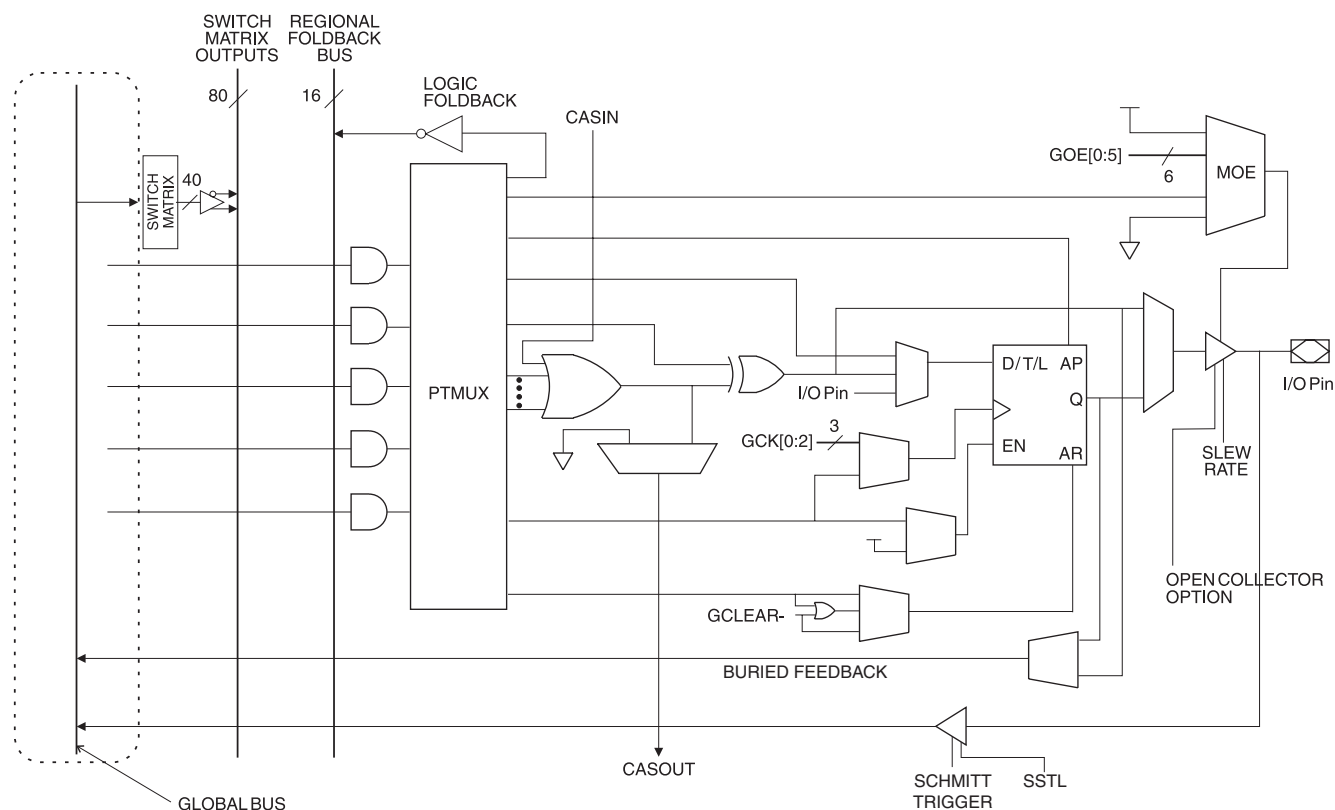
Each of the 128 macrocells generates a buried feedback signal that goes to the global bus (see [Figure 1-3](#)). Each input and I/O pin also feeds into the global bus. The switch matrix in each logic block then selects 40 individual signals from the global bus. Each macrocell also generates a foldback logic term that goes to a regional bus. Cascade logic between macrocells in the ATF1508BE allows fast, efficient generation of complex logic functions. The ATF1508BE contains eight such logic chains, each capable of creating sum term logic with a fan-in of up to 40 product terms.

The ATF1508BE macrocell, shown in [Figure 1-4](#), is highly flexible and capable of supporting complex logic functions operating at high speed. The macrocell consists of five sections: product terms and product term select multiplexer, OR/XOR/CASCADE logic, a flip-flop, output select and enable, and logic array inputs.

A security fuse, when programmed, protects the contents of the ATF1508BE. Two bytes (16 bits) of User Electronic Signature are accessible to the user for purposes such as storing project name, part number, revision or date. The User Electronic Signature is accessible regardless of the state of the security fuse.

The ATF1508BE device supports In-System Programming (ISP) via the industry-standard 4-pin JTAG interface (IEEE 1532 standard), and is fully compliant with IEEE 1149.1 for Boundary Scan Test. ISP allows the device to be programmed without removing it from the printed circuit board. In addition to simplifying the manufacturing flow, ISP also allows design modifications to be made in the field via software.

Figure 1-4. ATF1508BE Macrocell



1.6 Global Bus/Switch Matrix

The global bus contains all input and I/O pin signals as well as the buried feedback signal from all 128 macrocells. The switch matrix in each logic block receives as its inputs all signals from the global bus. Under software control, up to 40 of these signals can be selected as inputs to the logic block.

1.7 Foldback Bus

Each macrocell also generates a foldback product term. This signal goes to the regional bus and is available to all 16 macrocells within the logic block. The foldback is an inverse polarity of one of the macrocell's product terms. The 16 foldback terms in each logic block allow generation of high fan-in sum terms or other complex logic functions with little additional delay.

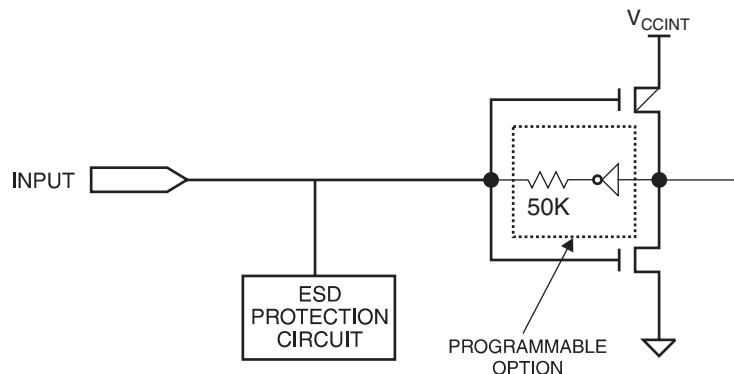
2. Input and I/O Pins

2.1 Programmable Pin-keeper Option for Inputs and I/Os

The ATF1508BE offers the option of individually programming each of its input or I/O pin so that pin-keeper circuit can be utilized. When any pin is driven high or low and then subsequently left floating, it will stay at that previous high or low level. This circuitry prevents undriven input and I/O lines from floating to intermediate voltage levels, which causes unnecessary power consumption and system noise. The keeper circuits eliminate the need for external pull-up resistors and eliminate their DC power consumption.

Figure 2-1 shows the pin-keeper circuit for an Input Pin and Figure 2-2 shows the same for an I/O pin. The pin-keeper circuit is a weak feedback latch and has an effective resistance that is approximately 50 k Ω .

Figure 2-1. Input with Programmable Pin-keeper



3. Power Management

Unlike conventional CPLDs with sense amplifiers, the ATF1508BE is designed using low-power full CMOS design techniques. This enables the ATF1508BE to achieve extremely low power consumption over the full operating frequency spectrum.

The ATF1508BE also has an optional power-down mode. In this mode, current drops to below 100 μ A. When the power-down option is selected, either PD1 or PD2 pins (or both) can be used to power down the part. When enabled, the device goes into power-down when either PD1 or PD2 is high. In the power-down mode, all internal logic signals are latched and held, as are any enabled outputs.

All pin transitions are ignored until the PD pin is brought low. When the power-down feature is enabled, the PD1 or PD2 pin cannot be used as a logic input or output. However, the pin's macrocell may still be used to generate buried foldback and cascade logic signals.

All power-down AC characteristic parameters are computed from external input or I/O pins.

4. Security Feature

A fuse is provided to prevent unauthorized copying of the ATF1508BE fuse patterns. Once enabled, fuse reading or verification is inhibited. However, the 16-bit User Electronic Signature remains accessible. To reset this feature, the entire memory array in the device must be erased.

5. Programming Methods

The ATF1508BE devices are In-System Programmable (ISP) or In-System Configurable (ISC) devices utilizing the 4-pin JTAG protocol. This capability eliminates package handling normally required for programming and facilitates rapid design iterations and field changes.

When using the ISP hardware or software to program the ATF1508BE devices, four I/O pins must be reserved for the JTAG interface. However, the logic features that the macrocells have associated with these I/O pins are still available to the design for buried logic functions.

To facilitate ISP programming by the Automated Test Equipment (ATE) vendors, Serial Vector Format (SVF) files can be created by Atmel-provided software utilities. ATF1508BE devices can also be programmed using standard third-party programmers. With a third-party programmer, the JTAG ISP port can be disabled, thereby allowing four additional I/O pins to be used for logic.

The ATF1508BE device supports several configuration modes which gives designers several unique options for programming.

The different modes of programming are:

- ISC – In-System Configuration
- OTF – On-the-Fly Reconfiguration
- DRA – Direct Reconfiguration Access

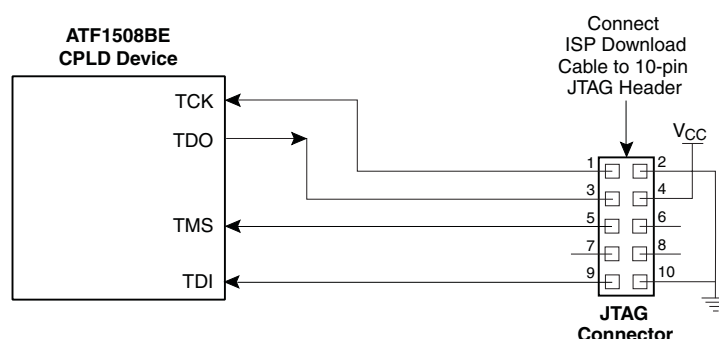
5.1 In-System Configuration – ISC (Also Referred to as ISP)

This mode is the de-facto standard used to program the CPLD when it is attached to a PCB. The term ISC can also be used interchangeably with ISP (In-system Programming). ISC or ISP eliminates the need for an external device programmer, and the devices can be soldered to a PCB without being preprogrammed.

In the ISC mode, the logic operation of the ATF1508BE is halted and the embedded configuration memory is programmed. The device is programmed by first erasing the configuration memory in the CPLD and then loading the new configuration data into the memory, which in-turn configures the PLD for functional mode. When the device is in the ISC programming mode, all user I/Os are held in the high impedance state.

The ISC mode is best suited for working with the ATF1508BE device in a design development or production environment. Configuration of the ATF1508BE device done via a Download Cable (see [Figure 5-1 on page 11](#)) is the default mode used to program the device in the ISC mode. In this mode, the PC is typically the controlling device that communicates with the CPLD.

Figure 5-1. Configuration of ATF1508BE Device Using a Download Cable



5.2 On-the-Fly Reconfiguration – OTF

In this mode, the CPLD design pattern stored in the internal configuration memory can be modified while the previously-programmed design pattern is operating with minimal disturbance to the programming operation of the new design. The new configuration will take affect after the OTF programming process is completed and the OTF mode is exited.

The configuration data for any design is stored in the internal configuration memory. Once the configuration data is transferred to the internal static registers of the CPLD, the CPLD operates with the design pattern and the configuration memory is free to be re-loaded with a new set of configuration data. The design pattern due to the new configuration content is activated through an initialization cycle that occurs on exiting the OTF mode or after the next power up sequence.

[Figure 5-2](#) shows the electrical interface for configuration of the ATF1508BE device in the OTF mode. The processor is the controlling device that communicates with the CPLD and uses configuration data stored in the external memory to configure the CPLD.

6. JTAG-BST/ISP Overview

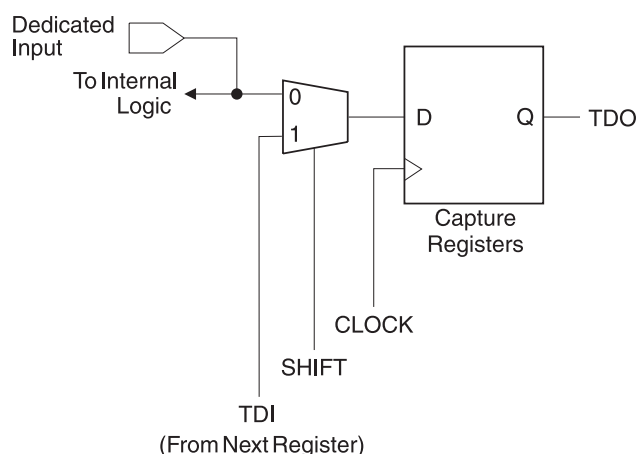
The JTAG boundary-scan testing is controlled by the Test Access Port (TAP) controller in the ATF1508BE. The boundary-scan technique involves the inclusion of a shift-register stage (contained in a boundary-scan cell) adjacent to each component so that signals at component boundaries can be controlled and observed using scan testing methods. Each input pin and I/O pin has its own boundary-scan cell (BSC) to support boundary-scan testing. The TAP controller is automatically reset at power-up. The five JTAG modes supported include: SAMPLE/PRE-LOAD, EXTEST, BYPASS, IDCODE and HIGHZ. The ATF1508BE's BSC can be fully described using a BSDL file as described in IEEE 1149.1 standard. This allows ATF1508BE testing to be described and implemented using any one of the third-party development tools supporting this standard.

The ATF1508BE also has the option of using the four JTAG-standard I/O pins for ISP. The ATF1508BE is programmable through the four JTAG pins using the IEEE standard JTAG programming protocol established by IEEE 1532 standard using 1.8V/2.5V/3.3V LVCMOS level programming signals from the ISP interface for in-system programming. The JTAG feature is a programmable option. If JTAG (BST or ISP) is not needed, then the four JTAG control pins are available as I/O pins.

6.1 JTAG Boundary-scan Cell (BSC) Testing

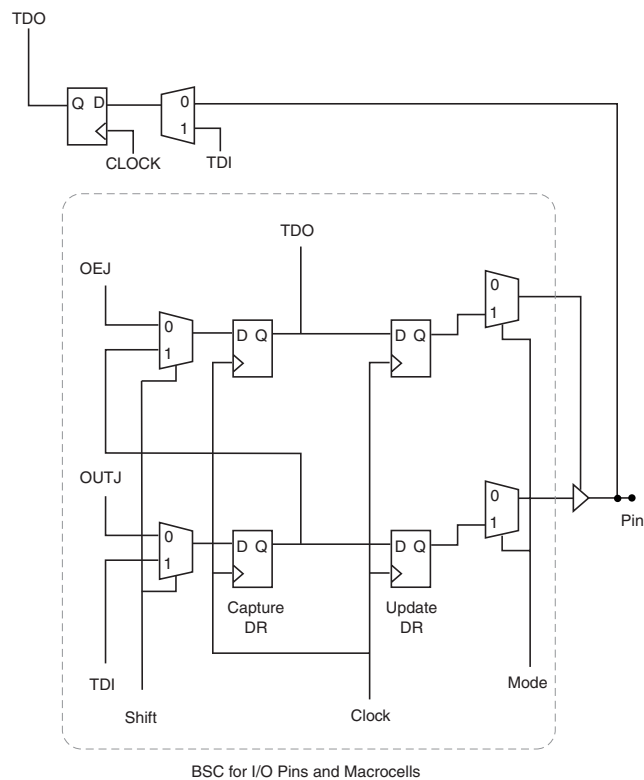
The ATF1508BE contains 80 I/O pins and four dedicated input pins. Each input pin and I/O pin has its own boundary-scan cell (BSC) in order to support boundary-scan testing as described in detail by IEEE 1532 standard. A typical BSC consists of three capture registers or scan registers and up to two update registers. There are two types of BSCs, one for input or I/O pin, and one for the macrocells. The BSCs in the device are chained together through the capture registers. Input to the capture register chain is fed in from the TDI pin while the output is directed to the TDO pin. Capture registers are used to capture active device data signals, to shift data in and out of the device and to load data into the update registers. Control signals are generated internally by the JTAG TAP controller. The BSC configuration for the input and I/O pins and macrocells is shown below.

Figure 6-1. BSC Configuration for Input and I/O Pins (Except JTAG TAP Pins)



Note: The ATF1508BE has a pull-up option on TMS and TDI pins. This feature is selected as a design option.

Figure 6-2. BSC Configuration for Macrocell



7. Design Software Support

ATF1508BE designs are supported by several third-party tools. Automated fitters allow logic synthesis using a variety of high-level description languages such as VHDL® and Verilog®. Third party synthesis and simulation tools from Mentor Graphics® are integrated into Atmel's software tools.

8. Electrical Specifications

Table 8-1. Absolute Maximum Ratings*

Operating Temperature	–40° C to +85° C
Storage Temperature	–65° C to +150° C
Supply Voltage (V_{CCINT})	–0.5V to +2.5V
Supply Voltage for Output Drivers (V_{CCIO})	–0.5V to +4.5V
Junction Temperature	–55° C to +155° C

***NOTICE:** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 8-2. Operating Temperature Range

	Commercial	Industrial
Operating Temperature (Ambient)	0° C - 70° C	–40° C - 85° C

Table 8-3. Pin Capacitance⁽¹⁾

	Typ	Max	Units	Conditions
C_{IN}	8	10	pF	$V_{IN} = 0V$; $f = 1.0$ MHz
$C_{I/O}$	8	10	pF	$V_{OUT} = 0V$; $f = 1.0$ MHz

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Table 8-4. DC Characteristics (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Units
LVCMOS 1.8V						
V _{IL}	Input Low-voltage		-0.3		0.35 x V _{CCIO}	V
V _{IH}	Input High-voltage		1.2		3.9	V
V _{OL}	Output Low-voltage	HD: I _{OL} = 2 mA, V _{CCIO} = 1.7V			0.45	V
		LD: I _{OL} = 1 mA, V _{CCIO} = 1.7V			0.2	V
V _{OH}	Output High-voltage	HD: I _{OH} = -2 mA, V _{CCIO} = 1.7V	V _{CCIO} - 0.45V			V
		LD: I _{OH} = -1 mA, V _{CCIO} = 1.7V	V _{CCIO} - 0.45V			V
LVCMOS 1.5V						
V _{IL}	Input Low-voltage		-0.3		0.35 x V _{CCIO}	V
V _{IH}	Input High-voltage		1.2		3.9	V
V _{OL}	Output Low-voltage	HD: I _{OL} = 2 mA, V _{CCIO} = 1.4V			0.45	V
		LD: I _{OL} = 1 mA, V _{CCIO} = 1.4V			0.2	V
V _{OH}	Output High-voltage	HD: I _{OH} = -2 mA, V _{CCIO} = 1.4V	V _{CCIO} - 0.45V			V
		LD: I _{OH} = -1 mA, V _{CCIO} = 1.4V	V _{CCIO} - 0.45V			V

Note: 1. 16-bit up/down counter used in each LAB.

Table 8-5. Schmitt Trigger Input Threshold Voltage

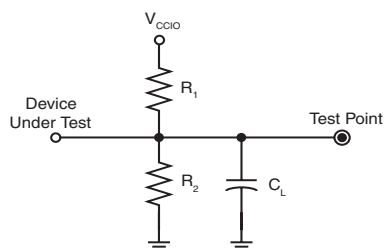
V_{CCINT}	V_{THL}		V_{TLH}	
	Min	Max	Min	Max
1.70	0.68	0.73	1.05	1.08
1.95	0.81	0.88	1.18	1.22

Table 8-6. SSTL2-1 DC Voltage Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CCIO}	Input Source Voltage		2.3	2.5	2.7	V
$V_{REF}^{(1)}$	Input Reference Voltage		1.15	1.25	1.35	V
$V_{TT}^{(2)}$	Termination Voltage		$V_{REF} - 0.05$	1.25	$V_{REF} + 0.04$	V
V_{IH}	Input High Voltage		$V_{REF} + 0.45$		3.9	V
V_{IL}	Input Low Voltage		-0.3		$V_{REF} - 0.6$	V
V_{OH}	Output High Voltage	$I_{OH} = -8 \text{ mA}$, $V_{CCIO} = 2.3\text{V}$	$V_{CCIO} - 0.6$			V
V_{OL}	Output Low Voltage	$I_{OL} = 8 \text{ mA}$, $V_{CCIO} = 2.3\text{V}$			0.54	V
$V_{IH(DC)}$	Input High Voltage		$V_{REF} + 0.15$		$V_{CCIO} + 0.3$	V
$V_{IL(DC)}$	Input Low Voltage		-0.3		$V_{REF} - 0.15$	V

Notes: 1. Peak-to-peak noise on V_{REF} may not exceed $\pm 2\% V_{REF}$. V_{REF} should track the variations in V_{CCIO} .
2. V_{TT} of transmitting device must track V_{REF} of receiving devices.

10. Output AC Test Loads



	R1	R2	CL
LVTTL	350 Ohm	350 Ohm	35 pF
LVC MOS33	300 Ohm	300 Ohm	35 pF
LVC MOS25	200 Ohm	200 Ohm	35 pF
LVC MOS18	150 Ohm	150 Ohm	35 pF

Note: C_L includes test fixtures and probe capacitance.

11. AC Characteristics

Table 11-1. AC Characteristics ⁽¹⁾

Symbol	Parameter	-5		-7		Units
		Min	Max	Min	Max	
t_{PD1_INP}	Delay for Single Input to Non-registered Output		5.0		6	ns
t_{PD1}	Input or Feedback to Non-registered Output		7		7.5	ns
t_{PD2}	Input or Feedback to Non-registered Feedback		4.2		4.7	ns
t_{SU}	Global Clock Setup Time	2.2		2.8		ns
t_H	Global Clock Hold Time	0		0		ns
t_{FSU}	Global Clock Setup Time of Fast Input	1		2		ns
t_{FH}	Global Clock Hold Time of Fast Input	0.5		0.75		ns
t_{COP}	Global Clock to Output Delay		6		6.9	ns
t_{CH}	Global Clock High Time	1.25		2		ns
t_{CL}	Global Clock Low Time	1.25		2		ns
t_{ASU}	Array Clock Setup Time	1.7		2.2		ns
t_{AH}	Array Clock Hold Time	0.50		0.60		ns
t_{ACOP}	Array Clock to Output Delay		6.5		7.5	ns
t_{ACH}	Array Clock High Time	1.75		2.5		ns
t_{ACL}	Array Clock Low Time	1.75		2.5		ns
t_{CNT}	Minimum Global Clock Period		3		4.75	ns
f_{CNT}	Maximum Internal Global Clock Frequency	333		210		MHz
t_{ACNT}	Minimum Array Clock Period		4		5.5	ns
f_{ACNT}	Maximum Internal Array Clock Frequency	250		181		MHz
$f_{MAX_EXT_SYNC}$	Maximum External Frequency $V_{CCIO} = 3.3V$		122		103	MHz
$f_{MAX_EXT_ASYN}$	Maximum External Frequency $V_{CCIO} = 3.3V$		122		103	MHz
t_{IN}	Input Pad and Buffer Delay	0.7			0.9	ns
t_{IO}	I/O Input Pad and Buffer Delay	0.7			0.9	ns
t_{FIN}	Fast Input Delay		1		1	ns
t_{SEXP}	Foldback Term Delay		2		3	ns
t_{PEXP}	Cascade Logic Delay		0.5		1.0	ns
t_{LAD}	Logic Array Delay		1.8		1.8	ns
t_{LAC}	Logic Control Delay		1.5		2	ns
t_{IOE}	Internal Output Enable Delay		2		2	ns
t_{OD1}	Output Buffer Delay (HD) (High Drive; $C_L = 35$ pF)		4.5 4.0 3.5 2.8		4.5 4.0 3.5 2.8	ns

12. Power-down Mode

The ATF1508BE includes an optional pin-controlled power-down feature. When this mode is enabled, the PD pin acts as the power-down pin. When the PD pin is high, the device supply current is reduced to less than 100 μ A. During power-down, all output data and internal logic states are latched and held. Therefore, all registered and combinatorial output data remain valid. Any outputs that were in a high-Z state at the onset will remain at high-Z. During power-down, all input signals except the power-down pin are blocked. Input and I/O hold latches remain active to ensure that pins do not float to indeterminate levels, further reducing system power. The power-down pin feature is enabled in the logic design file or through Atmel software. Designs using the power-down pin may not use the PD pin logic array input. However, all other PD pin macrocell resources may still be used, including the buried feedback and foldback product term array inputs.

Table 12-1. Power-down AC Characteristics⁽¹⁾⁽²⁾

Symbol	Parameter	-5/-7		Units
		Min	Max	
t_{IVDH}	Valid I, I/O before PD High	10		ns
t_{GVDH}	Valid OE ⁽²⁾ before PD High	10		ns
t_{CVDH}	Valid Clock ⁽²⁾ before PD High	10		ns
t_{DHIX}	I, I/O Don't Care after PD High		5	ns
t_{DHGX}	OE ⁽²⁾ Don't Care after PD High		5	ns
t_{DHCX}	Clock ⁽²⁾ Don't Care after PD High		5	ns
t_{DLIV}	PD Low to Valid I, I/O		2	μ s
t_{DLGV}	PD Low to Valid OE (Pin or Term)		2	μ s
t_{DLCV}	PD Low to Valid Clock (Pin or Term)		2	μ s
t_{DLOV}	PD Low to Valid Output		2	μ s

Notes: 1. For low-drive outputs, add t_{SSO} .
2. Pin or product term.

13. ATF1508BE Dedicated Pinouts

Table 13-1. ATF1508BE Dedicated Pinouts

Dedicated Pin	132-ball CBGA	100-lead TQFP
INPUT / OE2 / GCLK2	C3	90
INPUT / GCLR	A3	89
INPUT / OE1	C2	88
INPUT / GCLK1	L2	87
I/O / GCLK3	M8	85
I/O / PD (1,2)	F1, G12	1, 41
I/O / V _{REFA}	H1	12
I/O / V _{REFB}	L13	60
I/O / TDI (JTAG)	M9	4
I/O / TMS (JTAG)	N10	15
I/O / TCK (JTAG)	M10	62
I/O / TDO (JTAG)	B9	73
GND	A9, B14, B3, E14, H14, J14, K2, N1, N9, N12, P4	11, 26, 38, 43, 59, 74, 86, 95
V _{CCINT}	A2, K12, P1	39, 91
V _{CCIOA}	J3, P7, P13, G14	3, 18, 34
V _{CCIOB}	A7, A14, C4	51, 66, 82
N/C	L1, L3, M1, N4, C13, B10, D3, P6, P8, N2, N7, N8, M7, M2, M12, M13, M14, C7, C8, C14, B6, B7, B8, B13, A6, A8, A13	
# of Signal Pins	84	84
# User I/O Pins	80	80

OE (1, 2)	Global OE pins
GCLR	Global Clear pin
GCLK (1, 2, 3)	Global Clock pins
PD (1, 2)	Power-down pins
TDI, TMS, TCK, TDO	JTAG pins used for boundary-scan testing or in-system programming
GND	Ground pins
V _{CCINT}	V _{CC} pins for the device (+1.8V)
V _{CCIOA}	LAB A and B – V _{CC} supply pins for I/Os (1.5V, 1.8V, 2.5V, or 3.3V)
V _{CCIOB}	LAB C and D – V _{CC} supply pins for I/Os (1.5V, 1.8V, 2.5V, or 3.3V)
V _{REFA}	Reference voltage pin for SSTL inputs in bank A
V _{REFB}	Reference voltage pin for SSTL inputs in bank B

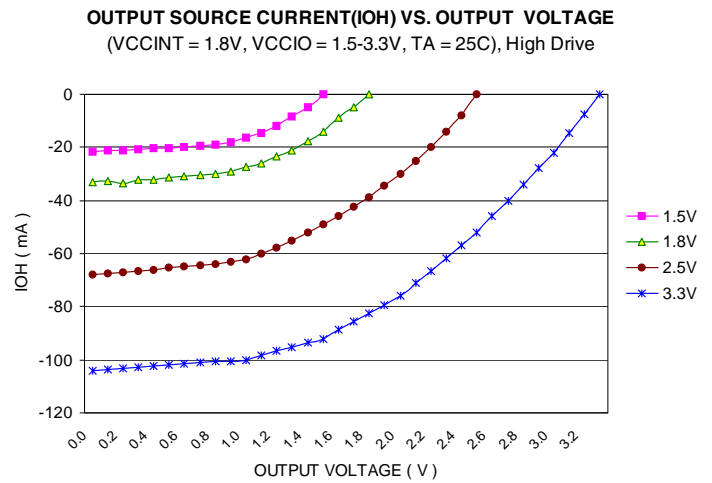
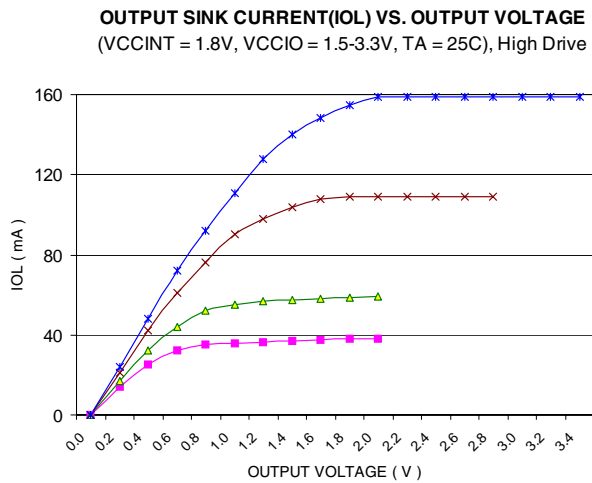
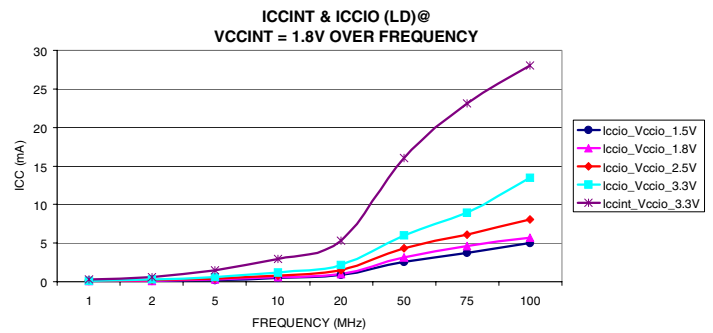
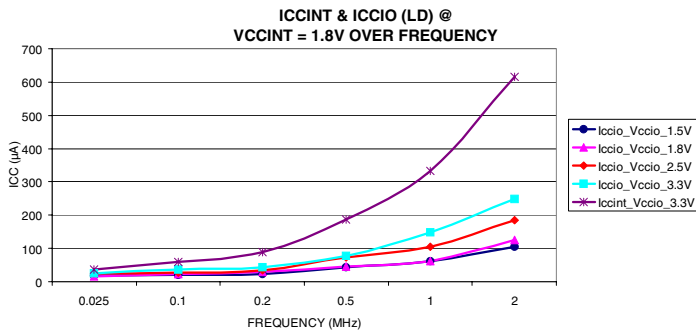
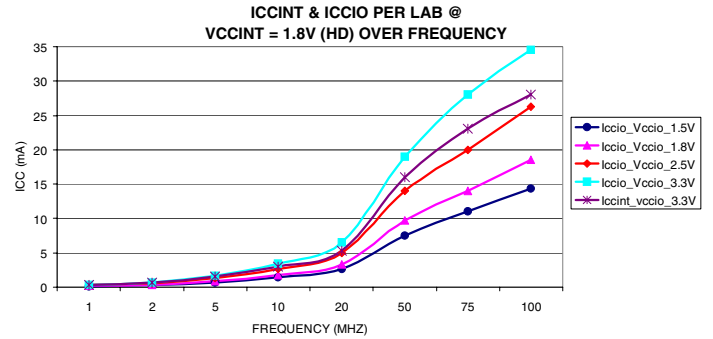
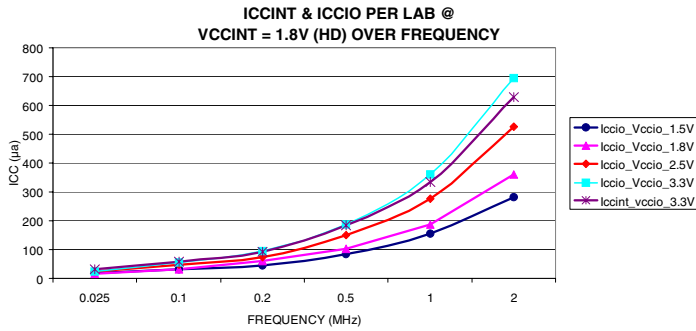
Table 13-2. ATF1508BE I/O Pinouts

MC	Logic Block	100-lead TQFP	132-ball CBGA	MC	Logic Block	100-lead TQFP	132-ball CBGA
1	A	2	G1	33	C	25	B1
2	A	-	-	34	C	-	-
3	A/ PD1	1	F1	35	C	24	B2
4	A	-	-	36	C	-	-
5	A	100	F2	37	C	23	A1
6	A	99	F3	38	C	22	B4
7	A	-	-	39	C	-	-
8	A	98	E1	40	C	21	A4
9	A	97	E2	41	C	20	C5
10	A	-	-	42	C	-	-
11	A	96	E3	43	C	19	B5
12	A	-	-	44	C	-	-
13	A	94	D1	45	C	17	A5
14	A	93	D2	46	C	16	C6
15	A	-	-	47	C	-	-
16	A	92	C1	48	C/ TMS	15	N10
17	B	14	C2	49	D	37	P2
18	B	-	-	50	D	-	-
19	B	13	G3	51	D	36	M3
20	B	-	-	52	D	-	-
21	B/VREFA	12	H1	53	D	35	N3
22	B	10	H2	54	D	33	P3
23	B	-	-	55	D	-	-
24	B	9	H3	56	D	32	M4
25	B	8	J1	57	D	31	M5
26	B	-	-	58	D	-	-
27	B	7	J2	59	D	30	N5
28	B	-	-	60	D	-	-
29	B	6	K1	61	D	29	P5
30	B	5	K3	62	D	28	M6
31	B	-	-	63	D	-	-
32	B/ TDI	4	M9	64	D	27	N6

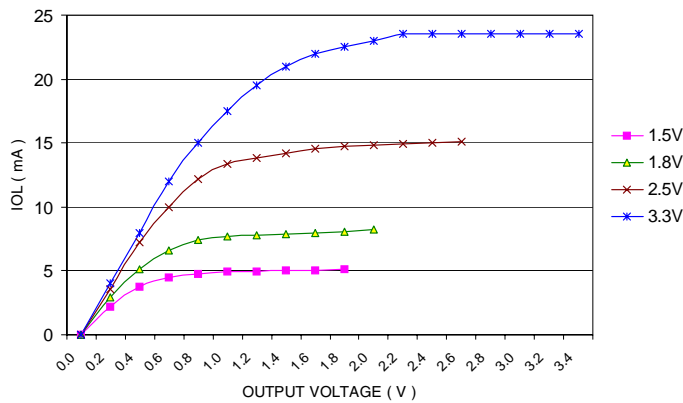
Table 13-2. ATF1508BE I/O Pinouts (Continued)

MC	Logic Block	100-lead TQFP	132-ball CBGA	MC	Logic Block	100-lead TQFP	132-ball CBGA
65	E	40	G13	97	G	63	C12
66	E	-	-	98	G	-	-
67	E/ PD2	41	G12	99	G	64	B12
68	E	-	-	100	G	-	-
69	E	42	F14	101	G	65	A12
70	E	44	F13	102	G	67	C11
71	E	-	-	103	G	-	-
72	E	45	F12	104	G	68	B11
73	E	46	E13	105	G	69	A11
74	E	-	-	106	G	-	-
75	E	47	E12	107	G	70	C10
76	E	-	-	108	G	-	-
77	E	48	D14	109	G	71	A10
78	E	49	D13	110	G	72	C9
79	E	-	-	111	G	-	-
80	E	50	D12	112	G/ TDO	73	B9
81	F	52	H12	113	H	75	N14
82	F	-	-	114	H	-	-
83	F	53	H13	115	H	76	N13
84	F	-	-	116	H	-	-
85	F	54	J13	117	H	77	P14
86	F	55	J12	118	H	78	P12
87	F	-	-	119	H	-	-
88	F	56	K14	120	H	79	M11
89	F	57	K13	121	H	80	N11
90	F	-	-	122	H	-	-
91	F	58	L14	123	H	81	P11
92	F	-	-	124	H	-	-
93	F/VREFB	60	L13	125	H	83	P10
94	F	61	L12	126	H	84	P9
95	F	-	-	127	H	-	-
96	F/ TCK	62	M10	128	H/ GCLK3	85	M8

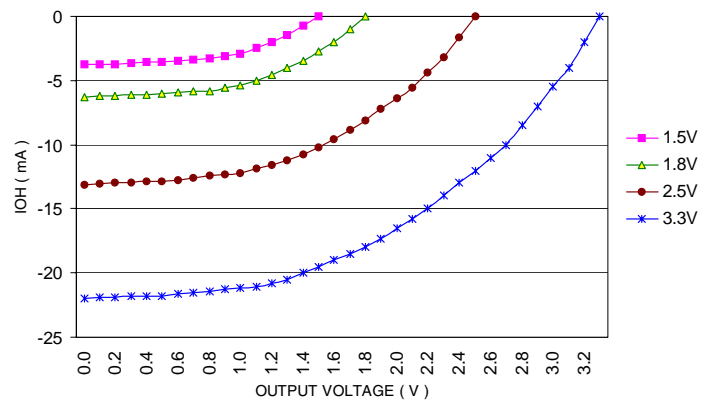
14. Typical DC and AC Characteristic Graphs



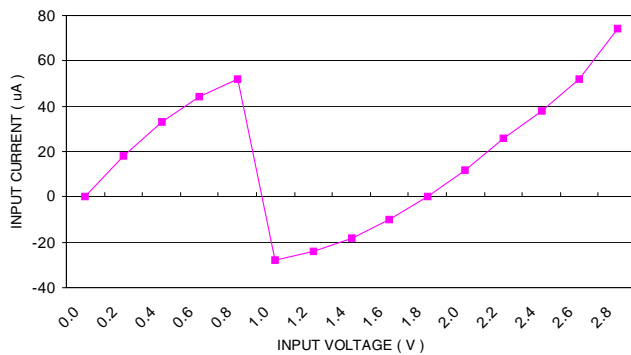
OUTPUT SINK CURRENT(IOL) VS. OUTPUT VOLTAGE
(VCCINT = 1.8V, VCCIO = 1.5-3.3V, TA = 25C), Low Drive



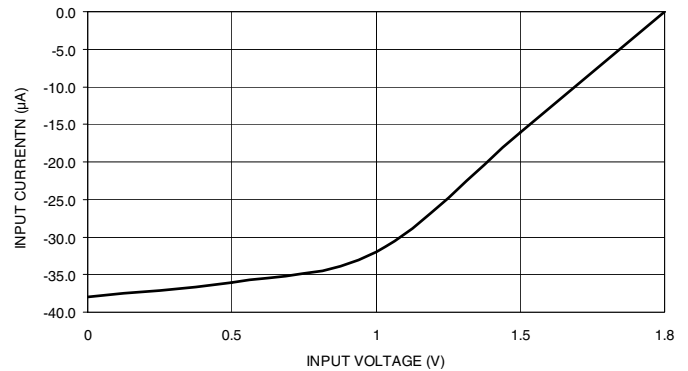
OUTPUT SOURCE CURRENT(IOH) VS. OUTPUT VOLTAGE
(VCCINT = 1.8V, VCCIO = 1.5-3.3V, TA = 25C), Low Drive



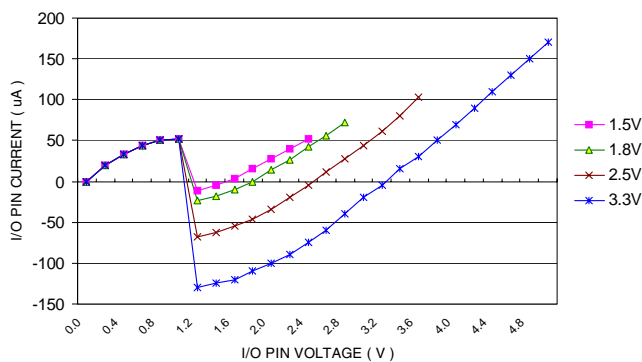
INPUT CURRENT VS. INPUT VOLTAGE
INPUT PIN (VCCINT = 1.8V, TA = 25C)
(PIN-KEEPER ON)



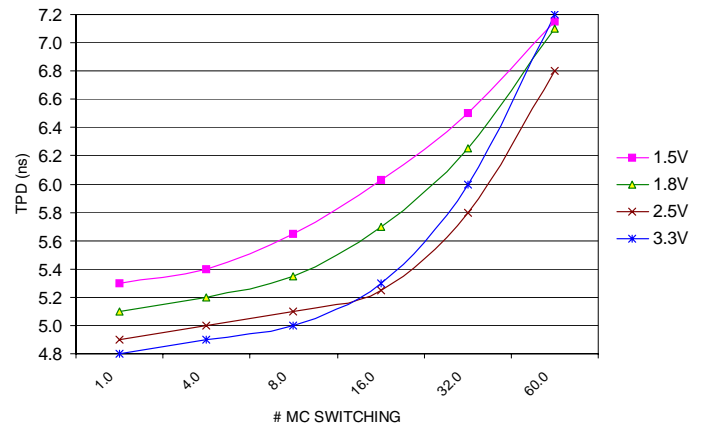
INPUT & I/O CURRENT VS. INPUT VOLTAGE
VCCINT = 1.8V, VCCIO = 1.8V (TA = 25°C)
(Pull-Up On)



I/O PIN CURRENT VS. I/O PIN VOLTAGE
I/O PIN (VCCINT = 1.8V, VCCIO = 1.5V-3.3V, TA = 25C)
(PIN KEEPER ON)



TPD VS. # MC SWITCHING
(VCCINT = 1.8V, VCCIO = 1.5-3.3V, TA = 25C)



15. Ordering Information

15.1 Lead-free Package Options (RoHS Compliant)

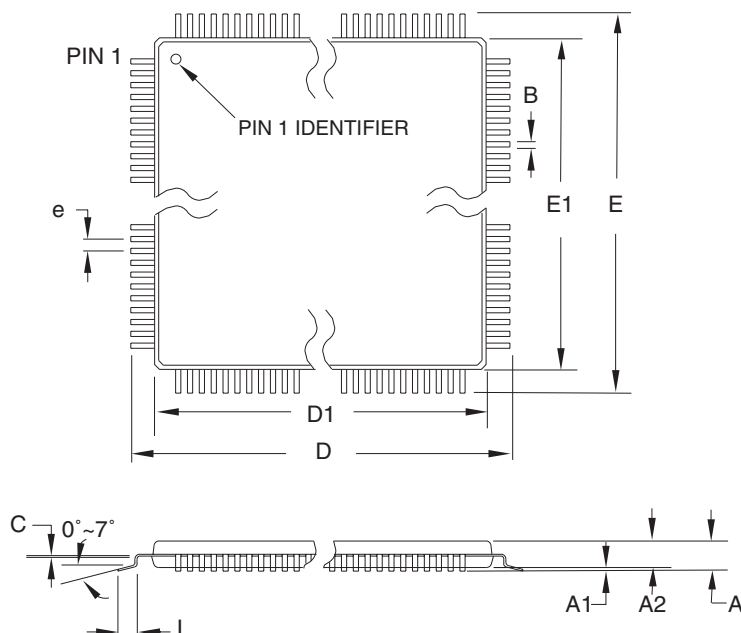
t_{PD} (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
5	6	ATF1508BE-5AX100	100A	Commercial (0° C to +70° C)
7	6.5	ATF1508BE-7AU100	100A	Industrial (-40° C to +85° C)
5	6	ATF1508BE-5CX132	132C1	Commercial (0° C to +70° C)
7	6.5	ATF1508BE-7CU132	132C1	Industrial (-40° C to +85° C)

Note: For shaded devices, contact marketing for availability.

Package Type	
100A	100-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
132C1	132-ball, Plastic Chip-Size Ball Grid Array Package (CBGA)

16. Packaging Information

16.1 100A – TQFP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	15.75	16.00	16.25	
D1	13.90	14.00	14.10	Note 2
E	15.75	16.00	16.25	
E1	13.90	14.00	14.10	Note 2
B	0.17	–	0.27	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.50 TYP			

- Notes:
1. This package conforms to JEDEC reference MS-026, Variation AED.
 2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
 3. Lead coplanarity is 0.08 mm maximum.

10/5/2001



2325 Orchard Parkway
San Jose, CA 95131

TITLE

100A, 100-lead, 14 x 14 mm Body Size, 1.0 mm Body Thickness,
0.5 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)

DRAWING NO.

100A

REV.

C



Headquarters

Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

International

Atmel Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Atmel Europe
Le Krebs
8, Rue Jean-Pierre Timbaud
BP 309
78054 Saint-Quentin-en-
Yvelines Cedex
France
Tel: (33) 1-30-60-70-00
Fax: (33) 1-30-60-71-11

Atmel Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Product Contact

Web Site
www.atmel.com

Technical Support
pld@atmel.com

Sales Contact
www.atmel.com/contacts

Literature Requests
www.atmel.com/literature

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