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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	19
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-LSSOP (0.220", 5.60mm Width)
Supplier Device Package	24-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f213g2ddsp-u0

1.1.2 Specifications

Tables 1.1 and 1.2 outline the Specifications for R8C/3GD Group.

Table 1.1 Specifications for R8C/3GD Group (1)

Item	Function	Specification
CPU	Central processing unit	R8C CPU core <ul style="list-style-type: none"> • Number of fundamental instructions: 89 • Minimum instruction execution time: <ul style="list-style-type: none"> 50 ns ($f(XIN) = 20$ MHz, $VCC = 2.7$ to 5.5 V) 200 ns ($f(XIN) = 5$ MHz, $VCC = 1.8$ to 5.5 V) • Multiplier: 16 bits \times 16 bits \rightarrow 32 bits • Multiply-accumulate instruction: 16 bits \times 16 bits + 32 bits \rightarrow 32 bits • Operation mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM, RAM	Refer to Table 1.3 Product List for R8C/3GD Group .
Power Supply Voltage Detection	Voltage detection circuit	<ul style="list-style-type: none"> • Power-on reset • Voltage detection 3 (detection level of voltage detection 0 and voltage detection 1 selectable)
I/O Ports	Programmable I/O ports	<ul style="list-style-type: none"> • Input-only: 1 pin • CMOS I/O ports: 19, selectable pull-up resistor • High current drive ports: 19
Clock	Clock generation circuits	4 circuits: XIN clock oscillation circuit, XCIN clock oscillation circuit (32 kHz), High-speed on-chip oscillator (with frequency adjustment function), Low-speed on-chip oscillator, <ul style="list-style-type: none"> • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16 • Low power consumption modes: <ul style="list-style-type: none"> Standard operating mode (high-speed clock, low-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode
Interrupts		Real-time clock (timer RE) <ul style="list-style-type: none"> • Number of interrupt vectors: 69 • External Interrupt: 7 ($INT \times 3$, Key input $\times 4$) • Priority levels: 7 levels
Watchdog Timer		<ul style="list-style-type: none"> • 14 bits \times 1 (with prescaler) • Reset start selectable • Low-speed on-chip oscillator for watchdog timer selectable
Timer	Timer RA	8 bits \times 1 (with 8-bit prescaler) Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB	8 bits \times 1 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timer RC	16 bits \times 1 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin)
	Timer RE	8 bits \times 1 Real-time clock mode (count seconds, minutes, hours, days of week)
Serial Interface	UART0	Clock synchronous serial I/O/UART
	UART2	Clock synchronous serial I/O/UART, I ² C mode (I ² C-bus), multiprocessor communication function
A/D Converter		10-bit resolution \times 8 channels, includes sample and hold function, with sweep mode
Comparator B		2 circuits

1.3 Block Diagram

Figure 1.2 shows a Block Diagram.

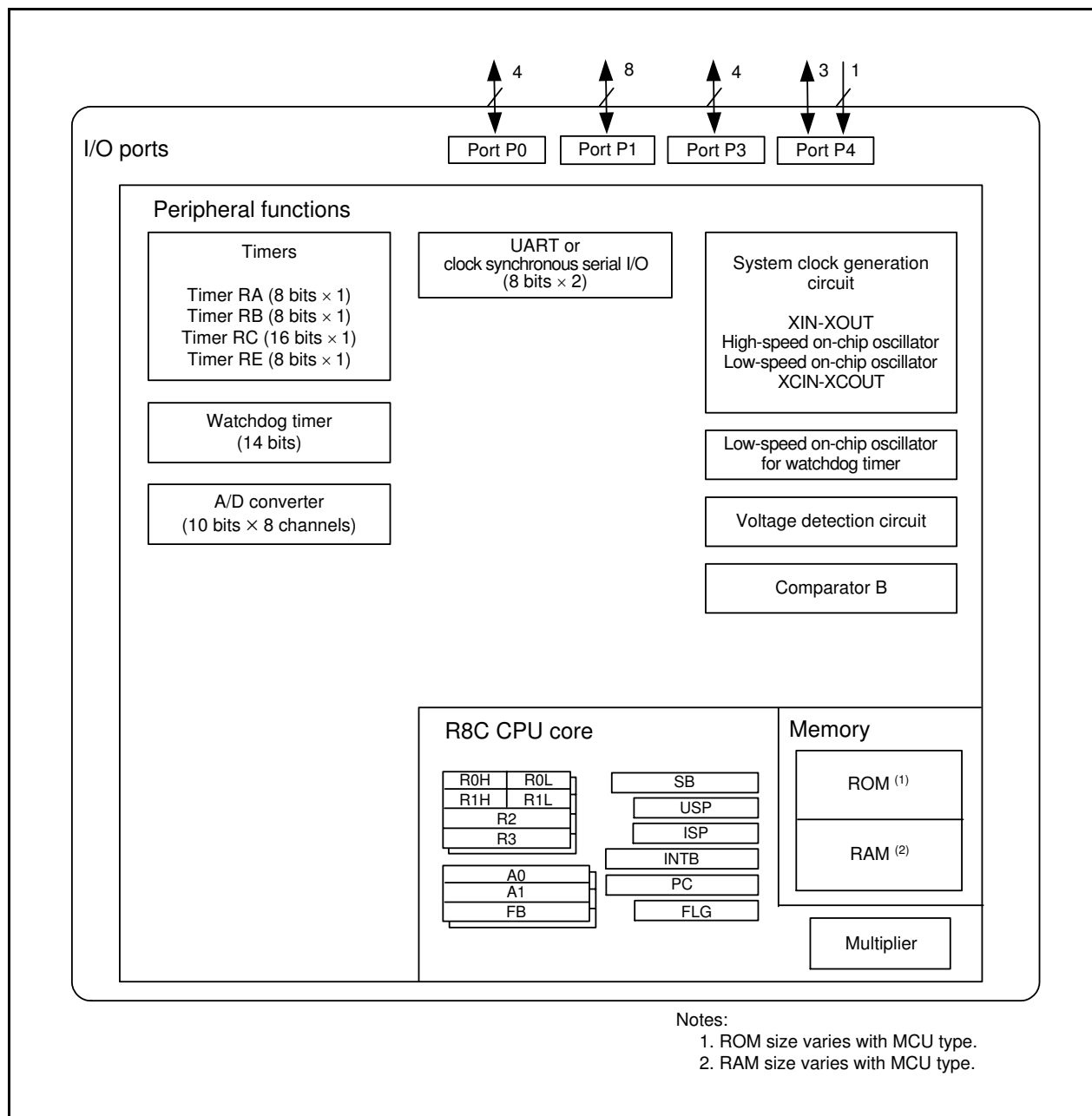


Figure 1.2 Block Diagram

Table 1.4 Pin Name Information by Pin Number

Pin Number	Control Pin	Port	I/O Pin Functions for Peripheral Modules			
			Interrupt	Timer	Serial Interface	A/D Converter, Comparator B
1		P0_2		(TRCIOA/TRCTRG)		AN5
2		P0_1		(TRCIOA/TRCTRG)		AN6
3		P4_2				VREF
4	MODE					
5	RESET					
6	XOUT(XCOUT)	P4_7				
7	VSS/AVSS					
8	XIN(XCIN)	P4_6				
9	VCC/AVCC					
10		P3_7		TRAO	(RXD2/SCL2/ TXD2/SDA2)	
11		P3_5		(TRCIOD)	(CLK2)	
12		P3_4		(TRCIOC)	(RXD2/SCL2/ TXD2/SDA2)	IVREF3
13		P3_3	$\overline{\text{INT3}}$	(TRCCLK)	(CTS2/RTS2)	IVCMP3
14		P4_5	$\overline{\text{INT0}}$		(RXD2/SCL2)	$\overline{\text{ADTRG}}$
15		P1_7	$\overline{\text{INT1}}$	(TRAIO)		IVCMP1
16		P1_6			(CLK0)	IVREF1
17		P1_5	($\overline{\text{INT1}}$)	(TRAIO)	(RXD0)	
18		P1_4		(TRCCLK)	(TXD0)	
19		P1_3	$\overline{\text{KI3}}$	TRBO/TRCIOC)		AN11
20		P1_2	$\overline{\text{KI2}}$	(TRCIOB)		AN10
21		P1_1	$\overline{\text{KI1}}$	(TRCIOA/TRCTRG)		AN9
22		P1_0	$\overline{\text{KI0}}$	(TRCIOD)		AN8
23		P0_7		(TRCIOC)		AN0
24		P0_6		(TRCIOD)		AN1

Note:

1. Can be assigned to the pin in parentheses by a program.

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.

Interrupts are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.

The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

3. Memory

3.1 R8C/3GD Group

Figure 3.1 is a Memory Map of R8C/3GD Group. The R8C/3GD Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 16-Kbyte internal ROM area is allocated addresses 0C000h to 0FFFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.

The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 1-Kbyte internal RAM area is allocated addresses 00400h to 007FFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh. Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.

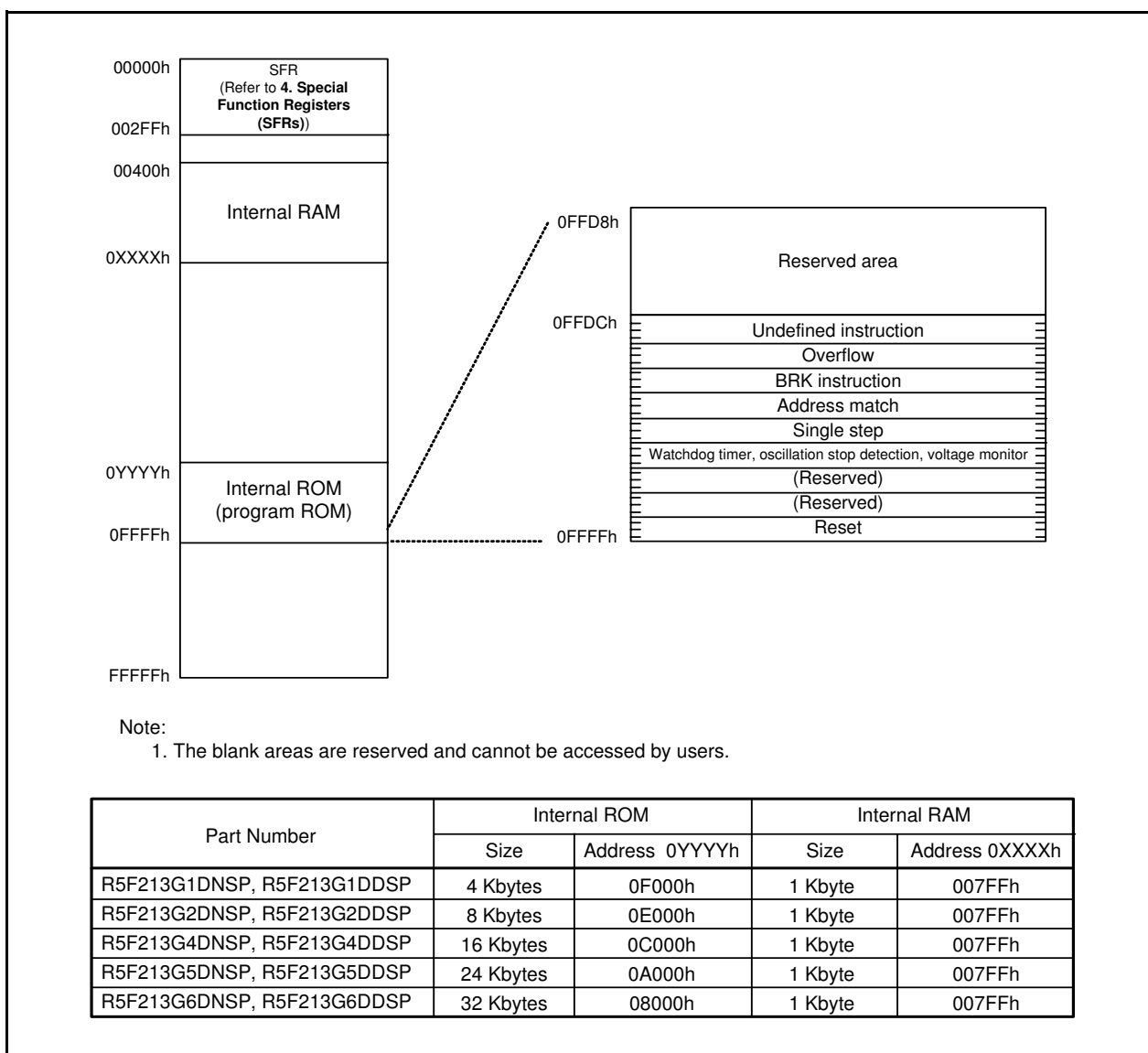


Figure 3.1 Memory Map of R8C/3GD Group

Table 4.7 SFR Information (7) (1)

Address	Register	Symbol	After Reset
01C0h	Address Match Interrupt Register 0	RMAD0	XXh
01C1h			XXh
01C2h			0000XXXXb
01C3h	Address Match Interrupt Enable Register	AIER	00h
01C4h	Address Match Interrupt Register 1	RMAD1	XXh
01C5h			XXh
01C6h			0000XXXXb
01C7h			
01C8h			
01C9h			
01CAh			
01CBh			
01CCh			
01CDh			
01CEh			
01CFh			
01D0h			
01D1h			
01D2h			
01D3h			
01D4h			
01D5h			
01D6h			
01D7h			
01D8h			
01D9h			
01DAh			
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			
01E0h	Pull-Up Control Register 0	PUR0	00h
01E1h	Pull-Up Control Register 1	PUR1	00h
01E2h			
01E3h			
01E4h			
01E5h			
01E6h			
01E7h			
01E8h			
01E9h			
01EAh			
01EBh			
01ECh			
01EDh			
01EEh			
01EFh			
01F0h	Port P1 Drive Capacity Control Register	P1DRR	00h
01F1h			
01F2h	Drive Capacity Control Register 0	DRR0	00h
01F3h	Drive Capacity Control Register 1	DRR1	00h
01F4h			
01F5h	Input Threshold Control Register 0	VLT0	00h
01F6h	Input Threshold Control Register 1	VLT1	00h
01F7h			
01F8h	Comparator B Control Register 0	INTCMP	00h
01F9h			
01FAh	External Input Enable Register 0	INTEN	00h
01FBh			
01FCh	INT Input Filter Select Register 0	INTF	00h
01FDh			
01FEh	Key Input Enable Register 0	KIEN	00h
01FFh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.8 ID Code Areas and Option Function Select Area

Address	Register	Symbol	After Reset
FFDBh	Option Function Select Register 2	OFS2	(Note 1)
FFDFh	ID1		(Note 2)
FFE3h	ID2		(Note 2)
FFEBh	ID3		(Note 2)
FEFh	ID4		(Note 2)
FFF3h	ID5		(Note 2)
FFF7h	ID6		(Note 2)
FFFBh	ID7		(Note 2)
FFFFh	Option Function Select Register	OFS	(Note 1)

Notes:

1. The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
Do not write additions to the option function select area. If the block including the option function select area is erased, the option function select area is set to FFh.
When blank products are shipped, the option function select area is set to FFh. It is set to the written value after written by the user.
When factory-programming products are shipped, the value of the option function select area is the value programmed by the user.
2. The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
Do not write additions to the ID code areas. If the block including the ID code areas is erased, the ID code areas are set to FFh.
When blank products are shipped, the ID code areas are set to FFh. They are set to the written value after written by the user.
When factory-programming products are shipped, the value of the ID code areas is the value programmed by the user.

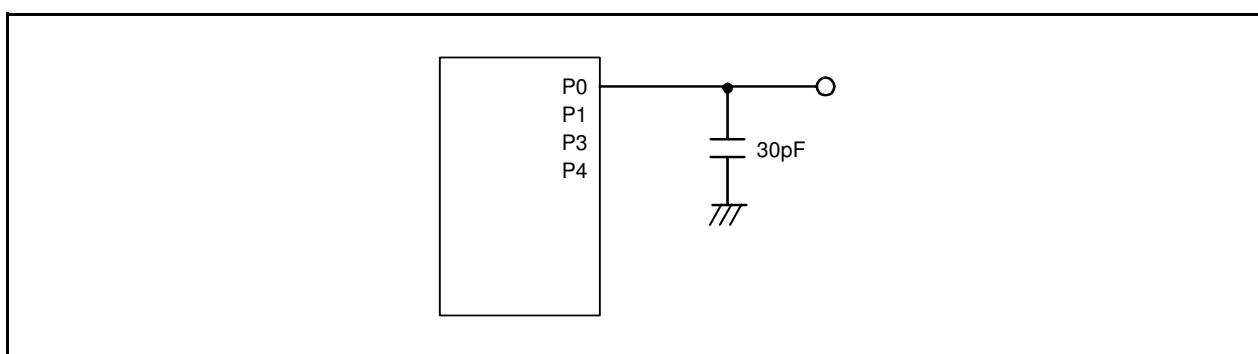


Figure 5.1 Ports P0, P1, P3, P4 Timing Measurement Circuit

Table 5.5 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance ⁽²⁾		1,000 ⁽³⁾	—	—	times
—	Byte program time		—	80	500	μs
—	Block erase time		—	0.3	—	s
t _d (SR-SUS)	Time delay from suspend request until suspend		—	—	5+CPU clock × 3 cycles	ms
—	Interval from erase start/restart until following suspend request		0	—	—	μs
—	Time from suspend until erase restart		—	—	30+CPU clock × 1 cycle	μs
t _d (CMDRST-READY)	Time from when command is forcibly stopped until reading is enabled		—	—	30+CPU clock × 1 cycle	μs
—	Program, erase voltage		2.7	—	5.5	V
—	Read voltage		1.8	—	5.5	V
—	Program, erase temperature		0	—	60	°C
—	Data hold time ⁽⁷⁾	Ambient temperature = 55°C	20	—	—	year

Notes:

1. V_{CC} = 2.7 to 5.5 V at T_{opr} = 0 to 60°C, unless otherwise specified.
2. Definition of programming/erasure endurance
The programming and erasure endurance is defined on a per-block basis.
If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

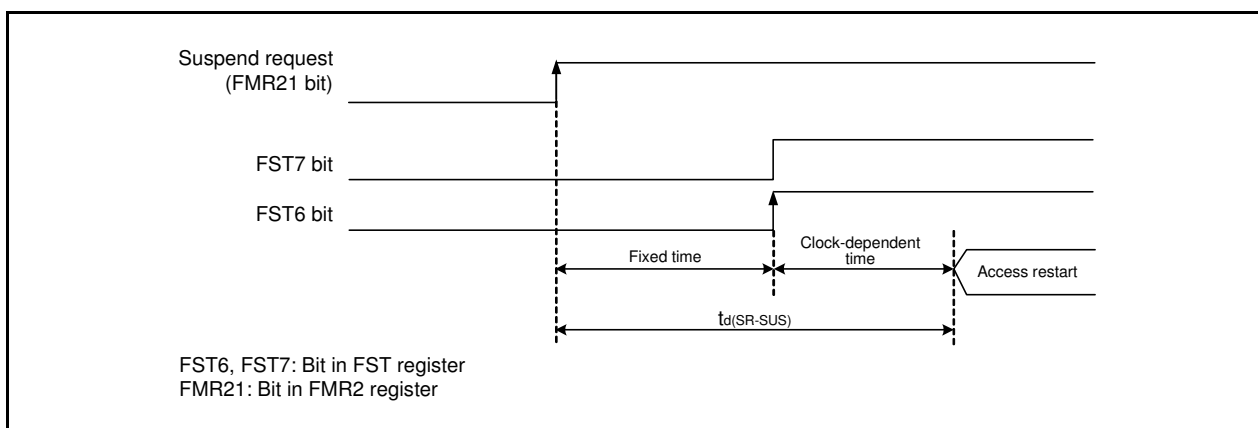
**Figure 5.2 Time delay until Suspend**

Table 5.6 Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V _{det0}	Voltage detection level V _{det0_0} ⁽²⁾		1.80	1.90	2.05	V
	Voltage detection level V _{det0_1} ⁽²⁾		2.15	2.35	2.50	V
	Voltage detection level V _{det0_2} ⁽²⁾		2.70	2.85	3.05	V
	Voltage detection level V _{det0_3} ⁽²⁾		3.55	3.80	4.05	V
—	Voltage detection 0 circuit response time ⁽⁴⁾	At the falling of V _{CC} from 5 V to (V _{det0_0} – 0.1) V	—	6	150	μs
—	Voltage detection circuit self power consumption	VCA25 = 1, V _{CC} = 5.0 V	—	1.5	—	μA
t _{d(E-A)}	Waiting time until voltage detection circuit operation starts ⁽³⁾		—	—	100	μs

Notes:

1. The measurement condition is V_{CC} = 1.8 V to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.
4. Time until the voltage monitor 0 reset is generated after the voltage passes V_{det0}.

Table 5.7 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V _{det1}	Voltage detection level V _{det1_0} ⁽²⁾	At the falling of V _{CC}	2.00	2.20	2.40	V
	Voltage detection level V _{det1_1} ⁽²⁾	At the falling of V _{CC}	2.15	2.35	2.55	V
	Voltage detection level V _{det1_2} ⁽²⁾	At the falling of V _{CC}	2.30	2.50	2.70	V
	Voltage detection level V _{det1_3} ⁽²⁾	At the falling of V _{CC}	2.45	2.65	2.85	V
	Voltage detection level V _{det1_4} ⁽²⁾	At the falling of V _{CC}	2.60	2.80	3.00	V
	Voltage detection level V _{det1_5} ⁽²⁾	At the falling of V _{CC}	2.75	2.95	3.15	V
	Voltage detection level V _{det1_6} ⁽²⁾	At the falling of V _{CC}	2.85	3.10	3.40	V
	Voltage detection level V _{det1_7} ⁽²⁾	At the falling of V _{CC}	3.00	3.25	3.55	V
	Voltage detection level V _{det1_8} ⁽²⁾	At the falling of V _{CC}	3.15	3.40	3.70	V
	Voltage detection level V _{det1_9} ⁽²⁾	At the falling of V _{CC}	3.30	3.55	3.85	V
	Voltage detection level V _{det1_A} ⁽²⁾	At the falling of V _{CC}	3.45	3.70	4.00	V
	Voltage detection level V _{det1_B} ⁽²⁾	At the falling of V _{CC}	3.60	3.85	4.15	V
	Voltage detection level V _{det1_C} ⁽²⁾	At the falling of V _{CC}	3.75	4.00	4.30	V
	Voltage detection level V _{det1_D} ⁽²⁾	At the falling of V _{CC}	3.90	4.15	4.45	V
	Voltage detection level V _{det1_E} ⁽²⁾	At the falling of V _{CC}	4.05	4.30	4.60	V
	Voltage detection level V _{det1_F} ⁽²⁾	At the falling of V _{CC}	4.20	4.45	4.75	V
—	Hysteresis width at the rising of V _{CC} in voltage detection 1 circuit	V _{det1_0} to V _{det1_5} selected	—	0.07	—	V
		V _{det1_6} to V _{det1_F} selected	—	0.10	—	V
—	Voltage detection 1 circuit response time ⁽³⁾	At the falling of V _{CC} from 5 V to (V _{det1_0} – 0.1) V	—	60	150	μs
—	Voltage detection circuit self power consumption	VCA26 = 1, V _{CC} = 5.0 V	—	1.7	—	μA
t _{d(E-A)}	Waiting time until voltage detection circuit operation starts ⁽⁴⁾		—	—	100	μs

Notes:

1. The measurement condition is V_{CC} = 1.8 V to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
3. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
4. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Table 5.8 Voltage Detection 2 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet2	Voltage detection level Vdet2_0	At the falling of Vcc	3.70	4.00	4.30	V
—	Hysteresis width at the rising of Vcc in voltage detection 2 circuit		—	0.10	—	V
—	Voltage detection 2 circuit response time ⁽²⁾	At the falling of Vcc from 5 V to (Vdet2_0 – 0.1) V	—	20	150	μs
—	Voltage detection circuit self power consumption	VCA27 = 1, Vcc = 5.0 V	—	1.7	—	μA
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽³⁾		—	—	100	μs

Notes:

1. The measurement condition is Vcc = 1.8 V to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes Vdet2.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 5.9 Power-on Reset Circuit (2)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
trth	External power Vcc rise gradient	⁽¹⁾	0	—	50000	mV/msec

Notes:

1. The measurement condition is T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.

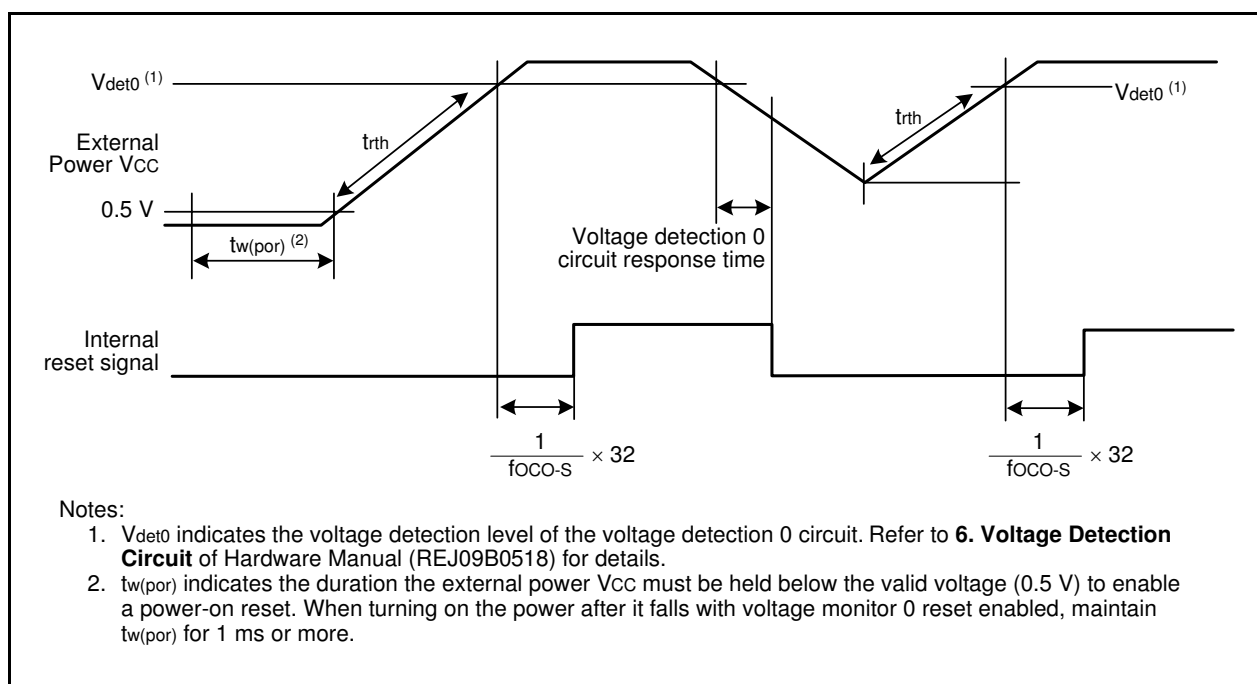
**Figure 5.3 Power-on Reset Circuit Electrical Characteristics**

Table 5.10 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
–	High-speed on-chip oscillator frequency after reset	$V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$ $-20^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}$	38.4	40	41.6	MHz
		$V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$ $-40^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}$	38.0	40	42.0	MHz
	High-speed on-chip oscillator frequency when the FRA4 register correction value is written into the FRA1 register and the FRA5 register correction value into the FRA3 register ⁽²⁾	$V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$ $-20^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}$	35.389	36.864	38.338	MHz
		$V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$ $-40^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}$	35.020	36.864	38.707	MHz
	High-speed on-chip oscillator frequency when the FRA6 register correction value is written into the FRA1 register and the FRA7 register correction value into the FRA3 register	$V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$ $-20^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}$	30.72	32	33.28	MHz
		$V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$ $-40^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}$	30.40	32	33.60	MHz
–	Oscillation stability time	$V_{CC} = 5.0 \text{ V}$, $T_{opr} = 25^{\circ}\text{C}$	–	0.5	3	ms
–	Self power consumption at oscillation	$V_{CC} = 5.0 \text{ V}$, $T_{opr} = 25^{\circ}\text{C}$	–	400	–	μA

Notes:

1. $V_{CC} = 1.8 \text{ to } 5.5 \text{ V}$, $T_{opr} = -20 \text{ to } 85^{\circ}\text{C}$ (N version) / $-40 \text{ to } 85^{\circ}\text{C}$ (D version), unless otherwise specified.
2. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

Table 5.11 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		60	125	250	kHz
–	Oscillation stability time	$V_{CC} = 5.0 \text{ V}$, $T_{opr} = 25^{\circ}\text{C}$	–	30	100	μs
–	Self power consumption at oscillation	$V_{CC} = 5.0 \text{ V}$, $T_{opr} = 25^{\circ}\text{C}$	–	2	–	μA

Note:

1. $V_{CC} = 1.8 \text{ to } 5.5 \text{ V}$, $T_{opr} = -20 \text{ to } 85^{\circ}\text{C}$ (N version) / $-40 \text{ to } 85^{\circ}\text{C}$ (D version), unless otherwise specified.

Table 5.12 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t _d (P-R)	Time for internal power supply stabilization during power-on ⁽²⁾		–	–	2000	μs

Notes:

1. The measurement condition is $V_{CC} = 1.8 \text{ to } 5.5 \text{ V}$ and $T_{opr} = 25^{\circ}\text{C}$.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.

Table 5.13 Electrical Characteristics (1) [4.2 V ≤ V_{CC} ≤ 5.5 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V _{OH}	Output "H" voltage	Other than XOUT	Drive capacity High V _{CC} = 5V	I _{OH} = -20 mA	V _{CC} - 2.0	—	V _{CC}	V
			Drive capacity Low V _{CC} = 5V	I _{OH} = -5 mA	V _{CC} - 2.0	—	V _{CC}	V
		XOUT	V _{CC} = 5V	I _{OH} = -200 μA	1.0	—	V _{CC}	V
V _{OL}	Output "L" voltage	Other than XOUT	Drive capacity High V _{CC} = 5V	I _{OL} = 20 mA	—	—	2.0	V
			Drive capacity Low V _{CC} = 5V	I _{OL} = 5 mA	—	—	2.0	V
		XOUT	V _{CC} = 5V	I _{OL} = 200 μA	—	—	0.5	V
V _{T+} -V _{T-}	Hysteresis	INT0, INT1, INT3, KI0, KI1, KI2, KI3, TRAIO, TRBO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRCTRG, TRCCLK, ADTRG, RXD0, RXD2, CLK0, CLK2			0.1	1.2	—	V
		RESET			0.1	1.2	—	V
I _{IH}	Input "H" current		V _I = 5 V, V _{CC} = 5.0V		—	—	5.0	μA
I _{IL}	Input "L" current		V _I = 0 V, V _{CC} = 5.0V		—	—	-5.0	μA
R _{PULLUP}	Pull-up resistance		V _I = 0 V, V _{CC} = 5.0V		25	50	100	kΩ
R _{IXIN}	Feedback resistance	XIN			—	0.3	—	MΩ
R _{IXCIN}	Feedback resistance	XCIN			—	8	—	MΩ
V _{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

Note:

1. 4.2 V ≤ V_{CC} ≤ 5.5 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 20 MHz, unless otherwise specified.

Table 5.14 Electrical Characteristics (2) [$3.3\text{ V} \leq V_{CC} \leq 5.5\text{ V}$]
($T_{opr} = -20\text{ to }85^{\circ}\text{C}$ (N version) / $-40\text{ to }85^{\circ}\text{C}$ (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	6.5	15	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	5.3	12.5	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	3.6	–	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3.0	–	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.2	–	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.5	–	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	7.0	15	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3.0	–	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-16 MSTTRC = 1	–	1	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	–	90	400	μA
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division FMR27 = 1, VCA20 = 0	–	85	400	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division Program operation on RAM Flash memory off, FMSTP = 1, VCA20 = 0	–	47	–	μA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	–	15	100	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	–	4	90	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (peripheral clock off) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	–	3.5	–	μA
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	2.0	5.0	μA
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	5.0	–	μA

Table 5.20 Electrical Characteristics (4) [$2.7\text{ V} \leq V_{CC} < 3.3\text{ V}$]
($T_{opr} = -20\text{ to }85^{\circ}\text{C}$ (N version) / $-40\text{ to }85^{\circ}\text{C}$ (D version), unless otherwise specified.)

Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	3.5	10	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.5	7.5	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	7.0	15	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3.0	–	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	4.0	–	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.5	–	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-16 MSTTRC = 1	–	1	–	mA
			Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	–	90	390
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division FMR27 = 1, VCA20 = 0	–	80	400	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division	–	40	–	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz Program operation on RAM Flash memory off, FMSTP = 1, VCA20 = 0	–	40	–	μA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	–	15	90	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	–	4	80	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (peripheral clock off) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	–	3.5	–	μA
			Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	2.0	5.0
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	5.0	–	μA

Table 5.25 Electrical Characteristics (5) [$1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$]

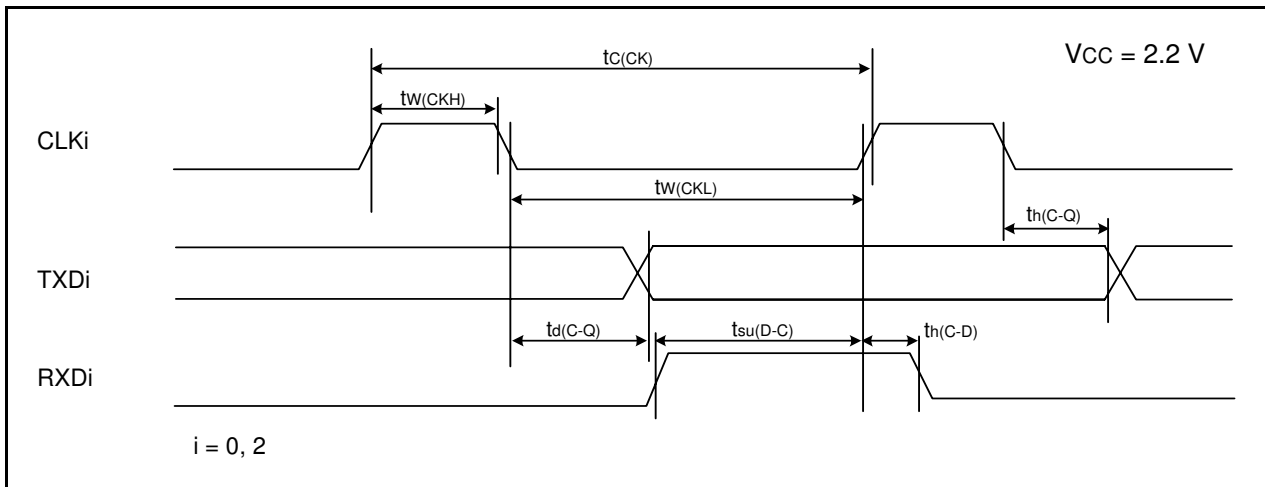
Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V _{OH}	Output "H" voltage	Other than XOUT	Drive capacity High	I _{OH} = -2 mA	V _{CC} - 0.5	—	V _{CC}	V
			Drive capacity Low	I _{OH} = -1 mA	V _{CC} - 0.5	—	V _{CC}	V
		XOUT		I _{OH} = -200 μ A	1.0	—	V _{CC}	V
V _{OL}	Output "L" voltage	Other than XOUT	Drive capacity High	I _{OL} = 2 mA	—	—	0.5	V
			Drive capacity Low	I _{OL} = 1 mA	—	—	0.5	V
		XOUT		I _{OL} = 200 μ A	—	—	0.5	V
V _{T+} -V _{T-}	Hysteresis	INT0, INT1, INT3, KI0, KI1, KI2, KI3, TRAIO, TRBO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRCTRG, TRCCLK, ADTRG, RXD0, RXD2, CLK0, CLK2			0.05	0.2	—	V
		RESET			0.05	0.20	—	V
I _{IH}	Input "H" current		V _I = 2.2 V, V _{CC} = 2.2 V		—	—	4.0	μ A
I _{IL}	Input "L" current		V _I = 0 V, V _{CC} = 2.2 V		—	—	-4.0	μ A
R _{PULLUP}	Pull-up resistance		V _I = 0 V, V _{CC} = 2.2 V		70	140	300	k Ω
R _{IXIN}	Feedback resistance	XIN			—	0.3	—	M Ω
R _{IXCIN}	Feedback resistance	XCIN			—	8	—	M Ω
V _{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

Note:

1. $1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$ at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 5 MHz, unless otherwise specified.

Table 5.29 Serial Interface

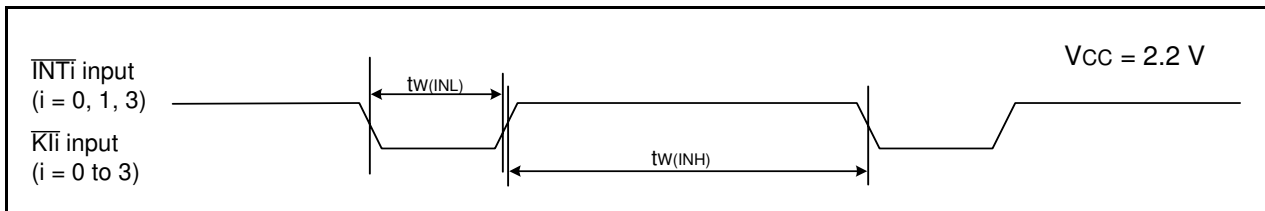
Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	800	—	ns
$t_{w(CKH)}$	CLKi input "H" width	400	—	ns
$t_{w(CKL)}$	CLKi input "L" width	400	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	200	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	150	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

 $i = 0, 2$ **Figure 5.14 Serial Interface Timing Diagram when $V_{CC} = 2.2\text{ V}$** **Table 5.30 External Interrupt \overline{INTi} ($i = 0, 1, 3$) Input, Key Input Interrupt \overline{Kli} ($i = 0$ to 3)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	\overline{INTi} input "H" width, \overline{Kli} input "H" width	1000 ⁽¹⁾	—	ns
$t_{w(INL)}$	\overline{INTi} input "L" width, \overline{Kli} input "L" width	1000 ⁽²⁾	—	ns

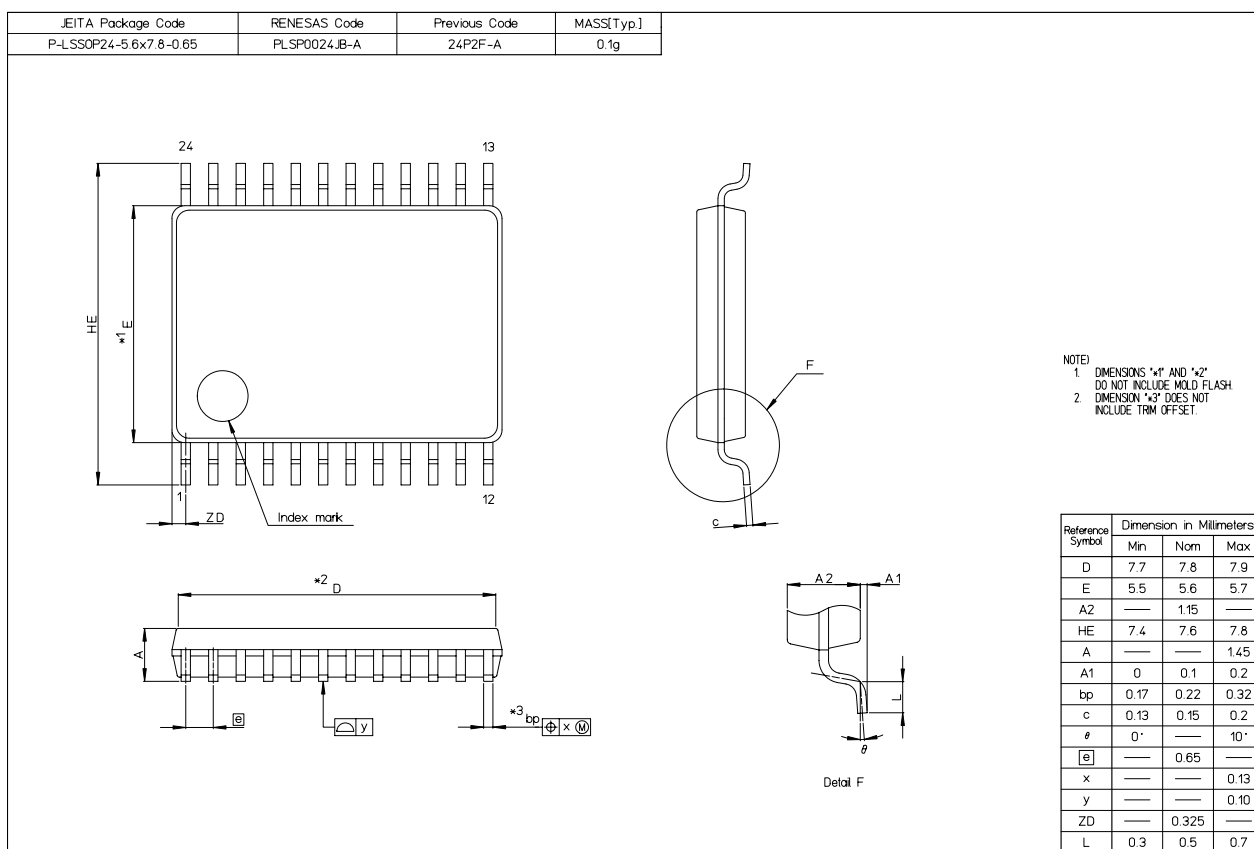
Notes:

- When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input HIGH width of either (1/digital filter clock frequency $\times 3$) or the minimum value of standard, whichever is greater.
- When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input LOW width of either (1/digital filter clock frequency $\times 3$) or the minimum value of standard, whichever is greater.

**Figure 5.15 Input Timing for External Interrupt \overline{INTi} and Key Input Interrupt \overline{Kli} when $V_{CC} = 2.2\text{ V}$**

Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Technology website.



REVISION HISTORY	R8C/3GD Group Datasheet
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Rev.	Date	Description	
		Page	Summary
0.01	Sep. 10, 2009	–	First Edition issued
1.00	Feb. 26, 2010	All pages 4 21 to 40	“Preliminary”, “Under development” deleted Table 1.3 revised “5. Electrical Characteristics” added

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