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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	19
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-LSSOP (0.220", 5.60mm Width)
Supplier Device Package	24-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f213g4dnsp-u0

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RENESAS MCU

1. Overview

1.1 Features

The R8C/3GD Group of single-chip MCUs incorporates the R8C CPU core, employing sophisticated instructions for a high level of efficiency. With 1 Mbyte of address space, and it is capable of executing instructions at high speed. In addition, the CPU core boasts a multiplier for high-speed operation processing.

Power consumption is low, and the supported operating modes allow additional power control. These MCUs are designed to maximize EMI/EMS performance.

Integration of many peripheral functions, including multifunction timer and serial interface, reduces the number of system components.

1.1.1 Applications

Electronic household appliances, office equipment, audio equipment, consumer equipment, etc.

Item	Function	Specification	
Flash Memory		 Programming and erasure voltage: VCC = 2.7 to 5.5 V 	
		 Programming and erasure endurance: 1,000 times (program ROM) 	
		 Program security: ROM code protect, ID code check 	
		 Debug functions: On-chip debug, on-board flash rewrite function 	
Operating Freq	uency/Supply	f(XIN) = 20 MHz (VCC = 2.7 to 5.5 V)	
Voltage		f(XIN) = 5 MHz (VCC = 1.8 to 5.5 V)	
Current consur	nption	Typ. 6.5mA (VCC = 5.0 V, f(XIN) = 20 MHz) Typ. 3.5mA (VCC = 3.0 V, f(XIN) = 10 MHz)	
		$V_{\text{IVP}} = 0.5 \text{ mA} (VCC = 3.0 \text{ V}, f(XIN) = 10 \text{ MHz})$	
		Typ. 3.5μ A (VCC = 3.0 V, wait mode (f(XCIN) = 32 kHz)) Typ. 2.0μ A (VCC = 3.0 V, stop mode)	
On a ratio a Arab	is at Tanan a wature		
Operating Ambient Temperature		$-20 \text{ to } 85^{\circ}\text{C} \text{ (N version)}$	
		-40 to 85°C (D version) ⁽¹⁾	
Package		24-pin LSSOP	
		Package code: PLSP0024JB-A (previous code: 24P2F-A)	

Specifications for R8C/3GD Group (2) Table 1.2

Note: 1. Specify the D version if D version functions are to be used.

Current of Feb. 2010

1.2 Product List

Table 1.3 lists Product List for R8C/3GD Group, and Figure 1.1 shows a Part Number, Memory Size, and Package of R8C/3GD Group.

Part No.	ROM Capacity	RAM Capacity	Package Type	Remarks
R5F213G1DNSP	4 Kbytes	1 Kbyte	PLSP0024JB-A	N version
R5F213G2DNSP	8 Kbytes	1 Kbyte	PLSP0024JB-A	
R5F213G4DNSP	16 Kbytes	1 Kbyte	PLSP0024JB-A	
R5F213G5DNSP	24 Kbytes	1 Kbyte	PLSP0024JB-A	
R5F213G6DNSP	32 Kbytes	1 Kbyte	PLSP0024JB-A	
R5F213G1DDSP (D)	4 Kbytes	1 Kbyte	PLSP0024JB-A	D version
R5F213G2DDSP (D)	8 Kbytes	1 Kbyte	PLSP0024JB-A	
R5F213G4DDSP (D)	16 Kbytes	1 Kbyte	PLSP0024JB-A	
R5F213G5DDSP (D)	24 Kbytes	1 Kbyte	PLSP0024JB-A	1
R5F213G6DDSP (D)	32 Kbytes	1 Kbyte	PLSP0024JB-A]

Table 1.3 Product List for R8C/3GD Group

(D): Under development



Figure 1.1 Part Number, Memory Size, and Package of R8C/3GD Group

1.3 Block Diagram

Figure 1.2 shows a Block Diagram.





2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.



2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the starting address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

Special Function Registers (SFRs) 4.

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.7 list the special function registers and Table 4.8 lists the ID Code Areas and Option Function Select Area.

Table 4.1	SFR Information (1) (1)				
Address	Register	Symbol	After Reset		
0000h					
0001h					
0002h					
0003h					
0004h	Processor Mode Register 0	PM0	00h		
0005h	Processor Mode Register 1	PM1	00h		
0006h	System Clock Control Register 0	CM0	00101000b		
0007h	System Clock Control Register 1	CM1	0010000b		
0008h	Module Standby Control Register	MSTCR	00h		
0009h	System Clock Control Register 3	CM3	00h		
000Ah	Protect Register	PRCR	00h		
000Bh	Reset Source Determination Register	RSTFR	0XXXXXXb ⁽²⁾		
000Ch	Oscillation Stop Detection Register	OCD	00000100b		
000Dh	Watchdog Timer Reset Register	WDTR	XXh		
000Eh	Watchdog Timer Start Register	WDTS	XXh		
000Fh	Watchdog Timer Control Register	WDTC	00111111b		
0010h					
0011h 0012h					
0012h 0013h					
0013h					
0015h	High-Speed On-Chip Oscillator Control Register 7	FRA7	When shipping		
0016h	Thigh-opeed on-only oscillator oblittor negister 7	11127	When shipping		
0017h					
0018h					
0019h					
001Ah					
001Bh					
001Ch	Count Source Protection Mode Register	CSPR	00h		
	, and the second s		1000000b ⁽³⁾		
001Dh					
001Eh					
001Fh					
0020h					
0021h					
0022h					
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h		
0024h	High-Speed On-Chip Oscillator Control Register 1	FRA1	When shipping		
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	00h		
0026h	On-Chip Reference Voltage Control Register	OCVREFCR	00h		
0027h		00005			
0028h	Clock Prescaler Reset Flag	CPSRF	00h		
0029h	High-Speed On-Chip Oscillator Control Register 4	FRA4 FRA5	When Shipping When Shipping		
002Ah	High-Speed On-Chip Oscillator Control Register 5				
002Bh 002Ch	High-Speed On-Chip Oscillator Control Register 6	FRA6	When Shipping		
002Ch 002Dh					
002Eh					
002En	High-Speed On-Chip Oscillator Control Register 3	FRA3	When shipping		
0030h	Voltage Monitor Circuit Control Register	CMPA	00h		
0031h	Voltage Monitor Circuit Edge Select Register	VCAC	00h		
0032h					
0033h	Voltage Detect Register 1	VCA1	00001000b		
0034h	Voltage Detect Register 2	VCA2	00h ⁽⁴⁾		
-		-	00100000b ⁽⁵⁾		
0035h					
0036h	Voltage Detection 1 Level Select Register	VD1LS	00000111b		
0037h					
0038h	Voltage Monitor 0 Circuit Control Register	VW0C	1100X010b (4)		
			1100X011b (5)		
0039h	Voltage Monitor 1 Circuit Control Register	VW1C	10001010b		

Table 4.1	SFR Information (1) ⁽¹⁾

X: Undefined Notes:

1.

The blank areas are reserved and cannot be accessed by users. The CWR bit in the RSTFR register is set to 0 after power-on and voltage monitor 0 reset. Hardware reset, software reset, or watchdog timer 2. reset does not affect this bit.

The CSPROINI bit in the OFS register is set to 0. 3.

The LVDAS bit in the OFS register is set to 1. 4.

5. The LVDAS bit in the OFS register is set to 0.

Address	Register	Symbol	After Reset
003Ah	Voltage Monitor 2 Circuit Control Register	VW2C	10000010b
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			
0040h			
0041h	Flash Memory Ready Interrupt Control Register	FMRDYIC	XXXXX000b
0042h			
0043h			
0044h 0045h			
0045h 0046h			
0040h	Timer RC Interrupt Control Register	TRCIC	XXXXX000b
0048h		1100	
0049h			
004Ah	Timer RE Interrupt Control Register	TREIC	XXXXX000b
004Bh	UART2 Transmit Interrupt Control Register	S2TIC	XXXXX000b
004Ch	UART2 Receive Interrupt Control Register	S2RIC	XXXXX000b
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh	-		
0050h			
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	SORIC	XXXXX000b
0053h			
0054h			
0055h			
0056h	Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0057h		70010	
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah 005Bh	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh 005Ch			
005Dh	INT0 Interrupt Control Register	INTOIC	XX00X000b
005Eh	UART2 Bus Collision Detection Interrupt Control Register	U2BCNIC	XXXXX000b
005Eh		02DOINIG	~~~~~
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h	Veltage Meniter 1 Interrupt Control D-sister	VOMPTIO	
0072h 0073h	Voltage Monitor 1 Interrupt Control Register Voltage Monitor 2 Interrupt Control Register	VCMP1IC VCMP2IC	XXXXX000b XXXXX000b
0073h 0074h		VUMP2IU	^^^^U
0074h 0075h			
0075h	<u> </u>		
	<u> </u>		
0077h	<u> </u>		
0077h 0078h			
0078h			
0078h 0079h			
0078h 0079h 007Ah			
0078h 0079h 007Ah 007Bh			
0078h 0079h 007Ah 007Bh 007Ch			
0078h 0079h 007Ah 007Bh			
0078h 0079h 007Ah 007Bh 007Ch 007Dh			

SFR Information (2)⁽¹⁾ Table 4.2

X: Undefined Note: 1. The blank areas are reserved and cannot be accessed by users.

Address	Bogister	Symbol	After Reset
	Register		
00C0h	A/D Register 0	AD0	XXXh 000000XXb
00C1h		4.54	
00C2h	A/D Register 1	AD1	XXh
00C3h			000000XXb
00C4h	A/D Register 2	AD2	XXh
00C5h			000000XXb
00C6h	A/D Register 3	AD3	XXh
00C7h			00000XXb
00C8h	A/D Register 4	AD4	XXh
00C9h	, č		000000XXb
00CAh	A/D Register 5	AD5	XXh
00CBh			00000XXb
00CCh	A/D Register 6	AD6	XXh
00CDh		1.20	000000XXb
00CEh	A/D Register 7	AD7	XXh
00CFh		AD1	000000XXb
00CFI			000000000
00D0h			
00D2h			4
00D3h		1.51.(0.5	
00D4h	A/D Mode Register	ADMOD	00h
00D5h	A/D Input Select Register	ADINSEL	11000000b
00D6h	A/D Control Register 0	ADCON0	00h
00D7h	A/D Control Register 1	ADCON1	00h
00D8h		1	
00D9h			
00DAh			
00DBh			
00DCh			
00DDh			+
00DEh			
00DFh	Deut DO De sietes	D0	
00E0h	Port PO Register	P0	XXh
00E1h	Port P1 Register	P1	XXh
00E2h	Port P0 Direction Register	PD0	00h
00E3h	Port P1 Direction Register	PD1	00h
00E4h			
00E5h	Port P3 Register	P3	XXh
00E6h			
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	XXh
00E9h			
00EAh	Port P4 Direction Register	PD4	00h
00EBh	-	1	
00ECh			1 1
00EDh			1 1
00EEh		1	+
00EFh			+
00E111			4
00F1h		+	+
00F1h			
			4
00F3h			
00F4h			
00F5h			4
00F6h			
00F7h			
00F8h			
00F9h			
00FAh			
00FBh			
00FCh		1	
00FDh			
00FEh		1	+
00FFh		1	+
X: Undefined	1	1	

SFR Information (4)⁽¹⁾ Table 4.4

X: Undefined Note: 1. The blank areas are reserved and cannot be accessed by users.

0100h Timer RA Control Register TRACR 00h 0101h Timer RA Uo Control Register TRAMR 00h 0102h Timer RA Mode Register TRAMR 00h 0103h Timer RA Mode Register TRAMR 00h 0104h Timer RA Mode Register TRAP FFh 0104h Timer RA Control Register TRACE 00h 0106h Timer RB Control Register TRBCR 00h 0106h Timer RB Control Register TRBCR 00h 0106h Timer RB Control Register TRBCR 00h 0106h Timer RB Social Control Register TRBCR FFh 0106h Timer RB Social Register TRBCR FFh </th <th>Address</th> <th>Register</th> <th>Symbol</th> <th>After Reset</th>	Address	Register	Symbol	After Reset
010b. Timer RA Mode Register TRAMR 00h 010b. Timer RA Prescue Register TRAPE FFh 010b. Timer RA Prescue Register TRAP FFh 010b. Timer RA Register TRAP FFh 010b. Timer RA Control Register TRACR 00h 010b. Timer RB Control Register TRBCR 00h 010b. Timer RB Control Register TRBCR 00h 010b. Timer RB Control Register TRBCR PFh 010b. Timer RB Control Register TRBCR PFh 010b. Timer RB Scondary Register TRBCR PFh 010b. Timer RB Scondary Register TRBCR PFh 010b. Timer RB Scondary Register TRBCR PFh 010b. Timer RB Scond Data Register TRESEC 00h 0111h Timer RE Second Data Register TRESEC 00h 0116h Timer RE Second Data Register TRESEC 00h 0116h Timer RE Second Data Register TRESEC	0100h		TRACR	00h
0100h Time RA Prescaler Register TRAPE FFh 010h Time RA Register TRA FFh 010bh Time RA Register TRE FFh 010bh Time RE Control Register TRBCR 00h 010bh Timer RE Control Register TRBCR 00h 010bh Timer RE Control Register TRBMR 00h 010bh Timer RE Vocotrol Register TRBMR 00h 010bh Timer RE Prescaler Register TRBMR 00h 010bh Timer RE Prescaler Register TRBPRE FFh 010bh Timer RE Prescaler Register TRBPRE FFh 010bh Timer RE Prinzing Register TRBPRE FFh 010bh Timer RE Prinzing Register TRBPRE FFh 0111h Timer RE Second Data Register TRBPRE FFh 0115h Timer RE Second Data Register TREMR 00h 0115h Timer RE Second Data Register TREMR 00h 0115h Timer RE Second Data Register TREMR				
0104h Timer RA Register TRA FPh 0105h				
0106h				
0100h Immer RB Control Register THBCR 00h 0108h Timer RB Constrol Register THBCR 00h 0108h Timer RB Inde Social Control Register THBCR 00h 0108h Timer RB Inde Social Register THBBRC 00h 0108h Timer RB Social Register THBBRE FFh 0108h Timer RE Social Register THBBRE FFh 0118h Timer RE Social Register THBESC OPh 0118h Timer RE Social Register THESCE OPh 0118h Timer RE Social Register THESCE OPh 0118h Timer RE Social Register THESCH OPh 0118h Timer RE Social Register THESCH OPh 0118h Timer RE Contrit Register THEC		Timer RA Register	TRA	FFh
0107h mer RB Cartrol Register TRBCR 00h 0108h Timer RB Cartrol Register TRBCC 00h 0108h Timer RB UC Cartrol Register TRBINC 00h 0108h Timer RB Work Register TRBNRE FFh 0100h Timer RB Prescaler Register TRBNRE FFh 0100h Timer RB Prescaler Register TRBNR FFh 0100h Timer RB Primary Register TRBNR FFh 010h Timer RB Primary Register TRBNR FFh 010h Timer RB Second Data Register TRESE FFh 0111h				
0109h Timer RB Concitol Register THBCR 00h 0104h Timer RB One-Shot Control Register THBIOC 00h 0104h Timer RB One-Shot Control Register THBINC 00h 0106h Timer RB One-Shot Control Register THBINC 00h 0106h Timer RB Socondray Register THBBRE FFh 0106h Timer RB Socondray Register THBSC FFh 0107h				
010h Timer RB One-Shot Control Register TRBOCR 00h 010hA Timer RB VO Control Register TRBNRE IFR 010ch Timer RB Prescuer Register TRBNRE IFR 010ch Timer RB Prescuer Register TRBNRE IFR 010ch Timer RB Primary Register TRBNRE IFR 010ch Timer RB Primary Register TRBNRE IFR 010ch Timer RB Primary Register TRBNRE IFR 0111h				
010Ah Timer RB UGC Control Register TRBINR 00h 010Dh Timer RB Mode Register TRBPRE FFh 010Dh Timer RB Soccatory Register TRBPC FFh 010Dh Timer RB Soccatory Register TRBPC FFh 010Dh Timer RB Soccatory Register TRBPC FFh 010Dh Timer RB Soccatory Register TRBPR FFh 010Dh Immer RB Jong Register TRBPR FFh 0111h Immer RE Soccatory Register Immer RE Jong View Register Immer RE Jong View Register 0113h Immer RE Soccatory Register TRESCC Oth Immer RE Jong View Register Immer RES				
0100h Timer RB Mode Register TBBMR 00h 0100h Timer RB Prescuer Register TBBSC FFh 0100h Timer RB primary Register TBBSC FFh 0100h Timer RB primary Register TBBSC FFh 0100h Timer RB primary Register TBBSC FFh 0100h Imer RB primary Register TBBSC FFh 0110h Imer RE Second Data Register Imer RE Second Data Register Imer RESC 00h 0118h Imer RE Second Data Register TRESEC 00h Imer RE Second Data Register Imer RESC 00h 0118h Timer RE Second Data Register TRESEC 00h Imer RE Second Data Register Imer RESC 00h 0118h Timer RE Second Data Register TRESEC 00h Imer RE Second Data Register Imer RESC 00h 0118h Timer RE Second Data Register TRESEC 00h Imer RE Second Data Register Imer RESC 00h 0118h Timer RE Second Data Register TRESE 00h Imer RE Second Data Register <td< td=""><td></td><td></td><td>TRBOCR</td><td>00h</td></td<>			TRBOCR	00h
0100h Timer RB Seccaler Register TRBPRE FFn 0100h Timer RB Seccaler Register TRBPC FFn 0101h Timer RB Primary Register TRBPR FFn 0101h TRBP R FFn F 0101h TRBPR FFn F 0111h TRBPR F F 0112h TRBPR F F F 0112h Tmer RE Second Data Register TRESEC Oth T 0118h Timer RE Second Data Register TRESEC Oth T T F <td>010Ah</td> <td></td> <td>TRBIOC</td> <td>00h</td>	010Ah		TRBIOC	00h
0100h Timer RB Secondary Register TRBSC FFn 010eh Timer RB Primary Register TRBPR FFn 0100h Imer RB Primary Register TRBPR FFn 0110h Imer RB Primary Register TRBPR FFn 0111h Imer RE Primary Register Imer RE Imer RE 0111h Imer RE Second Data Register TRESEC 00h 0118h Imer RE Second Data Register TRESEC 00h 0118h Timer RE Second Data Register TRESE 00h 0118h Timer RE Second Data Register TREVR 00h 0118h Timer RE Second Data Register TREVR 00h 0118h Timer RE Second Register TREVR 00h 0118h Timer RE Second Register TREVR 00h 0118h Timer RE Second Register TREVR 00h 0118h Timer RE Control Register TRECR 00h 0118h Timer RE Control Register TRECR 00h 0118h Timer RC Imorrupt Enable Register			TRBMR	00h
010Eh Timer RB Primary Register TRBPR FFh 0110h			TRBPRE	
0107h	010Dh	Timer RB Secondary Register	TRBSC	FFh
0110h	010Eh		TRBPR	FFh
0111h	010Fh			
0112h	0110h			
0113h	0111h			
0113h	0112h			
0114h				
0115h				
0116h				
0117h Imer RE Second Data Register TRESEC 00h 0118h Timer RE Munute Data Register TREMIN 00h 0111h Timer RE Day Of Week Data Register TREWK 00h 0111bh Timer RE Day Of Week Data Register TREWK 00h 0111bh Timer RE Day Of Week Data Register TRECR1 00h 0111bh Timer RE Control Register 2 TRECR2 00h 0111bh Timer RE Control Register 2 TRECSR 00001000b 0111bh Timer RE Control Register 2 TRECSR 01001000b 012bh Timer RC Mode Register TRCCR1 00h 012bh Timer RC Control Register 1 TRCCR1 00h 012bh Timer RC Iolorontol Register 0 TRCICR0 1110000b 012bh Timer RC Control Register 0 TRCICR1 10001000b 012bh Timer RC Goenral Register 0 TRCGRA FFh 012bh Timer RC General Register 0 TRCGRA FFh 012bh Timer RC General Register 0 TRCGRB FFh				
Offshow Timer RE Second Data Register TRESEC 00h 0119h Timer RE Minute Data Register TREMIN 00h 0111h Timer RE Day of Week Data Register TREMIN 00h 0111h Timer RE Day of Week Data Register TREV 00h 0111h Timer RE Control Register 1 TRECR1 00h 0111bh Timer RE Control Register 2 TRECR2 00h 0111bh Timer RE Control Register 1 TRECR2 00h 0112bh Timer RE Control Register 1 TRECR2 00h 012bh Timer RE Control Register 1 TRECR2 00h 012bh Timer RE Control Register 1 TRCCR1 00h 012bh Timer RE Control Register 0 TRCICR1 10001000b 012bh Timer RC Control Register 1 TRCCR1 10001000b 012bh Timer RC Control Register 1 TRCCR1 00h 012bh Timer RC General Register A TRCCR0 100h 012bh Timer RC General Register C TRCGR0 FFh 012bh <td></td> <td></td> <td></td> <td></td>				
0119h Timer RE Minute Data Register THEMIN ODh 011Ah Timer RE Hour Data Register TREHR OOh 011Bh Timer RE Dav of Week Data Register TREVR OOh 011Dh Timer RE Control Register 1 TRECR1 OOh 011Dh Timer RE Control Register 2 TRECR2 OOh 011Dh Timer RE Control Register 2 TRECR2 00h 011Ph Timer RE Control Register 2 TRECR8 01001000b 012h Timer RC Mode Register TRCMR 01001000b 012h Timer RC Control Register 1 TRCCR1 00h 012h Timer RC Ior Control Register 0 TRCIRCR 01110000b 012h Timer RC IO Control Register 1 TRCIRCR 10001000b 012h Timer RC Goundre Register 0 TRCIRCR 00h 012h Timer RC Goundre Register 1 TRCGR0 10001000b 012h Timer RC Goundre Register A TRCGRA FFh 012h Timer RC General Register A TRCGRB FFh 012Eh		Timer BE Second Data Begister	TRESEC	00h
011Ah Timer RE Hour Data Register THEHR 00h 011Bh Timer RE Day of Week Data Register TREWK 00h 011Ch Timer RE Control Register 1 TRECR2 00h 011Dh Timer RE Control Register 2 TRECR2 00h 011Eh Timer RE Control Register 2 TRECR2 00h 011Eh Timer RE Control Register 1 TRECR2 00h 012h Timer RC Control Register 1 TRECR8 01001000b 012h Timer RC Control Register 1 TRECR8 01110000b 012h Timer RC Interrupt Enable Register TRECR8 01110000b 012h Timer RC I/O Control Register 1 TRECR0 110000b 012h Timer RC I/O Control Register 1 TRECR1 10001000b 012h Timer RC General Register A TRCGRA FFh 012h Timer RC General Register B TRCGRA FFh 012h Timer RC General Register C TRCGRC FFh 012h Timer RC General Register C TRCGRC FFh 012h				
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0138h				
0139h				
013Ah				
013Bh				
013Ch				
013Dh				
013Eh				
013Fh 0140h				
0140h				
	: 017Fh	1		

SFR Information (5)⁽¹⁾ Table 4.5

Note: 1. The blank areas are reserved and cannot be accessed by users.

Address	Register	Symbol	After Reset
01C0h	Address Match Interrupt Register 0	RMAD0	XXh
01C1h			XXh
01C2h			0000XXXXb
01C3h	Address Match Interrupt Enable Register	AIER	00h
01C4h	Address Match Interrupt Register 1	RMAD1	XXh
01C5h	· · · · · · · · · · · · · · · · · · ·		XXh
01C6h			0000XXXXb
01C7h			000070000
01C8h			
01C9h			
01CAh			
01CBh			
01CCh			
01CDh			
01CEh			
01CFh			
01D0h			
01D1h			
01D2h			
01D3h			
01D4h			
01D5h			
01D6h			
01D7h			
01D8h			
01D9h			
01DAh			
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			
01E0h	Pull-Up Control Register 0	PUR0	00h
01E1h	Pull-Up Control Register 1	PUR1	00h
01E2h			
01E3h			
01E4h			
01E5h			
01E6h			
01E7h			
01E8h			
01E9h			
01EAh			
01EBh			
01ECh			
01EDh			
01EEh			
01EFh			
01F0h	Port P1 Drive Capacity Control Register	P1DRR	00h
01F1h			
01F2h	Drive Capacity Control Register 0	DRR0	00h
01F3h	Drive Capacity Control Register 1	DRR1	00h
01F4h			
01F5h	Input Threshold Control Register 0	VLT0	00h
01F6h	Input Threshold Control Register 1	VLT1	00h
01F7h			
01F8h	Comparator B Control Register 0	INTCMP	00h
01F9h			
01FAh	External Input Enable Register 0	INTEN	00h
01FBh			
01FCh	INT Input Filter Select Register 0	INTF	00h
01FDh			
01FEh	Key Input Enable Register 0	KIEN	00h
01FFh			
X: Undefined			

Table 4.7	SFR Information (7) ⁽¹⁾
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X: Undefined Note: 1. The blank areas are reserved and cannot be accessed by users.

Symbol	Parameter	Conditions	Standard			Linit
		Conditions	Min.	Тур.	Max.	Unit
—	Program/erase endurance (2)		1,000 (3)	-	-	times
-	Byte program time		-	80	500	μs
-	Block erase time		-	0.3	-	s
td(SR-SUS)	Time delay from suspend request until suspend		-	-	5+CPU clock × 3 cycles	ms
-	Interval from erase start/restart until following suspend request		0	-	_	μS
-	Time from suspend until erase restart		-	-	30+CPU clock × 1 cycle	μS
td(CMDRST- READY)	Time from when command is forcibly stopped until reading is enabled		-	-	30+CPU clock × 1 cycle	μS
-	Program, erase voltage		2.7	-	5.5	V
-	Read voltage		1.8	-	5.5	V
-	Program, erase temperature		0	-	60	°C
-	Data hold time ⁽⁷⁾	Ambient temperature = 55°C	20	-	-	year

Table 5.5 Flash Memory (Program ROM) Electrical Characteristics

Notes:

1. Vcc = 2.7 to 5.5 V at Topr = 0 to 60°C, unless otherwise specified.

2. Definition of programming/erasure endurance

The programming and erasure endurance is defined on a per-block basis. If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.

However, the same address must not be programmed more than once per erase operation (overwriting prohibited).

Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
 In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit

the number of erase operations to a certain number.
If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.

6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.

7. The data hold time includes time that the power supply is off or the clock is not supplied.





Symbol	Parameter	Condition	Standard			Unit
Symbol	Faranieter	Condition	Min.	Тур.	Max.	Unit
Vdet0	Voltage detection level Vdet0_0 (2)		1.80	1.90	2.05	V
	Voltage detection level Vdet0_1 (2)		2.15	2.35	2.50	V
	Voltage detection level Vdet0_2 (2)		2.70	2.85	3.05	V
	Voltage detection level Vdet0_3 (2)		3.55	3.80	4.05	V
-	Voltage detection 0 circuit response time (4)	At the falling of Vcc from 5 V to $(Vdet0_0 - 0.1)$ V	_	6	150	μs
-	Voltage detection circuit self power consumption	VCA25 = 1, Vcc = 5.0 V	-	1.5	-	μA
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽³⁾		-	-	100	μS

Table 5.6 Voltage Detection 0 Circuit Electrical Characteristics

Notes:

1. The measurement condition is Vcc = 1.8 V to 5.5 V and $T_{opr} = -20$ to $85^{\circ}C$ (N version) / -40 to $85^{\circ}C$ (D version).

2. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.

3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.

4. Time until the voltage monitor 0 reset is generated after the voltage passes Vdet0.

Table 5.7 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition		Unit		
Symbol	Falailletei	Condition	Min.	Тур.	Max.	Unit
Vdet1	Voltage detection level Vdet1_0 ⁽²⁾	At the falling of Vcc	2.00	2.20	2.40	V
	Voltage detection level Vdet1_1 (2)	At the falling of Vcc	2.15	2.35	2.55	V
	Voltage detection level Vdet1_2 (2)	At the falling of Vcc	2.30	2.50	2.70	V
	Voltage detection level Vdet1_3 (2)	At the falling of Vcc	2.45	2.65	2.85	V
	Voltage detection level Vdet1_4 (2)	At the falling of Vcc	2.60	2.80	3.00	V
	Voltage detection level Vdet1_5 (2)	At the falling of Vcc	2.75	2.95	3.15	V
	Voltage detection level Vdet1_6 ⁽²⁾	At the falling of Vcc	2.85	3.10	3.40	V
	Voltage detection level Vdet1_7 (2)	At the falling of Vcc	3.00	3.25	3.55	V
	Voltage detection level Vdet1_8 (2)	At the falling of Vcc	3.15	3.40	3.70	V
	Voltage detection level Vdet1_9 (2)	At the falling of Vcc	3.30	3.55	3.85	V
	Voltage detection level Vdet1_A (2)	At the falling of Vcc	3.45	3.70	4.00	V
	Voltage detection level Vdet1_B (2)	At the falling of Vcc	3.60	3.85	4.15	V
	Voltage detection level Vdet1_C ⁽²⁾	At the falling of Vcc	3.75	4.00	4.30	V
	Voltage detection level Vdet1_D (2)	At the falling of Vcc	3.90	4.15	4.45	V
	Voltage detection level Vdet1_E (2)	At the falling of Vcc	4.05	4.30	4.60	V
	Voltage detection level Vdet1_F (2)	At the falling of Vcc	4.20	4.45	4.75	V
-	Hysteresis width at the rising of Vcc in voltage detection 1 circuit	Vdet1_0 to Vdet1_5 selected	_	0.07	-	V
		Vdet1_6 to Vdet1_F selected	_	0.10	-	V
-	Voltage detection 1 circuit response time (3)	At the falling of Vcc from 5 V to (Vdet1_0 - 0.1) V	-	60	150	μS
_	Voltage detection circuit self power consumption	VCA26 = 1, Vcc = 5.0 V	-	1.7	-	μA
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽⁴⁾		-	-	100	μS

Notes:

1. The measurement condition is Vcc = 1.8 V to 5.5 V and Topr = -20 to $85^{\circ}C$ (N version) / -40 to $85^{\circ}C$ (D version).

2. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.

3. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1} .

4. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Symbol	Parameter	r Condition		Standard Min. Typ. Max.			Unit	
				win.				
lcc	Power supply current (Vcc = 3.3 to 5.5 V)	High-speed clock mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	-	6.5	15	mA	
	Single-chip mode, output pins are open, other pins		XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	-	5.3	12.5	mA	
	are Vss		XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	-	3.6	-	mA	
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	-	3.0	_	mA	
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	-	2.2	_	mA	
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	-	1.5	_	mA	
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	-	7.0	15	mA	
			XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	-	3.0	_	mA	
			XIN clock off High-speed on-chip oscillator on fOCO-F = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-16 MSTTRC = 1	-	1	-	mA	
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	-	90	400	μA	
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division FMR27 = 1, VCA20 = 0	_	85	400	μA	
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division Program operation on RAM Flash memory off, FMSTP = 1, VCA20 = 0	-	47	_	μA	
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	-	15	100	μA	
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	-	4	90	μA	
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (peripheral clock off) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	_	3.5	_	μA	
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	_	2.0	5.0	μA	
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	-	5.0	_	μA	

Table 5.14Electrical Characteristics (2) [3.3 V \leq Vcc \leq 5.5 V]
(Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Timing Requirements (Unless Otherwise Specified: Vcc = 5 V, Vss = 0 V at Topr = 25°C)

Table 5.15 External clock input (XOUT, XCIN)

Symbol	Parameter		Standard		
Symbol			Max.	Unit	
tc(XOUT)	XOUT input cycle time	50	-	ns	
twh(xout)	XOUT input "H" width	24	-	ns	
twl(xout)	XOUT input "L" width	24	-	ns	
tc(XCIN)	XCIN input cycle time	14	-	μS	
twh(xcin)	XCIN input "H" width	7	-	μS	
twl(xcin)	XCIN input "L" width	7	-	μS	



Figure 5.4 External Clock Input Timing Diagram when Vcc = 5 V

Table 5.16 TRAIO Input

Symbol	Parameter		Standard		
Symbol	Farameter	Min.	Max.	Unit	
tc(TRAIO)	TRAIO input cycle time	100	-	ns	
twh(traio)	TRAIO input "H" width	40	-	ns	
twl(traio)	TRAIO input "L" width	40	-	ns	



Figure 5.5 TRAIO Input Timing Diagram when Vcc = 5 V

Symbol	Parameter		Standard		
Symbol			Max.	Unit	
tc(CK)	CLKi input cycle time	200	-	ns	
tW(CKH)	CLKi input "H" width	100	-	ns	
tW(CKL)	CLKi input "L" width	100	-	ns	
td(C-Q)	TXDi output delay time	-	50	ns	
th(C-Q)	TXDi hold time	0	-	ns	
tsu(D-C)	RXDi input setup time	50	=	ns	
th(C-D)	RXDi input hold time	90	=	ns	

i = 0, 2



Figure 5.6 Serial Interface Timing Diagram when Vcc = 5 V

Table 5.18 External Interrupt INTi (i = 0, 1, 3) Input, Key Input Interrupt Kli (i = 0 to 3)

Symbol	Parameter		Standard		
			Max.	Unit	
tw(INH)	INTi input "H" width, Kli input "H" width	250 (1)	-	ns	
tw(INL)	INTi input "L" width, Kli input "L" width	250 (2)	I	ns	

Notes:

1. When selecting the digital filter by the INTi input filter select bit, use an INTi input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

2. When selecting the digital filter by the INTi input filter select bit, use an INTi input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.



Figure 5.7 Input Timing for External Interrupt INTi and Key Input Interrupt Kli when Vcc = 5 V

Table 5.20Electrical Characteristics (4) [2.7 V \leq Vcc < 3.3 V]
(Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Parameter Condition			Standard	ł	Unit	
Symbol				Min.	Тур.	Max.	Unit	
lcc	Power supply current (Vcc = 2.7 to 3.3 V) Single-chip mode,	High-speed clock mode	XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	-	3.5	10	mA	
	output pins are open, other pins are Vss		XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	1	1.5	7.5	mA	
		High-speed on-chip oscillator	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	_	7.0	15	mA	
		mode	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	-	3.0	-	mA	
			XIN clock off High-speed on-chip oscillator on fOCO-F = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	-	4.0	-	mA	
		XIN clock off High-speed on-chip oscillator on fOCO-F = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	-	1.5	-	mA		
			XIN clock off High-speed on-chip oscillator on fOCO-F = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-16 MSTTRC = 1	-	1	-	mA	
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	-	90	390	μA	
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division FMR27 = 1, VCA20 = 0	-	80	400	μA	
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division Program operation on RAM Flash memory off, FMSTP = 1, VCA20 = 0	_	40	_	μA	
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	_	15	90	μA	
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	-	4	80	μA	
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (peripheral clock off) While a WAIT instruction is executed	-	3.5	-	μA	
		Stop mode	$\begin{array}{l} VCA27 = VCA26 = VCA25 = 0, VCA20 = 1 \\ \hline XIN clock off, T_{opr} = 25^{\circ}C \\ High-speed on-chip oscillator off \\ Low-speed on-chip oscillator off \\ CM10 = 1 \\ \hline \end{array}$	_	2.0	5.0	μA	
			Peripheral clock off VCA27 = VCA26 = VCA25 = 0 XIN clock off, $T_{opr} = 85^{\circ}C$ High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1	_	5.0	_	μA	
			Peripheral clock off VCA27 = VCA26 = VCA25 = 0					

Table 5.23 Seri	al Interface
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Symbol	Parameter		Standard		
Symbol			Max.	Unit	
tc(CK)	CLKi input cycle time	300	-	ns	
tW(CKH)	CLKi input "H" width	150	-	ns	
tW(CKL)	CLKi Input "L" width	150	-	ns	
td(C-Q)	TXDi output delay time	-	80	ns	
th(C-Q)	TXDi hold time	0	-	ns	
tsu(D-C)	RXDi input setup time	70	-	ns	
th(C-D)	RXDi input hold time	90	-	ns	

i = 0, 2



Figure 5.10 Serial Interface Timing Diagram when Vcc = 3 V

Table 5.24 External Interrupt INTi (i = 0, 1, 3) Input, Key Input Interrupt Kli (i = 0 to 3)

Symbol	Parameter		Standard		
			Max.	Unit	
tw(INH)	INTi input "H" width, Kli input "H" width	380 (1)	-	ns	
tw(INL)	INTi input "L" width, Kli input "L" width	380 (2)	I	ns	

Notes:

1. When selecting the digital filter by the INTi input filter select bit, use an INTi input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

2. When selecting the digital filter by the INTi input filter select bit, use an INTi input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.



Figure 5.11 Input Timing for External Interrupt INTi and Key Input Interrupt Kli when Vcc = 3 V

Symbol	Po	rameter	Conditi	Condition -		tandard		Unit
Symbol	Fai	ameter	Conditi			Min. Typ. Max.		Unit
Vон	Output "H" voltage	Other than XOUT	Drive capacity High	Iон = -2 mA	Vcc - 0.5	-	Vcc	V
			Drive capacity Low	Iон = -1 mA	Vcc - 0.5	-	Vcc	V
		XOUT		Іон = -200 μА	1.0	-	Vcc	V
Vol	Output "L" voltage	Other than XOUT	Drive capacity High	Iol = 2 mA	-	-	0.5	V
			Drive capacity Low	IOL = 1 mA	-	-	0.5	V
		XOUT		IOL = 200 μA	-	-	0.5	V
VT+-VT-	Hysteresis	INTO, INT1, INT3, KIO, KI1, KI2, KI3, TRAIO, TRBO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRCTRG, TRCCLK, ADTRG, RXD0, RXD2, CLK0, CLK2 RESET			0.05	0.2	_	V
Ін	Input "H" current	ILUE I	VI = 2.2 V, Vcc = 2.2	2 V	_		4.0	μA
lıL	Input "L" current		VI = 0 V, Vcc = 2.2 V		_	_	-4.0	μA
RPULLUP	Pull-up resistance		VI = 0 V, Vcc = 2.2 \		70	140	300	kΩ
Rfxin	Feedback resistance	XIN			_	0.3	-	MΩ
Rfxcin	Feedback resistance	XCIN			-	8	-	MΩ
VRAM	RAM hold voltage		During stop mode		1.8		_	V

Table 5.25	Electrical Characteristics (5) [1.8 V \leq Vcc $<$ 2.7 V]
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Note:

1. $1.8 \text{ V} \le \text{Vcc} < 2.7 \text{ V}$ at Topr = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 5 MHz, unless otherwise specified.

Timing Requirements (Unless Otherwise Specified: Vcc = 2.2 V, Vss = 0 V at Topr = 25°C)

Table 5.27 External clock input (XOUT, XCIN)

Symbol	Parameter	Standard		Unit
		Min.	Max.	Unit
tc(XOUT)	XOUT input cycle time	200	-	ns
twh(xout)	XOUT input "H" width	90	-	ns
twl(xout)	XOUT input "L" width	90	-	ns
tc(XCIN)	XCIN input cycle time	14	-	μS
twh(xcin)	XCIN input "H" width	7	-	μS
twl(xcin)	XCIN input "L" width	7	-	μS



Figure 5.12 External Clock Input Timing Diagram when Vcc = 2.2 V

Table 5.28 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	Unit
tc(TRAIO)	TRAIO input cycle time	500	-	ns
twh(traio)	TRAIO input "H" width	200	-	ns
twl(traio)	TRAIO input "L" width	200	-	ns



Figure 5.13 TRAIO Input Timing Diagram when Vcc = 2.2 V