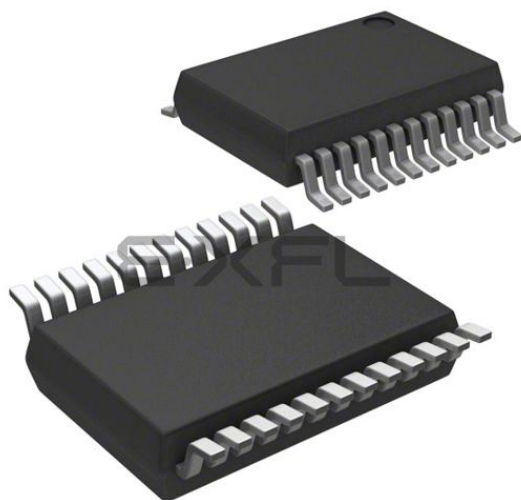




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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	19
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-LSSOP (0.220", 5.60mm Width)
Supplier Device Package	24-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f213g6ddsp-u0

1.4 Pin Assignment

Figure 1.3 shows Pin Assignment (Top View). Table 1.4 outlines the Pin Name Information by Pin Number.

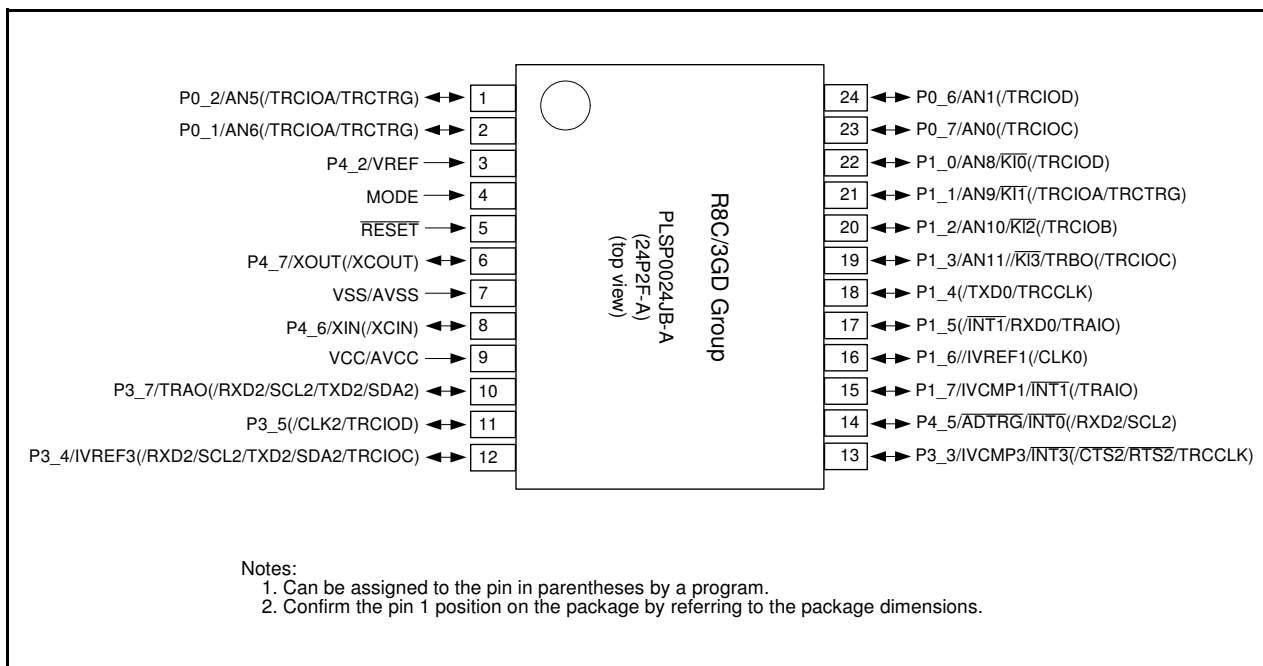


Figure 1.3 Pin Assignment (Top View)

1.5 Pin Functions

Table 1.5 lists Pin Functions.

Table 1.5 Pin Functions

Item	Pin Name	I/O Type	Description
Power supply input	VCC, VSS	–	Apply 1.8 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	–	Power supply for the A/D converter. Connect a capacitor between AVCC and AVSS.
Reset input	$\overline{\text{RESET}}$	I	Input “L” on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
XIN clock input	XIN	I	These pins are provided for XIN clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins ⁽¹⁾ . To use an external clock, input it to the XOUT pin and leave the XIN pin open.
XIN clock output	XOUT	I/O	
XCIN clock input	XCIN	I	These pins are provided for XCIN clock generation circuit I/O. Connect a crystal oscillator between the XCIN and XCOUT pins ⁽¹⁾ . To use an external clock, input it to the XCIN pin and leave the XCOUT pin open.
XCIN clock output	XCOUT	O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$, $\overline{\text{INT1}}$, $\overline{\text{INT3}}$	I	$\overline{\text{INT}}$ interrupt input pins. $\overline{\text{INT0}}$ is timer RB, and RC input pin.
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Key input interrupt input pins
Timer RA	TRAIO	I/O	Timer RA I/O pin
	TRAO	O	Timer RA output pin
Timer RB	TRBO	O	Timer RB output pin
Timer RC	TRCCLK	I	External clock input pin
	TRCTRIG	I	External trigger input pin
	TRCIOA, TRCIOB, TRCIOC, TRCIOD	I/O	Timer RC I/O pins
Serial interface	CLK0, CLK2	I/O	Transfer clock I/O pins
	RXD0, RXD2	I	Serial data input pins
	TXD0, TXD2	O	Serial data output pins
	$\overline{\text{CTS2}}$	I	Transmission control input pin
	RTS2	O	Reception control output pin
	SCL2	I/O	I ² C mode clock I/O pin
	SDA2	I/O	I ² C mode data I/O pin
Reference voltage input	VREF	I	Reference voltage input pin to A/D converter
A/D converter	AN0, AN1, AN5, AN6, AN8 to AN11	I	Analog input pins to A/D converter
	$\overline{\text{ADTRG}}$	I	A/D external trigger input pin
Comparator B	IVCMP1, IVCMP3	I	Comparator B analog voltage input pins
	IVREF1, IVREF3	I	Comparator B reference voltage input pins
I/O port	P0_1, P0_2, P0_6, P0_7, P1_0 to P1_7, P3_3 to P3_5, P3_7, P4_5 to P4_7	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program. All ports can be used as LED drive ports.
Input port	P4_2	I	Input-only port

I: Input O: Output I/O: Input and output

Note:

1. Refer to the oscillator manufacturer for oscillation characteristics.

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.

Interrupts are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.

The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

Table 4.2 SFR Information (2) (1)

Address	Register	Symbol	After Reset
003Ah	Voltage Monitor 2 Circuit Control Register	VW2C	10000010b
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			
0040h			
0041h	Flash Memory Ready Interrupt Control Register	FMRDYIC	XXXXX000b
0042h			
0043h			
0044h			
0045h			
0046h			
0047h	Timer RC Interrupt Control Register	TRCIC	XXXXX000b
0048h			
0049h			
004Ah	Timer RE Interrupt Control Register	TREIC	XXXXX000b
004Bh	UART2 Transmit Interrupt Control Register	S2TIC	XXXXX000b
004Ch	UART2 Receive Interrupt Control Register	S2RIC	XXXXX000b
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh			
0050h			
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h			
0054h			
0055h			
0056h	Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh			
005Ch			
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh	UART2 Bus Collision Detection Interrupt Control Register	U2BCNIC	XXXXX000b
005Fh			
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h	Voltage Monitor 1 Interrupt Control Register	VCMP1IC	XXXXX000b
0073h	Voltage Monitor 2 Interrupt Control Register	VCMP2IC	XXXXX000b
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.3 SFR Information (3) (1)

Address	Register	Symbol	After Reset
0080h			
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h			
0089h			
008Ah			
008Bh			
008Ch			
008Dh			
008Eh			
008Fh			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah			
009Bh			
009Ch			
009Dh			
009Eh			
009Fh			
00A0h	UART0 Transmit / Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit / Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit / Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h	UART2 Transmit / Receive Mode Register	U2MR	00h
00A9h	UART2 Bit Rate Register	U2BRG	XXh
00AAh	UART2 Transmit Buffer Register	U2TB	XXh
00ABh			XXh
00ACh	UART2 Transmit / Receive Control Register 0	U2C0	00001000b
00ADh	UART2 Transmit / Receive Control Register 1	U2C1	00000010b
00AEh	UART2 Receive Buffer Register	U2RB	XXh
00AFh			XXh
00B0h	UART2 Digital Filter Function Select Register	URXDF	00h
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h			
00B9h			
00BAh			
00BBh	UART2 Special Mode Register 5	U2SMR5	00h
00BCh	UART2 Special Mode Register 4	U2SMR4	00h
00BDh	UART2 Special Mode Register 3	U2SMR3	000X0X0Xb
00BEh	UART2 Special Mode Register 2	U2SMR2	X0000000b
00BFh	UART2 Special Mode Register	U2SMR	X0000000b

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.6 SFR Information (6) (1)

Address	Register	Symbol	After Reset
0180h	Timer RA Pin Select Register	TRASR	00h
0181h	Timer RC Pin Select Register	TRBRCSR	00h
0182h	Timer RC Pin Select Register 0	TRCPSR0	00h
0183h	Timer RC Pin Select Register 1	TRCPSR1	00h
0184h			
0185h			
0186h			
0187h			
0188h	UART0 Pin Select Register	U0SR	00h
0189h			
018Ah	UART2 Pin Select Register 0	U2SR0	00h
018Bh	UART2 Pin Select Register 1	U2SR1	00h
018Ch			
018Dh			
018Eh	INT Interrupt Input Pin Select Register	INTSR	00h
018Fh	I/O Function Pin Select Register	PINSR	00h
0190h			
0191h			
0192h			
0193h			
0194h			
0195h			
0196h			
0197h			
0198h			
0199h			
019Ah			
019Bh			
019Ch			
019Dh			
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h	Flash Memory Status Register	FST	10000X00b
01B3h			
01B4h	Flash Memory Control Register 0	FMR0	00h
01B5h	Flash Memory Control Register 1	FMR1	00h
01B6h	Flash Memory Control Register 2	FMR2	00h
01B7h			
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.8 ID Code Areas and Option Function Select Area

Address	Register	Symbol	After Reset
FFDBh	Option Function Select Register 2	OFS2	(Note 1)
FFDFh	ID1		(Note 2)
FFE3h	ID2		(Note 2)
FFEBh	ID3		(Note 2)
FFEFh	ID4		(Note 2)
FFF3h	ID5		(Note 2)
FFF7h	ID6		(Note 2)
FFFBh	ID7		(Note 2)
FFFFh	Option Function Select Register	OFS	(Note 1)

Notes:

1. The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
Do not write additions to the option function select area. If the block including the option function select area is erased, the option function select area is set to FFh.
When blank products are shipped, the option function select area is set to FFh. It is set to the written value after written by the user.
When factory-programming products are shipped, the value of the option function select area is the value programmed by the user.
2. The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
Do not write additions to the ID code areas. If the block including the ID code areas is erased, the ID code areas are set to FFh.
When blank products are shipped, the ID code areas are set to FFh. They are set to the written value after written by the user.
When factory-programming products are shipped, the value of the ID code areas is the value programmed by the user.

Table 5.2 Recommended Operating Conditions

Symbol	Parameter				Conditions	Standard			Unit
						Min.	Typ.	Max.	
Vcc/AVcc	Supply voltage					1.8	–	5.5	V
Vss/AVss	Supply voltage					–	0	–	V
VIH	Input “H” voltage	Other than CMOS input				0.8 Vcc	–	Vcc	V
		CMOS input	Input level switching function (I/O port)	Input level selection : 0.35 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0.5 Vcc	–	Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0.55 Vcc	–	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.65 Vcc	–	Vcc	V
				Input level selection : 0.5 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0.65 Vcc	–	Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0.7 Vcc	–	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.8 Vcc	–	Vcc	V
				Input level selection : 0.7 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0.85 Vcc	–	Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0.85 Vcc	–	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.85 Vcc	–	Vcc	V
		External clock input (XOUT)				1.2	–	Vcc	V
		VIL	Input “L” voltage	Other than CMOS input				0	–
CMOS input	Input level switching function (I/O port)			Input level selection : 0.35 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0	–	0.2 Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0	–	0.2 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	–	0.2 Vcc	V
				Input level selection : 0.5 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0	–	0.4 Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0	–	0.3 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	–	0.2 Vcc	V
				Input level selection : 0.7 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0	–	0.55 Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0	–	0.45 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	–	0.35 Vcc	V
External clock input (XOUT)					0	–	0.4	V	
IOH(sum)	Peak sum output “H” current			Sum of all pins IOH(peak)			–	–	–160
IOH(sum)	Average sum output “H” current		Sum of all pins IOH(avg)			–	–	–80	mA
IOH(peak)	Peak output “H” current		Drive capacity Low			–	–	–10	mA
			Drive capacity High			–	–	–40	mA
IOH(avg)	Average output “H” current		Drive capacity Low			–	–	–5	mA
			Drive capacity High			–	–	–20	mA
IOL(sum)	Peak sum output “L” current		Sum of all pins IOL(peak)			–	–	160	mA
IOL(sum)	Average sum output “L” current		Sum of all pins IOL(avg)			–	–	80	mA
IOL(peak)	Peak output “L” current		Drive capacity Low			–	–	10	mA
			Drive capacity High			–	–	40	mA
IOL(avg)	Average output “L” current		Drive capacity Low			–	–	5	mA
			Drive capacity High			–	–	20	mA
f(XIN)	XIN clock input oscillation frequency				2.7 V ≤ Vcc ≤ 5.5 V	–	–	20	MHz
					1.8 V ≤ Vcc < 2.7 V	–	–	5	MHz
f(XCIN)	XCIN clock input oscillation frequency				1.8 V ≤ Vcc ≤ 5.5 V	–	32.768	50	kHz
fOCO40M	When used as the count source for timer RC ⁽³⁾				2.7 V ≤ Vcc ≤ 5.5 V	32	–	40	MHz
fOCO-F	fOCO-F frequency				2.7 V ≤ Vcc ≤ 5.5 V	–	–	20	MHz
					1.8 V ≤ Vcc < 2.7 V	–	–	5	MHz
–	System clock frequency				2.7 V ≤ Vcc ≤ 5.5 V	–	–	20	MHz
					1.8 V ≤ Vcc < 2.7 V	–	–	5	MHz
f(BCLK)	CPU clock frequency				2.7 V ≤ Vcc ≤ 5.5 V	–	–	20	MHz
					1.8 V ≤ Vcc < 2.7 V	–	–	5	MHz

Notes:

1. V_{CC} = 1.8 to 5.5 V at T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.
3. f_{OCO40M} can be used as the count source for timer RC in the range of V_{CC} = 2.7 V to 5.5 V.

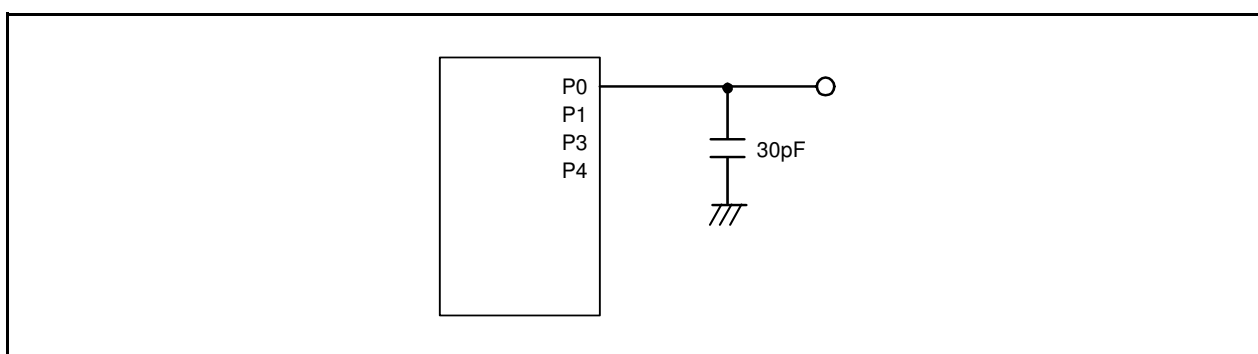


Figure 5.1 Ports P0, P1, P3, P4 Timing Measurement Circuit

Table 5.3 A/D Converter Characteristics

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
–	Resolution		Vref = AVCC		–	–	10	Bit
–	Absolute accuracy	10-bit mode	Vref = AVCC = 5.0 V	AN0, AN1, AN5, AN6, AN8 to AN11 input	–	–	±3	LSB
			Vref = AVCC = 3.3 V	AN0, AN1, AN5, AN6, AN8 to AN11 input	–	–	±5	LSB
			Vref = AVCC = 3.0 V	AN0, AN1, AN5, AN6, AN8 to AN11 input	–	–	±5	LSB
			Vref = AVCC = 2.2 V	AN0, AN1, AN5, AN6, AN8 to AN11 input	–	–	±5	LSB
		8-bit mode	Vref = AVCC = 5.0 V	AN0, AN1, AN5, AN6, AN8 to AN11 input	–	–	±2	LSB
			Vref = AVCC = 3.3 V	AN0, AN1, AN5, AN6, AN8 to AN11 input	–	–	±2	LSB
			Vref = AVCC = 3.0 V	AN0, AN1, AN5, AN6, AN8 to AN11 input	–	–	±2	LSB
			Vref = AVCC = 2.2 V	AN0, AN1, AN5, AN6, AN8 to AN11 input	–	–	±2	LSB
φAD	A/D conversion clock		4.0 ≤ Vref = AVCC ≤ 5.5 V (2)		2	–	20	MHz
			3.2 ≤ Vref = AVCC ≤ 5.5 V (2)		2	–	16	MHz
			2.7 ≤ Vref = AVCC ≤ 5.5 V (2)		2	–	10	MHz
			2.2 ≤ Vref = AVCC ≤ 5.5 V (2)		2	–	5	MHz
–	Tolerance level impedance				–	3	–	kΩ
tCONV	Conversion time	10-bit mode	Vref = AVCC = 5.0 V, φAD = 20 MHz		2.15	–	–	μs
		8-bit mode	Vref = AVCC = 5.0 V, φAD = 20 MHz		2.15	–	–	μs
tsAMP	Sampling time		φAD = 20 MHz		0.75	–	–	μs
IVref	Vref current		Vcc = 5 V, XIN = f1 = φAD = 20 MHz		–	45	–	μA
Vref	Reference voltage				2.2	–	AVcc	V
VIA	Analog input voltage (3)				0	–	Vref	V
OCVREF	On-chip reference voltage		2 MHz ≤ φAD ≤ 4 MHz		1.19	1.34	1.49	V

Notes:

- $V_{CC}/AV_{CC} = V_{ref} = 2.2$ to 5.5 V , $V_{SS} = 0\text{ V}$ at $T_{opr} = -20$ to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
- The A/D conversion result will be undefined in wait mode, stop mode, when the flash memory stops, and in low-current-consumption mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.
- When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 5.4 Comparator B Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{ref}	IVREF1, IVREF3 input reference voltage		0	—	$V_{CC} - 1.4$	V
V_I	IVCMP1, IVCMP3 input voltage		-0.3	—	$V_{CC} + 0.3$	V
—	Offset		—	5	100	mV
t_d	Comparator output delay time ⁽²⁾	$V_I = V_{ref} \pm 100\text{ mV}$	—	0.1	—	μs
I_{CMP}	Comparator operating current	$V_{CC} = 5.0\text{ V}$	—	17.5	—	μA

Notes:

- $V_{CC} = 2.7$ to 5.5 V , $T_{opr} = -20$ to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
- When the digital filter is disabled.

Table 5.5 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance ⁽²⁾		1,000 ⁽³⁾	—	—	times
—	Byte program time		—	80	500	μs
—	Block erase time		—	0.3	—	s
t _d (SR-SUS)	Time delay from suspend request until suspend		—	—	5+CPU clock × 3 cycles	ms
—	Interval from erase start/restart until following suspend request		0	—	—	μs
—	Time from suspend until erase restart		—	—	30+CPU clock × 1 cycle	μs
t _d (CMDRST-READY)	Time from when command is forcibly stopped until reading is enabled		—	—	30+CPU clock × 1 cycle	μs
—	Program, erase voltage		2.7	—	5.5	V
—	Read voltage		1.8	—	5.5	V
—	Program, erase temperature		0	—	60	°C
—	Data hold time ⁽⁷⁾	Ambient temperature = 55°C	20	—	—	year

Notes:

1. V_{CC} = 2.7 to 5.5 V at T_{opr} = 0 to 60°C, unless otherwise specified.
2. Definition of programming/erasure endurance
The programming and erasure endurance is defined on a per-block basis.
If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

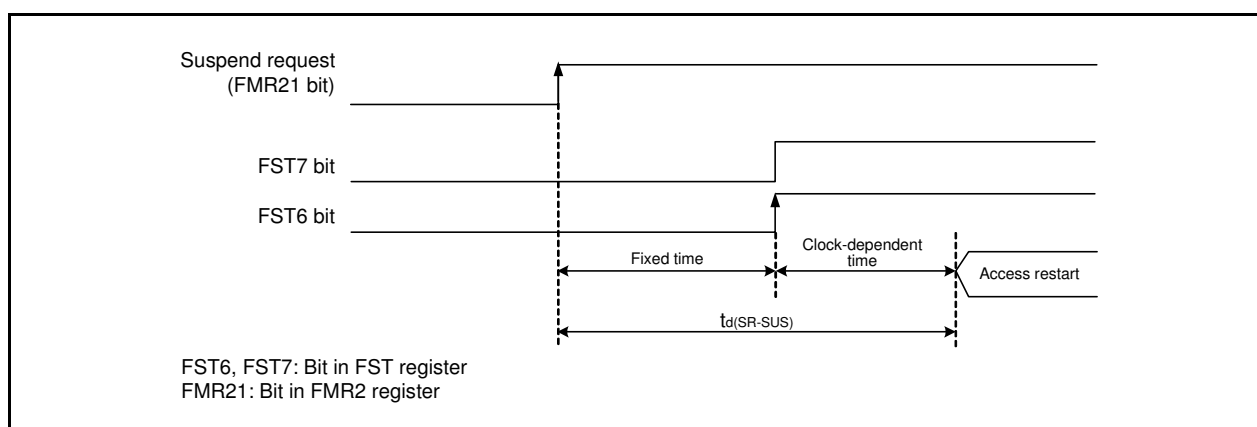
**Figure 5.2 Time delay until Suspend**

Table 5.6 Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V _{det0}	Voltage detection level V _{det0_0} (2)		1.80	1.90	2.05	V
	Voltage detection level V _{det0_1} (2)		2.15	2.35	2.50	V
	Voltage detection level V _{det0_2} (2)		2.70	2.85	3.05	V
	Voltage detection level V _{det0_3} (2)		3.55	3.80	4.05	V
–	Voltage detection 0 circuit response time (4)	At the falling of V _{CC} from 5 V to (V _{det0_0} – 0.1) V	–	6	150	μs
–	Voltage detection circuit self power consumption	VCA25 = 1, V _{CC} = 5.0 V	–	1.5	–	μA
t _{d(E-A)}	Waiting time until voltage detection circuit operation starts (3)		–	–	100	μs

Notes:

1. The measurement condition is V_{CC} = 1.8 V to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.
4. Time until the voltage monitor 0 reset is generated after the voltage passes V_{det0}.

Table 5.7 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V _{det1}	Voltage detection level V _{det1_0} (2)	At the falling of V _{CC}	2.00	2.20	2.40	V
	Voltage detection level V _{det1_1} (2)	At the falling of V _{CC}	2.15	2.35	2.55	V
	Voltage detection level V _{det1_2} (2)	At the falling of V _{CC}	2.30	2.50	2.70	V
	Voltage detection level V _{det1_3} (2)	At the falling of V _{CC}	2.45	2.65	2.85	V
	Voltage detection level V _{det1_4} (2)	At the falling of V _{CC}	2.60	2.80	3.00	V
	Voltage detection level V _{det1_5} (2)	At the falling of V _{CC}	2.75	2.95	3.15	V
	Voltage detection level V _{det1_6} (2)	At the falling of V _{CC}	2.85	3.10	3.40	V
	Voltage detection level V _{det1_7} (2)	At the falling of V _{CC}	3.00	3.25	3.55	V
	Voltage detection level V _{det1_8} (2)	At the falling of V _{CC}	3.15	3.40	3.70	V
	Voltage detection level V _{det1_9} (2)	At the falling of V _{CC}	3.30	3.55	3.85	V
	Voltage detection level V _{det1_A} (2)	At the falling of V _{CC}	3.45	3.70	4.00	V
	Voltage detection level V _{det1_B} (2)	At the falling of V _{CC}	3.60	3.85	4.15	V
	Voltage detection level V _{det1_C} (2)	At the falling of V _{CC}	3.75	4.00	4.30	V
	Voltage detection level V _{det1_D} (2)	At the falling of V _{CC}	3.90	4.15	4.45	V
	Voltage detection level V _{det1_E} (2)	At the falling of V _{CC}	4.05	4.30	4.60	V
	Voltage detection level V _{det1_F} (2)	At the falling of V _{CC}	4.20	4.45	4.75	V
–	Hysteresis width at the rising of V _{CC} in voltage detection 1 circuit	V _{det1_0} to V _{det1_5} selected	–	0.07	–	V
		V _{det1_6} to V _{det1_F} selected	–	0.10	–	V
–	Voltage detection 1 circuit response time (3)	At the falling of V _{CC} from 5 V to (V _{det1_0} – 0.1) V	–	60	150	μs
–	Voltage detection circuit self power consumption	VCA26 = 1, V _{CC} = 5.0 V	–	1.7	–	μA
t _{d(E-A)}	Waiting time until voltage detection circuit operation starts (4)		–	–	100	μs

Notes:

1. The measurement condition is V_{CC} = 1.8 V to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
3. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
4. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Table 5.13 Electrical Characteristics (1) [4.2 V ≤ V_{CC} ≤ 5.5 V]

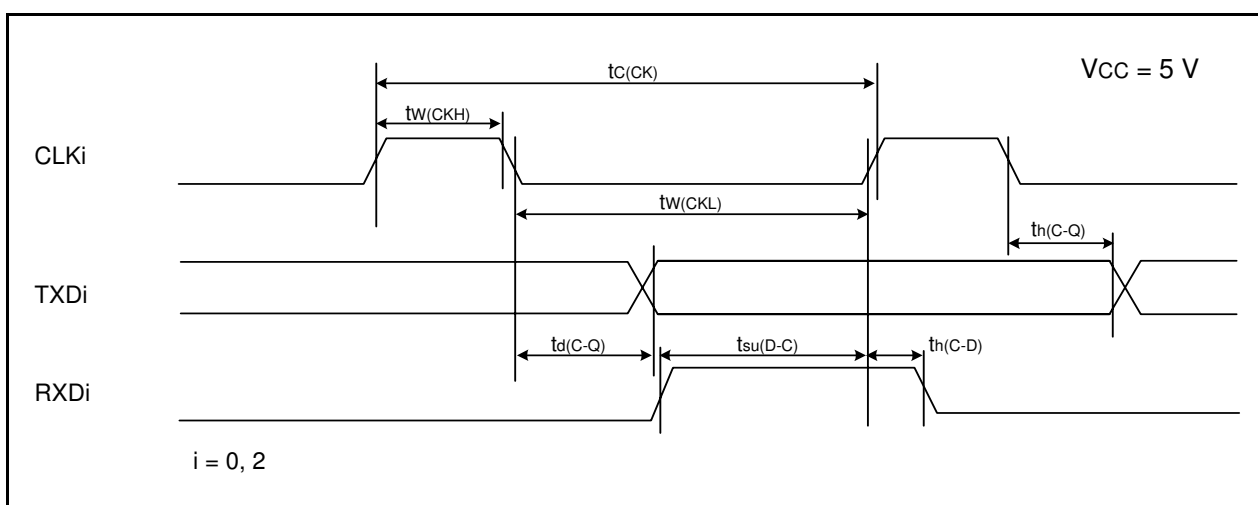
Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V _{OH}	Output "H" voltage	Other than XOUT	Drive capacity High V _{CC} = 5V	I _{OH} = -20 mA	V _{CC} - 2.0	—	V _{CC}	V
			Drive capacity Low V _{CC} = 5V	I _{OH} = -5 mA	V _{CC} - 2.0	—	V _{CC}	V
		XOUT	V _{CC} = 5V	I _{OH} = -200 μA	1.0	—	V _{CC}	V
V _{OL}	Output "L" voltage	Other than XOUT	Drive capacity High V _{CC} = 5V	I _{OL} = 20 mA	—	—	2.0	V
			Drive capacity Low V _{CC} = 5V	I _{OL} = 5 mA	—	—	2.0	V
		XOUT	V _{CC} = 5V	I _{OL} = 200 μA	—	—	0.5	V
V _{T+} -V _{T-}	Hysteresis	INT0, INT1, INT3, KI0, KI1, KI2, KI3, TRAIO, TRBO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRCTRG, TRCCLK, ADTRG, RXD0, RXD2, CLK0, CLK2			0.1	1.2	—	V
		RESET			0.1	1.2	—	V
I _{IH}	Input "H" current		V _I = 5 V, V _{CC} = 5.0V		—	—	5.0	μA
I _{IL}	Input "L" current		V _I = 0 V, V _{CC} = 5.0V		—	—	-5.0	μA
R _{PULLUP}	Pull-up resistance		V _I = 0 V, V _{CC} = 5.0V		25	50	100	kΩ
R _{IXIN}	Feedback resistance	XIN			—	0.3	—	MΩ
R _{IXCIN}	Feedback resistance	XCIN			—	8	—	MΩ
V _{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

Note:

1. 4.2 V ≤ V_{CC} ≤ 5.5 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 20 MHz, unless otherwise specified.

Table 5.17 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200	—	ns
$t_{w(CKH)}$	CLKi input "H" width	100	—	ns
$t_{w(CKL)}$	CLKi input "L" width	100	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	50	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

 $i = 0, 2$ **Figure 5.6 Serial Interface Timing Diagram when Vcc = 5 V****Table 5.18 External Interrupt $\overline{INTi}$ ($i = 0, 1, 3$) Input, Key Input Interrupt $\overline{Kli}$ ($i = 0$ to 3)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input "H" width, $\overline{Kli}$ input "H" width	250 ⁽¹⁾	—	ns
$t_{w(INL)}$	$\overline{INTi}$ input "L" width, $\overline{Kli}$ input "L" width	250 ⁽²⁾	—	ns

Notes:

1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency $\times$ 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency $\times$ 3) or the minimum value of standard, whichever is greater.

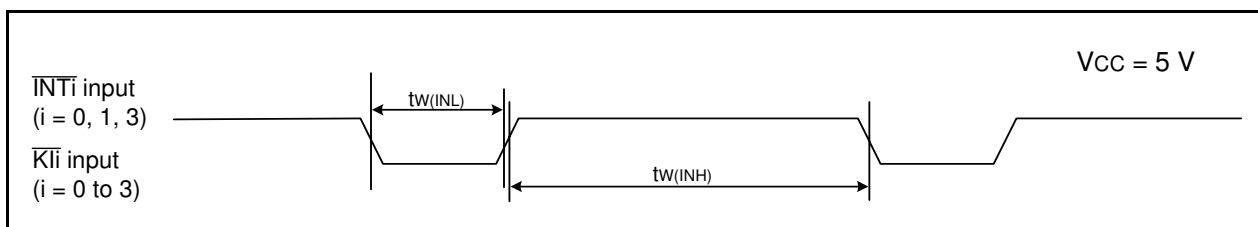
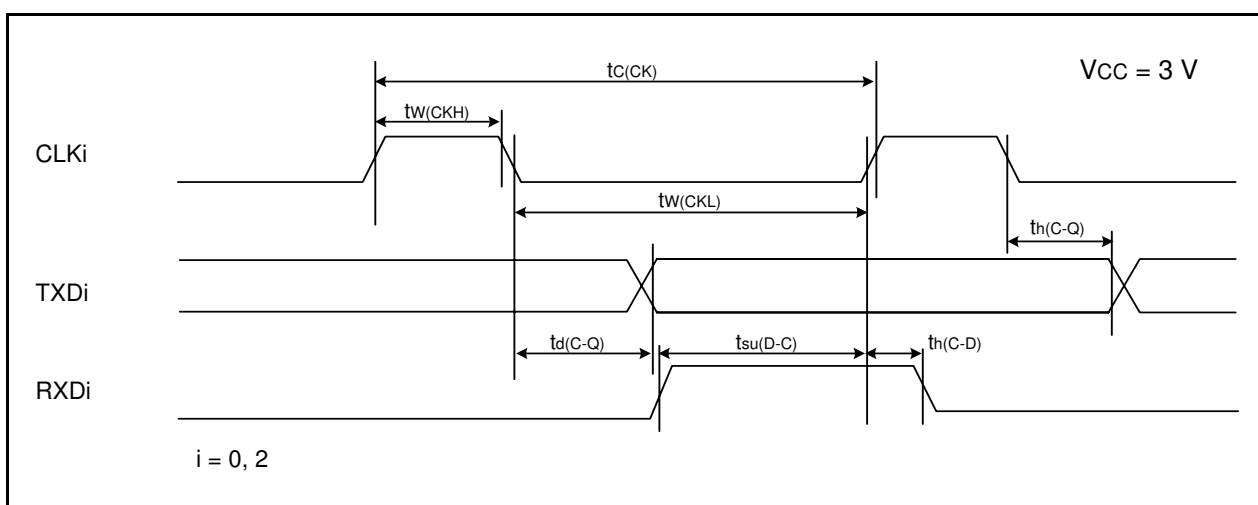
**Figure 5.7 Input Timing for External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{Kli}$ when Vcc = 5 V**

Table 5.20 Electrical Characteristics (4) [$2.7\text{ V} \leq V_{CC} < 3.3\text{ V}$]
($T_{opr} = -20\text{ to }85^{\circ}\text{C}$ (N version) / $-40\text{ to }85^{\circ}\text{C}$ (D version), unless otherwise specified.)

Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	3.5	10	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	1.5	7.5	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	—	7.0	15	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	3.0	—	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	—	4.0	—	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	1.5	—	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-16 MSTTRC = 1	—	1	—	mA
			Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	—	90	390
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division FMR27 = 1, VCA20 = 0	—	80	400	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division	—	40	—	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz Program operation on RAM Flash memory off, FMSTP = 1, VCA20 = 0	—	40	—	μA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	15	90	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	4	80	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (peripheral clock off) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	3.5	—	μA
			Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	2.0	5.0
				XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	5.0	—

Table 5.23 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300	—	ns
$t_{w(CKH)}$	CLKi input "H" width	150	—	ns
$t_{w(CKL)}$	CLKi Input "L" width	150	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	70	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

 $i = 0, 2$ **Figure 5.10 Serial Interface Timing Diagram when Vcc = 3 V****Table 5.24 External Interrupt $\overline{INTi}$ ($i = 0, 1, 3$) Input, Key Input Interrupt $\overline{Kli}$ ($i = 0$ to 3)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input "H" width, $\overline{Kli}$ input "H" width	380 (1)	—	ns
$t_{w(INL)}$	$\overline{INTi}$ input "L" width, $\overline{Kli}$ input "L" width	380 (2)	—	ns

Notes:

1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency $\times$ 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency $\times$ 3) or the minimum value of standard, whichever is greater.

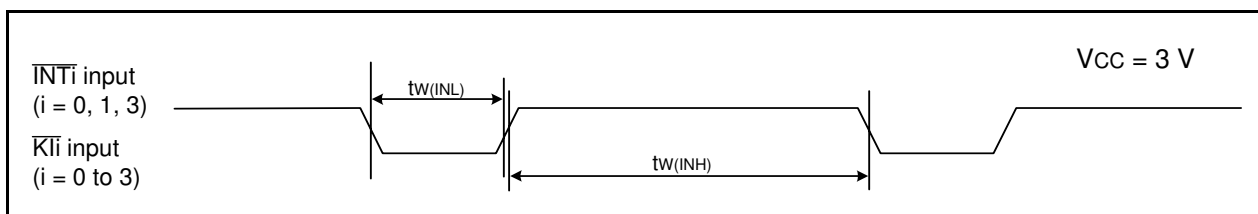
**Figure 5.11 Input Timing for External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{Kli}$ when Vcc = 3 V**

Table 5.25 Electrical Characteristics (5) [$1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V _{OH}	Output "H" voltage	Other than XOUT	Drive capacity High	I _{OH} = -2 mA	V _{CC} - 0.5	—	V _{CC}	V
			Drive capacity Low	I _{OH} = -1 mA	V _{CC} - 0.5	—	V _{CC}	V
		XOUT		I _{OH} = -200 μ A	1.0	—	V _{CC}	V
V _{OL}	Output "L" voltage	Other than XOUT	Drive capacity High	I _{OL} = 2 mA	—	—	0.5	V
			Drive capacity Low	I _{OL} = 1 mA	—	—	0.5	V
		XOUT		I _{OL} = 200 μ A	—	—	0.5	V
V _{T+} -V _{T-}	Hysteresis	INT0, INT1, INT3, KI0, KI1, KI2, KI3, TRAIO, TRBO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRCTRG, TRCCLK, ADTRG, RXD0, RXD2, CLK0, CLK2			0.05	0.2	—	V
		RESET			0.05	0.20	—	V
I _{IH}	Input "H" current		V _I = 2.2 V, V _{CC} = 2.2 V		—	—	4.0	μ A
I _{IL}	Input "L" current		V _I = 0 V, V _{CC} = 2.2 V		—	—	-4.0	μ A
R _{PULLUP}	Pull-up resistance		V _I = 0 V, V _{CC} = 2.2 V		70	140	300	k Ω
R _{IXIN}	Feedback resistance	XIN			—	0.3	—	M Ω
R _{IXCIN}	Feedback resistance	XCIN			—	8	—	M Ω
V _{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

Note:

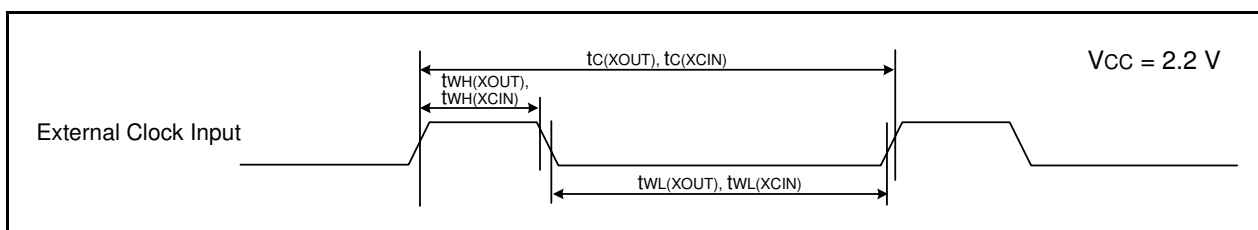
1. $1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$ at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 5 MHz, unless otherwise specified.

Table 5.26 Electrical Characteristics (6) [$1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$]
($T_{opr} = -20\text{ to }85^{\circ}\text{C}$ (N version) / $-40\text{ to }85^{\circ}\text{C}$ (D version), unless otherwise specified.)

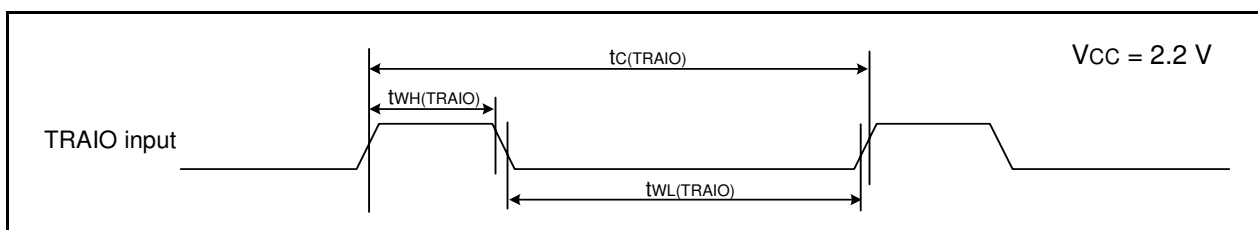
Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
I _{CC}	Power supply current ($V_{CC} = 1.8\text{ to }2.7\text{ V}$) Single-chip mode, output pins are open, other pins are V _{SS}	High-speed clock mode	—	2.2	—	mA
				0.8	—	mA
		High-speed on-chip oscillator mode	—	2.5	10	mA
			—	1.7	—	mA
			—	1	—	mA
		Low-speed on-chip oscillator mode	—	90	300	μA
			—	80	350	μA
		Low-speed clock mode	—	40	—	μA
			—	—	—	μA
		Wait mode	—	15	90	μA
			—	4	80	μA
			—	3.5	—	μA
		Stop mode	—	2.0	5	μA
			—	5.0	—	μA

Timing Requirements (Unless Otherwise Specified: $V_{CC} = 2.2\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{opr} = 25^{\circ}\text{C}$)**Table 5.27 External clock input (XOUT, XCIN)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_c(\text{XOUT})$	XOUT input cycle time	200	—	ns
$t_{WH}(\text{XOUT})$	XOUT input "H" width	90	—	ns
$t_{WL}(\text{XOUT})$	XOUT input "L" width	90	—	ns
$t_c(\text{XCIN})$	XCIN input cycle time	14	—	μs
$t_{WH}(\text{XCIN})$	XCIN input "H" width	7	—	μs
$t_{WL}(\text{XCIN})$	XCIN input "L" width	7	—	μs

**Figure 5.12 External Clock Input Timing Diagram when $V_{CC} = 2.2\text{ V}$** **Table 5.28 TRAIO Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_c(\text{TRAIO})$	TRAIO input cycle time	500	—	ns
$t_{WH}(\text{TRAIO})$	TRAIO input "H" width	200	—	ns
$t_{WL}(\text{TRAIO})$	TRAIO input "L" width	200	—	ns

**Figure 5.13 TRAIO Input Timing Diagram when $V_{CC} = 2.2\text{ V}$**

Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Technology website.

