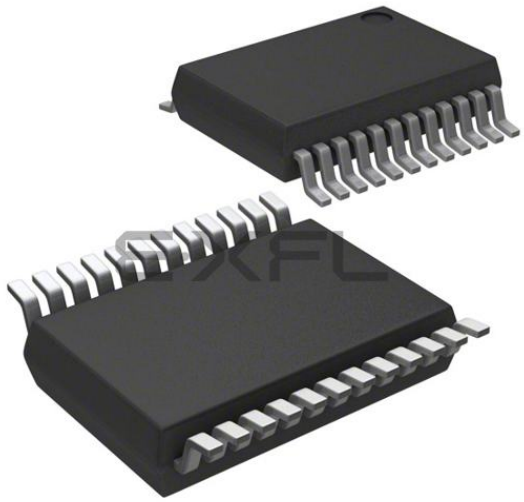

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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | R8C |
| Core Size | 16-Bit |
| Speed | 20MHz |
| Connectivity | I²C, UART/USART |
| Peripherals | POR, PWM, Voltage Detect, WDT |
| Number of I/O | 19 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 1K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.5V |
| Data Converters | A/D 8x10b |
| Oscillator Type | Internal |
| Operating Temperature | -20°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 24-LSSOP (0.220", 5.60mm Width) |
| Supplier Device Package | 24-LSSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f213g6dnsp-u0 |

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# 1. Overview

## 1.1 Features

The R8C/3GD Group of single-chip MCUs incorporates the R8C CPU core, employing sophisticated instructions for a high level of efficiency. With 1 Mbyte of address space, and it is capable of executing instructions at high speed. In addition, the CPU core boasts a multiplier for high-speed operation processing.
Power consumption is low, and the supported operating modes allow additional power control. These MCUs are designed to maximize EMI/EMS performance.
Integration of many peripheral functions, including multifunction timer and serial interface, reduces the number of system components.

### 1.1.1 Applications

Electronic household appliances, office equipment, audio equipment, consumer equipment, etc.

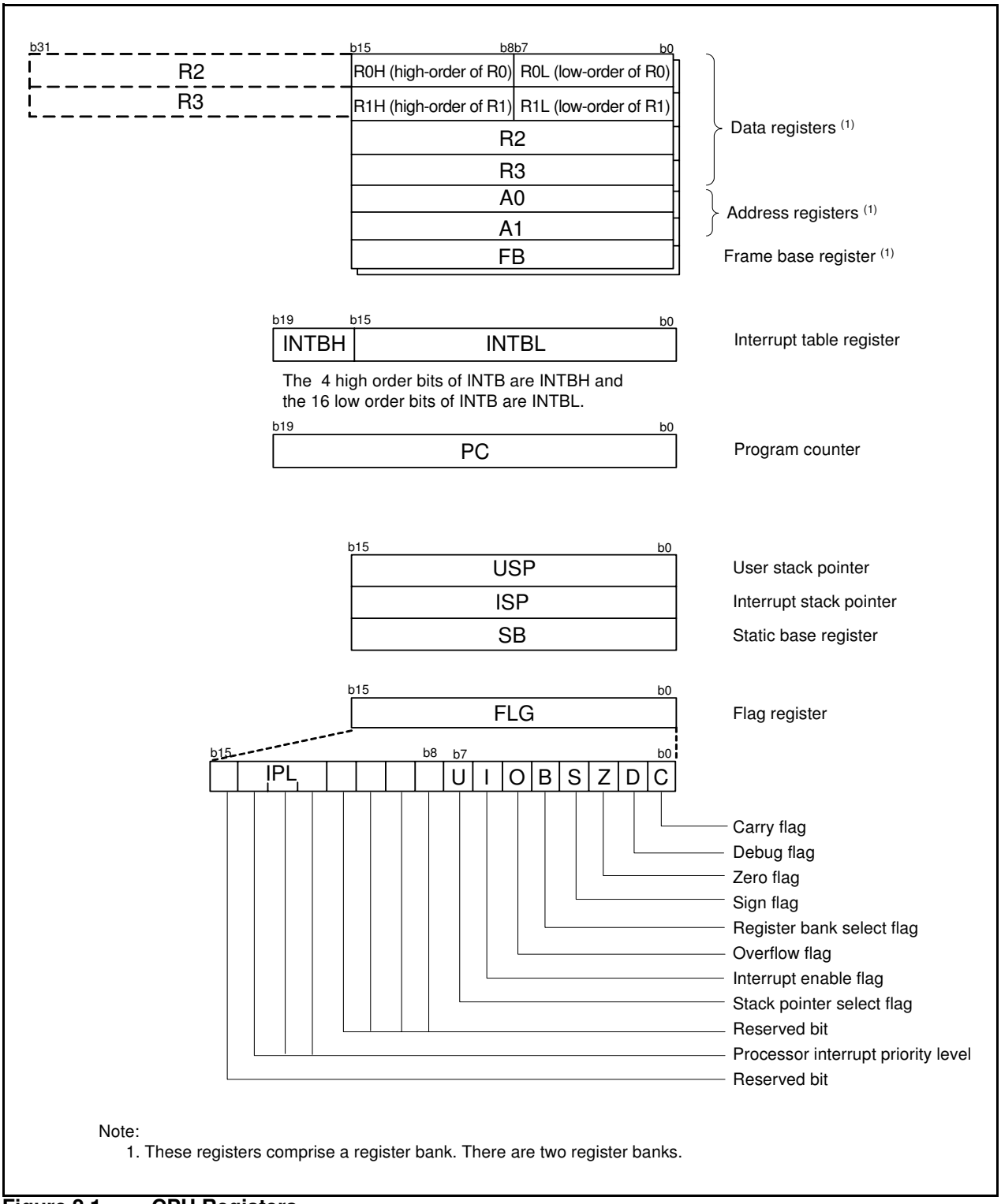
**Table 1.4 Pin Name Information by Pin Number**

| Pin Number | Control Pin | Port | I/O Pin Functions for Peripheral Modules | | | |
|---|---|---|---|---|---|---|
| | | | Interrupt | Timer | Serial Interface | A/D Converter, Comparator B |
| 1 | | P0_2 | | (TRCIOA/TRCTRG) | | AN5 |
| 2 | | P0_1 | | (TRCIOA/TRCTRG) | | AN6 |
| 3 | | P4_2 | | | | VREF |
| 4 | MODE | | | | | |
| 5 | $\overline{\text{RESET}}$ | | | | | |
| 6 | XOUT(/XCOUT) | P4_7 | | | | |
| 7 | VSS/AVSS | | | | | |
| 8 | XIN(/XCIN) | P4_6 | | | | |
| 9 | VCC/AVCC | | | | | |
| 10 | | P3_7 | | TRAO | (RXD2/SCL2/ TXD2/SDA2) | |
| 11 | | P3_5 | | (TRCIOD) | (CLK2) | |
| 12 | | P3_4 | | (TRCIOC) | (RXD2/SCL2/ TXD2/SDA2) | IVREF3 |
| 13 | | P3_3 | $\overline{\text{INT3}}$ | (TRCCLK) | ($\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$) | IVCMP3 |
| 14 | | P4_5 | $\overline{\text{INT0}}$ | | (RXD2/SCL2) | $\overline{\text{ADTRG}}$ |
| 15 | | P1_7 | $\overline{\text{INT1}}$ | (TRAIO) | | IVCMP1 |
| 16 | | P1_6 | | | (CLK0) | IVREF1 |
| 17 | | P1_5 | ($\overline{\text{INT1}}$) | (TRAIO) | (RXD0) | |
| 18 | | P1_4 | | (TRCCLK) | (TXD0) | |
| 19 | | P1_3 | $\overline{\text{KI3}}$ | TRBO(/TRCIOC) | | AN11 |
| 20 | | P1_2 | $\overline{\text{KI2}}$ | (TRCIOB) | | AN10 |
| 21 | | P1_1 | $\overline{\text{KI1}}$ | (TRCIOA/TRCTRG) | | AN9 |
| 22 | | P1_0 | $\overline{\text{KI0}}$ | (TRCIOD) | | AN8 |
| 23 | | P0_7 | | (TRCIOC) | | AN0 |
| 24 | | P0_6 | | (TRCIOD) | | AN1 |

Note:
1. Can be assigned to the pin in parentheses by a program.

# 2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.




Note:
1. These registers comprise a register bank. There are two register banks.

**Figure 2.1 CPU Registers**

## 2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

## 2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

## 2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

## 2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the starting address of an interrupt vector table.

## 2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

## 2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

## 2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

## 2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

### 2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

### 2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

### 2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

### 2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

### 2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

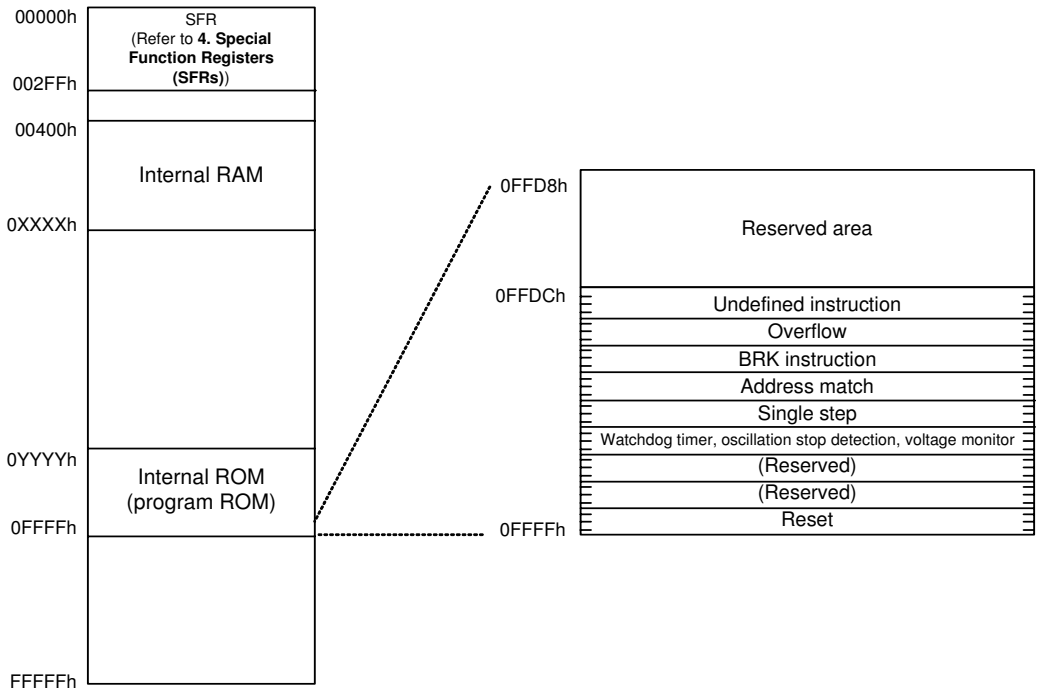
### 2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

# 3. Memory

## 3.1 R8C/3GD Group

Figure 3.1 is a Memory Map of R8C/3GD Group. The R8C/3GD Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 16-Kbyte internal ROM area is allocated addresses 0C000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 1-Kbyte internal RAM area is allocated addresses 00400h to 007FFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh. Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.




Note:
1. The blank areas are reserved and cannot be accessed by users.

| Part Number | Internal ROM | | Internal RAM | |
|---|---|---|---|---|
| | Size | Address 0YYYYh | Size | Address 0XXXXh |
| R5F213G1DNSP, R5F213G1DDSP | 4 Kbytes | 0F000h | 1 Kbyte | 007FFh |
| R5F213G2DNSP, R5F213G2DDSP | 8 Kbytes | 0E000h | 1 Kbyte | 007FFh |
| R5F213G4DNSP, R5F213G4DDSP | 16 Kbytes | 0C000h | 1 Kbyte | 007FFh |
| R5F213G5DNSP, R5F213G5DDSP | 24 Kbytes | 0A000h | 1 Kbyte | 007FFh |
| R5F213G6DNSP, R5F213G6DDSP | 32 Kbytes | 08000h | 1 Kbyte | 007FFh |

**Figure 3.1 Memory Map of R8C/3GD Group**

# 4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.7 list the special function registers and Table 4.8 lists the ID Code Areas and Option Function Select Area.

**Table 4.1 SFR Information (1) (1)**

| Address | Register | Symbol | After Reset |
|---|---|---|---|
| 0000h | | | |
| 0001h | | | |
| 0002h | | | |
| 0003h | | | |
| 0004h | Processor Mode Register 0 | PM0 | 00h |
| 0005h | Processor Mode Register 1 | PM1 | 00h |
| 0006h | System Clock Control Register 0 | CM0 | 00101000b |
| 0007h | System Clock Control Register 1 | CM1 | 00100000b |
| 0008h | Module Standby Control Register | MSTCR | 00h |
| 0009h | System Clock Control Register 3 | CM3 | 00h |
| 000Ah | Protect Register | PRCR | 00h |
| 000Bh | Reset Source Determination Register | RSTFR | 0XXXXXXXb (2) |
| 000Ch | Oscillation Stop Detection Register | OCD | 00000100b |
| 000Dh | Watchdog Timer Reset Register | WDTR | XXh |
| 000Eh | Watchdog Timer Start Register | WDTS | XXh |
| 000Fh | Watchdog Timer Control Register | WDTC | 00111111b |
| 0010h | | | |
| 0011h | | | |
| 0012h | | | |
| 0013h | | | |
| 0014h | | | |
| 0015h | High-Speed On-Chip Oscillator Control Register 7 | FRA7 | When shipping |
| 0016h | | | |
| 0017h | | | |
| 0018h | | | |
| 0019h | | | |
| 001Ah | | | |
| 001Bh | | | |
| 001Ch | Count Source Protection Mode Register | CSPR | 00h<br>10000000b (3) |
| 001Dh | | | |
| 001Eh | | | |
| 001Fh | | | |
| 0020h | | | |
| 0021h | | | |
| 0022h | | | |
| 0023h | High-Speed On-Chip Oscillator Control Register 0 | FRA0 | 00h |
| 0024h | High-Speed On-Chip Oscillator Control Register 1 | FRA1 | When shipping |
| 0025h | High-Speed On-Chip Oscillator Control Register 2 | FRA2 | 00h |
| 0026h | On-Chip Reference Voltage Control Register | OCVREFCR | 00h |
| 0027h | | | |
| 0028h | Clock Prescaler Reset Flag | CPSRF | 00h |
| 0029h | High-Speed On-Chip Oscillator Control Register 4 | FRA4 | When Shipping |
| 002Ah | High-Speed On-Chip Oscillator Control Register 5 | FRA5 | When Shipping |
| 002Bh | High-Speed On-Chip Oscillator Control Register 6 | FRA6 | When Shipping |
| 002Ch | | | |
| 002Dh | | | |
| 002Eh | | | |
| 002Fh | High-Speed On-Chip Oscillator Control Register 3 | FRA3 | When shipping |
| 0030h | Voltage Monitor Circuit Control Register | CMPA | 00h |
| 0031h | Voltage Monitor Circuit Edge Select Register | VCAC | 00h |
| 0032h | | | |
| 0033h | Voltage Detect Register 1 | VCA1 | 00001000b |
| 0034h | Voltage Detect Register 2 | VCA2 | 00h (4)<br>00100000b (5) |
| 0035h | | | |
| 0036h | Voltage Detection 1 Level Select Register | VD1LS | 00000111b |
| 0037h | | | |
| 0038h | Voltage Monitor 0 Circuit Control Register | VW0C | 1100X010b (4)<br>1100X011b (5) |
| 0039h | Voltage Monitor 1 Circuit Control Register | VW1C | 10001010b |

X: Undefined

Notes:
1. The blank areas are reserved and cannot be accessed by users.
2. The CWR bit in the RSTFR register is set to 0 after power-on and voltage monitor 0 reset. Hardware reset, software reset, or watchdog timer reset does not affect this bit.
3. The CSPROINI bit in the OFS register is set to 0.
4. The LVDAS bit in the OFS register is set to 1.
5. The LVDAS bit in the OFS register is set to 0.

**Table 4.6 SFR Information (6) (1)**

| Address | Register | Symbol | After Reset |
|---|---|---|---|
| 0180h | Timer RA Pin Select Register | TRASR | 00h |
| 0181h | Timer RC Pin Select Register | TRBRCSR | 00h |
| 0182h | Timer RC Pin Select Register 0 | TRCPSR0 | 00h |
| 0183h | Timer RC Pin Select Register 1 | TRCPSR1 | 00h |
| 0184h | | | |
| 0185h | | | |
| 0186h | | | |
| 0187h | | | |
| 0188h | UART0 Pin Select Register | U0SR | 00h |
| 0189h | | | |
| 018Ah | UART2 Pin Select Register 0 | U2SR0 | 00h |
| 018Bh | UART2 Pin Select Register 1 | U2SR1 | 00h |
| 018Ch | | | |
| 018Dh | | | |
| 018Eh | INT Interrupt Input Pin Select Register | INTSR | 00h |
| 018Fh | I/O Function Pin Select Register | PINSR | 00h |
| 0190h | | | |
| 0191h | | | |
| 0192h | | | |
| 0193h | | | |
| 0194h | | | |
| 0195h | | | |
| 0196h | | | |
| 0197h | | | |
| 0198h | | | |
| 0199h | | | |
| 019Ah | | | |
| 019Bh | | | |
| 019Ch | | | |
| 019Dh | | | |
| 019Eh | | | |
| 019Fh | | | |
| 01A0h | | | |
| 01A1h | | | |
| 01A2h | | | |
| 01A3h | | | |
| 01A4h | | | |
| 01A5h | | | |
| 01A6h | | | |
| 01A7h | | | |
| 01A8h | | | |
| 01A9h | | | |
| 01AAh | | | |
| 01ABh | | | |
| 01ACh | | | |
| 01ADh | | | |
| 01AEh | | | |
| 01AFh | | | |
| 01B0h | | | |
| 01B1h | | | |
| 01B2h | Flash Memory Status Register | FST | 10000X00b |
| 01B3h | | | |
| 01B4h | Flash Memory Control Register 0 | FMR0 | 00h |
| 01B5h | Flash Memory Control Register 1 | FMR1 | 00h |
| 01B6h | Flash Memory Control Register 2 | FMR2 | 00h |
| 01B7h | | | |
| 01B8h | | | |
| 01B9h | | | |
| 01BAh | | | |
| 01BBh | | | |
| 01BCh | | | |
| 01BDh | | | |
| 01BEh | | | |
| 01BFh | | | |

X: Undefined
Note:
1. The blank areas are reserved and cannot be accessed by users.

**Table 4.7 SFR Information (7) (1)**

| Address | Register | Symbol | After Reset |
|---|---|---|---|
| 01C0h | Address Match Interrupt Register 0 | RMAD0 | XXh |
| 01C1h | | | XXh |
| 01C2h | | | 0000XXXXb |
| 01C3h | Address Match Interrupt Enable Register | AIER | 00h |
| 01C4h | Address Match Interrupt Register 1 | RMAD1 | XXh |
| 01C5h | | | XXh |
| 01C6h | | | 0000XXXXb |
| 01C7h | | | |
| 01C8h | | | |
| 01C9h | | | |
| 01CAh | | | |
| 01CBh | | | |
| 01CCh | | | |
| 01CDh | | | |
| 01CEh | | | |
| 01CFh | | | |
| 01D0h | | | |
| 01D1h | | | |
| 01D2h | | | |
| 01D3h | | | |
| 01D4h | | | |
| 01D5h | | | |
| 01D6h | | | |
| 01D7h | | | |
| 01D8h | | | |
| 01D9h | | | |
| 01DAh | | | |
| 01DBh | | | |
| 01DCh | | | |
| 01DDh | | | |
| 01DEh | | | |
| 01DFh | | | |
| 01E0h | Pull-Up Control Register 0 | PUR0 | 00h |
| 01E1h | Pull-Up Control Register 1 | PUR1 | 00h |
| 01E2h | | | |
| 01E3h | | | |
| 01E4h | | | |
| 01E5h | | | |
| 01E6h | | | |
| 01E7h | | | |
| 01E8h | | | |
| 01E9h | | | |
| 01EAh | | | |
| 01EBh | | | |
| 01ECh | | | |
| 01EDh | | | |
| 01EEh | | | |
| 01EFh | | | |
| 01F0h | Port P1 Drive Capacity Control Register | P1DRR | 00h |
| 01F1h | | | |
| 01F2h | Drive Capacity Control Register 0 | DRR0 | 00h |
| 01F3h | Drive Capacity Control Register 1 | DRR1 | 00h |
| 01F4h | | | |
| 01F5h | Input Threshold Control Register 0 | VLT0 | 00h |
| 01F6h | Input Threshold Control Register 1 | VLT1 | 00h |
| 01F7h | | | |
| 01F8h | Comparator B Control Register 0 | INTCMP | 00h |
| 01F9h | | | |
| 01FAh | External Input Enable Register 0 | INTEN | 00h |
| 01FBh | | | |
| 01FCh | INT Input Filter Select Register 0 | INTF | 00h |
| 01FDh | | | |
| 01FEh | Key Input Enable Register 0 | KIEN | 00h |
| 01FFh | | | |

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

**Table 4.8 ID Code Areas and Option Function Select Area**

| Address | Register | Symbol | After Reset |
|---|---|---|---|
| : | | | |
| FFDBh | Option Function Select Register 2 | OFS2 | (Note 1) |
| : | | | |
| FFDFh | ID1 | | (Note 2) |
| : | | | |
| FFE3h | ID2 | | (Note 2) |
| : | | | |
| FFEBh | ID3 | | (Note 2) |
| : | | | |
| FFEFh | ID4 | | (Note 2) |
| : | | | |
| FFF3h | ID5 | | (Note 2) |
| : | | | |
| FFF7h | ID6 | | (Note 2) |
| : | | | |
| FFFBh | ID7 | | (Note 2) |
| : | | | |
| FFFFh | Option Function Select Register | OFS | (Note 1) |

Notes:
1. The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
Do not write additions to the option function select area. If the block including the option function select area is erased, the option function select area is set to FFh.
When blank products are shipped, the option function select area is set to FFh. It is set to the written value after written by the user.
When factory-programming products are shipped, the value of the option function select area is the value programmed by the user.
2. The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
Do not write additions to the ID code areas. If the block including the ID code areas is erased, the ID code areas are set to FFh.
When blank products are shipped, the ID code areas are set to FFh. They are set to the written value after written by the user.
When factory-programming products are shipped, the value of the ID code areas is the value programmed by the user.

**Table 5.2 Recommended Operating Conditions**

| Symbol | Parameter | | | | Conditions | Standard | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min. | Typ. | Max. | |
| $V_{CC}$/$AV_{CC}$ | Supply voltage | | | | | 1.8 | – | 5.5 | V |
| $V_{SS}$/$AV_{SS}$ | Supply voltage | | | | | – | 0 | – | V |
| $V_{IH}$ | Input “H” voltage | Other than CMOS input | | | | 0.8 $V_{CC}$ | – | $V_{CC}$ | V |
| | | CMOS input | Input level switching function (I/O port) | Input level selection : 0.35 $V_{CC}$ | 4.0 V ≤ $V_{CC}$ ≤ 5.5 V | 0.5 $V_{CC}$ | – | $V_{CC}$ | V |
| | | | | | 2.7 V ≤ $V_{CC}$ < 4.0 V | 0.55 $V_{CC}$ | – | $V_{CC}$ | V |
| | | | | | 1.8 V ≤ $V_{CC}$ < 2.7 V | 0.65 $V_{CC}$ | – | $V_{CC}$ | V |
| | | | | Input level selection : 0.5 $V_{CC}$ | 4.0 V ≤ $V_{CC}$ ≤ 5.5 V | 0.65 $V_{CC}$ | – | $V_{CC}$ | V |
| | | | | | 2.7 V ≤ $V_{CC}$ < 4.0 V | 0.7 $V_{CC}$ | – | $V_{CC}$ | V |
| | | | | | 1.8 V ≤ $V_{CC}$ < 2.7 V | 0.8 $V_{CC}$ | – | $V_{CC}$ | V |
| | | | | Input level selection : 0.7 $V_{CC}$ | 4.0 V ≤ $V_{CC}$ ≤ 5.5 V | 0.85 $V_{CC}$ | – | $V_{CC}$ | V |
| | | | | | 2.7 V ≤ $V_{CC}$ < 4.0 V | 0.85 $V_{CC}$ | – | $V_{CC}$ | V |
| | | | | | 1.8 V ≤ $V_{CC}$ < 2.7 V | 0.85 $V_{CC}$ | – | $V_{CC}$ | V |
| | | External clock input (XOUT) | | | | 1.2 | – | $V_{CC}$ | V |
| $V_{IL}$ | Input “L” voltage | Other than CMOS input | | | | 0 | – | 0.2 $V_{CC}$ | V |
| | | CMOS input | Input level switching function (I/O port) | Input level selection : 0.35 $V_{CC}$ | 4.0 V ≤ $V_{CC}$ ≤ 5.5 V | 0 | – | 0.2 $V_{CC}$ | V |
| | | | | | 2.7 V ≤ $V_{CC}$ < 4.0 V | 0 | – | 0.2 $V_{CC}$ | V |
| | | | | | 1.8 V ≤ $V_{CC}$ < 2.7 V | 0 | – | 0.2 $V_{CC}$ | V |
| | | | | Input level selection : 0.5 $V_{CC}$ | 4.0 V ≤ $V_{CC}$ ≤ 5.5 V | 0 | – | 0.4 $V_{CC}$ | V |
| | | | | | 2.7 V ≤ $V_{CC}$ < 4.0 V | 0 | – | 0.3 $V_{CC}$ | V |
| | | | | | 1.8 V ≤ $V_{CC}$ < 2.7 V | 0 | – | 0.2 $V_{CC}$ | V |
| | | | | Input level selection : 0.7 $V_{CC}$ | 4.0 V ≤ $V_{CC}$ ≤ 5.5 V | 0 | – | 0.55 $V_{CC}$ | V |
| | | | | | 2.7 V ≤ $V_{CC}$ < 4.0 V | 0 | – | 0.45 $V_{CC}$ | V |
| | | | | | 1.8 V ≤ $V_{CC}$ < 2.7 V | 0 | – | 0.35 $V_{CC}$ | V |
| | | External clock input (XOUT) | | | | 0 | – | 0.4 | V |
| $I_{OH(sum)}$ | Peak sum output “H” current | Sum of all pins $I_{OH(peak)}$ | | | | – | – | –160 | mA |
| $I_{OH(sum)}$ | Average sum output “H” current | Sum of all pins $I_{OH(avg)}$ | | | | – | – | –80 | mA |
| $I_{OH(peak)}$ | Peak output “H” current | Drive capacity Low | | | | – | – | –10 | mA |
| | | Drive capacity High | | | | – | – | –40 | mA |
| $I_{OH(avg)}$ | Average output “H” current | Drive capacity Low | | | | – | – | –5 | mA |
| | | Drive capacity High | | | | – | – | –20 | mA |
| $I_{OL(sum)}$ | Peak sum output “L” current | Sum of all pins $I_{OL(peak)}$ | | | | – | – | 160 | mA |
| $I_{OL(sum)}$ | Average sum output “L” current | Sum of all pins $I_{OL(avg)}$ | | | | – | – | 80 | mA |
| $I_{OL(peak)}$ | Peak output “L” current | Drive capacity Low | | | | – | – | 10 | mA |
| | | Drive capacity High | | | | – | – | 40 | mA |
| $I_{OL(avg)}$ | Average output “L” current | Drive capacity Low | | | | – | – | 5 | mA |
| | | Drive capacity High | | | | – | – | 20 | mA |
| $f_{(XIN)}$ | XIN clock input oscillation frequency | | | | 2.7 V ≤ $V_{CC}$ ≤ 5.5 V | – | – | 20 | MHz |
| | | | | | 1.8 V ≤ $V_{CC}$ < 2.7 V | – | – | 5 | MHz |
| $f_{(XCIN)}$ | XCIN clock input oscillation frequency | | | | 1.8 V ≤ $V_{CC}$ ≤ 5.5 V | – | 32.768 | 50 | kHz |
| fOCO40M | When used as the count source for timer RC (3) | | | | 2.7 V ≤ $V_{CC}$ ≤ 5.5 V | 32 | – | 40 | MHz |
| fOCO-F | fOCO-F frequency | | | | 2.7 V ≤ $V_{CC}$ ≤ 5.5 V | – | – | 20 | MHz |
| | | | | | 1.8 V ≤ $V_{CC}$ < 2.7 V | – | – | 5 | MHz |
| – | System clock frequency | | | | 2.7 V ≤ $V_{CC}$ ≤ 5.5 V | – | – | 20 | MHz |
| | | | | | 1.8 V ≤ $V_{CC}$ < 2.7 V | – | – | 5 | MHz |
| $f_{(BCLK)}$ | CPU clock frequency | | | | 2.7 V ≤ $V_{CC}$ ≤ 5.5 V | – | – | 20 | MHz |
| | | | | | 1.8 V ≤ $V_{CC}$ < 2.7 V | – | – | 5 | MHz |

Notes:
1. $V_{CC}$ = 1.8 to 5.5 V at $T_{opr}$ = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.
3. fOCO40M can be used as the count source for timer RC in the range of $V_{CC}$ = 2.7 V to 5.5 V.

### Table 5.3 A/D Converter Characteristics

| Symbol | Parameter | | Conditions | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | |
| – | Resolution | | $V_{ref}$ = $AV_{CC}$ | | – | – | 10 | Bit |
| – | Absolute accuracy | 10-bit mode | $V_{ref}$ = $AV_{CC}$ = 5.0 V | AN0, AN1, AN5, AN6, AN8 to AN11 input | – | – | ±3 | LSB |
| | | | $V_{ref}$ = $AV_{CC}$ = 3.3 V | AN0, AN1, AN5, AN6, AN8 to AN11 input | – | – | ±5 | LSB |
| | | | $V_{ref}$ = $AV_{CC}$ = 3.0 V | AN0, AN1, AN5, AN6, AN8 to AN11 input | – | – | ±5 | LSB |
| | | | $V_{ref}$ = $AV_{CC}$ = 2.2 V | AN0, AN1, AN5, AN6, AN8 to AN11 input | – | – | ±5 | LSB |
| | | 8-bit mode | $V_{ref}$ = $AV_{CC}$ = 5.0 V | AN0, AN1, AN5, AN6, AN8 to AN11 input | – | – | ±2 | LSB |
| | | | $V_{ref}$ = $AV_{CC}$ = 3.3 V | AN0, AN1, AN5, AN6, AN8 to AN11 input | – | – | ±2 | LSB |
| | | | $V_{ref}$ = $AV_{CC}$ = 3.0 V | AN0, AN1, AN5, AN6, AN8 to AN11 input | – | – | ±2 | LSB |
| | | | $V_{ref}$ = $AV_{CC}$ = 2.2 V | AN0, AN1, AN5, AN6, AN8 to AN11 input | – | – | ±2 | LSB |
| $\phi$AD | A/D conversion clock | | 4.0 ≤ $V_{ref}$ = $AV_{CC}$ ≤ 5.5 V (2) | | 2 | – | 20 | MHz |
| | | | 3.2 ≤ $V_{ref}$ = $AV_{CC}$ ≤ 5.5 V (2) | | 2 | – | 16 | MHz |
| | | | 2.7 ≤ $V_{ref}$ = $AV_{CC}$ ≤ 5.5 V (2) | | 2 | – | 10 | MHz |
| | | | 2.2 ≤ $V_{ref}$ = $AV_{CC}$ ≤ 5.5 V (2) | | 2 | – | 5 | MHz |
| – | Tolerance level impedance | | | | – | 3 | – | kΩ |
| $t_{CONV}$ | Conversion time | 10-bit mode | $V_{ref}$ = $AV_{CC}$ = 5.0 V, $\phi$AD = 20 MHz | | 2.15 | – | – | µs |
| | | 8-bit mode | $V_{ref}$ = $AV_{CC}$ = 5.0 V, $\phi$AD = 20 MHz | | 2.15 | – | – | µs |
| $t_{SAMP}$ | Sampling time | | $\phi$AD = 20 MHz | | 0.75 | – | – | µs |
| $I_{Vref}$ | $V_{ref}$ current | | Vcc = 5 V, XIN = f1 = $\phi$AD = 20 MHz | | – | 45 | – | µA |
| $V_{ref}$ | Reference voltage | | | | 2.2 | – | $AV_{CC}$ | V |
| $V_{IA}$ | Analog input voltage (3) | | | | 0 | – | $V_{ref}$ | V |
| OCVREF | On-chip reference voltage | | 2 MHz ≤ $\phi$AD ≤ 4 MHz | | 1.19 | 1.34 | 1.49 | V |

Notes:
1. $V_{CC}$/$AV_{CC}$ = $V_{ref}$ = 2.2 to 5.5 V, $V_{SS}$ = 0 V at $T_{opr}$ = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. The A/D conversion result will be undefined in wait mode, stop mode, when the flash memory stops, and in low-current-consumption mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.
3. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

### Table 5.4 Comparator B Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| Vref | IVREF1, IVREF3 input reference voltage | | 0 | – | $V_{CC}$ – 1.4 | V |
| $V_I$ | IVCMP1, IVCMP3 input voltage | | –0.3 | – | $V_{CC}$ + 0.3 | V |
| – | Offset | | – | 5 | 100 | mV |
| td | Comparator output delay time (2) | $V_I$ = Vref ± 100 mV | – | 0.1 | – | µs |
| $I_{CMP}$ | Comparator operating current | $V_{CC}$ = 5.0 V | – | 17.5 | – | µA |

Notes:
1. $V_{CC}$ = 2.7 to 5.5 V, $T_{opr}$ = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. When the digital filter is disabled.

**Table 5.13 Electrical Characteristics (1) [4.2 V ≤ Vcc ≤ 5.5 V]**

| Symbol | Parameter | | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | |
| $V_{OH}$ | Output "H" voltage | Other than XOUT | Drive capacity High $V_{CC}$ = 5V | $I_{OH}$ = –20 mA | $V_{CC}$ – 2.0 | – | $V_{CC}$ | V |
| | | | Drive capacity Low $V_{CC}$ = 5V | $I_{OH}$ = –5 mA | $V_{CC}$ – 2.0 | – | $V_{CC}$ | V |
| | | XOUT | $V_{CC}$ = 5V | $I_{OH}$ = –200 μA | 1.0 | – | $V_{CC}$ | V |
| $V_{OL}$ | Output "L" voltage | Other than XOUT | Drive capacity High $V_{CC}$ = 5V | $I_{OL}$ = 20 mA | – | – | 2.0 | V |
| | | | Drive capacity Low $V_{CC}$ = 5V | $I_{OL}$ = 5 mA | – | – | 2.0 | V |
| | | XOUT | $V_{CC}$ = 5V | $I_{OL}$ = 200 μA | – | – | 0.5 | V |
| $V_{T+}$-$V_{T-}$ | Hysteresis | $\overline{INT0}$, $\overline{INT1}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, TRBO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, $\overline{TRCTRG}$, TRCCLK, $\overline{ADTRG}$, RXD0, RXD2, CLK0, CLK2 | | | 0.1 | 1.2 | – | V |
| | | $\overline{RESET}$ | | | 0.1 | 1.2 | – | V |
| $I_{IH}$ | Input "H" current | | VI = 5 V, $V_{CC}$ = 5.0V | | – | – | 5.0 | μA |
| $I_{IL}$ | Input "L" current | | VI = 0 V, $V_{CC}$ = 5.0V | | – | – | –5.0 | μA |
| $R_{PULLUP}$ | Pull-up resistance | | VI = 0 V, $V_{CC}$ = 5.0V | | 25 | 50 | 100 | kΩ |
| $R_{fXIN}$ | Feedback resistance | XIN | | | – | 0.3 | – | MΩ |
| $R_{fXCIN}$ | Feedback resistance | XCIN | | | – | 8 | – | MΩ |
| $V_{RAM}$ | RAM hold voltage | | During stop mode | | 1.8 | – | – | V |

Note:
1. 4.2 V ≤ $V_{CC}$ ≤ 5.5 V at $T_{opr}$ = –20 to 85°C (N version) / –40 to 85°C (D version), f(XIN) = 20 MHz, unless otherwise specified.

**Table 5.14 Electrical Characteristics (2) [3.3 V ≤ Vcc ≤ 5.5 V]**
**(Topr = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.)**

| Symbol | Parameter | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| ICC | Power supply current (VCC = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are VSS | High-speed clock mode | XIN = 20 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 6.5 | 15 | mA |
| | | | XIN = 16 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 5.3 | 12.5 | mA |
| | | | XIN = 10 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 3.6 | – | mA |
| | | | XIN = 20 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 3.0 | – | mA |
| | | | XIN = 16 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 2.2 | – | mA |
| | | | XIN = 10 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 1.5 | – | mA |
| | | High-speed on-chip oscillator mode | XIN clock off<br>High-speed on-chip oscillator on fOCO-F = 20 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 7.0 | 15 | mA |
| | | | XIN clock off<br>High-speed on-chip oscillator on fOCO-F = 20 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 3.0 | – | mA |
| | | | XIN clock off<br>High-speed on-chip oscillator on fOCO-F = 4 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-16<br>MSTTRC = 1 | – | 1 | – | mA |
| | | Low-speed on-chip oscillator mode | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8, FMR27 = 1, VCA20 = 0 | – | 90 | 400 | µA |
| | | Low-speed clock mode | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>XCIN clock oscillator on = 32 kHz<br>No division<br>FMR27 = 1, VCA20 = 0 | – | 85 | 400 | µA |
| | | | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>XCIN clock oscillator on = 32 kHz<br>No division<br>Program operation on RAM<br>Flash memory off, FMSTP = 1, VCA20 = 0 | – | 47 | – | µA |
| | | Wait mode | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>While a WAIT instruction is executed<br>Peripheral clock operation<br>VCA27 = VCA26 = VCA25 = 0, VCA20 = 1 | – | 15 | 100 | µA |
| | | | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>While a WAIT instruction is executed<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0, VCA20 = 1 | – | 4 | 90 | µA |
| | | | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>XCIN clock oscillator on = 32 kHz (peripheral clock off)<br>While a WAIT instruction is executed<br>VCA27 = VCA26 = VCA25 = 0, VCA20 = 1 | – | 3.5 | – | µA |
| | | Stop mode | XIN clock off, Topr = 25°C<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10 = 1<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0 | – | 2.0 | 5.0 | µA |
| | | | XIN clock off, Topr = 85°C<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10 = 1<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0 | – | 5.0 | – | µA |

**Table 5.17 Serial Interface**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{C(CK)}$ | CLKi input cycle time | 200 | – | ns |
| $t_{W(CKH)}$ | CLKi input “H” width | 100 | – | ns |
| $t_{W(CKL)}$ | CLKi input “L” width | 100 | – | ns |
| $t_{d(C-Q)}$ | TXDi output delay time | – | 50 | ns |
| $t_{h(C-Q)}$ | TXDi hold time | 0 | – | ns |
| $t_{su(D-C)}$ | RXDi input setup time | 50 | – | ns |
| $t_{h(C-D)}$ | RXDi input hold time | 90 | – | ns |

i = 0, 2

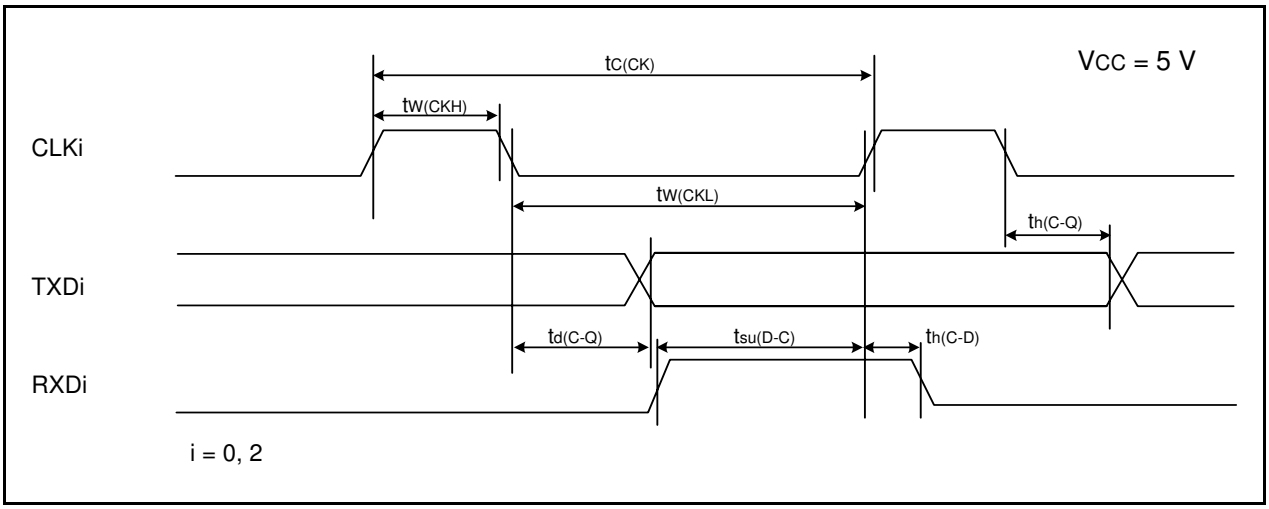



**Figure 5.6 Serial Interface Timing Diagram when VCC = 5 V**

**Table 5.18 External Interrupt $\overline{INTi}$ (i = 0, 1, 3) Input, Key Input Interrupt $\overline{KIi}$ (i = 0 to 3)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{W(INH)}$ | $\overline{INTi}$ input “H” width, $\overline{KIi}$ input “H” width | 250 (1) | – | ns |
| $t_{W(INL)}$ | $\overline{INTi}$ input “L” width, $\overline{KIi}$ input “L” width | 250 (2) | – | ns |

Notes:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

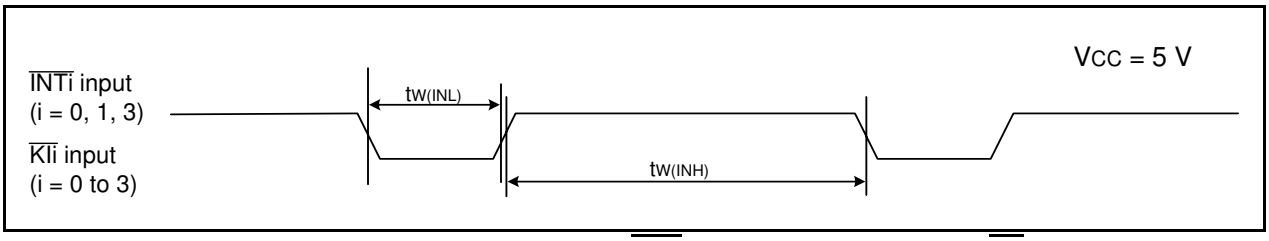



**Figure 5.7 Input Timing for External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{KIi}$ when Vcc = 5 V**

**Table 5.20 Electrical Characteristics (4) [2.7 V ≤ Vcc < 3.3 V]**
**(Topr = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.)**

| Symbol | Parameter | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| ICC | Power supply current (VCC = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are VSS | High-speed clock mode | XIN = 10 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 3.5 | 10 | mA |
| | | | XIN = 10 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 1.5 | 7.5 | mA |
| | | High-speed on-chip oscillator mode | XIN clock off<br>High-speed on-chip oscillator on fOCO-F = 20 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 7.0 | 15 | mA |
| | | | XIN clock off<br>High-speed on-chip oscillator on fOCO-F = 20 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 3.0 | – | mA |
| | | | XIN clock off<br>High-speed on-chip oscillator on fOCO-F = 10 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 4.0 | – | mA |
| | | | XIN clock off<br>High-speed on-chip oscillator on fOCO-F = 10 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 1.5 | – | mA |
| | | | XIN clock off<br>High-speed on-chip oscillator on fOCO-F = 4 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-16<br>MSTTRC = 1 | – | 1 | – | mA |
| | | Low-speed on-chip oscillator mode | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8, FMR27 = 1, VCA20 = 0 | – | 90 | 390 | µA |
| | | Low-speed clock mode | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>XCIN clock oscillator on = 32 kHz<br>No division<br>FMR27 = 1, VCA20 = 0 | – | 80 | 400 | µA |
| | | | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>XCIN clock oscillator on = 32 kHz<br>No division<br>Program operation on RAM<br>Flash memory off, FMSTP = 1, VCA20 = 0 | – | 40 | – | µA |
| | | Wait mode | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>While a WAIT instruction is executed<br>Peripheral clock operation<br>VCA27 = VCA26 = VCA25 = 0, VCA20 = 1 | – | 15 | 90 | µA |
| | | | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>While a WAIT instruction is executed<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0, VCA20 = 1 | – | 4 | 80 | µA |
| | | | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>XCIN clock oscillator on = 32 kHz (peripheral clock off)<br>While a WAIT instruction is executed<br>VCA27 = VCA26 = VCA25 = 0, VCA20 = 1 | – | 3.5 | – | µA |
| | | Stop mode | XIN clock off, Topr = 25°C<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10 = 1<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0 | – | 2.0 | 5.0 | µA |
| | | | XIN clock off, Topr = 85°C<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10 = 1<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0 | – | 5.0 | – | µA |

**Table 5.25 Electrical Characteristics (5) [1.8 V ≤ Vcc < 2.7 V]**

| Symbol | Parameter | | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | |
| $V_{OH}$ | Output “H” voltage | Other than XOUT | Drive capacity High | $I_{OH}$ = –2 mA | $V_{CC}$ – 0.5 | – | $V_{CC}$ | V |
| | | | Drive capacity Low | $I_{OH}$ = –1 mA | $V_{CC}$ – 0.5 | – | $V_{CC}$ | V |
| | | XOUT | | $I_{OH}$ = –200 μA | 1.0 | – | $V_{CC}$ | V |
| $V_{OL}$ | Output “L” voltage | Other than XOUT | Drive capacity High | $I_{OL}$ = 2 mA | – | – | 0.5 | V |
| | | | Drive capacity Low | $I_{OL}$ = 1 mA | – | – | 0.5 | V |
| | | XOUT | | $I_{OL}$ = 200 μA | – | – | 0.5 | V |
| $V_{T+}$-$V_{T-}$ | Hysteresis | $\overline{INT0}$, $\overline{INT1}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, TRBO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, $\overline{TRCTRG}$, TRCCLK, $\overline{ADTRG}$, RXD0, RXD2, CLK0, CLK2 | | | 0.05 | 0.2 | – | V |
| | | $\overline{RESET}$ | | | 0.05 | 0.20 | – | V |
| $I_{IH}$ | Input “H” current | | VI = 2.2 V, $V_{CC}$ = 2.2 V | | – | – | 4.0 | μA |
| $I_{IL}$ | Input “L” current | | VI = 0 V, $V_{CC}$ = 2.2 V | | – | – | –4.0 | μA |
| $R_{PULLUP}$ | Pull-up resistance | | VI = 0 V, $V_{CC}$ = 2.2 V | | 70 | 140 | 300 | kΩ |
| $R_{fXIN}$ | Feedback resistance | XIN | | | – | 0.3 | – | MΩ |
| $R_{fXCIN}$ | Feedback resistance | XCIN | | | – | 8 | – | MΩ |
| $V_{RAM}$ | RAM hold voltage | | During stop mode | | 1.8 | – | – | V |

Note:
1. 1.8 V ≤ $V_{CC}$ < 2.7 V at $T_{opr}$ = –20 to 85°C (N version) / –40 to 85°C (D version), f(XIN) = 5 MHz, unless otherwise specified.

**Timing Requirements (Unless Otherwise Specified: $V_{CC}$ = 2.2 V, $V_{SS}$ = 0 V at Topr = 25°C)**

**Table 5.27 External clock input (XOUT, XCIN)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(XOUT)}$ | XOUT input cycle time | 200 | – | ns |
| $t_{WH(XOUT)}$ | XOUT input “H” width | 90 | – | ns |
| $t_{WL(XOUT)}$ | XOUT input “L” width | 90 | – | ns |
| $t_{c(XCIN)}$ | XCIN input cycle time | 14 | – | µs |
| $t_{WH(XCIN)}$ | XCIN input “H” width | 7 | – | µs |
| $t_{WL(XCIN)}$ | XCIN input “L” width | 7 | – | µs |

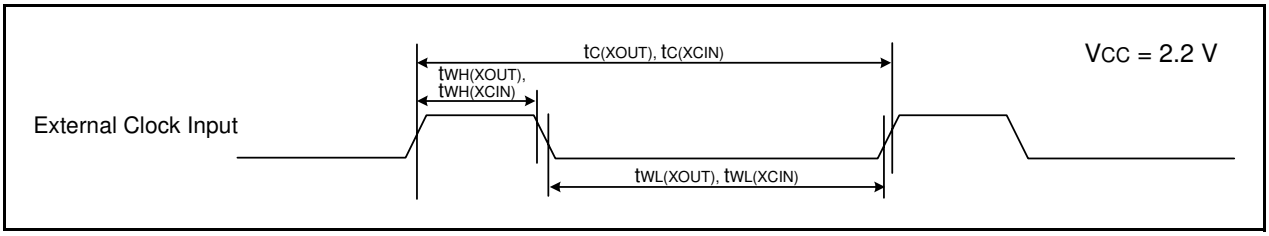



**Figure 5.12 External Clock Input Timing Diagram when $V_{CC}$ = 2.2 V**

**Table 5.28 TRAIO Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TRAIO)}$ | TRAIO input cycle time | 500 | – | ns |
| $t_{WH(TRAIO)}$ | TRAIO input “H” width | 200 | – | ns |
| $t_{WL(TRAIO)}$ | TRAIO input “L” width | 200 | – | ns |

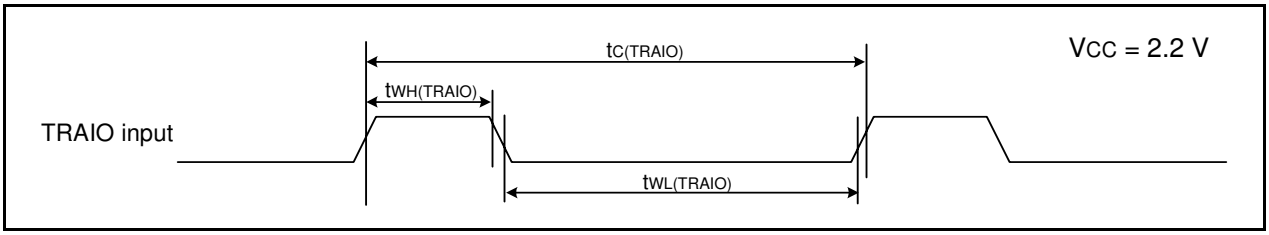



**Figure 5.13 TRAIO Input Timing Diagram when $V_{CC}$ = 2.2 V**

| REVISION HISTORY | R8C/3GD Group Datasheet |
|---|---|

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 0.01 | Sep. 10, 2009 | – | First Edition issued |
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| | | 4 | Table 1.3 revised |
| | | 21 to 40 | “5. Electrical Characteristics” added |
| | | | |

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