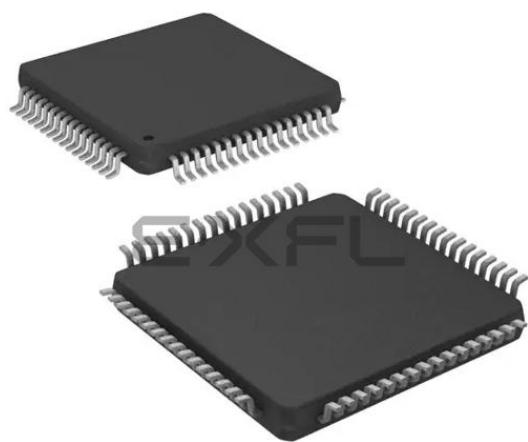




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Obsolete
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I ² C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	50
Program Memory Size	128KB (64K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega128c3-anr

7.8 Memory Timing

Read and write access to the I/O memory takes one CPU clock cycle. A write to SRAM takes one cycle, and a read from SRAM takes two cycles. EEPROM page load (write) takes one cycle, and three cycles are required for read. For burst read, new data are available every second cycle. Refer to the instruction summary for more details on instructions and instruction timing.

7.9 Device ID and Revision

Each device has a three-byte device ID. This ID identifies Atmel as the manufacturer of the device and the device type. A separate register contains the revision number of the device.

7.10 I/O Memory Protection

Some features in the device are regarded as critical for safety in some applications. Due to this, it is possible to lock the I/O register related to the clock system, the event system, and the advanced waveform extensions. As long as the lock is enabled, all related I/O registers are locked and they can not be written from the application software. The lock registers themselves are protected by the configuration change protection mechanism.

7.11 Flash and EEPROM Page Size

The flash program memory and EEPROM data memory are organized in pages. The pages are word accessible for the flash and byte accessible for the EEPROM.

Table 7-2 on page 16 shows the Flash Program Memory organization and Program Counter (PC) size. Flash write and erase operations are performed on one page at a time, while reading the Flash is done one byte at a time. For Flash access the Z-pointer (Z[m:n]) is used for addressing. The most significant bits in the address (FPAGE) give the page number and the least significant address bits (FWORD) give the word in the page.

Table 7-2. Number of Words and Pages in the Flash

Devices	PC size	Flash size	Page size	FWORD	FPAGE	Application		Boot	
	bits	bytes	words			Size	No. of pages	Size	No. of pages
ATxmega32C3	16	32K + 4K	128	Z[7:1]	Z[16:8]	32K	128	4K	16
ATxmega64C3	16	64K + 4K	128	Z[7:1]	Z[16:8]	64K	256	4K	16
ATxmega128C3	17	128K + 8K	256	Z[8:1]	Z[17:9]	128K	256	8K	16
ATxmega192C3	17	192K + 8K	256	Z[8:1]	Z[17:9]	192K	384	8K	16
ATxmega256C3	18	256K + 8K	256	Z[8:1]	Z[18:9]	256K	512	8K	16

Table 7-3 on page 17 shows EEPROM memory organization. EEPROM write and erase operations can be performed one page or one byte at a time, while reading the EEPROM is done one byte at a time. For EEPROM access the NVM address register (ADDR[m:n]) is used for addressing. The most significant bits in the address (E2PAGE) give the page number and the least significant address bits (E2BYTE) give the byte in the page.

Multipacket transfer enables a data payload exceeding the maximum packet size of an endpoint to be transferred as multiple packets without software intervention. This reduces the CPU intervention and the interrupts needed for USB transfers.

For low-power operation, the USB module can put the microcontroller into any sleep mode when the USB bus is idle and a suspend condition is given. Upon bus resumes, the USB module can wake up the microcontroller from any sleep mode.

PORTD has one USB. Notation of this is USB.

31. Instruction Set Summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
Arithmetic and Logic Instructions					
ADD	Rd, Rr	Add without Carry	$Rd \leftarrow Rd + Rr$	Z,C,N,V,S,H	1
ADC	Rd, Rr	Add with Carry	$Rd \leftarrow Rd + Rr + C$	Z,C,N,V,S,H	1
ADIW	Rd, K	Add Immediate to Word	$Rd \leftarrow Rd + 1:Rd + K$	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract without Carry	$Rd \leftarrow Rd - Rr$	Z,C,N,V,S,H	1
SUBI	Rd, K	Subtract Immediate	$Rd \leftarrow Rd - K$	Z,C,N,V,S,H	1
SBC	Rd, Rr	Subtract with Carry	$Rd \leftarrow Rd - Rr - C$	Z,C,N,V,S,H	1
SBCI	Rd, K	Subtract Immediate with Carry	$Rd \leftarrow Rd - K - C$	Z,C,N,V,S,H	1
SBIW	Rd, K	Subtract Immediate from Word	$Rd + 1:Rd \leftarrow Rd + 1:Rd - K$	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND	$Rd \leftarrow Rd \bullet Rr$	Z,N,V,S	1
ANDI	Rd, K	Logical AND with Immediate	$Rd \leftarrow Rd \bullet K$	Z,N,V,S	1
OR	Rd, Rr	Logical OR	$Rd \leftarrow Rd \vee Rr$	Z,N,V,S	1
ORI	Rd, K	Logical OR with Immediate	$Rd \leftarrow Rd \vee K$	Z,N,V,S	1
EOR	Rd, Rr	Exclusive OR	$Rd \leftarrow Rd \oplus Rr$	Z,N,V,S	1
COM	Rd	One's Complement	$Rd \leftarrow \$FF - Rd$	Z,C,N,V,S	1
NEG	Rd	Two's Complement	$Rd \leftarrow \$00 - Rd$	Z,C,N,V,S,H	1
SBR	Rd,K	Set Bit(s) in Register	$Rd \leftarrow Rd \vee K$	Z,N,V,S	1
CBR	Rd,K	Clear Bit(s) in Register	$Rd \leftarrow Rd \bullet (\$FFh - K)$	Z,N,V,S	1
INC	Rd	Increment	$Rd \leftarrow Rd + 1$	Z,N,V,S	1
DEC	Rd	Decrement	$Rd \leftarrow Rd - 1$	Z,N,V,S	1
TST	Rd	Test for Zero or Minus	$Rd \leftarrow Rd \bullet Rd$	Z,N,V,S	1
CLR	Rd	Clear Register	$Rd \leftarrow Rd \oplus Rd$	Z,N,V,S	1
SER	Rd	Set Register	$Rd \leftarrow \$FF$	None	1
MUL	Rd,Rr	Multiply Unsigned	$R1:R0 \leftarrow Rd \times Rr (UU)$	Z,C	2
MULS	Rd,Rr	Multiply Signed	$R1:R0 \leftarrow Rd \times Rr (SS)$	Z,C	2
MULSU	Rd,Rr	Multiply Signed with Unsigned	$R1:R0 \leftarrow Rd \times Rr (SU)$	Z,C	2
FMUL	Rd,Rr	Fractional Multiply Unsigned	$R1:R0 \leftarrow Rd \times Rr << 1 (UU)$	Z,C	2
FMULS	Rd,Rr	Fractional Multiply Signed	$R1:R0 \leftarrow Rd \times Rr << 1 (SS)$	Z,C	2
FMULSU	Rd,Rr	Fractional Multiply Signed with Unsigned	$R1:R0 \leftarrow Rd \times Rr << 1 (SU)$	Z,C	2
DES	K	Data Encryption	if (H = 0) then R15:R0 $\leftarrow$ Encrypt(R15:R0, K) else if (H = 1) then R15:R0 $\leftarrow$ Decrypt(R15:R0, K)		1/2
Branch instructions					
RJMP	k	Relative Jump	$PC \leftarrow PC + k + 1$	None	2
IJMP		Indirect Jump to (Z)	$PC(15:0) \leftarrow Z,$ $PC(21:16) \leftarrow 0$	None	2
EIJMP		Extended Indirect Jump to (Z)	$PC(15:0) \leftarrow Z,$ $PC(21:16) \leftarrow EIND$	None	2
JMP	k	Jump	$PC \leftarrow k$	None	3

Mnemonics	Operands	Description	Operation	Flags	#Clocks
RCALL	k	Relative Call Subroutine	PC ← PC + k + 1	None	2 / 3
ICALL		Indirect Call to (Z)	PC(15:0) ← Z, PC(21:16) ← 0	None	2 / 3
EICALL		Extended Indirect Call to (Z)	PC(15:0) ← Z, PC(21:16) ← EIND	None	3
CALL	k	call Subroutine	PC ← k	None	3 / 4
RET		Subroutine Return	PC ← STACK	None	4 / 5
RETI		Interrupt Return	PC ← STACK	I	4 / 5
CPSE	Rd,Rr	Compare, Skip if Equal	if (Rd = Rr) PC ← PC + 2 or 3	None	1 / 2 / 3
CP	Rd,Rr	Compare	Rd - Rr	Z,C,N,V,S,H	1
CPC	Rd,Rr	Compare with Carry	Rd - Rr - C	Z,C,N,V,S,H	1
CPI	Rd,K	Compare with Immediate	Rd - K	Z,C,N,V,S,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b) = 0) PC ← PC + 2 or 3	None	1 / 2 / 3
SBRS	Rr, b	Skip if Bit in Register Set	if (Rr(b) = 1) PC ← PC + 2 or 3	None	1 / 2 / 3
SBIC	A, b	Skip if Bit in I/O Register Cleared	if (I/O(A,b) = 0) PC ← PC + 2 or 3	None	2 / 3 / 4
SBIS	A, b	Skip if Bit in I/O Register Set	If (I/O(A,b) = 1) PC ← PC + 2 or 3	None	2 / 3 / 4
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then PC ← PC + k + 1	None	1 / 2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then PC ← PC + k + 1	None	1 / 2
BREQ	k	Branch if Equal	if (Z = 1) then PC ← PC + k + 1	None	1 / 2
BRNE	k	Branch if Not Equal	if (Z = 0) then PC ← PC + k + 1	None	1 / 2
BRCS	k	Branch if Carry Set	if (C = 1) then PC ← PC + k + 1	None	1 / 2
BRCC	k	Branch if Carry Cleared	if (C = 0) then PC ← PC + k + 1	None	1 / 2
BRSH	k	Branch if Same or Higher	if (C = 0) then PC ← PC + k + 1	None	1 / 2
BRLO	k	Branch if Lower	if (C = 1) then PC ← PC + k + 1	None	1 / 2
BRMI	k	Branch if Minus	if (N = 1) then PC ← PC + k + 1	None	1 / 2
BRPL	k	Branch if Plus	if (N = 0) then PC ← PC + k + 1	None	1 / 2
BRGE	k	Branch if Greater or Equal, Signed	if (N ⊕ V = 0) then PC ← PC + k + 1	None	1 / 2
BRLT	k	Branch if Less Than, Signed	if (N ⊕ V = 1) then PC ← PC + k + 1	None	1 / 2
BRHS	k	Branch if Half Carry Flag Set	if (H = 1) then PC ← PC + k + 1	None	1 / 2
BRHC	k	Branch if Half Carry Flag Cleared	if (H = 0) then PC ← PC + k + 1	None	1 / 2
BRTS	k	Branch if T Flag Set	if (T = 1) then PC ← PC + k + 1	None	1 / 2
BRTC	k	Branch if T Flag Cleared	if (T = 0) then PC ← PC + k + 1	None	1 / 2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then PC ← PC + k + 1	None	1 / 2
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then PC ← PC + k + 1	None	1 / 2
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then PC ← PC + k + 1	None	1 / 2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then PC ← PC + k + 1	None	1 / 2
Data transfer instructions					
MOV	Rd, Rr	Copy Register	Rd ← Rr	None	1

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
C_{XTAL1}	Parasitic capacitance XTAL1 pin			5.9		pF
C_{XTAL2}	Parasitic capacitance XTAL2 pin			8.3		
C_{LOAD}	Parasitic capacitance load			3.5		

Note: 1. Numbers for negative impedance are not tested in production but guaranteed from design and characterization.

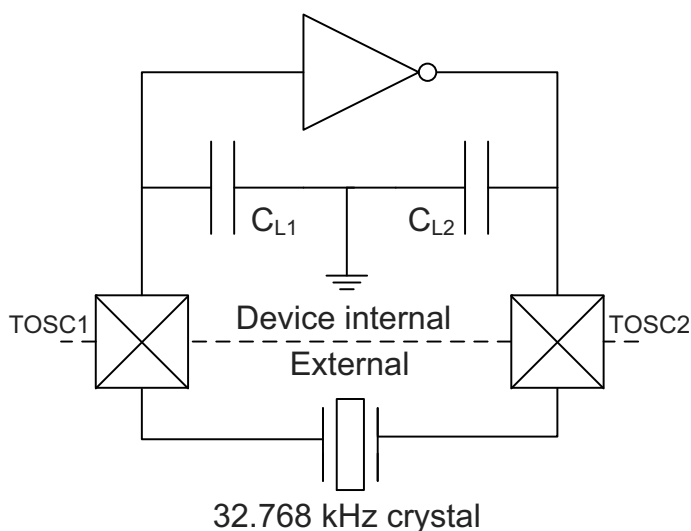
33.1.13.8 External 32.768kHz Crystal Oscillator and TOSC Characteristics

Table 33-27. External 32.768kHz Crystal Oscillator and TOSC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
ESR/R1	Recommended crystal equivalent series resistance (ESR)	Crystal load capacitance 6.5pF			60	k Ω
		Crystal load capacitance 9.0pF			35	
		Crystal load capacitance 12pF			28	
C_{TOSC1}	Parasitic capacitance TOSC1 pin			3.5		pF
C_{TOSC2}	Parasitic capacitance TOSC2 pin			3.5		
	Recommended safety factor	capacitance load matched to crystal specification	3			

Note: See Figure 33-4 for definition.

Figure 33-4. TOSC Input Capacitance



The parasitic capacitance between the TOSC pins is $C_{L1} + C_{L2}$ in series as seen from the crystal when oscillating without external capacitors.

Table 33-40. Gain Stage Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
R_{in}	Input resistance	Switched in normal mode		4.0		k Ω
C_{sample}	Input capacitance	Switched in normal mode		4.4		pF
	Signal range	Gain stage output	0		$AV_{CC} - 0.6$	V
	Propagation delay	ADC conversion rate	1/2	1	3	Clk _{ADC} cycles
	Clock frequency	Same as ADC	100		1800	kHz
	Gain error	0.5x gain, normal mode		-1		%
		1x gain, normal mode		-1		
		8x gain, normal mode		-1		
		64x gain, normal mode		5		
	Offset error, input referred	0.5x gain, normal mode		10		mV
		1x gain, normal mode		5		
		8x gain, normal mode		-20		
		64x gain, normal mode		-126		

33.2.7 Analog Comparator Characteristics

Table 33-41. Analog Comparator Characteristics

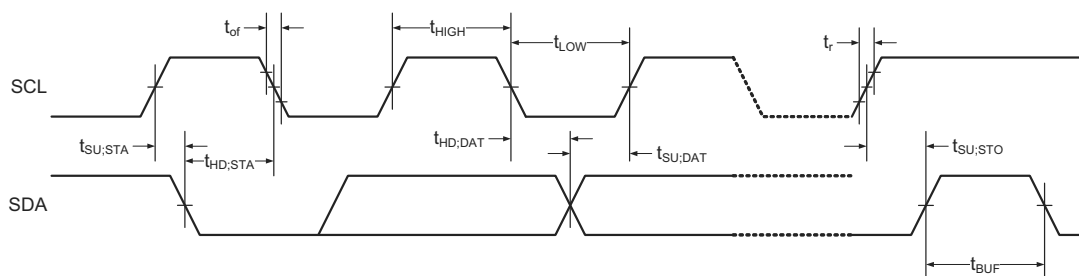
Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{off}	Input offset voltage			10		mV
I_{lk}	Input leakage current			<10	50	nA
	Input voltage range		-0.1		AV_{CC}	V
	AC startup time			50		μ s
V_{hys1}	Hysteresis, none	$V_{CC} = 1.6V - 3.6V$		0		mV
V_{hys2}	Hysteresis, small	$V_{CC} = 1.6V - 3.6V$		15		
V_{hys3}	Hysteresis, large	$V_{CC} = 1.6V - 3.6V$		30		
t_{delay}	Propagation delay	$V_{CC} = 3.0V, T = 85^{\circ}C$		20	40	ns
		$V_{CC} = 3.0V$		17		
	64-level voltage scaler	Integral non-linearity (INL)		0.3	0.5	lsb
	Current source accuracy after calibration			5		%
	Current source calibration range	Single mode	4		6	μ A

Table 33-57. SPI Timing Characteristics and Requirements

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_{SCK}	SCK period	Master		(See Table 20-3 in XMEGA C Manual)		ns
t_{SCKW}	SCK high/low width	Master		$0.5 \cdot SCK$		
t_{SCKR}	SCK rise time	Master		2.7		
t_{SCKF}	SCK fall time	Master		2.7		
t_{MIS}	MISO setup to SCK	Master		10		
t_{MIH}	MISO hold after SCK	Master		10		
t_{MOS}	MOSI setup SCK	Master		$0.5 \cdot SCK$		
t_{MOH}	MOSI hold after SCK	Master		1		
t_{SSCK}	Slave SCK period	Slave	$4 \cdot t_{Clk_{PER}}$			
t_{SSCKW}	SCK high/low width	Slave	$2 \cdot t_{Clk_{PER}}$			
t_{SSCKR}	SCK rise time	Slave			1600	
t_{SSCKF}	SCK fall time	Slave			1600	
t_{SIS}	MOSI setup to SCK	Slave	3			
t_{SIH}	MOSI hold after SCK	Slave	$t_{Clk_{PER}}$			
t_{SSS}	$\overline{SS}$ setup to SCK	Slave	21			
t_{SSH}	$\overline{SS}$ hold after SCK	Slave	20			
t_{SOS}	MISO setup SCK	Slave		8		
t_{SOH}	MISO hold after SCK	Slave		13		
t_{SOSS}	MISO setup after $\overline{SS}$ low	Slave		11		
t_{SOSH}	MISO hold after $\overline{SS}$ high	Slave		8		

33.2.15 Two-Wire Interface Characteristics

Table 33-58 describes the requirements for devices connected to the Two-Wire Interface Bus. The Atmel AVR XMEGA Two-Wire Interface meets or exceeds these requirements under the noted conditions. Timing symbols refer to Figure 33-14.

Figure 33-14. Two-wire Interface Bus Timing


33.4.3 Current Consumption

Table 33-91. Current Consumption for Active Mode and Sleep Mode

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I _{CC}	Active power consumption ⁽¹⁾	32kHz, Ext. Clk	V _{CC} = 1.8V	60		μA
			V _{CC} = 3.0V	140		
		1MHz, Ext. Clk	V _{CC} = 1.8V	245		
			V _{CC} = 3.0V	550		
		2MHz, Ext. Clk	V _{CC} = 1.8V	440	700	mA
			V _{CC} = 3.0V	0.9	1.5	
		32MHz, Ext. Clk	V _{CC} = 1.8V	9.0	15	
			V _{CC} = 3.0V			
	Idle power consumption ⁽²⁾	32kHz, Ext. Clk	V _{CC} = 1.8V	3.0		μA
			V _{CC} = 3.0V	3.5		
		1MHz, Ext. Clk	V _{CC} = 1.8V	55		
			V _{CC} = 3.0V	110		
		2MHz, Ext. Clk	V _{CC} = 1.8V	105	350	mA
			V _{CC} = 3.0V	215	650	
		32MHz, Ext. Clk	V _{CC} = 1.8V	3.4	8.0	
			V _{CC} = 3.0V			
	Power-down power consumption	T = 25°C	V _{CC} = 3.0V	0.1	1.0	μA
		T = 85°C		3.5	6.0	
		T = 105°C		10.0	15	
		WDT and sampled BOD enabled, T = 25°C	V _{CC} = 3.0V	1.5	2.0	
		WDT and sampled BOD enabled, T = 85°C		5.8	10	
		WDT and sampled BOD enabled, T = 105°C		12	20	
	Power-save power consumption ⁽³⁾	RTC from ULP clock, WDT and sampled BOD enabled, T = 25°C	V _{CC} = 1.8V	1.3		
			V _{CC} = 3.0V	1.4		
		RTC from 1.024kHz low power 32.768kHz TOSC, T = 25°C	V _{CC} = 1.8V	0.7	2.0	
			V _{CC} = 3.0V	0.8	2.0	
		RTC from low power 32.768kHz TOSC, T = 25°C	V _{CC} = 1.8V	0.9	3.0	
			V _{CC} = 3.0V	1.1	3.0	
	Reset power consumption	Current through RESET pin subtracted	V _{CC} = 3.0V	170		

- Notes:
1. All Power Reduction Registers set including FPRM and EPRM.
 2. All Power Reduction Registers set without FPRM and EPRM.
 3. Maximum limits are based on characterization, and not tested in production.

Figure 34-13. Idle Mode Supply Current vs. V_{CC}
 $f_{SYS} = 32\text{MHz}$ internal oscillator prescaled to 8MHz

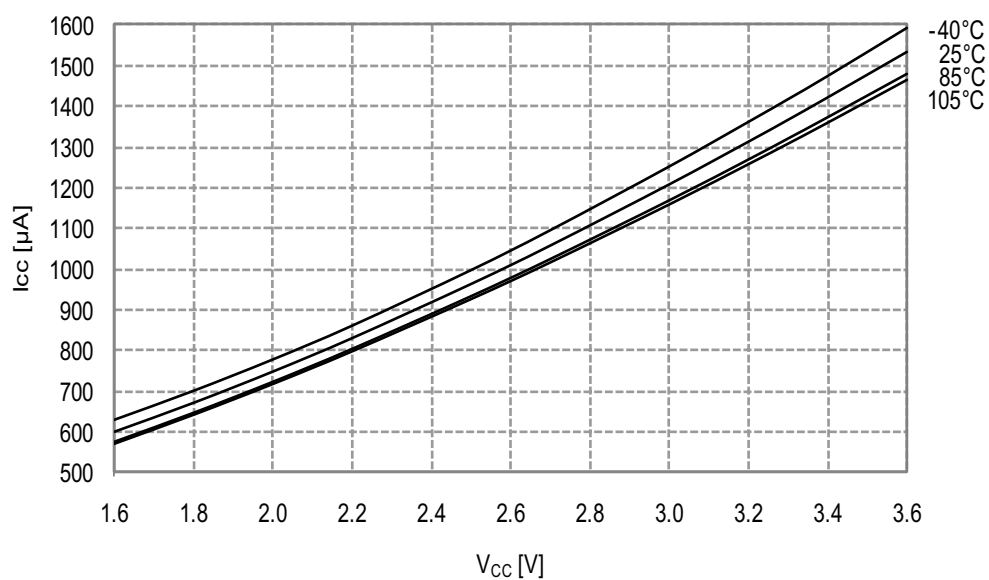


Figure 34-14. Idle Mode Current vs. V_{CC}
 $f_{SYS} = 32\text{MHz}$ internal oscillator

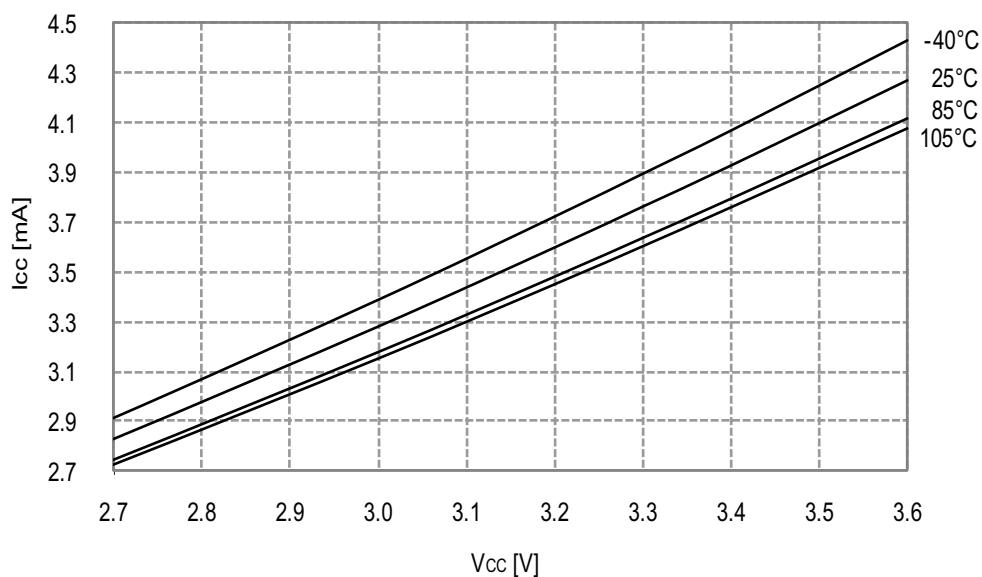
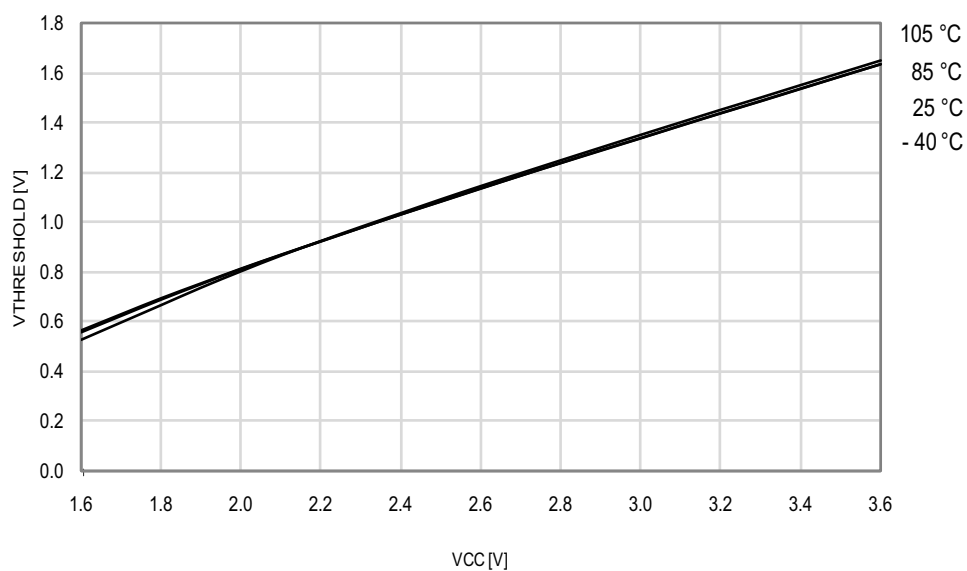


Figure 34-53. Reset Pin Input Threshold Voltage vs. V_{CC}

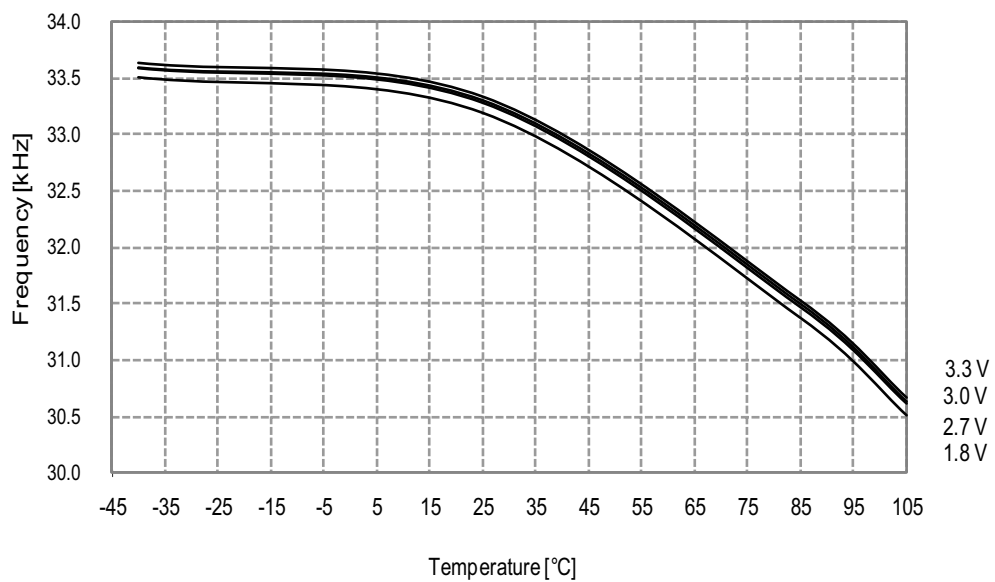
V_{IH} - Reset pin read as "1"



34.1.8 Oscillator Characteristics

34.1.8.1 Ultra Low-Power Internal Oscillator

Figure 34-54. Ultra Low-Power Internal Oscillator Frequency vs. Temperature



34.1.8.3 2MHz Internal Oscillator

Figure 34-57. 2MHz Internal Oscillator Frequency vs. Temperature
DFLL disabled

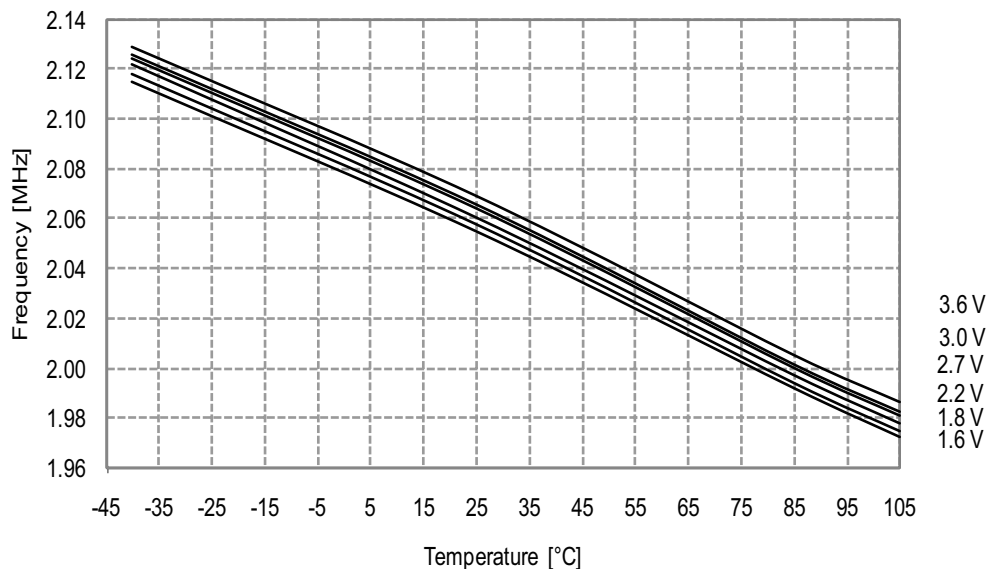


Figure 34-58. 2MHz Internal Oscillator Frequency vs. Temperature
DFLL enabled, from the 32.768kHz internal oscillator

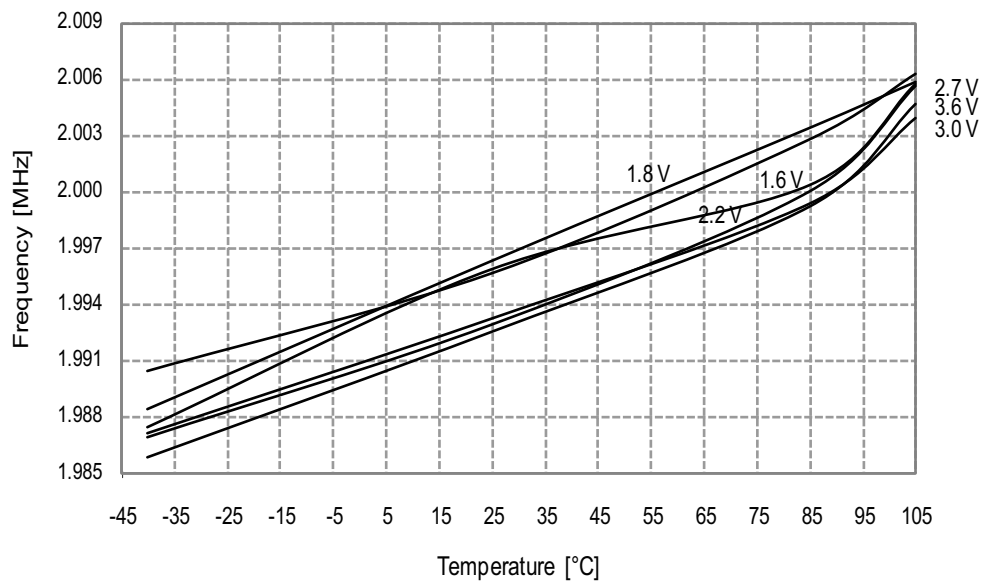


Figure 34-100. I/O Pin Input Threshold Voltage vs. V_{CC}

V_{IL} I/O pin read as "0"

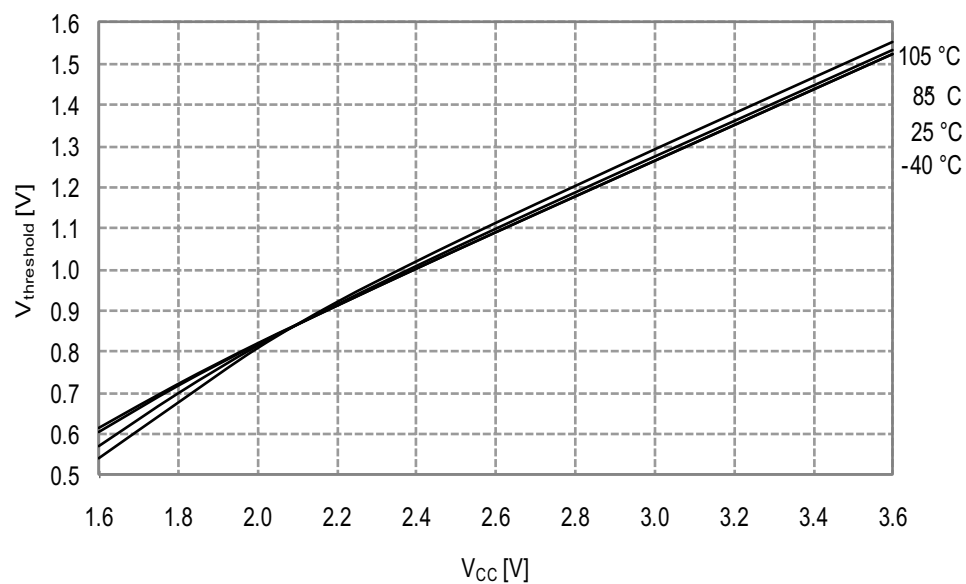


Figure 34-101. I/O Pin Input Hysteresis vs. V_{CC}

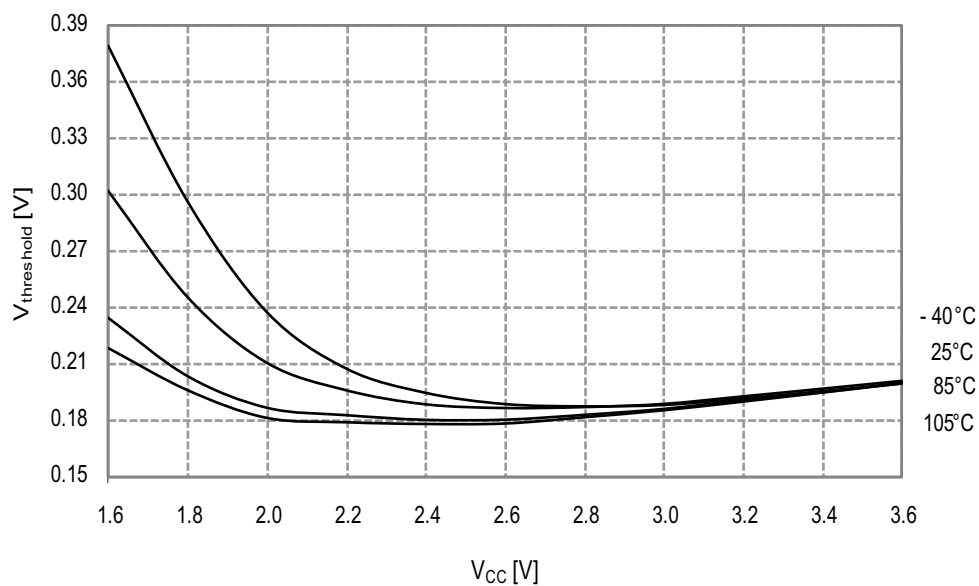


Figure 34-108. Gain Error vs. V_{REF}

$T = 25^{\circ}\text{C}$, $V_{CC} = 3.6\text{V}$, ADC sample rate = 300ksps

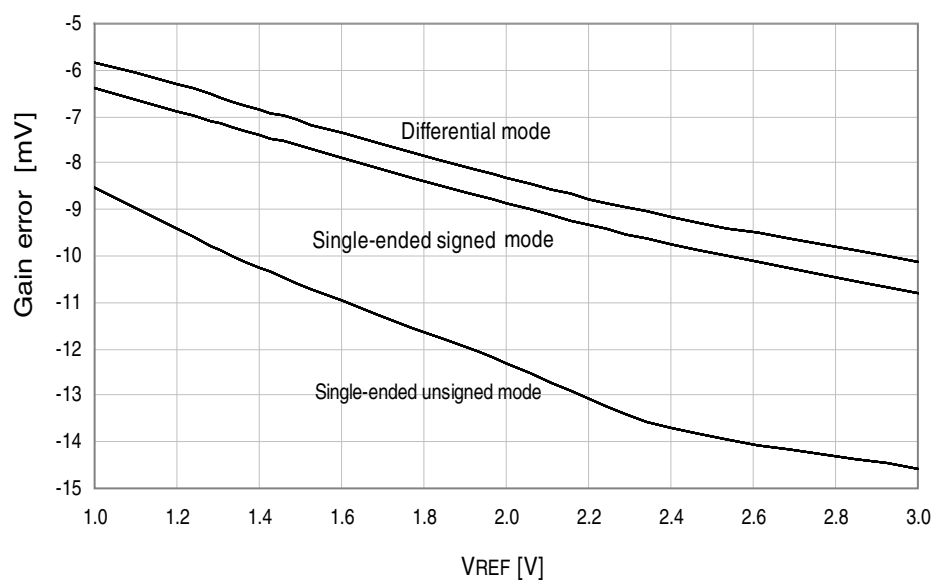


Figure 34-109. Gain Error vs. V_{CC}

$T = 25^{\circ}\text{C}$, $V_{REF} = \text{external } 1.0\text{V}$, ADC sample rate = 300ksps

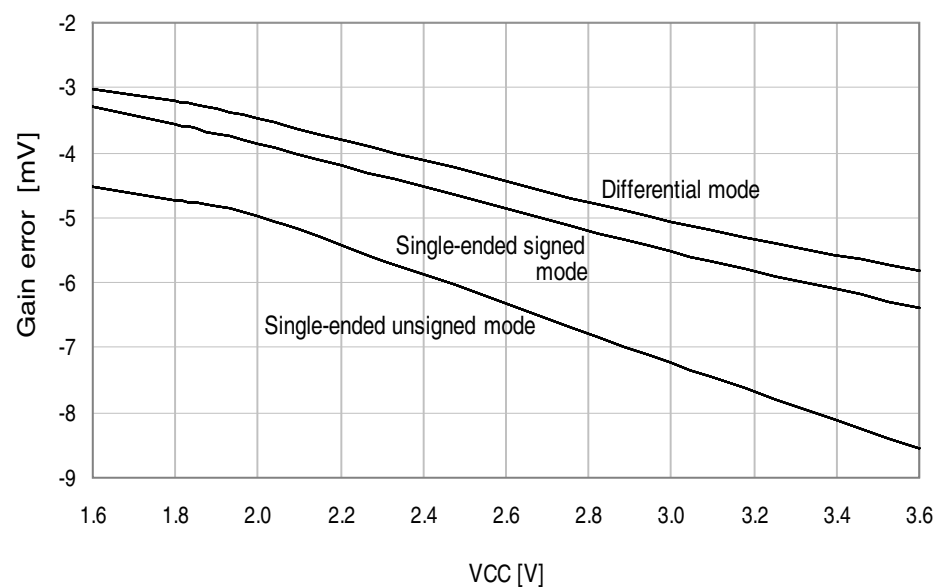


Figure 34-122. Reset Pin Pull-up Resistor Current vs. Reset Pin Voltage

$V_{CC} = 3.0V$

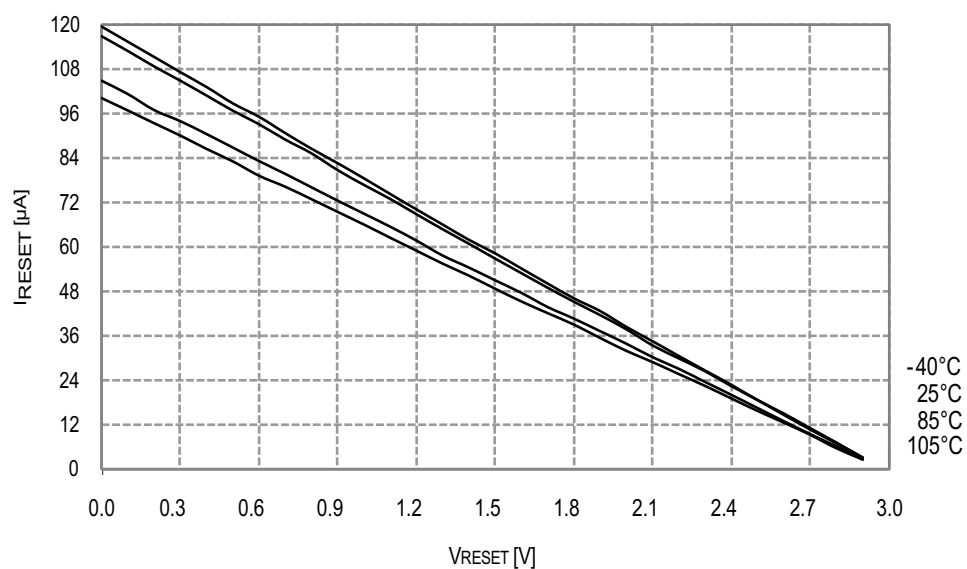
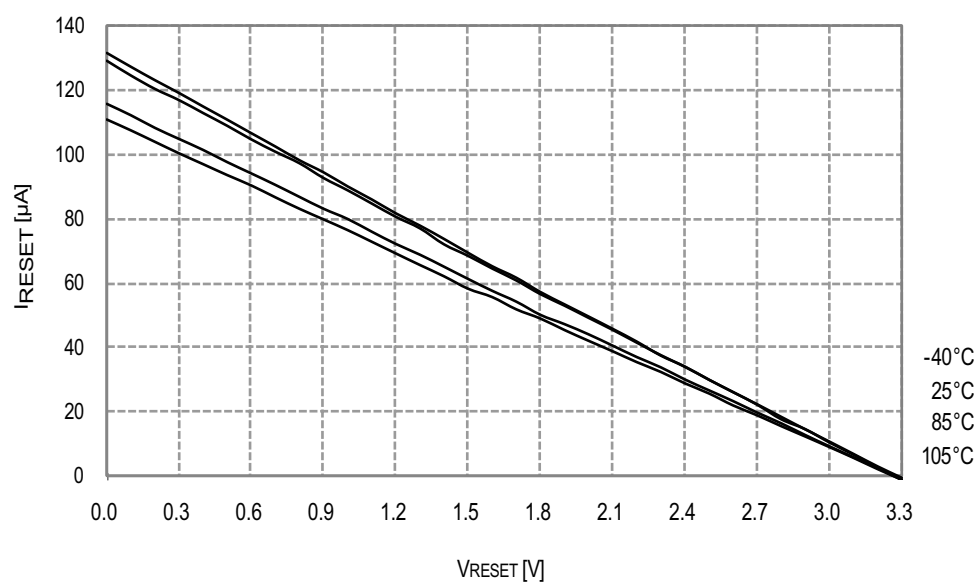


Figure 34-123. Reset Pin Pull-up Resistor Current vs. Reset Pin Voltage

$V_{CC} = 3.3V$



34.3.2.3 Thresholds and Hysteresis

Figure 34-169. I/O Pin Input Threshold Voltage vs. V_{CC}
 V_{IH} I/O pin read as "1"

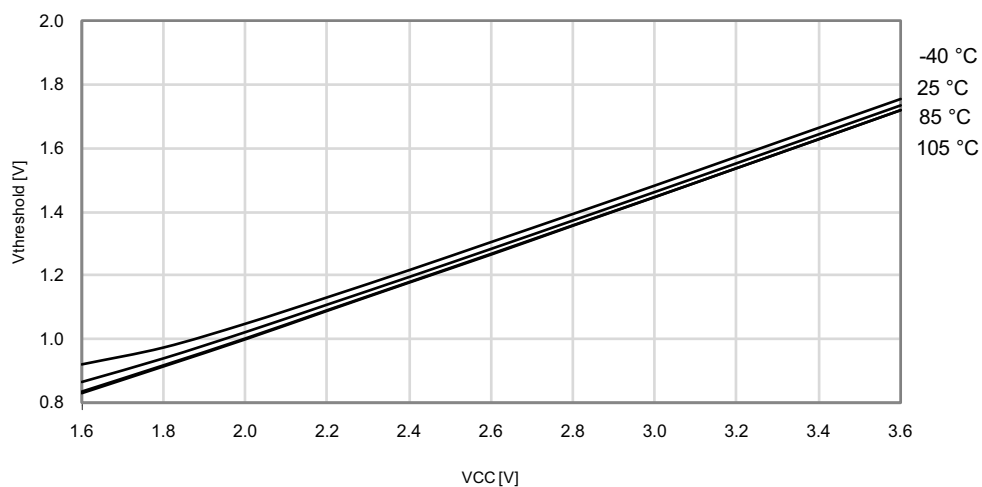


Figure 34-170. I/O Pin Input Threshold Voltage vs. V_{CC}
 V_{IL} I/O pin read as "0"

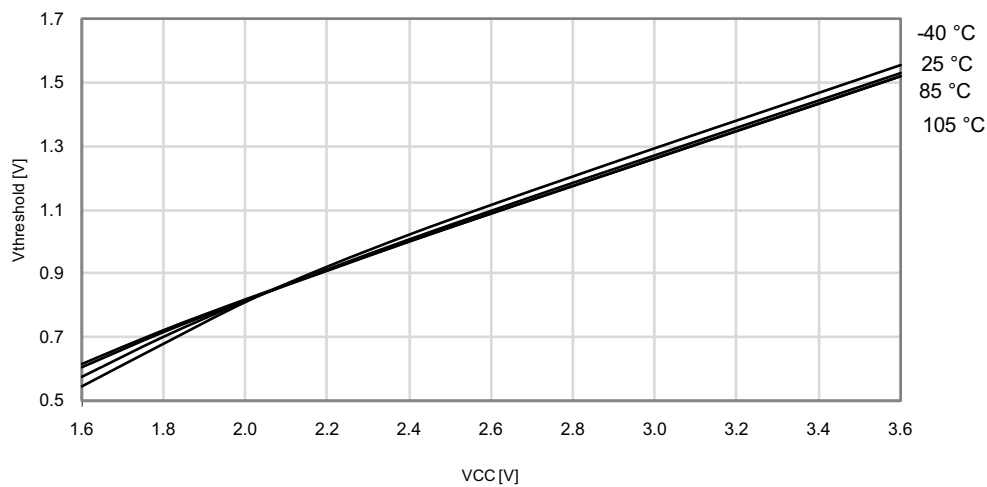


Figure 34-251. Gain Error vs. Temperature

$V_{CC} = 3.0V$, $V_{REF} = \text{external } 2.0V$

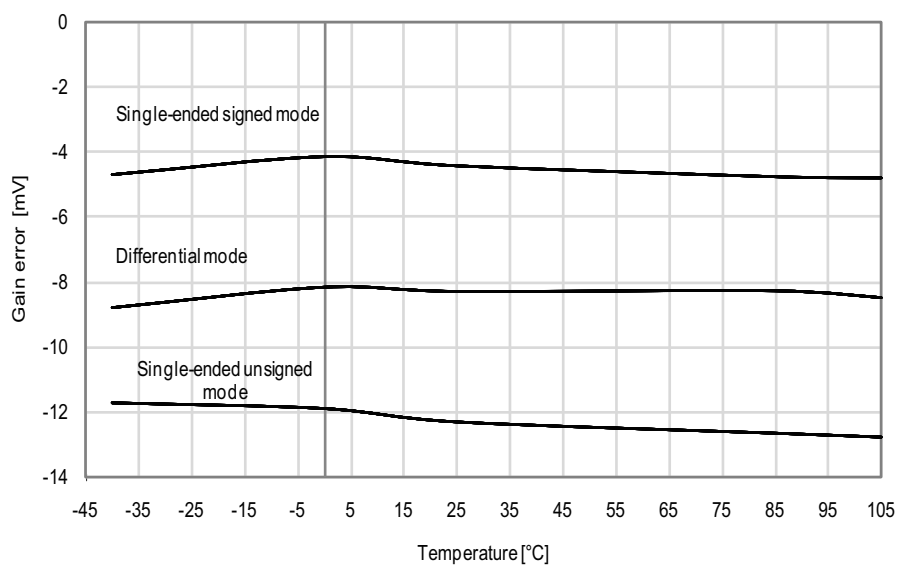


Figure 34-252. Offset Error vs. V_{CC}

$T = 25^{\circ}C$, $V_{REF} = \text{external } 1.0V$, ADC sample rate = 300ksps

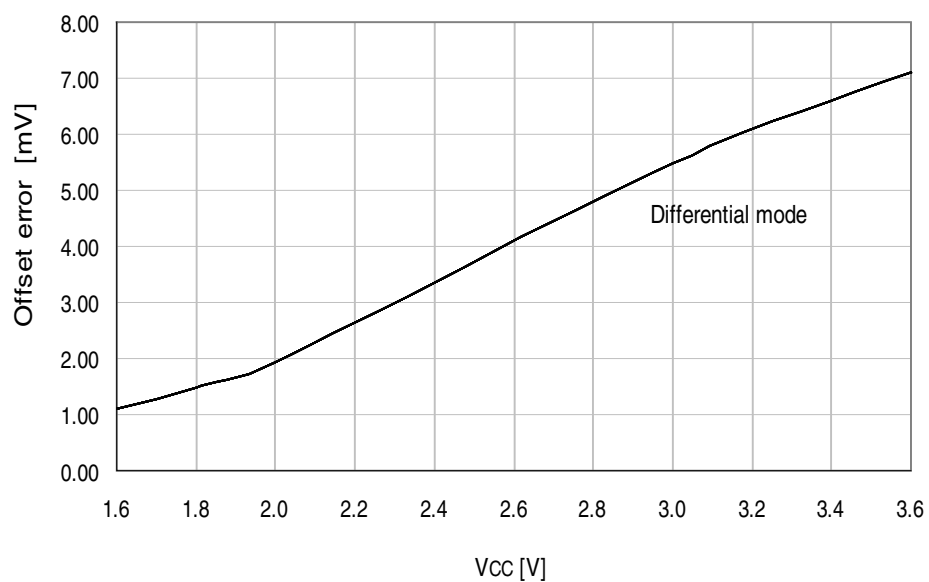
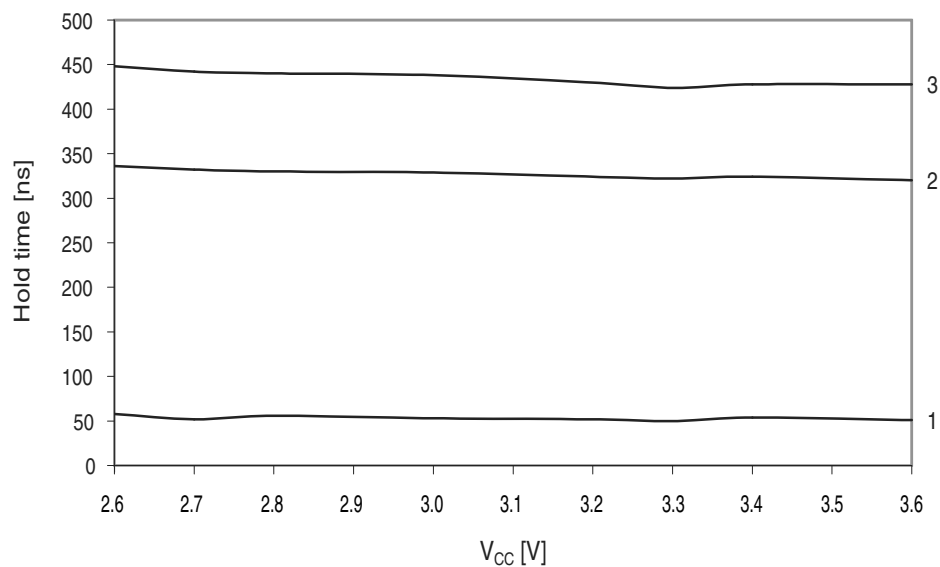


Figure 34-281. SDA Hold Time vs. Supply Voltage



34.4.10 PDI Characteristics

Figure 34-282. Maximum PDI Frequency vs. V_{CC}

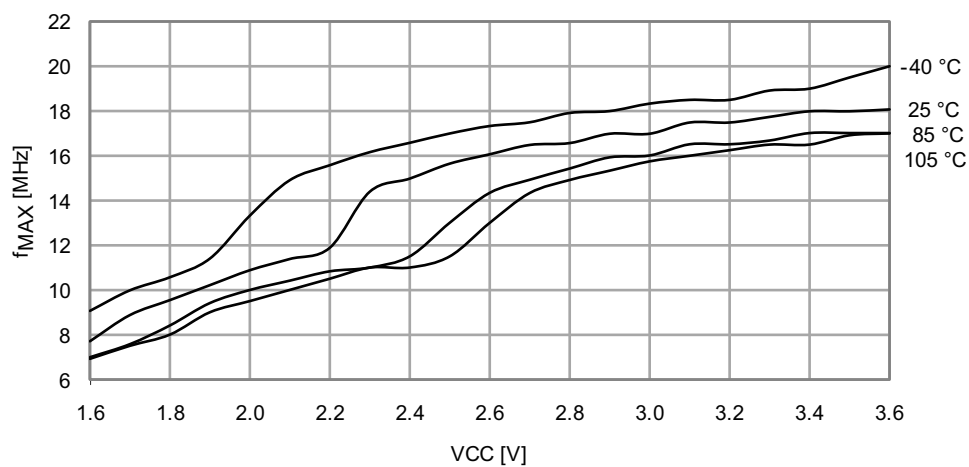


Figure 34-321. Gain Error vs. Temperature

$V_{CC} = 3.0V$, $V_{REF} = \text{external } 2.0V$

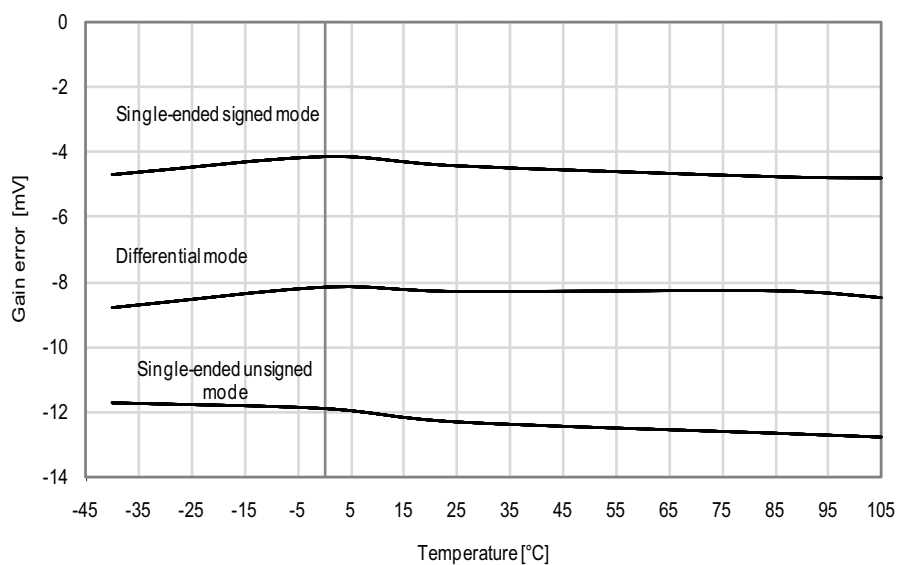


Figure 34-322. Offset Error vs. V_{CC}

$T = 25^{\circ}C$, $V_{REF} = \text{external } 1.0V$, ADC sample rate = 300ksps

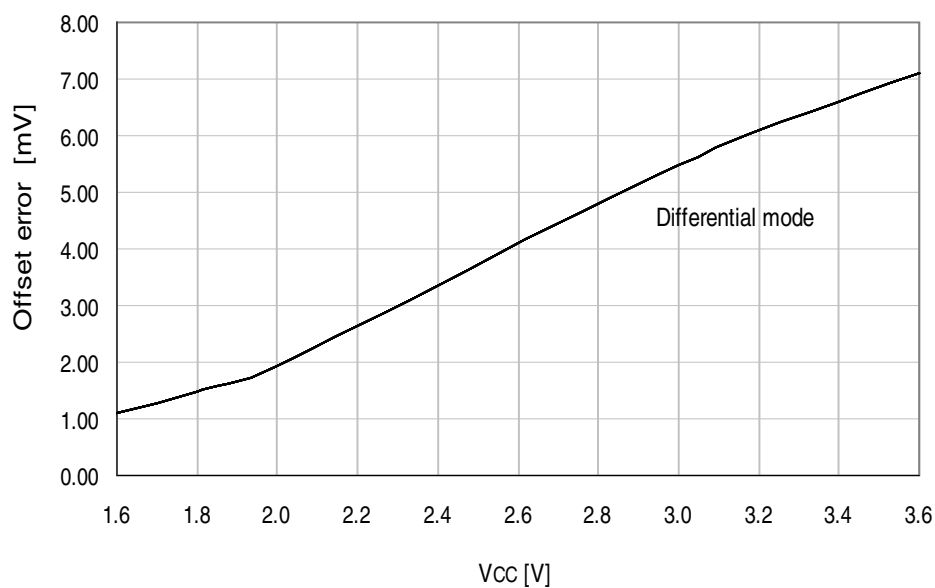


Figure 34-333. Reset Pin Pull-up Resistor Current vs. Reset Pin Voltage

$V_{CC} = 3.3V$

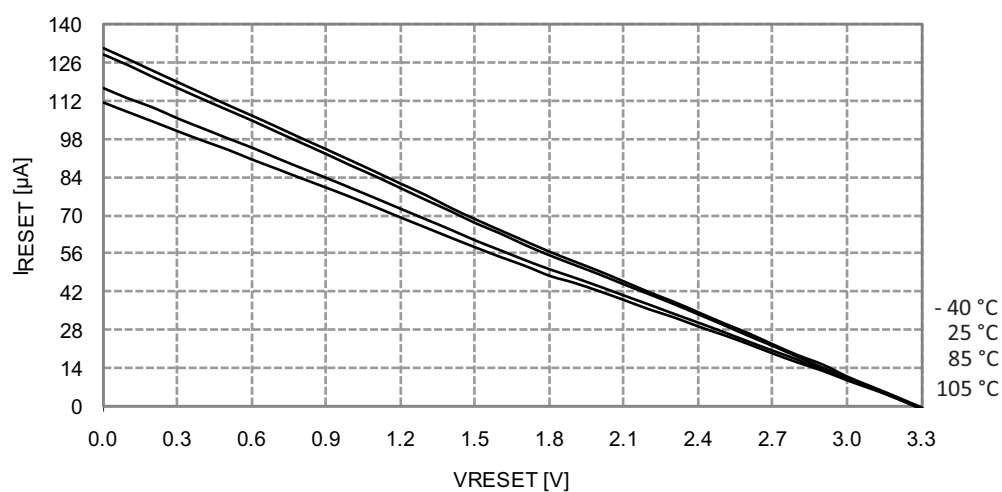
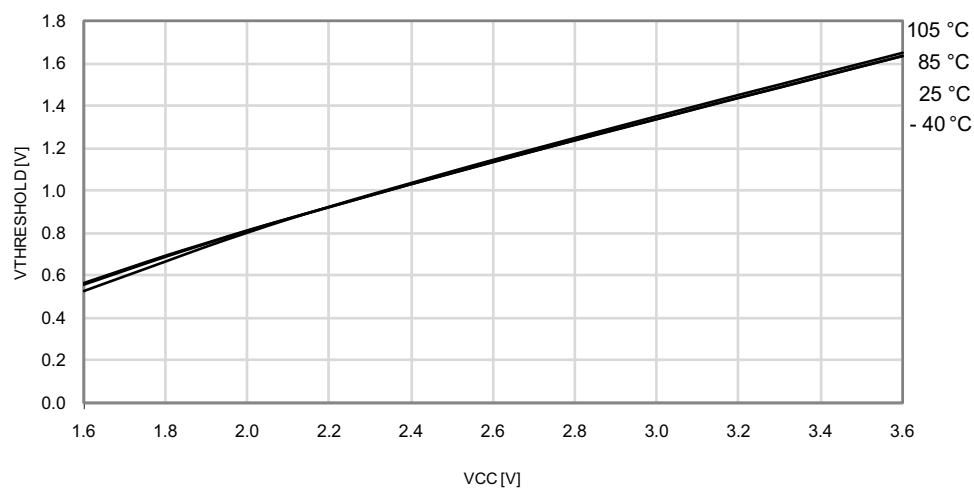


Figure 34-334. Reset Pin Input Threshold Voltage vs. V_{CC}

V_{IH} - Reset pin read as "1"



34.5.8.4 32MHz Internal Oscillator

Figure 34-341. 32MHz Internal Oscillator Frequency vs. Temperature
DPLL disabled

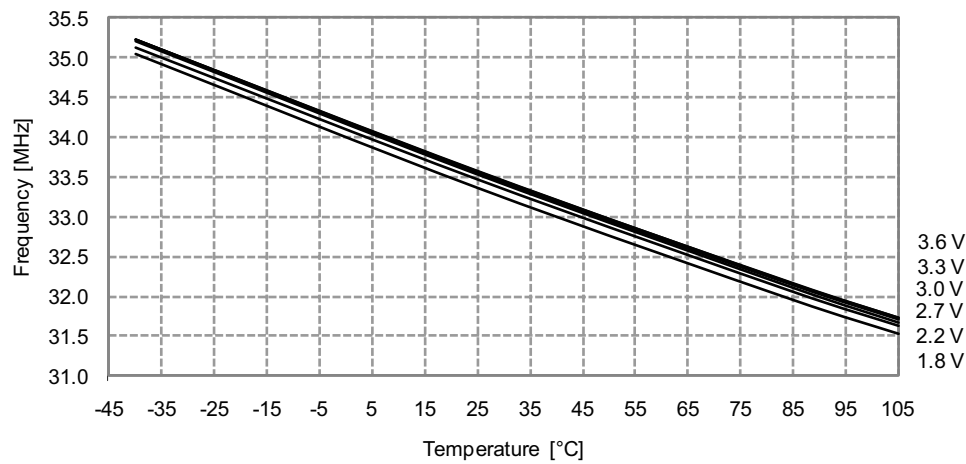


Figure 34-342. 32MHz Internal Oscillator Frequency vs. Temperature
DPLL enabled, from the 32.768kHz internal oscillator

