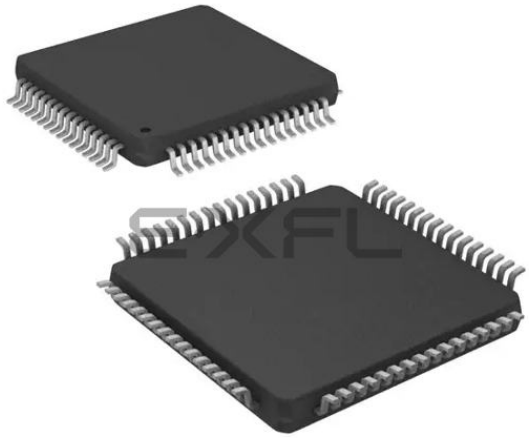

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	50
Program Memory Size	192KB (96K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega192c3-anr

7. Memories

7.1 Features

- Flash program memory
  - One linear address space
  - In-system programmable
  - Self-programming and boot loader support
  - Application section for application code
  - Application table section for application code or data storage
  - Boot section for application code or boot loader code
  - Separate read/write protection lock bits for all sections
  - Built in fast CRC check of a selectable flash program memory section
- Data memory
  - One linear address space
  - Single-cycle access from CPU
  - SRAM
  - EEPROM
    - Byte and page accessible
    - Optional memory mapping for direct load and store
  - I/O memory
    - Configuration and status registers for all peripherals and modules
    - Four bit-accessible general purpose registers for global variables or flags
  - Separate buses for SRAM, EEPROM and I/O memory
    - Simultaneous bus access for CPU
- Production signature row memory for factory programmed data
  - ID for each microcontroller device type
  - Serial number for each device
  - Calibration bytes for factory calibrated peripherals
- User signature row
  - One flash page in size
  - Can be read and written from software
  - Content is kept after chip erase

7.2 Overview

The Atmel AVR architecture has two main memory spaces, the program memory and the data memory. Executable code can reside only in the program memory, while data can be stored in the program memory and the data memory. The data memory includes the internal SRAM, and EEPROM for nonvolatile data storage. All memory spaces are linear and require no memory bank switching. Nonvolatile memory (NVM) spaces can be locked for further write and read/write operations. This prevents unrestricted access to the application software.

A separate memory section contains the fuse bytes. These are used for configuring important system functions, and can only be written by an external programmer.

The available memory size configurations are shown in “Pinout/Block Diagram” on page 4. In addition, each device has a Flash memory signature row for calibration data, device identification, serial number etc.

7.3 Flash Program Memory

The Atmel AVR XMEGA devices contain on-chip, in-system reprogrammable flash memory for program storage. The flash memory can be accessed for read and write from an external programmer through the PDI or from application software running in the device.

10. Power Management and Sleep Modes

10.1 Features

- Power management for adjusting power consumption and functions
- Five sleep modes
  - Idle
  - Power down
  - Power save
  - Standby
  - Extended standby
- Power reduction register to disable clock and turn off unused peripherals in active and idle modes

10.2 Overview

Various sleep modes and clock gating are provided in order to tailor power consumption to application requirements. This enables the Atmel AVR XMEGA microcontroller to stop unused modules to save power.

All sleep modes are available and can be entered from active mode. In active mode, the CPU is executing application code. When the device enters sleep mode, program execution is stopped and interrupts or a reset is used to wake the device again. The application code decides which sleep mode to enter and when. Interrupts from enabled peripherals and all enabled reset sources can restore the microcontroller from sleep to active mode.

In addition, power reduction registers provide a method to stop the clock to individual peripherals from software. When this is done, the current state of the peripheral is frozen, and there is no power consumption from that peripheral. This reduces the power consumption in active mode and idle sleep modes and enables much more fine-tuned power management than sleep modes alone.

10.3 Sleep Modes

Sleep modes are used to shut down modules and clock domains in the microcontroller in order to save power. XMEGA microcontrollers have five different sleep modes tuned to match the typical functional stages during application execution. A dedicated sleep instruction (SLEEP) is available to enter sleep mode. Interrupts are used to wake the device from sleep, and the available interrupt wake-up sources are dependent on the configured sleep mode. When an enabled interrupt occurs, the device will wake up and execute the interrupt service routine before continuing normal program execution from the first instruction after the SLEEP instruction. If other, higher priority interrupts are pending when the wake-up occurs, their interrupt service routines will be executed according to their priority before the interrupt service routine for the wake-up interrupt is executed. After wake-up, the CPU is halted for four cycles before execution starts.

The content of the register file, SRAM and registers are kept during sleep. If a reset occurs during sleep, the device will reset, start up, and execute from the reset vector.

10.3.1 Idle Mode

In idle mode the CPU and nonvolatile memory are stopped (note that any ongoing programming will be completed), but all peripherals, including the interrupt controller, and event system are kept running. Any enabled interrupt will wake the device.

10.3.2 Power-down Mode

In power-down mode, all clocks, including the real-time counter clock source, are stopped. This allows operation only of asynchronous modules that do not require a running clock. The only interrupts that can wake up the MCU are the two-wire interface address match interrupt, asynchronous port interrupts, and the USB resume interrupt.

33.1.5 I/O Pin Characteristics

The I/O pins complies with the JEDEC LVTTL and LVCMOS specification and the high- and low-level input and output voltage limits reflect or exceed this specification.

Table 33-7. I/O Pin Characteristics

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{OH} (1)/ I_{OL} (2)	I/O pin source/sink current			-15		15	mA
V_{IH}	High level input voltage	V_{CC} = 2.4 - 3.6V		0.7*Vcc		V_{CC}+0.5	V
		V_{CC} = 1.6 - 2.4V		0.8*V_{CC}		V_{CC}+0.5	
V_{IL}	Low level input voltage	V_{CC} = 2.4 - 3.6V		-0.5		0.3*V_{CC}	
		V_{CC} = 1.6 - 2.4V		-0.5		0.2*V_{CC}	
V_{OH}	High level output voltage	V_{CC} = 3.3V	I_{OH} = -4mA	2.6	2.9		
		V_{CC} = 3.0V	I_{OH} = -3mA	2.1	2.6		
		V_{CC} = 1.8V	I_{OH} = -1mA	1.4	1.6		
V_{OL}	Low level output voltage	V_{CC} = 3.3V	I_{OL} = 8mA		0.4	0.76	
		V_{CC} = 3.0V	I_{OL} = 5mA		0.3	0.64	
		V_{CC} = 1.8V	I_{OL} = 3mA		0.2	0.46	
I_{IN}	Input leakage current I/O pin	T = 25°C			<0.01	1.0	µA
R_P	Pull/Bus keeper resistor				25		kΩ

Notes:
1. The sum of all I_{OH} for PORTA and PORTB must not exceed 100mA.
   The sum of all I_{OH} for PORTC, PORTD, and PORTE must for each port not exceed 200mA.
   The sum of all I_{OH} for pins PF[0-5] on PORTF must not exceed 200mA.
   The sum of all I_{OL} for pins PF[6-7] on PORTF, PORTR, and PDI must not exceed 100mA.
2. The sum of all I_{OL} for PORTA and PORTB must not exceed 100mA.
   The sum of all I_{OL} for PORTC, PORTD, and PORTE must for each port not exceed 200mA.
   The sum of all I_{OL} for pins PF[0-5] on PORTF must not exceed 200mA.
   The sum of all I_{OL} for pins PF[6-7] on PORTF, PORTR, and PDI must not exceed 100mA.

33.2.3 Current Consumption

Table 33-33. Current Consumption for Active Mode and Sleep Modes

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{CC}	Active power consumption(1)	32kHz, Ext. Clk	V_{CC} = 1.8V		50		µA
			V_{CC} = 3.0V		130		
		1MHz, Ext. Clk	V_{CC} = 1.8V		215		
			V_{CC} = 3.0V		475		
		2MHz, Ext. Clk	V_{CC} = 1.8V		445	600	
			V_{CC} = 3.0V		0.95	1.5	mA
		32MHz, Ext. Clk			7.8	12	
	Idle power consumption(2)	32kHz, Ext. Clk	V_{CC} = 1.8V		2.8		µA
			V_{CC} = 3.0V		3.0		
		1MHz, Ext. Clk	V_{CC} = 1.8V		46		
			V_{CC} = 3.0V		92		
		2MHz, Ext. Clk	V_{CC} = 1.8V		93	225	
			V_{CC} = 3.0V		184	350	
		32MHz, Ext. Clk			2.9	5.0	mA
	Power-down power consumption	T = 25°C	V_{CC} = 3.0V		0.07	1.0	µA
		T = 85°C			1.3	5.0	
		T = 105°C			4.0	8.0	
		WDT and sampled BOD enabled, T = 25°C	V_{CC} = 3.0V		1.4	2.0	
		WDT and sampled BOD enabled, T = 85°C			2.6	6.0	
		WDT and sampled BOD enabled, T = 105°C			5.0	10	
	Power-save power consumption(3)	RTC from ULP clock, WDT and sampled BOD enabled, T = 25°C	V_{CC} = 1.8V		1.7		
			V_{CC} = 3.0V		1.8		
		RTC from 1.024kHz low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.7	2.0	
			V_{CC} = 3.0V		0.8	2.0	
		RTC from low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.9	3.0	
			V_{CC} = 3.0V		1.2	3.0	
	Reset power consumption	Current through $\overline{\text{RESET}}$ pin substracted	V_{CC} = 3.0V		120		

Notes:
1. All Power Reduction Registers set including FPRM and EPRM.
2. All Power Reduction Registers set without FPRM and EPRM.
3. Maximum limits are based on characterization, and not tested in production.

33.4.6 ADC Characteristics

Table 33-95. Power Supply, Reference, and Input Range

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
AV_{CC}	Analog supply voltage		V_{CC}- 0.3		V_{CC}+ 0.3	V
V_{REF}	Reference voltage		1		AV_{CC}- 0.6	
R_{in}	Input resistance	Switched			4.5	kΩ
C_{in}	Input capacitance	Switched			5	pF
R_{AREF}	Reference input resistance	(leakage only)		>10		MΩ
C_{AREF}	Reference input capacitance	Static load		7		pF
Vin	Input range		0		V_{REF}	V
	Conversion range	Differential mode, Vinp - Vinn	-V_{REF}		V_{REF}	
	Conversion range	Single ended unsigned mode, Vinp	-ΔV		V_{REF}-ΔV	
ΔV	Fixed offset voltage			200		lsb

Table 33-96. Clock and Timing

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{ADC}	ADC Clock frequency	Maximum is 1/4 of peripheral clock frequency	100		1800	kHz
		Measuring internal signals	100		125	
f_{ClkADC}	Sample rate		16		300	ksps
f_{ADC}	Sample rate	Current limitation (CURRLIMIT) off	16		300	
		CURRLIMIT = LOW	16		250	
		CURRLIMIT = MEDIUM	16		150	
		CURRLIMIT = HIGH	16		50	
	Sampling time	Configurable in steps of 1/2 Clk_{ADC} cycles up to 32 Clk_{ADC} cycles	0.28		320	µs
	Conversion time (latency)	(RES+2)/2+1+ GAIN RES (Resolution) = 8 or 12, GAIN=0 to 3	5.5		10	Clk_{ADC} cycles
	Start-up time	ADC clock cycles		12	24	
	ADC settling time	After changing reference or input mode		7	7	

33.4.13.5 Internal Phase Locked Loop (PLL) Characteristics

Table 33-110. Internal PLL Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{IN}	Input frequency	Output frequency must be within f_{OUT}	0.4		64	MHz
f_{OUT}	Output frequency (1)	V_{CC}= 1.6 - 1.8V	20		48	
		V_{CC}= 2.7 - 3.6V	20		128	
	Start-up time			25		µs
	Re-lock time			25		

Note: 1. The maximum output frequency vs. supply voltage is linear between 1.8V and 2.7V, and can never be higher than four times the maximum CPU frequency.

33.4.13.6 External Clock Characteristics

Figure 33-24.External Clock Drive Waveform

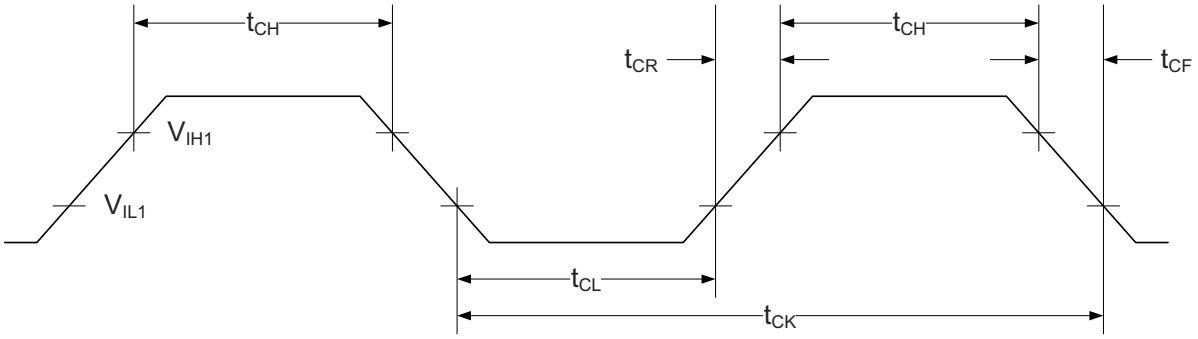


Table 33-111.External Clock used as System Clock without Prescaling

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock Frequency (1)	V_{CC} = 1.6 - 1.8V	0		12	MHz
		V_{CC} = 2.7 - 3.6V	0		32	
t_{CK}	Clock Period	V_{CC} = 1.6 - 1.8V	83.3			ns
		V_{CC} = 2.7 - 3.6V	31.5			
t_{CH}	Clock High Time	V_{CC} = 1.6 - 1.8V	30.0			
		V_{CC} = 2.7 - 3.6V	12.5			
t_{CL}	Clock Low Time	V_{CC} = 1.6 - 1.8V	30.0			
		V_{CC} = 2.7 - 3.6V	12.5			
t_{CR}	Rise Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			10	
		V_{CC} = 2.7 - 3.6V			3	
t_{CF}	Fall Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			10	
		V_{CC} = 2.7 - 3.6V			3	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Note: 1. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

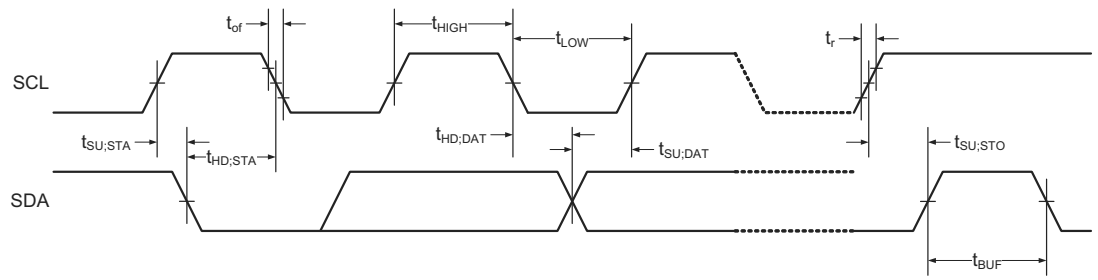
Table 33-115.SPI Timing Characteristics and Requirements

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_{SCK}	SCK period	Master		(See Table 20-3 in XMEGA C Manual)		ns
t_{SCKW}	SCK high/low width	Master		0.5*SCK		
t_{SCKR}	SCK rise time	Master		2.7		
t_{SCKF}	SCK fall time	Master		2.7		
t_{MIS}	MISO setup to SCK	Master		10		
t_{MIH}	MISO hold after SCK	Master		10		
t_{MOS}	MOSI setup SCK	Master		0.5*SCK		
t_{MOH}	MOSI hold after SCK	Master		1		
t_{SSCK}	Slave SCK period	Slave	4*t Clk_{PER}			
t_{SSCKW}	SCK high/low width	Slave	2*t Clk_{PER}			
t_{SSCKR}	SCK rise time	Slave			1600	
t_{SSCKF}	SCK fall time	Slave			1600	
t_{SIS}	MOSI setup to SCK	Slave	3			
t_{SIH}	MOSI hold after SCK	Slave	t Clk_{PER}			
t_{SSS}	$\overline{SS}$ setup to SCK	Slave	21			
t_{SSH}	$\overline{SS}$ hold after SCK	Slave	20			
t_{SOS}	MISO setup SCK	Slave		8		
t_{SOH}	MISO hold after SCK	Slave		13		
t_{SOSS}	MISO setup after $\overline{SS}$ low	Slave		11		
t_{SOSH}	MISO hold after $\overline{SS}$ high	Slave		8		

33.4.15 Two-Wire Interface Characteristics

Table 33-116 describes the requirements for devices connected to the Two-Wire Interface Bus. The Atmel AVR XMEGA Two-Wire Interface meets or exceeds these requirements under the noted conditions. Timing symbols refer to Figure 33-28.

Figure 33-28.Two-wire Interface Bus Timing



33.5.3 Current Consumption

Table 33-120.Current Consumption for Active Mode and Sleep Modes

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{CC}	Active power consumption(1)	32kHz, Ext. Clk	V_{CC} = 1.8V		60		µA
			V_{CC} = 3.0V		140		
		1MHz, Ext. Clk	V_{CC} = 1.8V		245		
			V_{CC} = 3.0V		550		
		2MHz, Ext. Clk	V_{CC} = 1.8V		440	700	
			V_{CC} = 3.0V		0.9	1.5	mA
		32MHz, Ext. Clk			9.0	15	
	Idle power consumption(2)	32kHz, Ext. Clk	V_{CC} = 1.8V		3.0		µA
			V_{CC} = 3.0V		3.5		
		1MHz, Ext. Clk	V_{CC} = 1.8V		55		
			V_{CC} = 3.0V		110		
		2MHz, Ext. Clk	V_{CC} = 1.8V		105	350	
			V_{CC} = 3.0V		215	650	
		32MHz, Ext. Clk			3.4	8.0	mA
	Power-down power consumption	T = 25°C	V_{CC} = 3.0V		0.1	1.0	µA
		T = 85°C			3.5	6.0	
		T = 105°C			10	15	
		WDT and sampled BOD enabled, T = 25°C	V_{CC} = 3.0V		1.5	2.0	
		WDT and sampled BOD enabled, T = 85°C			5.8	10	
		WDT and sampled BOD enabled, T = 105°C			12	20	
	Power-save power consumption(3)	RTC from ULP clock, WDT and sampled BOD enabled, T = 25°C	V_{CC} = 1.8V		1.3		
			V_{CC} = 3.0V		1.4		
		RTC from 1.024kHz low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.7	2.0	
			V_{CC} = 3.0V		0.8	2.0	
		RTC from low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.9	3.0	
			V_{CC} = 3.0V		1.1	3.0	
	Reset power consumption	Current through $\overline{\text{RESET}}$ pin substracted	V_{CC} = 3.0V		170		

Notes:
1. All Power Reduction Registers set including FPRM and EPRM.
2. All Power Reduction Registers set without FPRM and EPRM.
3. Maximum limits are based on characterization, and not tested in production.

34.1.3 ADC Characteristics

Figure 34-31. INL Error vs. External V_{REF}

T = 25°C, V_{CC} = 3.6V, external reference

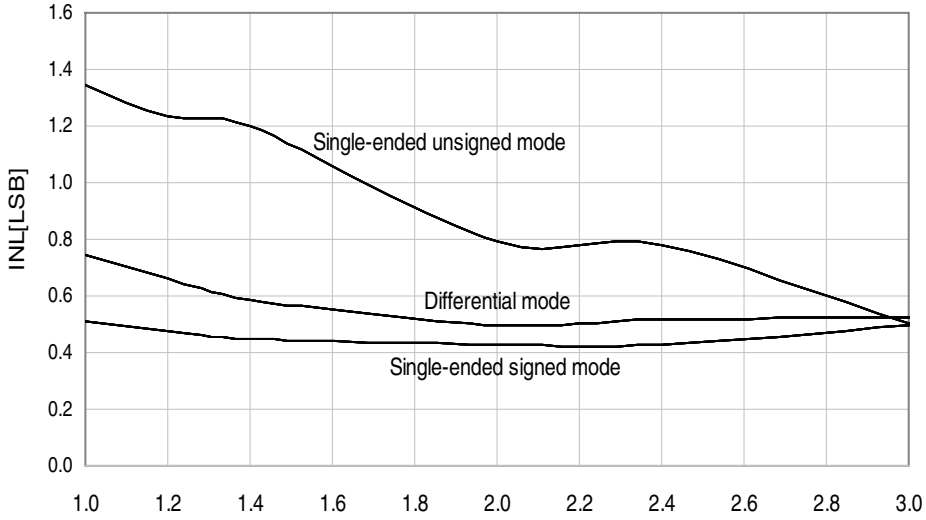
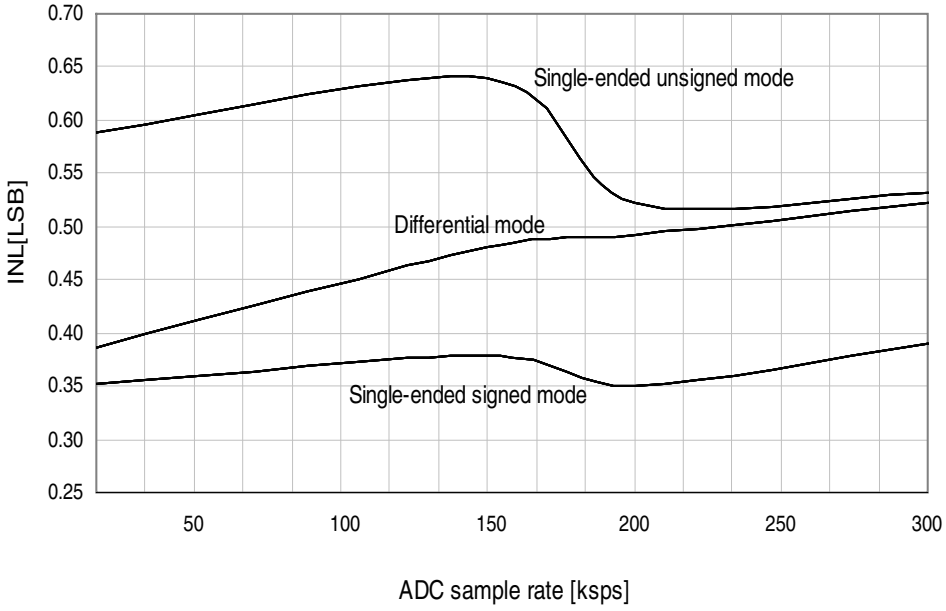


Figure 34-32. INL Error vs. Sample Rate

T = 25°C, V_{CC} = 3.6V, V_{REF} = 3.0V external



34.1.8.2 32.768kHz Internal Oscillator

Figure 34-55. 32.768kHz Internal Oscillator Frequency vs. Temperature

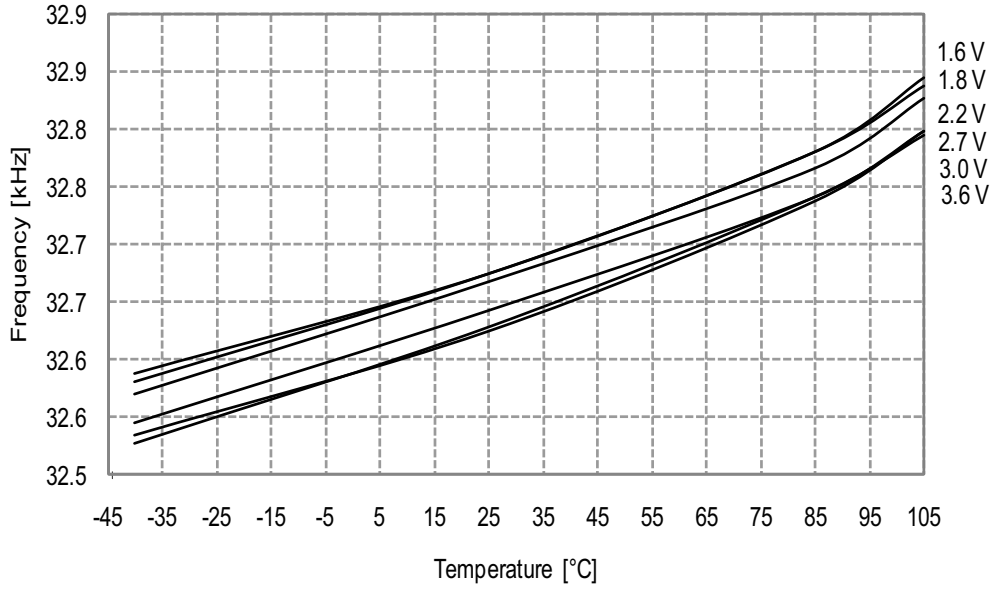


Figure 34-56. 32.768kHz Internal Oscillator Frequency vs. Calibration Value

V_{CC} = 3.0V, T = 25°C

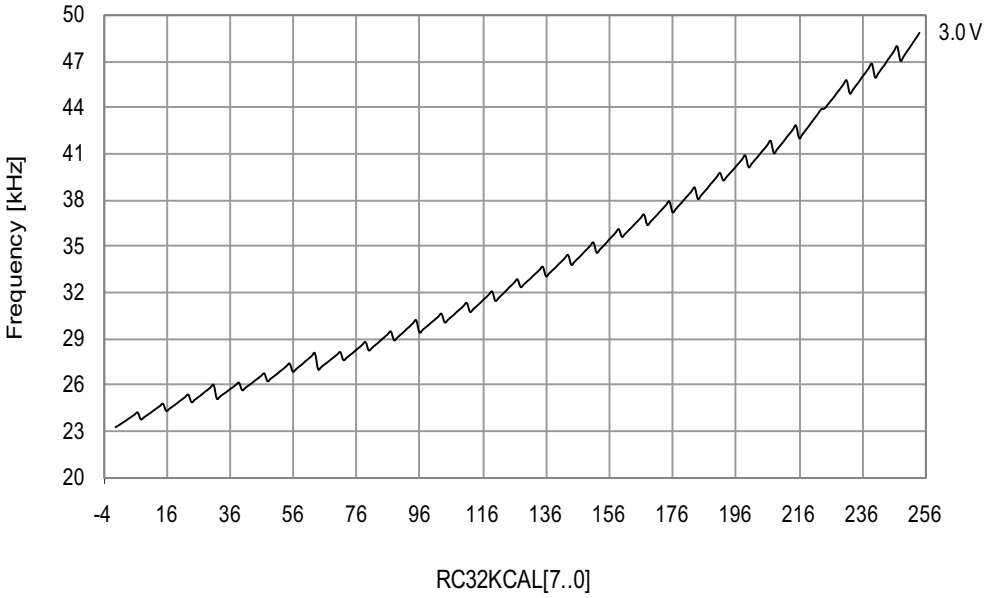


Figure 34-153. Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 1MHz external clock

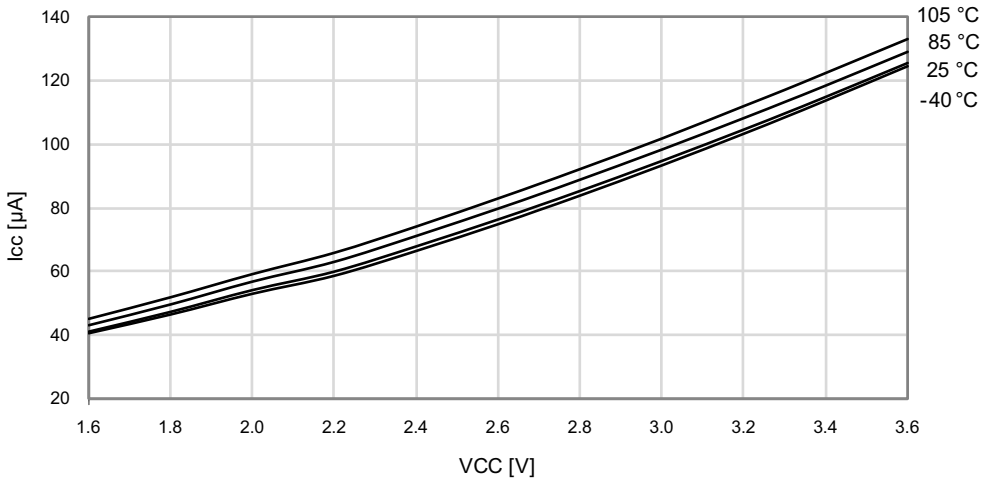


Figure 34-154. Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 2MHz internal oscillator

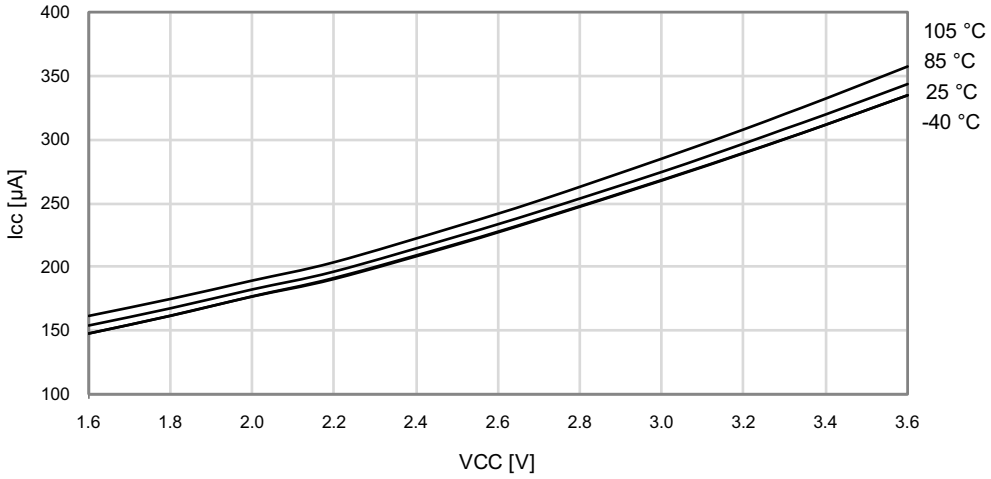


Figure 34-177. DNL Error vs. Input Code

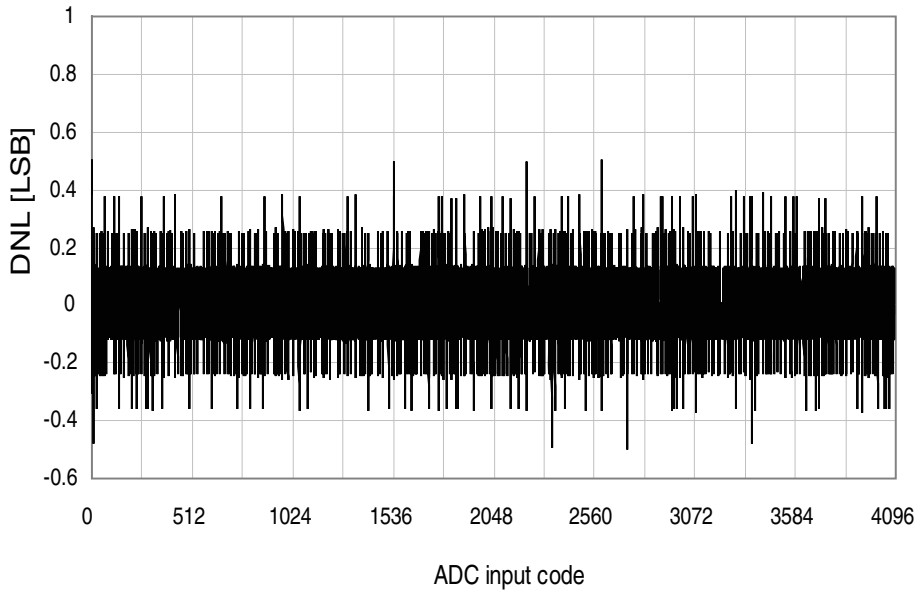
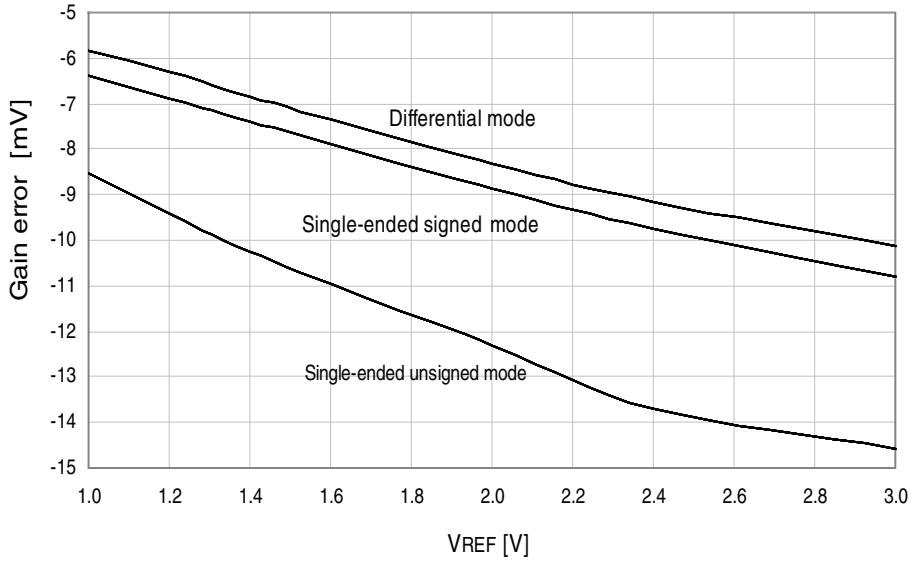


Figure 34-178. Gain Error vs. V_{REF}

T = 25°C, V_{CC} = 3.6V, ADC sample rate = 300ksps



34.4.1.3 Power-down Mode Supply Current

Figure 34-227. Power-down Mode Supply Current vs. V_{CC}
All functions disabled

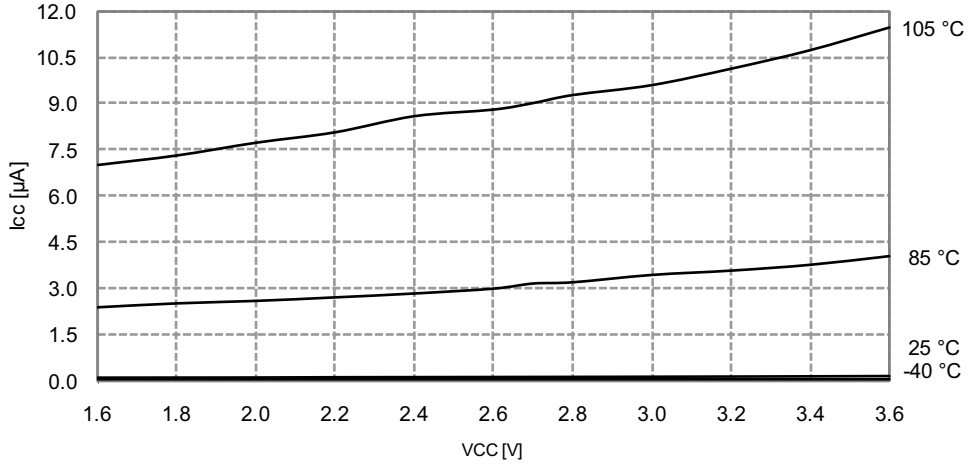
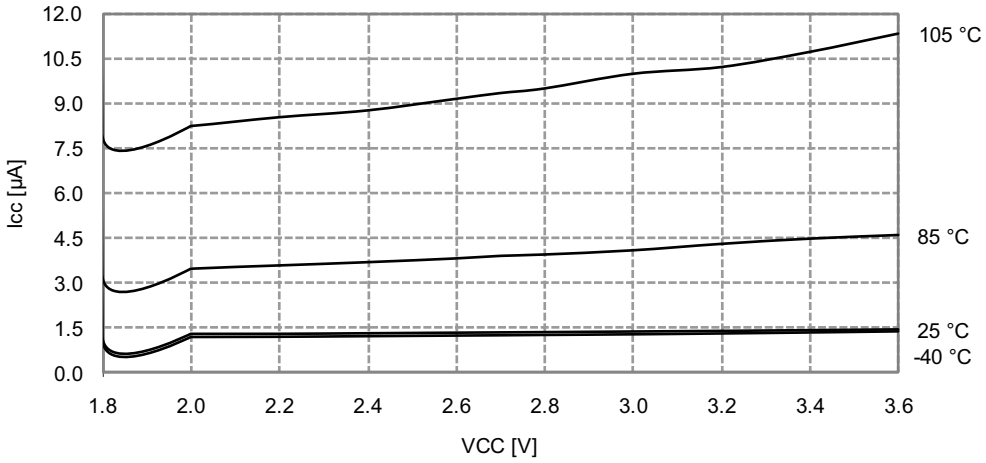


Figure 34-228. Power-down Mode Supply Current vs. V_{CC}
Watchdog and sampled BOD enabled



34.4.2.3 Thresholds and Hysteresis

Figure 34-239. I/O Pin Input Threshold Voltage vs. V_{CC}

V_{IH} I/O pin read as "1"

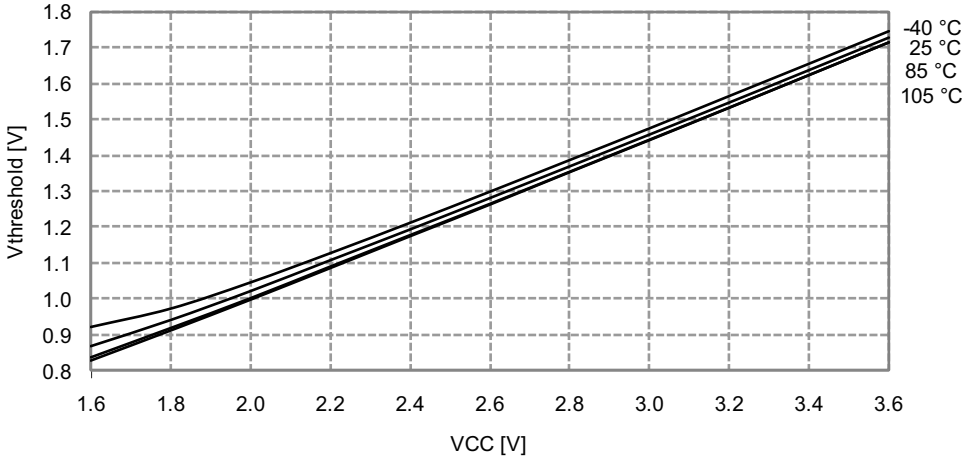


Figure 34-240. I/O Pin Input Threshold Voltage vs. V_{CC}

V_{IL} I/O pin read as "0"

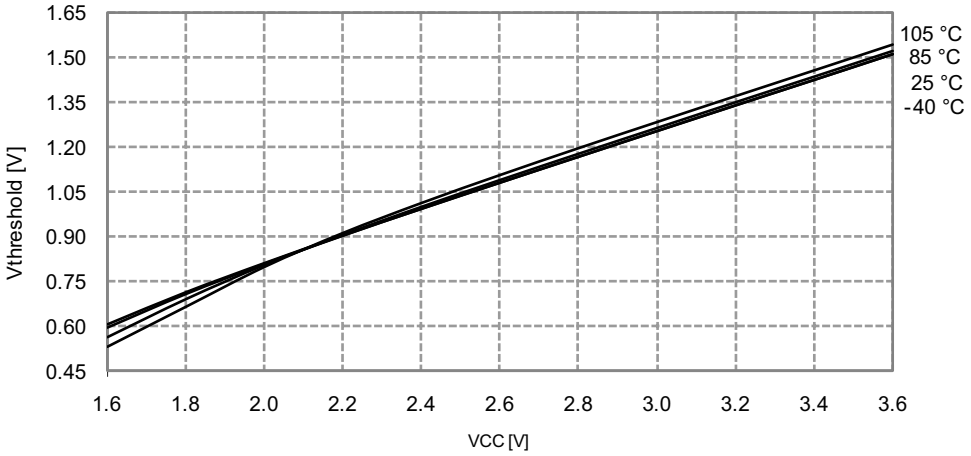


Figure 34-273. 32MHz Internal Oscillator CALA Calibration Step Size

T = -40°C, V_{CC} = 3.0V

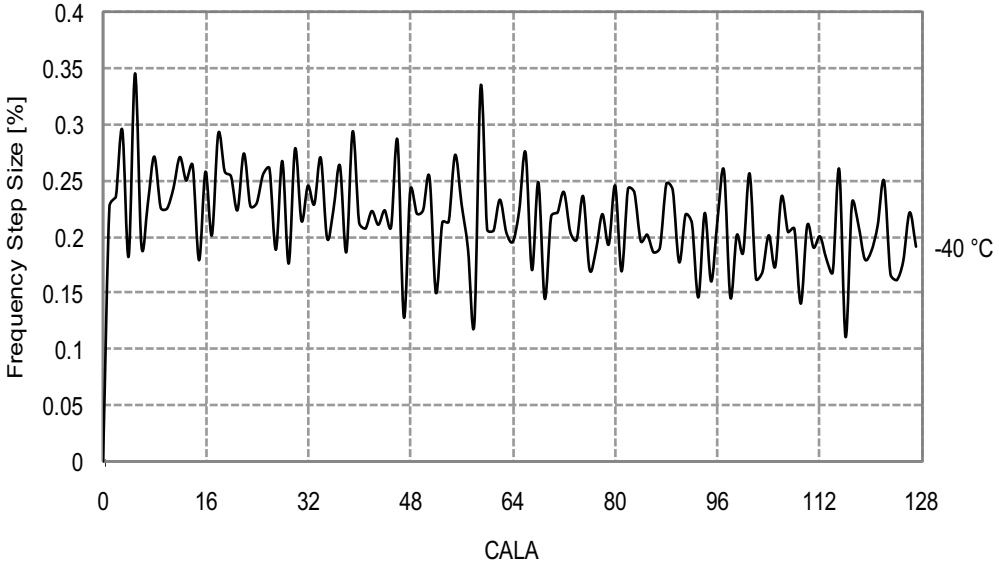


Figure 34-274. 32MHz Internal Oscillator CALA Calibration Step Size

T = 25°C, V_{CC} = 3.0V

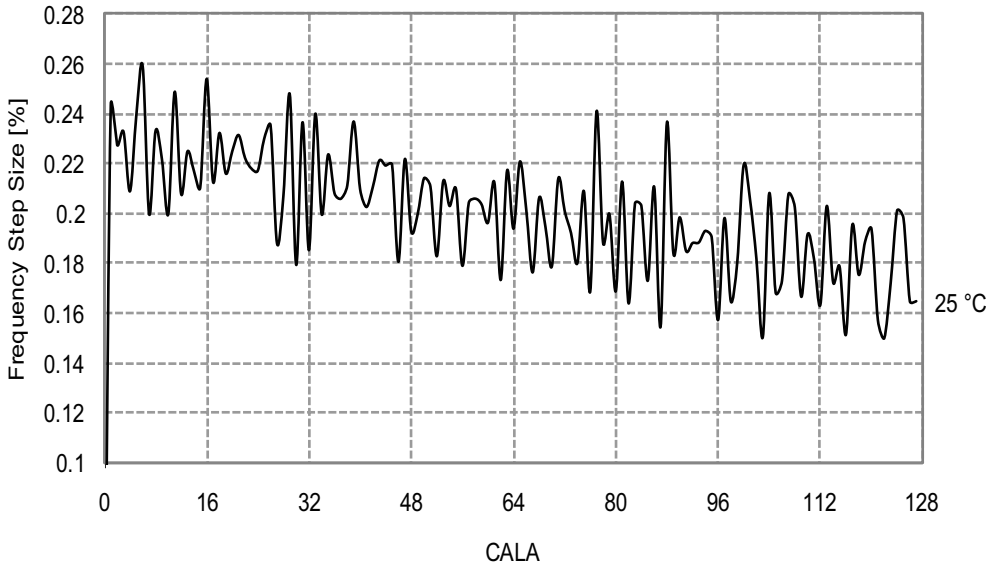
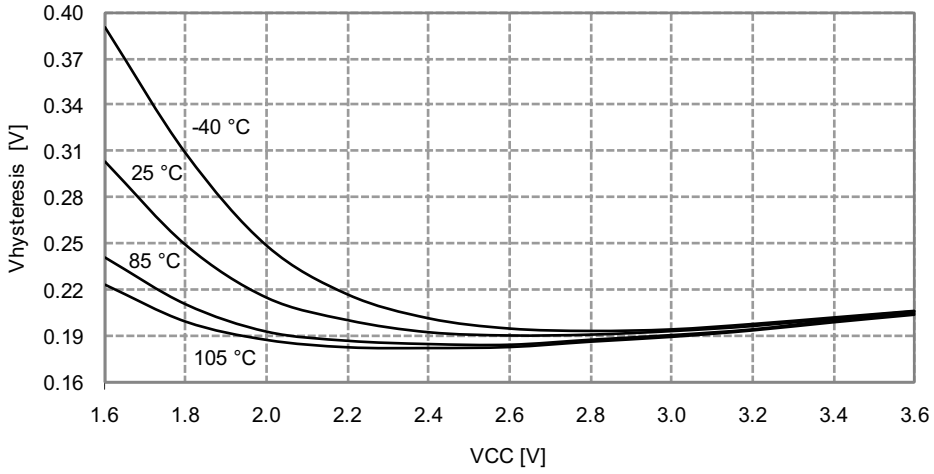


Figure 34-311. I/O Pin Input Hysteresis vs. V_{CC}



34.5.3 ADC Characteristics

Figure 34-312. INL Error vs. External V_{REF}

T = 25°C, V_{CC} = 3.6V, external reference

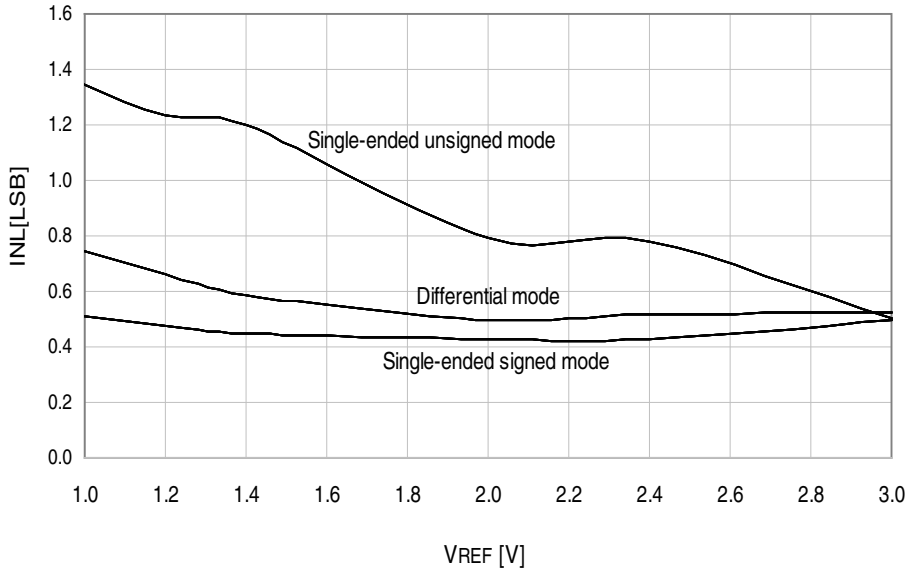


Figure 34-315. DNL Error vs. External V_{REF}

T = 25°C, V_{CC} = 3.6V, external reference

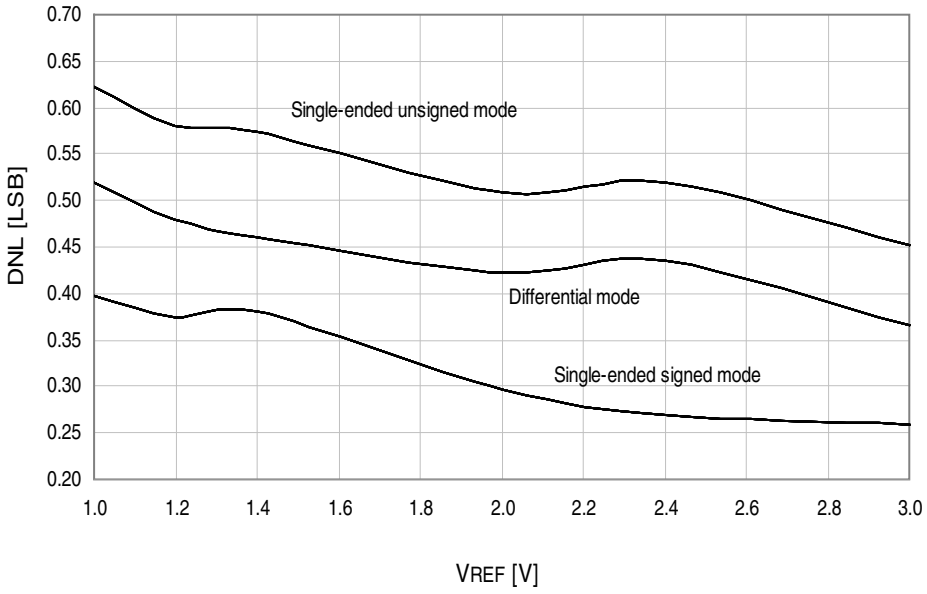
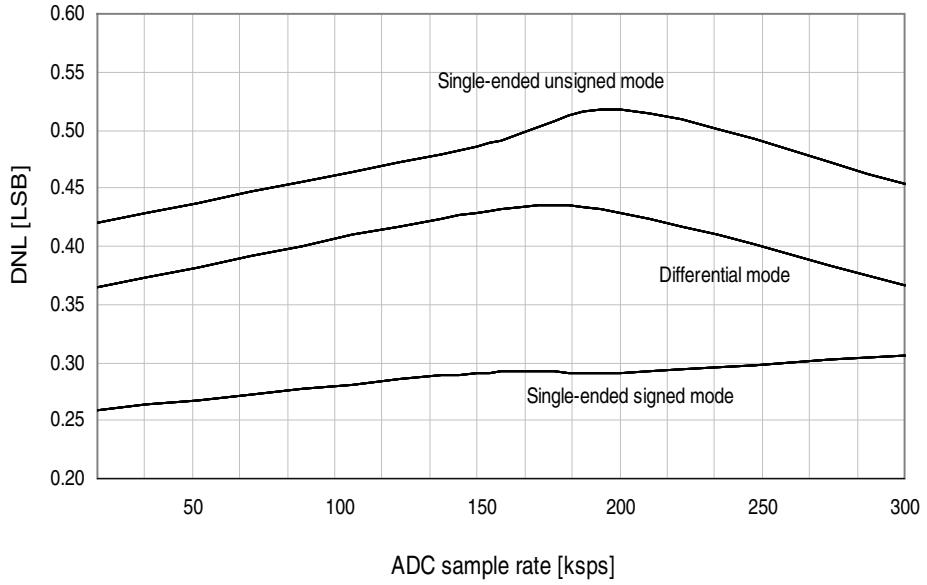


Figure 34-316. DNL Error vs. Sample Rate

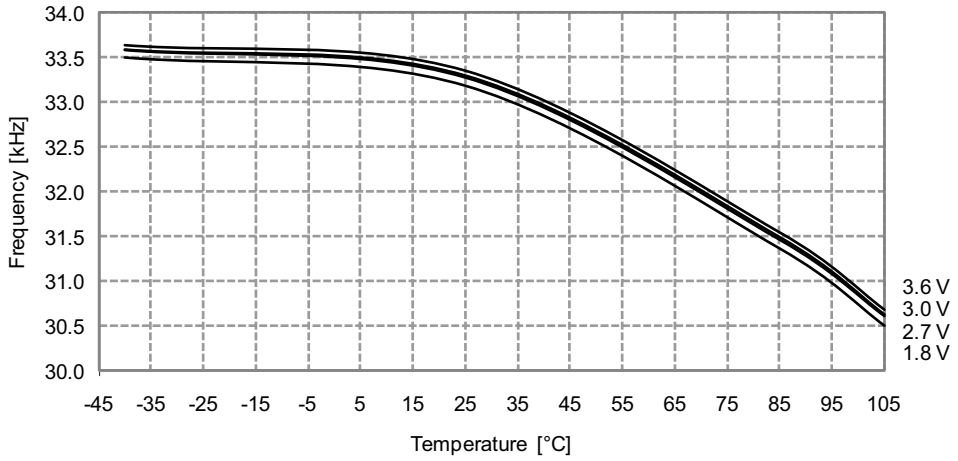
T = 25°C, V_{CC} = 3.6V, V_{REF} = 3.0V external



34.5.8 Oscillator Characteristics

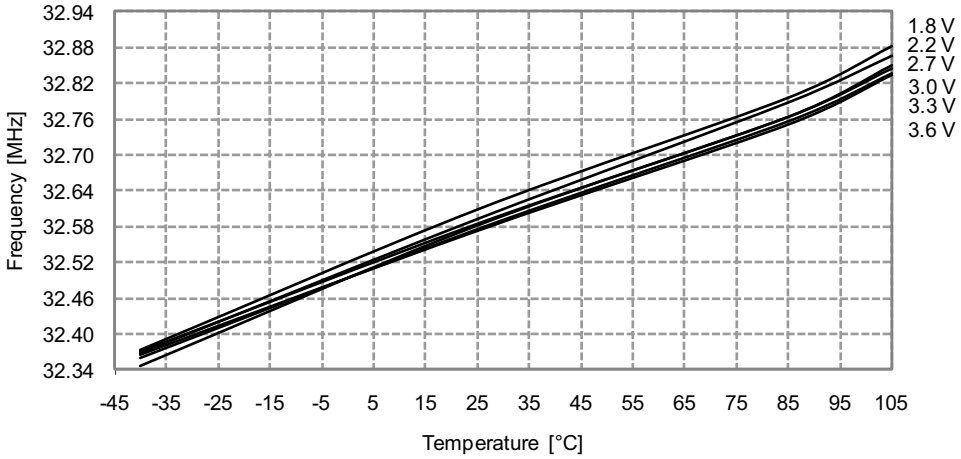
34.5.8.1 Ultra Low-Power Internal Oscillator

Figure 34-335. Ultra Low-Power Internal Oscillator Frequency vs. Temperature



34.5.8.2 32.768kHz Internal Oscillator

Figure 34-336. 32.768kHz Internal Oscillator Frequency vs. Temperature



35.5 Atmel ATxmega32C3

35.5.1 Rev I

- AC system status flags are only valid if AC-system is enabled
- Temperature sensor not calibrated

1. AC system status flags are only valid if AC-system is enabled

The status flags for the ac-output are updated even though the AC is not enabled which is invalid. Also, it is not possible to clear the AC interrupt flags without enabling either of the Analog comparators.

Problem fix/Workaround

Software should clear the AC system flags once, after enabling the AC system before using the AC system status flags.

2. Temperature sensor not calibrated

Temperature sensor factory calibration not implemented.

Problem fix/Workaround

None.

35.5.2 Rev A - H

Not sampled.