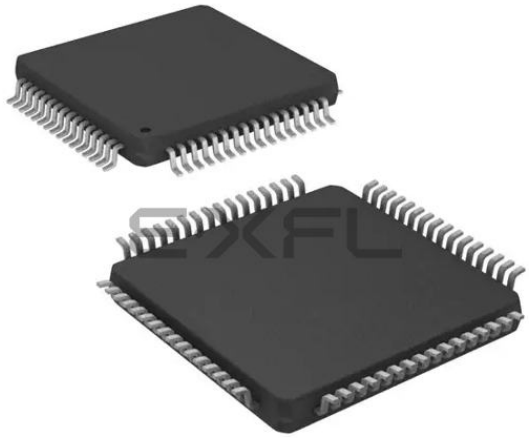

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	50
Program Memory Size	192KB (96K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega192c3-aur

The arithmetic logic unit (ALU) supports arithmetic and logic operations between registers or between a constant and a register. Single-register operations can also be executed in the ALU. After an arithmetic operation, the status register is updated to reflect information about the result of the operation.

The ALU is directly connected to the fast-access register file. The 32 x 8-bit general purpose working registers all have single clock cycle access time allowing single-cycle arithmetic logic unit (ALU) operation between registers or between a register and an immediate. Six of the 32 registers can be used as three 16-bit address pointers for program and data space addressing, enabling efficient address calculations.

The memory spaces are linear. The data memory space and the program memory space are two different memory spaces.

The data memory space is divided into I/O registers, SRAM, and external RAM. In addition, the EEPROM can be memory mapped in the data memory.

All I/O status and control registers reside in the lowest 4KB addresses of the data memory. This is referred to as the I/O memory space. The lowest 64 addresses can be accessed directly, or as the data space locations from 0x00 to 0x3F. The rest is the extended I/O memory space, ranging from 0x0040 to 0x0FFF. I/O registers here must be accessed as data space locations using load (LD/LDS/LDD) and store (ST/STS/STD) instructions.

The SRAM holds data. Code execution from SRAM is not supported. It can easily be accessed through the five different addressing modes supported in the AVR architecture. The first SRAM address is 0x2000.

Data addresses 0x1000 to 0x1FFF are reserved for memory mapping of EEPROM.

The program memory is divided in two sections, the application program section and the boot program section. Both sections have dedicated lock bits for write and read/write protection. The SPM instruction that is used for self-programming of the application flash memory must reside in the boot program section. The application section contains an application table section with separate lock bits for write and read/write protection. The application table section can be used for safe storing of nonvolatile data in the program memory.

6.4 ALU - Arithmetic Logic Unit

The arithmetic logic unit (ALU) supports arithmetic and logic operations between registers or between a constant and a register. Single-register operations can also be executed. The ALU operates in direct connection with all 32 general purpose registers. In a single clock cycle, arithmetic operations between general purpose registers or between a register and an immediate are executed and the result is stored in the register file. After an arithmetic or logic operation, the status register is updated to reflect information about the result of the operation.

ALU operations are divided into three main categories – arithmetic, logical, and bit functions. Both 8- and 16-bit arithmetic is supported, and the instruction set allows for efficient implementation of 32-bit aritmetic. The hardware multiplier supports signed and unsigned multiplication and fractional format.

6.4.1 Hardware Multiplier

The multiplier is capable of multiplying two 8-bit numbers into a 16-bit result. The hardware multiplier supports different variations of signed and unsigned integer and fractional numbers:

- Multiplication of unsigned integers
- Multiplication of signed integers
- Multiplication of a signed integer with an unsigned integer
- Multiplication of unsigned fractional numbers
- Multiplication of signed fractional numbers
- Multiplication of a signed fractional number with an unsigned one

A multiplication takes two CPU clock cycles.

All AVR CPU instructions are 16 or 32 bits wide, and each flash location is 16 bits wide. The flash memory is organized in two main sections, the application section and the boot loader section. The sizes of the different sections are fixed, but device-dependent. These two sections have separate lock bits, and can have different levels of protection. The store program memory (SPM) instruction, which is used to write to the flash from the application software, will only operate when executed from the boot loader section.

The application section contains an application table section with separate lock settings. This enables safe storage of nonvolatile data in the program memory.

Figure 7-1. Flash Program Memory (hexadecimal address)

Word Address									
ATxmega256C3		**ATxmega192C3**		**ATxmega128C3**		**ATxmega64C3**		**ATxmega32C3**	
0		0		0		0		0	Application section (256K/192K/128K/64K/32K)
									.....
1EFFF	/	16FFF	/	EFFF	/	77FF	/	37FF	
1F000	/	17000	/	F000	/	7800	/	3800	Application table section (8K/8K/8K/4K/4K)
1FFFF	/	17FFF	/	FFFF	/	7FFF	/	3FFF	
20000	/	18000	/	10000	/	8000	/	4000	Boot section (8K/8K/8K/4K/4K)
20FFF	/	18FFF	/	10FFF	/	87FF	/	47FF	

7.3.1 Application Section

The Application section is the section of the flash that is used for storing the executable application code. The protection level for the application section can be selected by the boot lock bits for this section. The application section can not store any boot loader code since the SPM instruction cannot be executed from the application section.

7.3.2 Application Table Section

The application table section is a part of the application section of the flash memory that can be used for storing data. The size is identical to the boot loader section. The protection level for the application table section can be selected by the boot lock bits for this section. The possibilities for different protection levels on the application section and the application table section enable safe parameter storage in the program memory. If this section is not used for data, application code can reside here.

7.3.3 Boot Loader Section

While the application section is used for storing the application code, the boot loader software must be located in the boot loader section because the SPM instruction can only initiate programming when executing from this section. The SPM instruction can access the entire flash, including the boot loader section itself. The protection level for the boot loader section can be selected by the boot loader lock bits. If this section is not used for boot loader software, application code can be stored here.

7.3.4 Production Signature Row

The production signature row is a separate memory section for factory programmed data. It contains calibration data for functions such as oscillators and analog modules. Some of the calibration values will be automatically loaded to the corresponding module or peripheral unit during reset. Other values must be loaded from the signature row and written to the corresponding peripheral registers from software. For details on calibration conditions, refer to “Electrical Characteristics” on page 65.

7.8 Memory Timing

Read and write access to the I/O memory takes one CPU clock cycle. A write to SRAM takes one cycle, and a read from SRAM takes two cycles. EEPROM page load (write) takes one cycle, and three cycles are required for read. For burst read, new data are available every second cycle. Refer to the instruction summary for more details on instructions and instruction timing.

7.9 Device ID and Revision

Each device has a three-byte device ID. This ID identifies Atmel as the manufacturer of the device and the device type. A separate register contains the revision number of the device.

7.10 I/O Memory Protection

Some features in the device are regarded as critical for safety in some applications. Due to this, it is possible to lock the I/O register related to the clock system, the event system, and the advanced waveform extensions. As long as the lock is enabled, all related I/O registers are locked and they can not be written from the application software. The lock registers themselves are protected by the configuration change protection mechanism.

7.11 Flash and EEPROM Page Size

The flash program memory and EEPROM data memory are organized in pages. The pages are word accessible for the flash and byte accessible for the EEPROM.

Table 7-2 on page 16 shows the Flash Program Memory organization and Program Counter (PC) size. Flash write and erase operations are performed on one page at a time, while reading the Flash is done one byte at a time. For Flash access the Z-pointer (Z[m:n]) is used for addressing. The most significant bits in the address (FPAGE) give the page number and the least significant address bits (FWORD) give the word in the page.

Table 7-2. Number of Words and Pages in the Flash

Devices	PC size	Flash size	Page size	FWORD	FPAGE	Application		Boot	
	bits	bytes	words			Size	No. of pages	Size	No. of pages
ATxmega32C3	16	32K + 4K	128	Z[7:1]	Z[16:8]	32K	128	4K	16
ATxmega64C3	16	64K + 4K	128	Z[7:1]	Z[16:8]	64K	256	4K	16
ATxmega128C3	17	128K + 8K	256	Z[8:1]	Z[17:9]	128K	256	8K	16
ATxmega192C3	17	192K + 8K	256	Z[8:1]	Z[17:9]	192K	384	8K	16
ATxmega256C3	18	256K + 8K	256	Z[8:1]	Z[18:9]	256K	512	8K	16

Table 7-3 on page 17 shows EEPROM memory organization. EEEPROM write and erase operations can be performed one page or one byte at a time, while reading the EEPROM is done one byte at a time. For EEPROM access the NVM address register (ADDR[m:n]) is used for addressing. The most significant bits in the address (E2PAGE) give the page number and the least significant address bits (E2BYTE) give the byte in the page.

Table 7-3. Number of Bytes and Pages in the EEPROM

Devices	EEPROM	Page size	E2BYTE	E2PAGE	No. of pages
	Size	bytes			
ATxmega32C3	1K	32	ADDR[4:0]	ADDR[10:5]	64
ATxmega64C3	2K	32	ADDR[4:0]	ADDR[10:5]	64
ATxmega128C3	2K	32	ADDR[4:0]	ADDR[10:5]	64
ATxmega192C3	2K	32	ADDR[4:0]	ADDR[10:5]	64
ATxmega256C3	4K	32	ADDR[4:0]	ADDR[11:5]	128

Multipacket transfer enables a data payload exceeding the maximum packet size of an endpoint to be transferred as multiple packets without software intervention. This reduces the CPU intervention and the interrupts needed for USB transfers.

For low-power operation, the USB module can put the microcontroller into any sleep mode when the USB bus is idle and a suspend condition is given. Upon bus resumes, the USB module can wake up the microcontroller from any sleep mode.

PORTD has one USB. Notation of this is USB.

33.1.3 Current Consumption

Table 33-4. Current Consumption for Active Mode and Sleep Modes

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{CC}	Active power consumption(1)	32kHz, Ext. Clk	V_{CC} = 1.8V		50		µA
			V_{CC} = 3.0V		130		
		1MHz, Ext. Clk	V_{CC} = 1.8V		215		
			V_{CC} = 3.0V		475		
		2MHz, Ext. Clk	V_{CC} = 1.8V		445	600	
			V_{CC} = 3.0V		0.95	1.5	mA
		32MHz, Ext. Clk			7.8	12	
	Idle power consumption(2)	32kHz, Ext. Clk	V_{CC} = 1.8V		2.8		µA
			V_{CC} = 3.0V		3.0		
		1MHz, Ext. Clk	V_{CC} = 1.8V		46		
			V_{CC} = 3.0V		92		
		2MHz, Ext. Clk	V_{CC} = 1.8V		93	225	
			V_{CC} = 3.0V		184	350	
		32MHz, Ext. Clk			2.9	5.0	mA
	Power-down power consumption	T = 25°C	V_{CC} = 3.0V		0.07	1.0	µA
		T = 85°C			1.3	5.0	
		T = 105°C			4.0	8.0	
		WDT and sampled BOD enabled, T = 25°C	V_{CC} = 3.0V		1.4	2.0	
		WDT and sampled BOD enabled, T = 85°C			2.6	6.0	
		WDT and sampled BOD enabled, T = 105°C			5.0	10	
	Power-save power consumption(3)	RTC from ULP clock, WDT and sampled BOD enabled, T = 25°C	V_{CC} = 1.8V		1.7		
			V_{CC} = 3.0V		1.8		
		RTC from 1.024kHz low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.7	2.0	
			V_{CC} = 3.0V		0.8	2.0	
		RTC from low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.9	3.0	
			V_{CC} = 3.0V		1.2	3.0	
	Reset power consumption	Current through $\overline{\text{RESET}}$ pin substracted	V_{CC} = 3.0V		120		

Notes:
1. All Power Reduction Registers set including FPRM and EPRM.
2. All Power Reduction Registers set without FPRM and EPRM.
3. Maximum limits are based on characterization, and not tested in production.

33.2.8 Bandgap and Internal 1.0V Reference Characteristics

Table 33-42. Bandgap and Internal 1.0V Reference Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Startup time	As reference for ADC		1 Clk_{PER} + 2.5µs		µs
		As input voltage to ADC and AC		1.5		
	Bandgap voltage			1.1		V
INT1V	Internal 1.00V reference	T= 85°C, calibrated at 85°C	0.99	1.0	1.01	
		T= 105°C, calibrated at 85°C	0.99	1.0	1.01	
	Variation over voltage and temperature	Calibrated at T= 85°C		1		%

33.2.9 Brownout Detection Characteristics

Table 33-43. Brownout Detection Characteristics(1)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{BOT}	BOD level 0 falling V_{CC}		1.40	1.60	1.70	V
	BOD level 1 falling V_{CC}			1.8		
	BOD level 2 falling V_{CC}			2.0		
	BOD level 3 falling V_{CC}			2.2		
	BOD level 4 falling V_{CC}			2.4		
	BOD level 5 falling V_{CC}			2.6		
	BOD level 6 falling V_{CC}			2.8		
	BOD level 7 falling V_{CC}			3.0		
t_{BOD}	Detection time	Continuous mode		0.4		µs
		Sampled mode		1000		
V_{HYST}	Hysteresis			1.0		%

Note: 1. BOD is calibrated at 85°C within BOD level 0 values, and BOD level 0 is the default level.

33.2.10 External Reset Characteristics

Table 33-44. External Reset Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_{EXT}	Minimum reset pulse width		1000	90		ns
V_{RST}	Reset threshold voltage	V_{CC} = 2.7 - 3.6V		0.45*V_{CC}		V
		V_{CC} = 1.6 - 2.7V		0.45*V_{CC}		
R_{RST}	Reset pin Pull-up Resistor			25		kΩ

33.3.11 Power-on Reset Characteristics

Table 33-74. Power-on Reset Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{POT-} (1)	POR threshold voltage falling V_{CC}	V_{CC} falls faster than 1V/ms	0.4	1.0		V
		V_{CC} falls at 1V/ms or slower	0.8	1.3		
V_{POT+}	POR threshold voltage rising V_{CC}			1.3	1.59	

Note: 1. V_{POT-} values are only valid when BOD is disabled. When BOD is enabled $V_{POT-} = V_{POT+}$.

33.3.12 Flash and EEPROM Memory Characteristics

Table 33-75. Endurance and Data Retention

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Flash	Write/Erase cycles	25°C	10K			Cycle
			85°C	10K			
			105°C	2K			
		Data retention	25°C	100			Year
			85°C	25			
			105°C	10			
	EEPROM	Write/Erase cycles	25°C	100K			Cycle
			85°C	100K			
			105°C	30K			
		Data retention	25°C	100			Year
			85°C	25			
			105°C	10			

Table 33-76. Programming Time

Symbol	Parameter	Condition		Min.	Typ. (1)	Max.	Units
	Chip erase(2)	128KB Flash, EEPROM			75		ms
	Application erase	Section erase			6		
	Flash	Page erase			4		
		Page write			4		
		Atomic page erase and write			8		
	EEPROM	Page erase			4		
		Page write			4		
		Atomic page erase and write			8		

Notes: 1. Programming is timed from the 2MHz internal oscillator.
2. EEPROM is not erased if the EESAVE fuse is programmed.

33.4.8 Bandgap and Internal 1.0V Reference Characteristics

Table 33-100.Bandgap and Internal 1.0V Reference Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Startup time	As reference for ADC		1 Clk_{PER} + 2.5µs		µs
		As input voltage to ADC and AC		1.5		
	Bandgap voltage			1.1		V
INT1V	Internal 1.00V reference	T= 85°C, after calibration	0.99	1.0	1.01	
	Variation over voltage and temperature	Calibrated at T= 85°C		1		%

33.4.9 Brownout Detection Characteristics

Table 33-101.Brownout Detection Characteristics(1)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{BOT}	BOD level 0 falling V_{CC}		1.40	1.60	1.70	V
	BOD level 1 falling V_{CC}			1.8		
	BOD level 2 falling V_{CC}			2.0		
	BOD level 3 falling V_{CC}			2.2		
	BOD level 4 falling V_{CC}			2.4		
	BOD level 5 falling V_{CC}			2.6		
	BOD level 6 falling V_{CC}			2.8		
	BOD level 7 falling V_{CC}			3.0		
t_{BOD}	Detection time	Continuous mode		0.4		µs
		Sampled mode		1000		
V_{HYST}	Hysteresis			1.0		%

Note: 1. BOD is calibrated at 85°C within BOD level 0 values, and BOD level 0 is the default level.

33.4.10 External Reset Characteristics

Table 33-102.External Reset Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_{EXT}	Minimum reset pulse width		1000	90		ns
V_{RST}	Reset threshold voltage	V_{CC} = 2.7 - 3.6V		0.45*V_{CC}		V
		V_{CC} = 1.6 - 2.7V		0.45*V_{CC}		
R_{RST}	Reset pin Pull-up Resistor			25		kΩ

33.5.4 Wake-up Time from Sleep Modes

Table 33-122. Device Wake-up Time from Sleep Modes with Various System Clock Sources

Symbol	Parameter	Condition	Min.	Typ.(1)	Max.	Units
t_{wakeup}	Wake-up time from idle, standby, and extended standby mode	External 2MHz clock		2.0		µs
		32.768kHz internal oscillator		125		
		2MHz internal oscillator		2.0		
		32MHz internal oscillator		0.2		
	Wake-up time from power-save and power-down mode	External 2MHz clock		4.6		
		32.768kHz internal oscillator		330		
		2MHz internal oscillator		9.5		
		32MHz internal oscillator		5.6		

Note: 1. The wake-up time is the time from the wake-up request is given until the peripheral clock is available on pin, see Figure 33-30. All peripherals and modules start execution from the first clock cycle, expect the CPU that is halted for four clock cycles before program execution starts.

Figure 33-30.Wake-up Time Definition

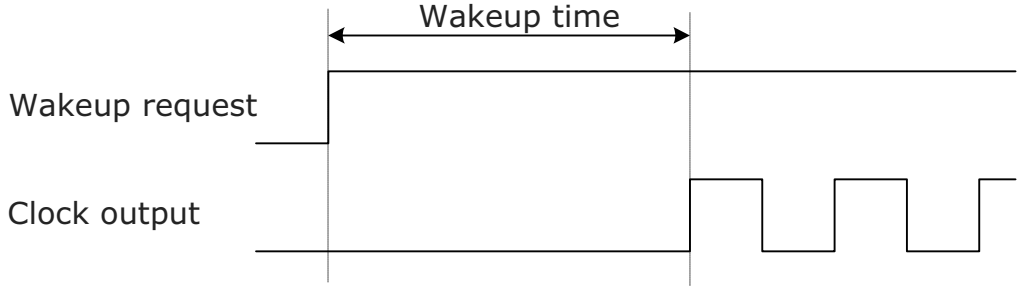


Figure 34-33. INL Error vs. Input Code

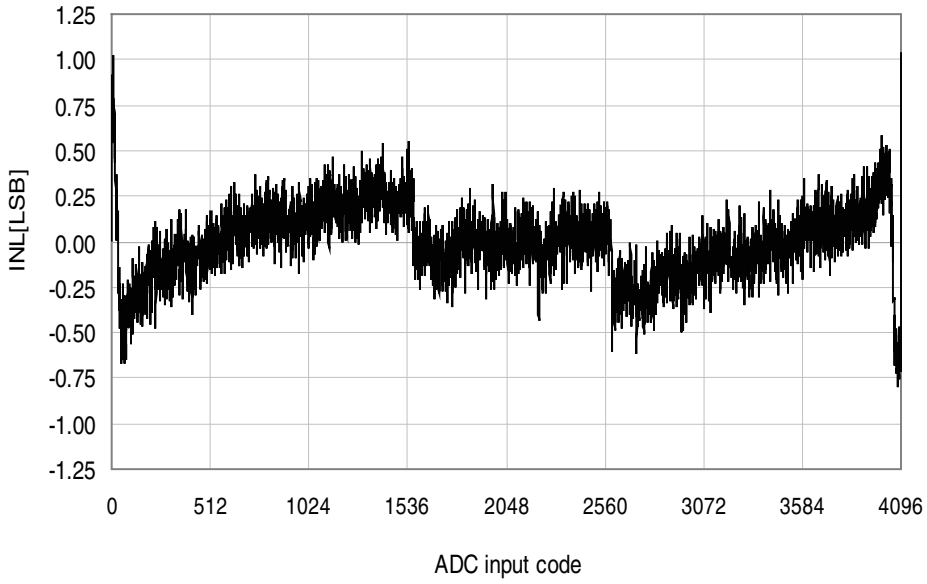
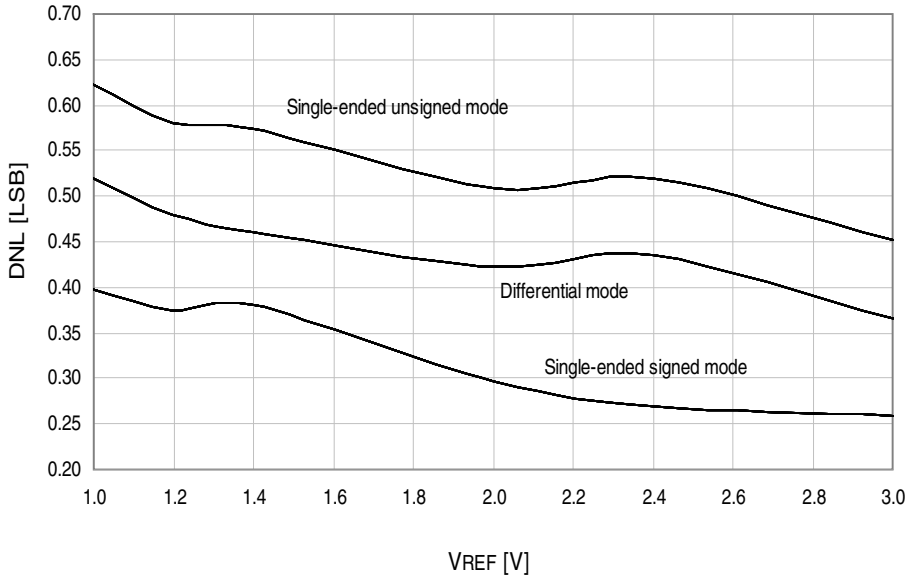


Figure 34-34. DNL Error vs. External V_{REF}

T = 25°C, V_{CC} = 3.6V, external reference



34.2.1.3 Power-down Mode Supply Current

Figure 34-86. Power-down Mode Supply Current vs. V_{CC}

All functions disabled

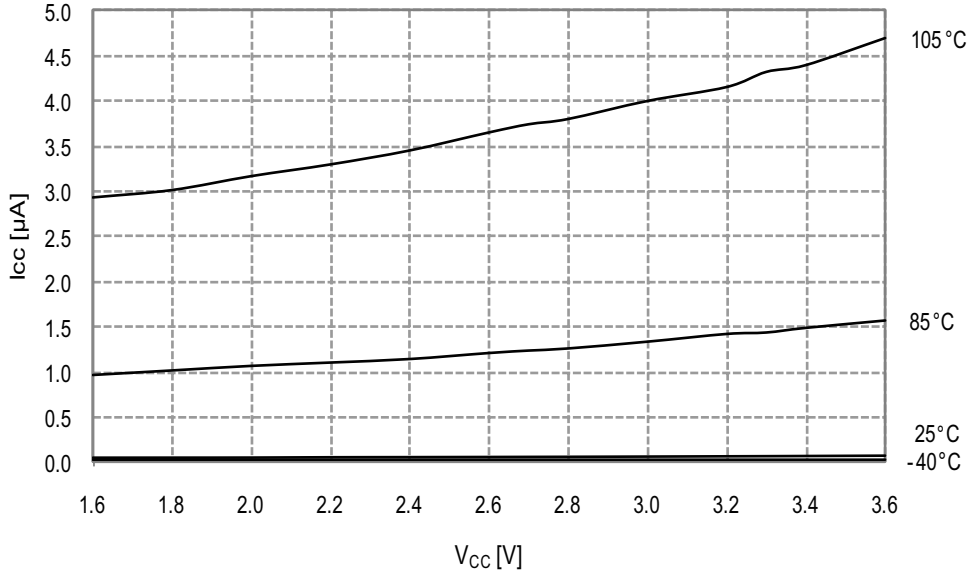


Figure 34-87. Power-down Mode Supply Current vs. V_{CC}

Watchdog and sampled BOD enabled

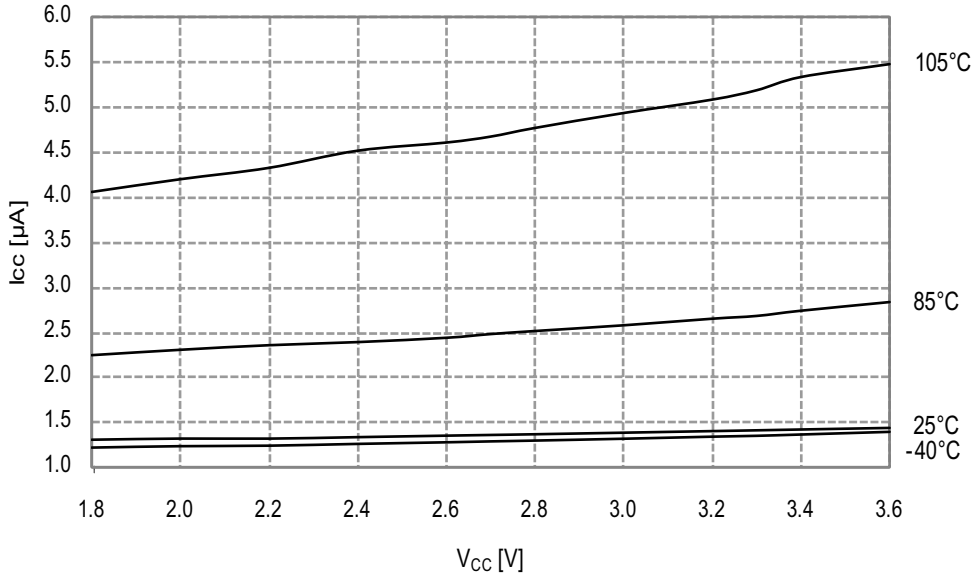


Figure 34-167. I/O Pin Output Voltage vs. Sink Current

V_{CC} = 3.0V

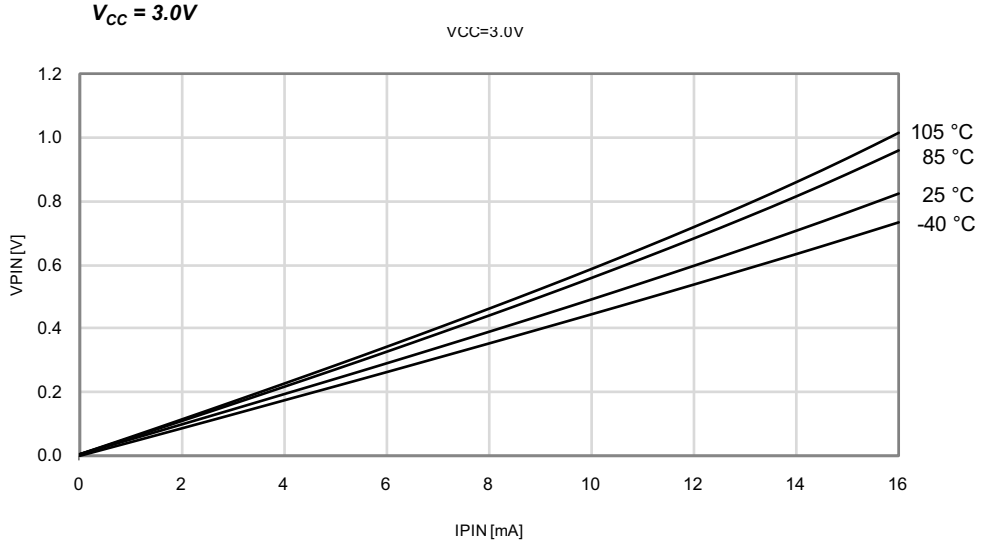


Figure 34-168. I/O Pin Output Voltage vs. Sink Current

V_{CC} = 3.3V

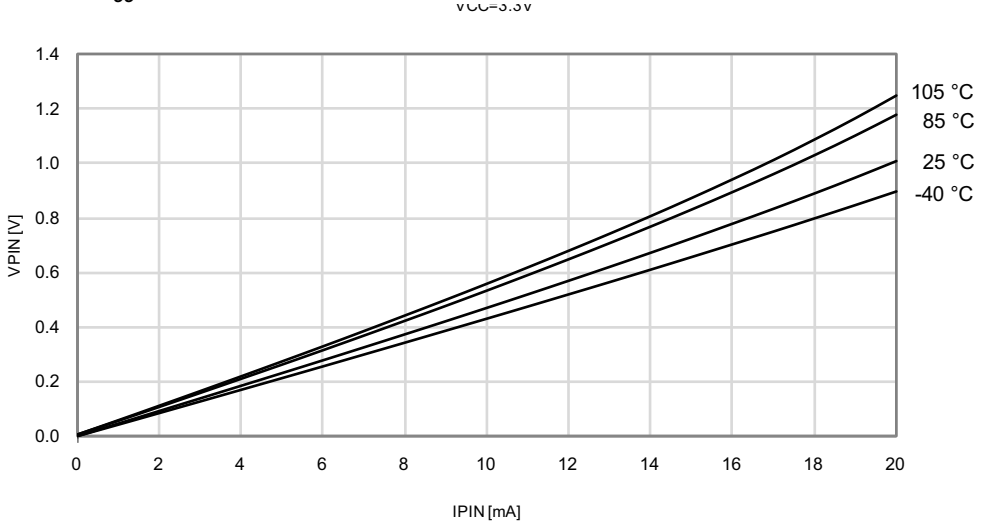


Figure 34-193. Reset Pin Pull-up Resistor Current vs. Reset Pin Voltage

V_{CC} = 3.3V

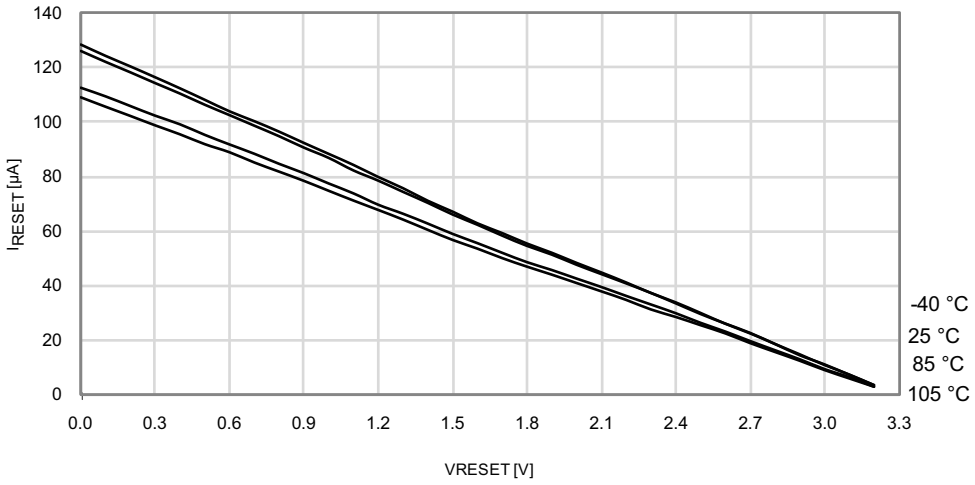


Figure 34-194. Reset Pin Input Threshold Voltage vs. V_{CC}

V_{IH} - Reset pin read as "1"

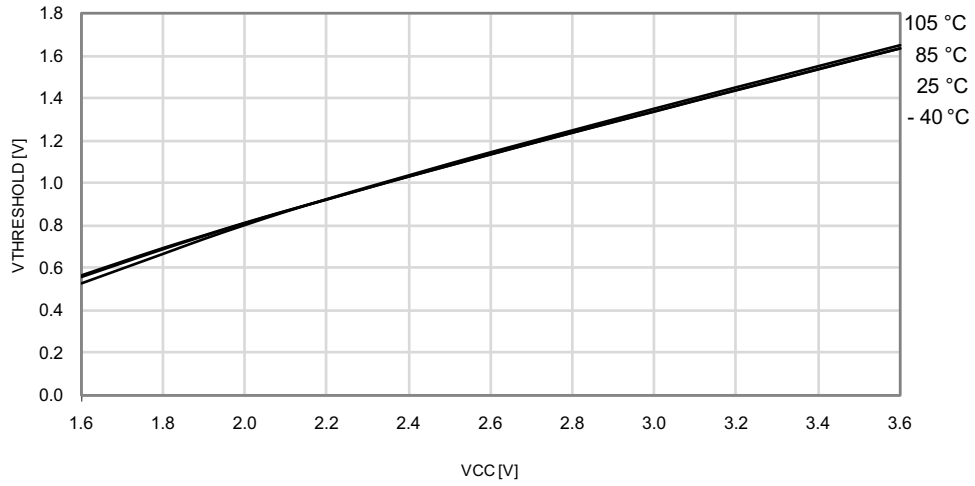


Figure 34-217. Active Mode Supply Current vs. V_{CC}

f_{SYS} = 2MHz internal oscillator

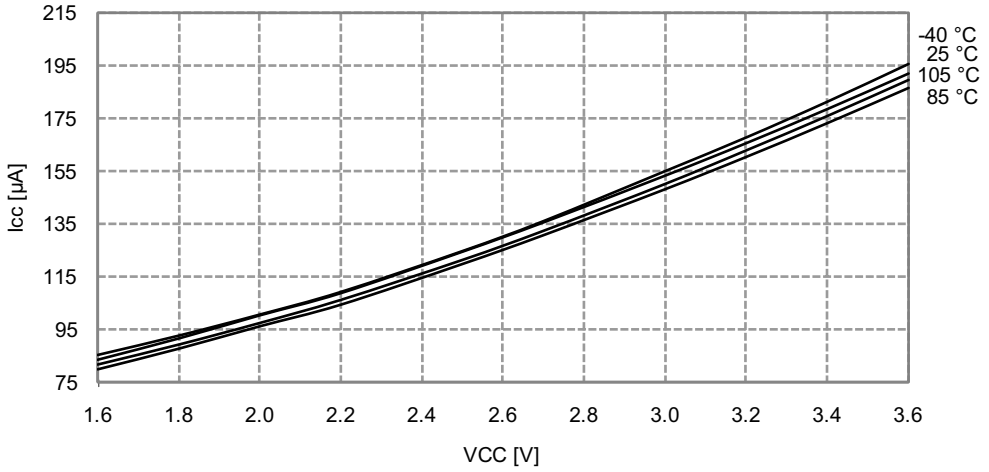
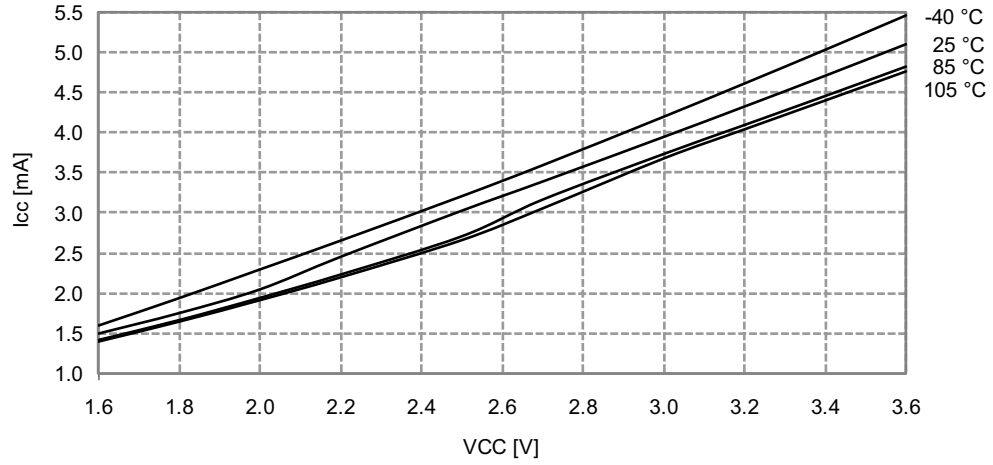


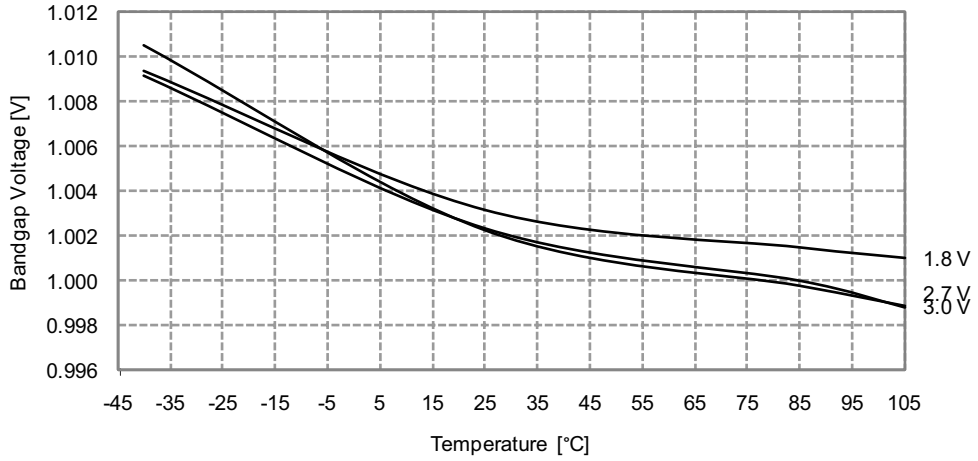
Figure 34-218. Active Mode Supply Current vs. V_{CC}

f_{SYS} = 32MHz internal oscillator prescaled to 8MHz



34.4.5 Internal 1.0V Reference Characteristics

Figure 34-257. ADC Internal 1.0V Reference vs. Temperature



34.4.6 BOD Characteristics

Figure 34-258. BOD Thresholds vs. Temperature

BOD level = 1.6V

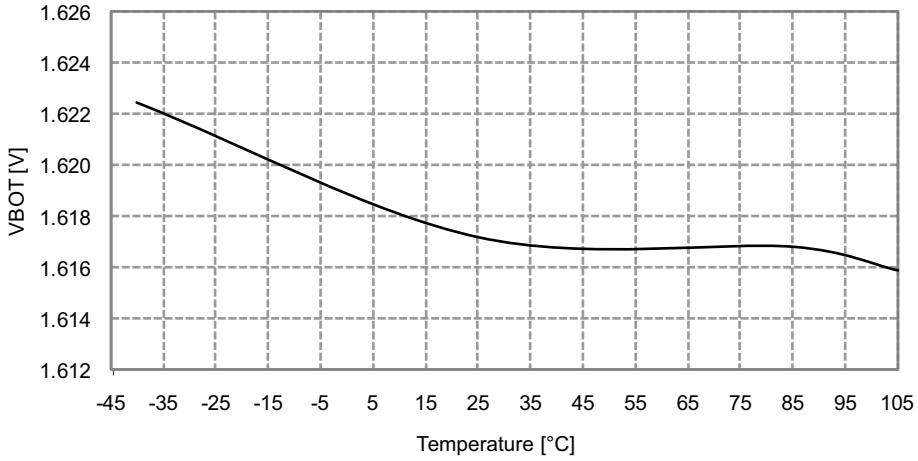
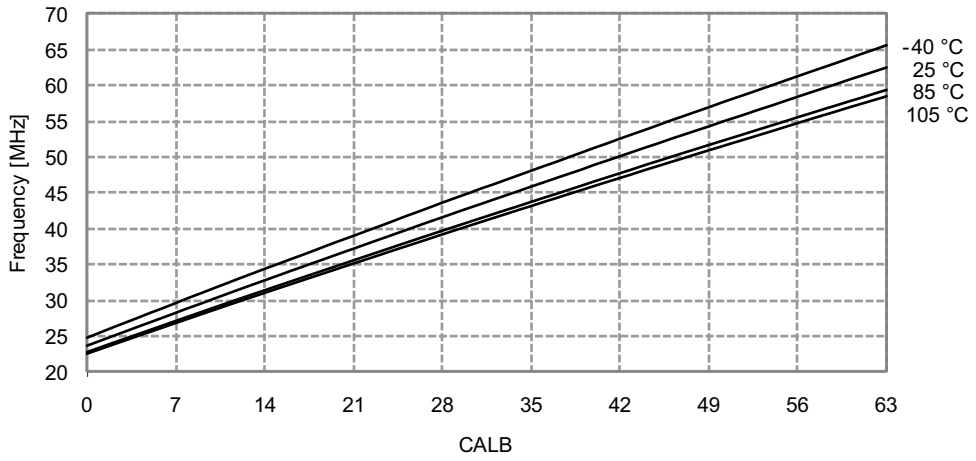


Figure 34-277. 32MHz Internal Oscillator Frequency vs. CALB Calibration Value

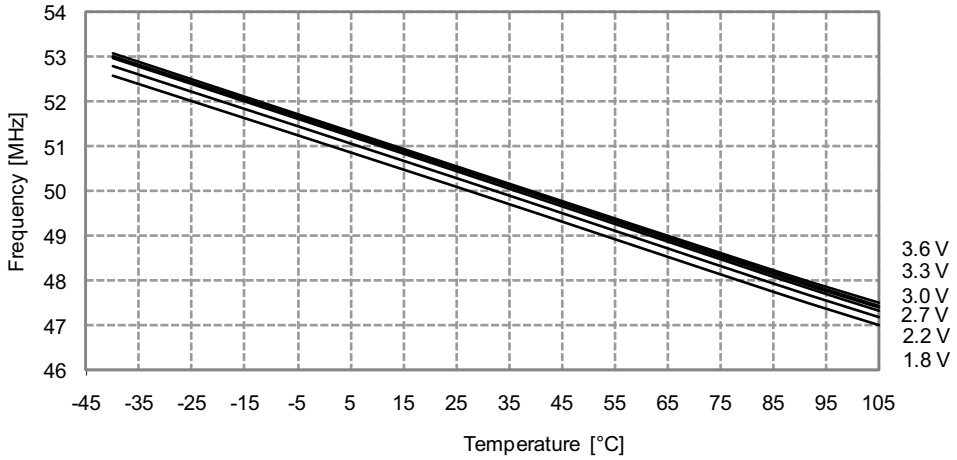
V_{CC} = 3.0V



34.4.8.5 32MHz Internal Oscillator Calibrated to 48MHz

Figure 34-278. 48MHz Internal Oscillator Frequency vs. Temperature

DFLL disabled



34.5.4 Analog Comparator Characteristics

Figure 34-323. Analog Comparator Hysteresis vs. V_{CC}

Small hysteresis

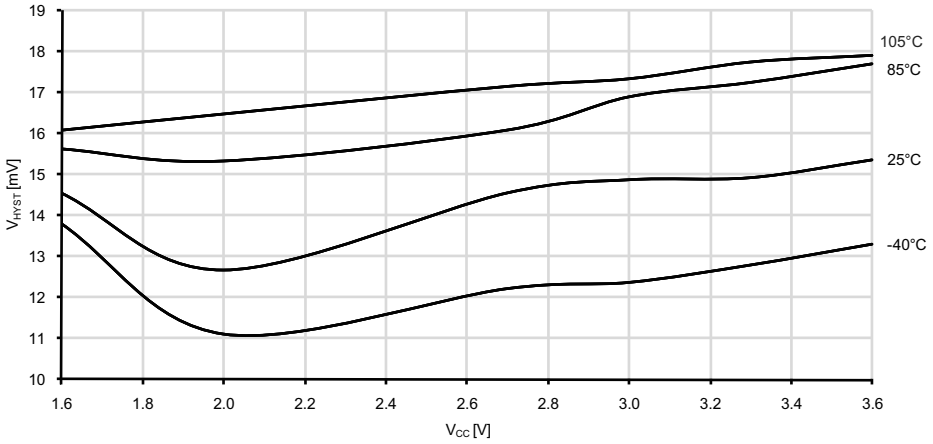
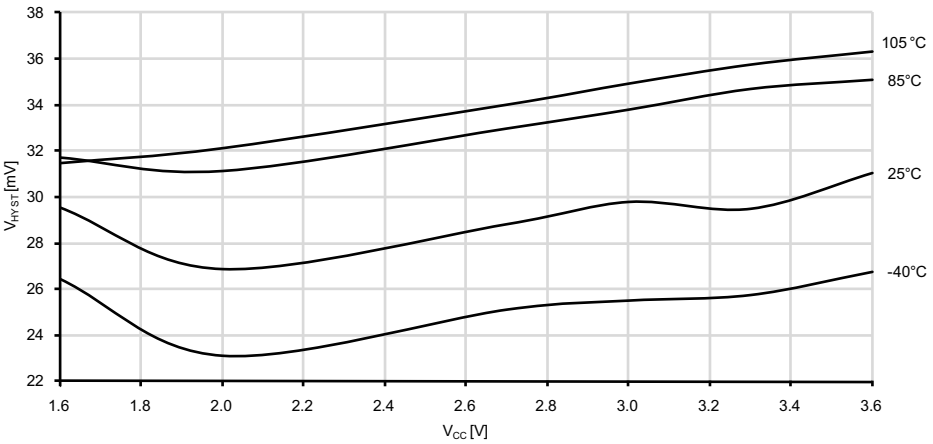


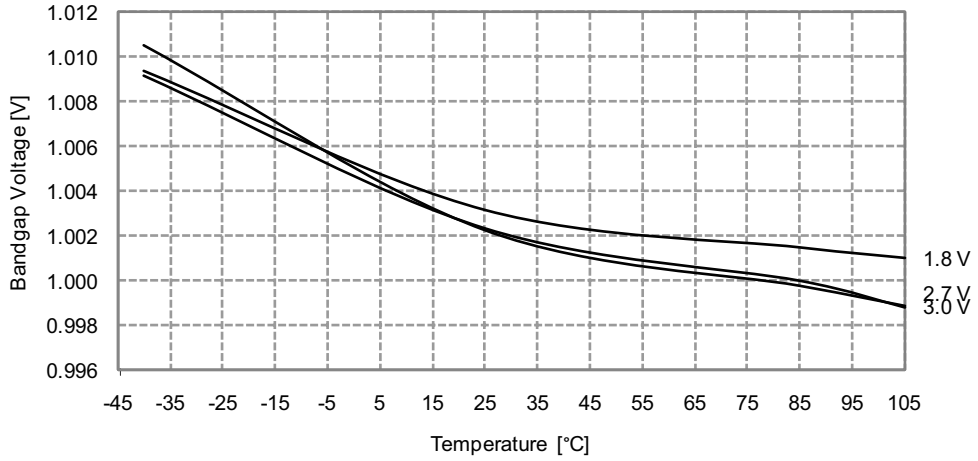
Figure 34-324. Analog Comparator Hysteresis vs. V_{CC}

Large hysteresis



34.5.5 Internal 1.0V Reference Characteristics

Figure 34-327. ADC Internal 1.0V Reference vs. Temperature



34.5.6 BOD Characteristics

Figure 34-328. BOD Thresholds vs. Temperature

BOD level = 1.6V

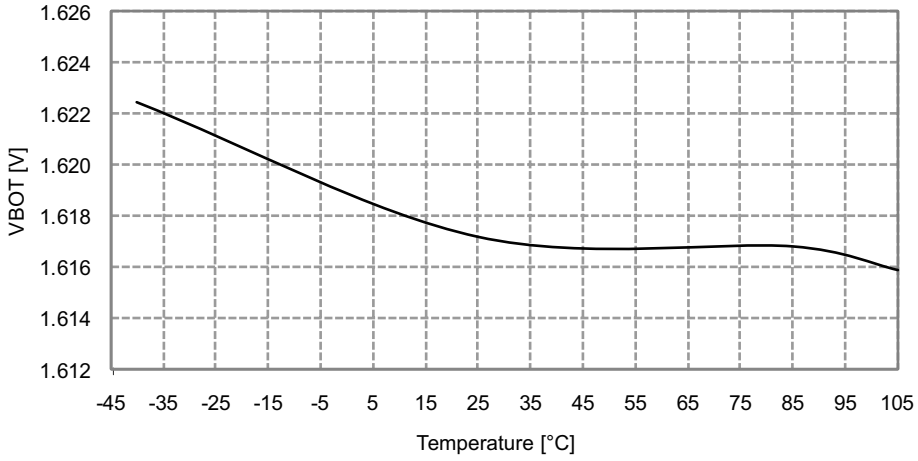
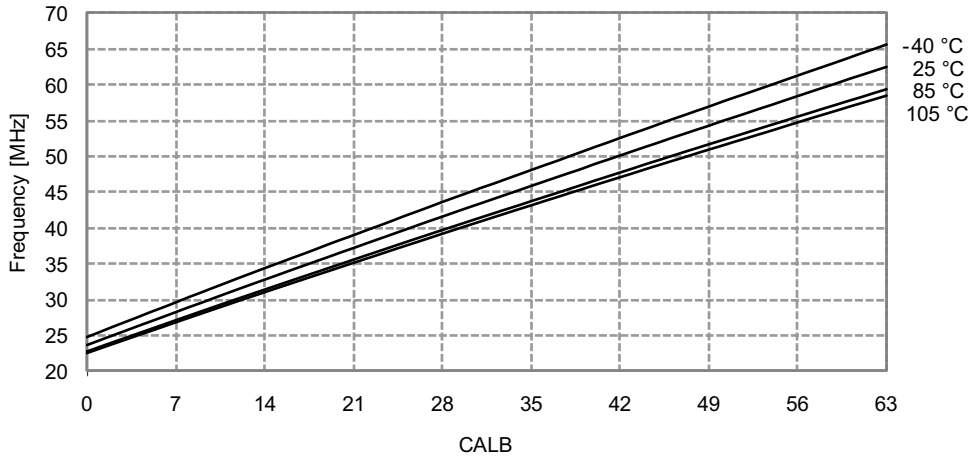


Figure 34-347. 32MHz Internal Oscillator Frequency vs. CALB Calibration Value

V_{CC} = 3.0V



34.5.8.5 32MHz Internal Oscillator Calibrated to 48MHz

Figure 34-348. 48MHz Internal Oscillator Frequency vs. Temperature

DFLL disabled