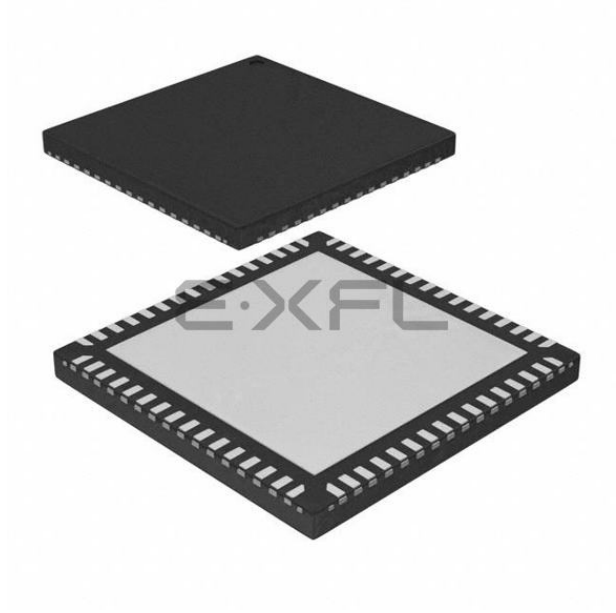

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	50
Program Memory Size	192KB (96K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega192c3-mhr

22. SPI – Serial Peripheral Interface

22.1 Features

- Two Identical SPI peripherals
- Full-duplex, three-wire synchronous data transfer
- Master or slave operation
- Lsb first or msb first data transfer
- Eight programmable bit rates
- Interrupt flag at the end of transmission
- Write collision flag to indicate data collision
- Wake up from idle sleep mode
- Double speed master mode

22.2 Overview

The Serial Peripheral Interface (SPI) is a high-speed synchronous data transfer interface using three or four pins. It allows fast communication between an Atmel AVR XMEGA device and peripheral devices or between several microcontrollers. The SPI supports full-duplex communication.

A device connected to the bus must act as a master or slave. The master initiates and controls all data transactions.

PORTC and PORTD each has one SPI. Notation of these peripherals are SPIC and SPID, respectively.

Mnemonics	Operands	Description	Operation	Flags	#Clocks
MOVW	Rd, Rr	Copy Register Pair	Rd+1:Rd ← Rr+1:Rr	None	1
LDI	Rd, K	Load Immediate	Rd ← K	None	1
LDS	Rd, k	Load Direct from data space	Rd ← (k)	None	2 (1)
LD	Rd, X	Load Indirect	Rd ← (X)	None	1 (1)
LD	Rd, X+	Load Indirect and Post-Increment	Rd ← (X) X ← X + 1	None	1 (1)
LD	Rd, -X	Load Indirect and Pre-Decrement	X ← X - 1, ← X - 1 Rd ← (X) ← (X)	None	2 (1)
LD	Rd, Y	Load Indirect	Rd ← (Y) ← (Y)	None	1 (1)
LD	Rd, Y+	Load Indirect and Post-Increment	Rd ← (Y) Y ← Y + 1	None	1 (1)
LD	Rd, -Y	Load Indirect and Pre-Decrement	Y ← Y - 1 Rd ← (Y)	None	2 (1)
LDD	Rd, Y+q	Load Indirect with Displacement	Rd ← (Y + q)	None	2 (1)
LD	Rd, Z	Load Indirect	Rd ← (Z)	None	1 (1)
LD	Rd, Z+	Load Indirect and Post-Increment	Rd ← (Z), Z ← Z+1	None	1 (1)
LD	Rd, -Z	Load Indirect and Pre-Decrement	Z ← Z - 1, Rd ← (Z)	None	2 (1)
LDD	Rd, Z+q	Load Indirect with Displacement	Rd ← (Z + q)	None	2 (1)
STS	k, Rr	Store Direct to Data Space	(k) ← Rd	None	2
ST	X, Rr	Store Indirect	(X) ← Rr	None	1
ST	X+, Rr	Store Indirect and Post-Increment	(X) ← Rr, X ← X + 1	None	1
ST	-X, Rr	Store Indirect and Pre-Decrement	X ← X - 1, (X) ← Rr	None	2
ST	Y, Rr	Store Indirect	(Y) ← Rr	None	1
ST	Y+, Rr	Store Indirect and Post-Increment	(Y) ← Rr, Y ← Y + 1	None	1
ST	-Y, Rr	Store Indirect and Pre-Decrement	Y ← Y - 1, (Y) ← Rr	None	2
STD	Y+q, Rr	Store Indirect with Displacement	(Y + q) ← Rr	None	2
ST	Z, Rr	Store Indirect	(Z) ← Rr	None	1
ST	Z+, Rr	Store Indirect and Post-Increment	(Z) ← Rr Z ← Z + 1	None	1
ST	-Z, Rr	Store Indirect and Pre-Decrement	Z ← Z - 1	None	2
STD	Z+q,Rr	Store Indirect with Displacement	(Z + q) ← Rr	None	2
LPM		Load Program Memory	R0 ← (Z)	None	3
LPM	Rd, Z	Load Program Memory	Rd ← (Z)	None	3
LPM	Rd, Z+	Load Program Memory and Post-Increment	Rd ← (Z), Z ← Z + 1	None	3
ELPM		Extended Load Program Memory	R0 ← (RAMPZ:Z)	None	3

Mnemonics	Operands	Description	Operation	Flags	#Clocks
SEN		Set Negative Flag	N ← 1	N	1
CLN		Clear Negative Flag	N ← 0	N	1
SEZ		Set Zero Flag	Z ← 1	Z	1
CLZ		Clear Zero Flag	Z ← 0	Z	1
SEI		Global Interrupt Enable	I ← 1	I	1
CLI		Global Interrupt Disable	I ← 0	I	1
SES		Set Signed Test Flag	S ← 1	S	1
CLS		Clear Signed Test Flag	S ← 0	S	1
SEV		Set Two’s Complement Overflow	V ← 1	V	1
CLV		Clear Two’s Complement Overflow	V ← 0	V	1
SET		Set T in SREG	T ← 1	T	1
CLT		Clear T in SREG	T ← 0	T	1
SEH		Set Half Carry Flag in SREG	H ← 1	H	1
CLH		Clear Half Carry Flag in SREG	H ← 0	H	1
MCU control instructions					
BREAK		Break	(See specific descr. for BREAK)	None	1
NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep)	None	1
WDR		Watchdog Reset	(see specific descr. for WDR)	None	1

Notes: 1. One extra cycle must be added when accessing internal SRAM.

33.1.3 Current Consumption

Table 33-4. Current Consumption for Active Mode and Sleep Modes

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{CC}	Active power consumption(1)	32kHz, Ext. Clk	V_{CC} = 1.8V		50		µA
			V_{CC} = 3.0V		130		
		1MHz, Ext. Clk	V_{CC} = 1.8V		215		
			V_{CC} = 3.0V		475		
		2MHz, Ext. Clk	V_{CC} = 1.8V		445	600	
			V_{CC} = 3.0V		0.95	1.5	mA
		32MHz, Ext. Clk			7.8	12	
	Idle power consumption(2)	32kHz, Ext. Clk	V_{CC} = 1.8V		2.8		µA
			V_{CC} = 3.0V		3.0		
		1MHz, Ext. Clk	V_{CC} = 1.8V		46		
			V_{CC} = 3.0V		92		
		2MHz, Ext. Clk	V_{CC} = 1.8V		93	225	
			V_{CC} = 3.0V		184	350	
		32MHz, Ext. Clk			2.9	5.0	mA
	Power-down power consumption	T = 25°C	V_{CC} = 3.0V		0.07	1.0	µA
		T = 85°C			1.3	5.0	
		T = 105°C			4.0	8.0	
		WDT and sampled BOD enabled, T = 25°C	V_{CC} = 3.0V		1.4	2.0	
		WDT and sampled BOD enabled, T = 85°C			2.6	6.0	
		WDT and sampled BOD enabled, T = 105°C			5.0	10	
	Power-save power consumption(3)	RTC from ULP clock, WDT and sampled BOD enabled, T = 25°C	V_{CC} = 1.8V		1.7		
			V_{CC} = 3.0V		1.8		
		RTC from 1.024kHz low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.7	2.0	
			V_{CC} = 3.0V		0.8	2.0	
		RTC from low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.9	3.0	
			V_{CC} = 3.0V		1.2	3.0	
	Reset power consumption	Current through $\overline{\text{RESET}}$ pin substracted	V_{CC} = 3.0V		120		

Notes:
1. All Power Reduction Registers set including FPRM and EPRM.
2. All Power Reduction Registers set without FPRM and EPRM.
3. Maximum limits are based on characterization, and not tested in production.

Table 33-11. Gain Stage Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
R_{in}	Input resistance	Switched in normal mode		4.0		kΩ
C_{sample}	Input capacitance	Switched in normal mode		4.4		pF
	Signal range	Gain stage output	0		AV_{CC}- 0.6	V
	Propagation delay	ADC conversion rate	1/2	1	3	Clk_{ADC} cycles
	Clock frequency	Same as ADC	100		1800	kHz
	Gain error	0.5x gain, normal mode		-1		%
		1x gain, normal mode		-1		
		8x gain, normal mode		-1		
		64x gain, normal mode		5		
	Offset error, input referred	0.5x gain, normal mode		10		mV
		1x gain, normal mode		5		
		8x gain, normal mode		-20		
		64x gain, normal mode		-126		

33.1.7 Analog Comparator Characteristics

Table 33-12. Analog Comparator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{off}	Input offset voltage			10		mV
I_{lk}	Input leakage current			<10	50	nA
	Input voltage range		-0.1		AV_{CC}	V
	AC startup time			50		µs
V_{hys1}	Hysteresis, none	Vcc=1.6V - 3.6V		0		mV
V_{hys2}	Hysteresis, small	Vcc=1.6V - 3.6V		15		
V_{hys3}	Hysteresis, large	Vcc=1.6V - 3.6V		30		
t_{delay}	Propagation delay	V_{CC} = 3.0V, T= 85°C		20	40	ns
		V_{CC} = 3.0V		17		
	64-level voltage scaler	Integral non-linearity (INL)		0.3	0.5	lsb
	Current source accuracy after calibration			5		%
	Current source calibration range	Single mode	4		6	µA

Table 33-25. External Clock with Prescaler (1) for System Clock

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock Frequency (2)	V_{CC} = 1.6 - 1.8V	0		90	MHz
		V_{CC} = 2.7 - 3.6V	0		142	
t_{CK}	Clock Period	V_{CC} = 1.6 - 1.8V	11			ns
		V_{CC} = 2.7 - 3.6V	7			
t_{CH}	Clock High Time	V_{CC} = 1.6 - 1.8V	4.5			
		V_{CC} = 2.7 - 3.6V	2.4			
t_{CL}	Clock Low Time	V_{CC} = 1.6 - 1.8V	4.5			
		V_{CC} = 2.7 - 3.6V	2.4			
t_{CR}	Rise Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			1.5	
		V_{CC} = 2.7 - 3.6V			1.0	
t_{CF}	Fall Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			1.5	
		V_{CC} = 2.7 - 3.6V			1.0	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Notes: 1. System Clock Prescalers must be set so that maximum CPU clock frequency for device is not exceeded.
2. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

33.1.13.7 External 16MHz Crystal Oscillator and XOSC Characteristics

Table 33-26. External 16MHz Crystal oOcillator and XOSC Characteristics

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Cycle to cycle jitter	XOSCPWR=0	FRQRANGE=0		0		ns
			FRQRANGE=1, 2, or 3		0		
		XOSCPWR=1			0		
	Long term jitter	XOSCPWR=0	FRQRANGE=0		0		
			FRQRANGE=1, 2, or 3		0		
		XOSCPWR=1			0		
	Frequency error	XOSCPWR=0	FRQRANGE=0		0.03		%
			FRQRANGE=1		0.03		
			FRQRANGE=2 or 3		0.03		
		XOSCPWR=1			0.003		
	Duty cycle	XOSCPWR=0	FRQRANGE=0		50		
			FRQRANGE=1		50		
			FRQRANGE=2 or 3		50		
		XOSCPWR=1			50		

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
C_{XTAL1}	Parasitic capacitance XTAL1 pin			5.9		pF
C_{XTAL2}	Parasitic capacitance XTAL2 pin			8.3		
C_{LOAD}	Parasitic capacitance load			3.5		

Note: 1. Numbers for negative impedance are not tested in production but guaranteed from design and characterization.

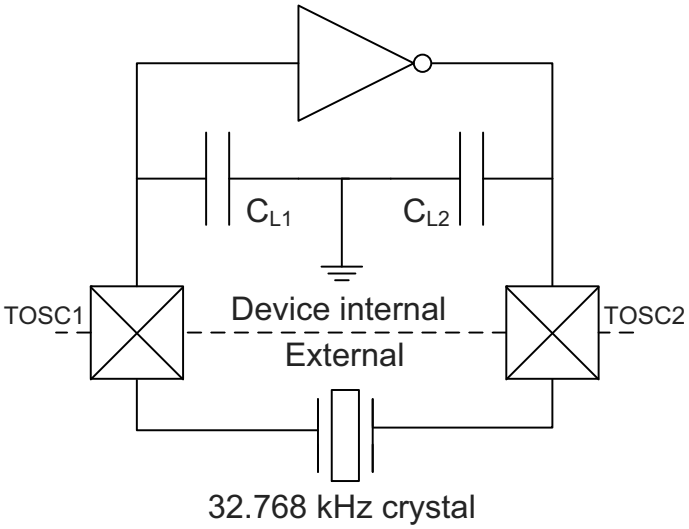
33.1.13.8 External 32.768kHz Crystal Oscillator and TOSC Characteristics

Table 33-27. External 32.768kHz Crystal Oscillator and TOSC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
ESR/R1	Recommended crystal equivalent series resistance (ESR)	Crystal load capacitance 6.5pF			60	kΩ
		Crystal load capacitance 9.0pF			35	
		Crystal load capacitance 12pF			28	
C_{TOSC1}	Parasitic capacitance TOSC1 pin			3.5		pF
C_{TOSC2}	Parasitic capacitance TOSC2 pin			3.5		
	Recommended safety factor	capacitance load matched to crystal specification	3			

Note: See Figure 33-4 for definition.

Figure 33-4. TOSC Input Capacitance



The parasitic capacitance between the TOSC pins is C_{L1} + C_{L2} in series as seen from the crystal when oscillating without external capacitors.

Table 33-92. Current Consumption for Modules and Peripherals

Symbol	Parameter	Condition [1]		Min.	Typ.	Max.	Units
I_{CC}	ULP oscillator				0.9		µA
	32.768kHz int. oscillator				25		
	2MHz int. oscillator				78		
		DFLL enabled with 32.768kHz int. osc. as reference			110		
	32MHz int. oscillator				250		
		DFLL enabled with 32.768kHz int. osc. as reference			440		
	PLL	20x multiplication factor, 32MHz int. osc. DIV4 as reference			310		
	Watchdog timer				1.0		
	BOD	Continuous mode			132		
		Sampled mode, includes ULP oscillator			1.4		
	Internal 1.0V reference				185		
	Temperature sensor				182		
	ADC	16ksps V_{REF} = Ext. ref.			1.12		mA
			CURRLIMIT = LOW		1.01		
			CURRLIMIT = MEDIUM		0.9		
			CURRLIMIT = HIGH		0.8		
		75ksps V_{REF} = Ext. ref.	CURRLIMIT = LOW		1.7		
		300ksps V_{REF} = Ext. ref.			3.1		
	USART	Rx and Tx enabled, 9600 BAUD			9.5		µA
	Flash memory and EEPROM programming				10		mA

Note: 1. All parameters measured as the difference in current consumption between module enabled and disabled. All data at V_{CC} = 3.0V, Clk_{SYS} = 1MHz external clock without prescaling, T = 25°C unless other conditions are given.

33.4.4 Wake-up Time from Sleep Modes

Table 33-93. Device Wake-up Time from Sleep Modes with Various System Clock Sources

Symbol	Parameter	Condition	Min.	Typ. (1)	Max.	Units
t_{wakeup}	Wake-up time from idle, standby, and extended standby mode	External 2MHz clock		2.0		µs
		32.768kHz internal oscillator		125		
		2MHz internal oscillator		2.0		
		32MHz internal oscillator		0.2		
	Wake-up time from Power-save and Power-down mode	External 2MHz clock		4.6		
		32.768kHz internal oscillator		330		
		2MHz internal oscillator		9.5		
		32MHz internal oscillator		5.6		

Note: 1. The wake-up time is the time from the wake-up request is given until the peripheral clock is available on pin, see Figure 33-23. All peripherals and modules start execution from the first clock cycle, expect the CPU that is halted for four clock cycles before program execution starts.

Figure 33-23.Wake-up Time Definition

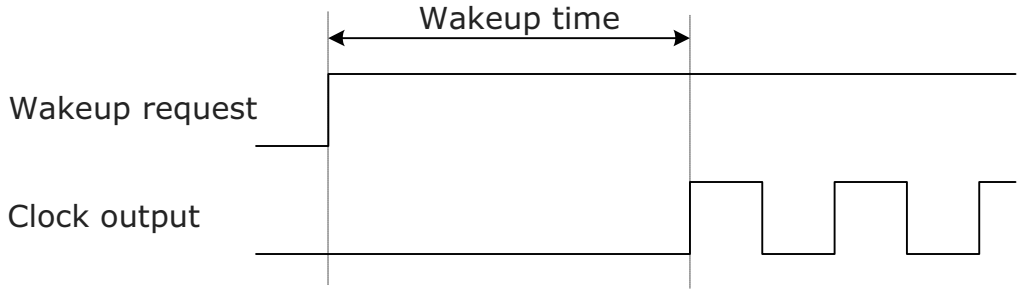


Figure 34-39. Offset Error vs. V_{REF}

T = 25°C, V_{CC} = 3.6V, ADC sample rate = 300ksps

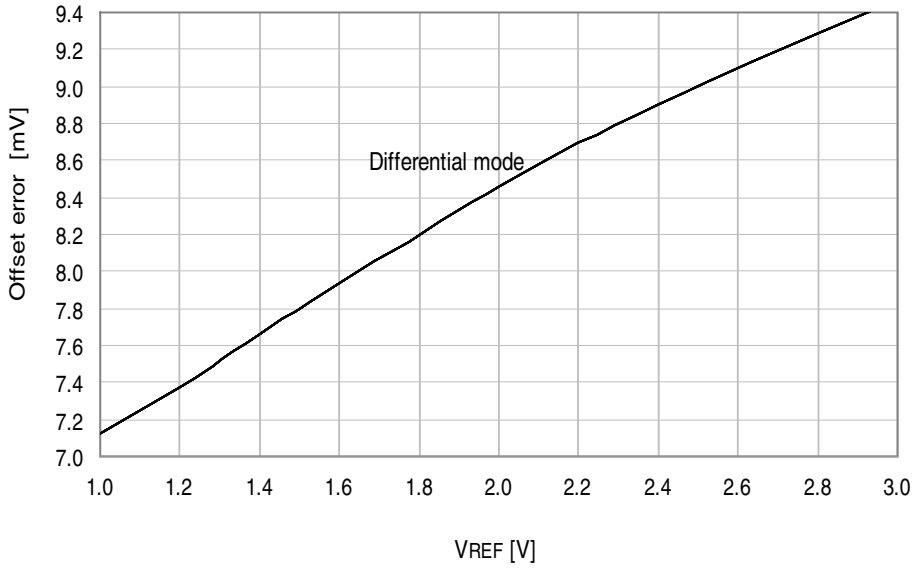


Figure 34-40. Gain Error vs. Temperature

V_{CC} = 3.0V, V_{REF} = external 2.0V

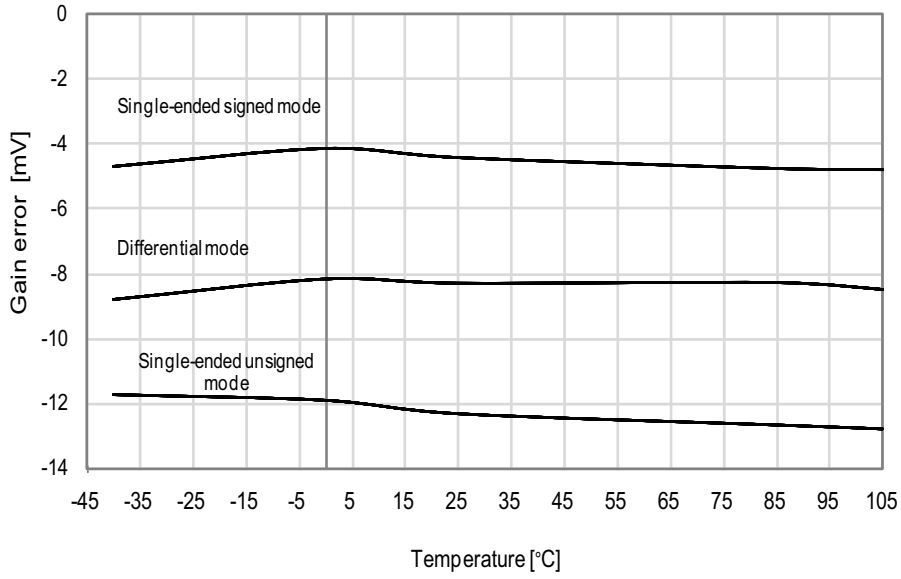


Figure 34-65. 32MHz Internal Oscillator CALA Calibration Step Size

$T = 105°C$, $V_{CC} = 3.0V$

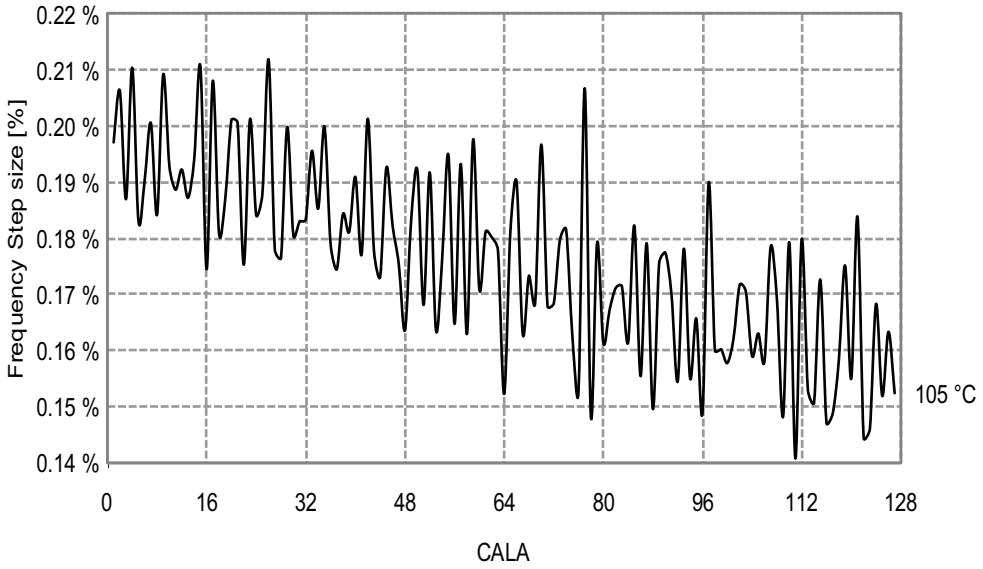


Figure 34-66. 32MHz Internal Oscillator Frequency vs. CALB Calibration Value

$V_{CC} = 3.0V$

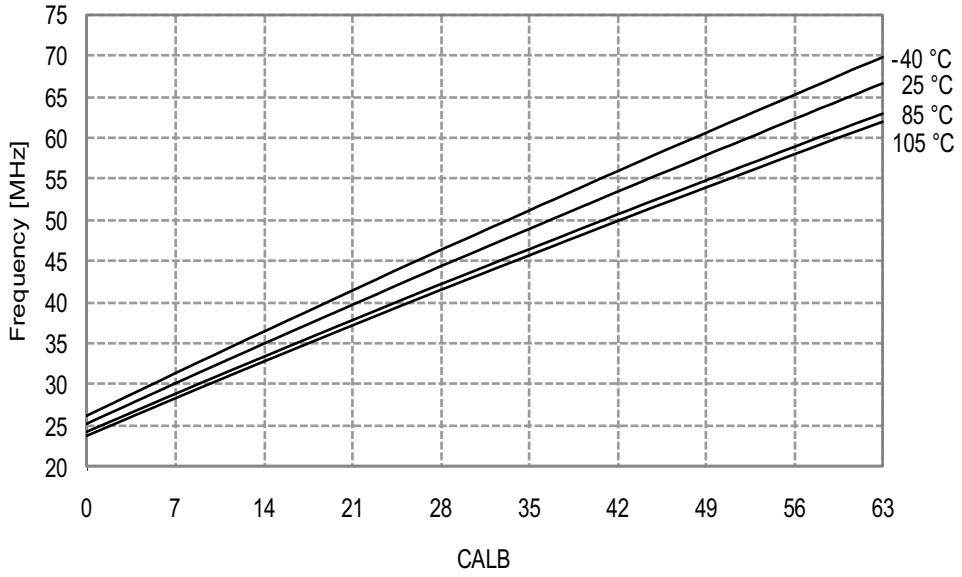
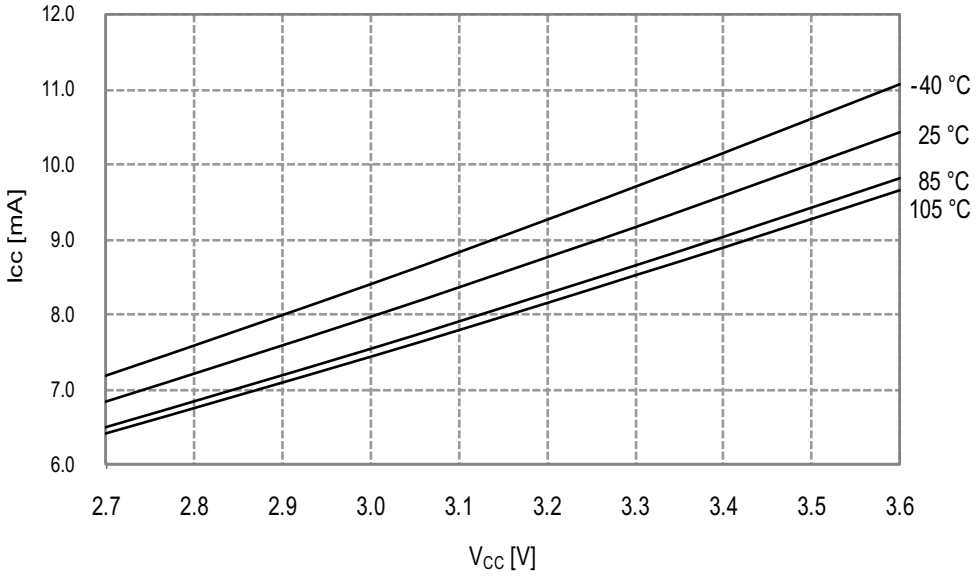


Figure 34-78.Active Mode Supply Current vs. V_{CC}

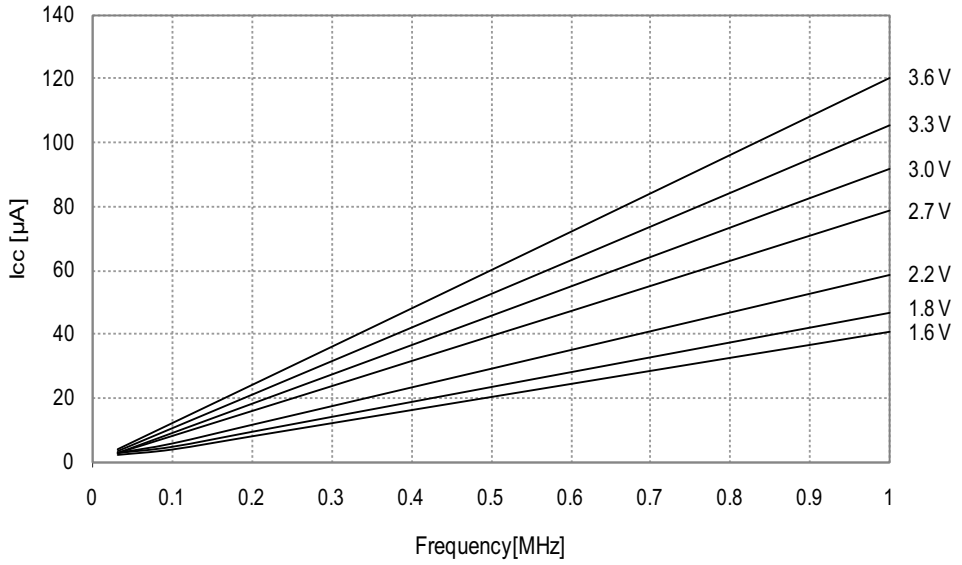
f_{SYS} = 32MHz internal oscillator



34.2.1.2 Idle Mode Supply Current

Figure 34-79.Idle Mode Supply Current vs. Frequency

f_{SYS} = 0 - 1MHz external clock, T = 25°C



34.2.3 ADC Characteristics

Figure 34-102. INL Error vs. External V_{REF}

T = 25°C, V_{CC} = 3.6V, external reference

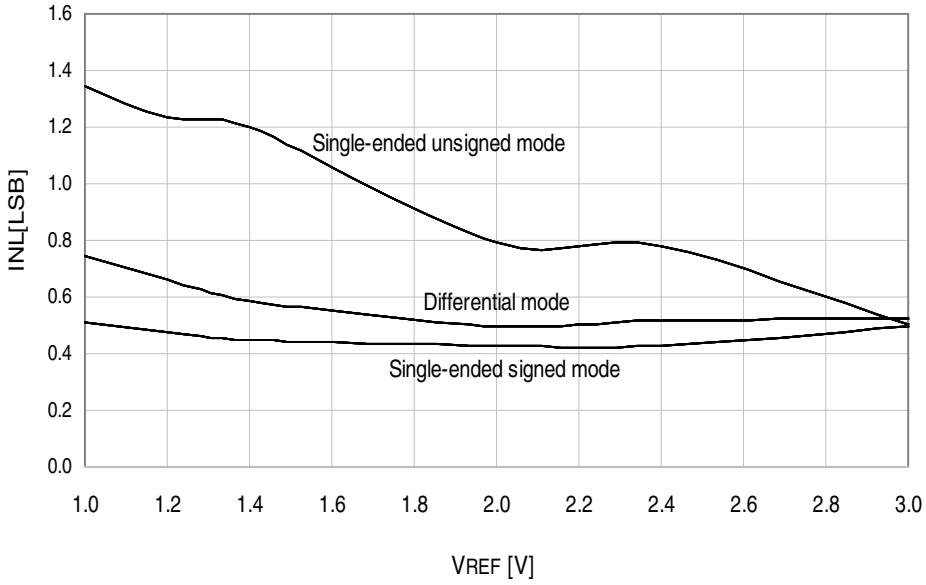


Figure 34-103. INL Error vs. Sample Rate

T = 25°C, V_{CC} = 3.6V, V_{REF} = 3.0V external

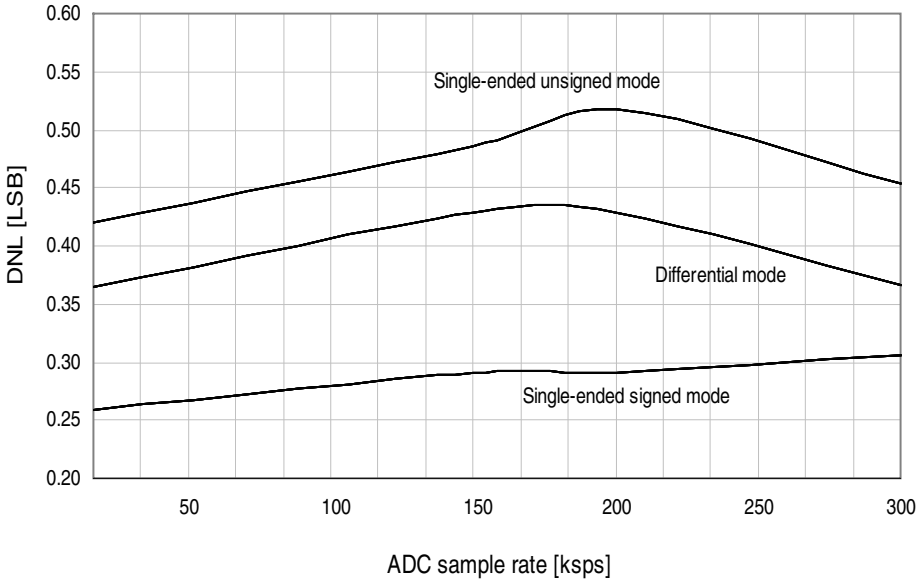


Figure 34-108. Gain Error vs. V_{REF}

T = 25°C, V_{CC} = 3.6V, ADC sample rate = 300ksps

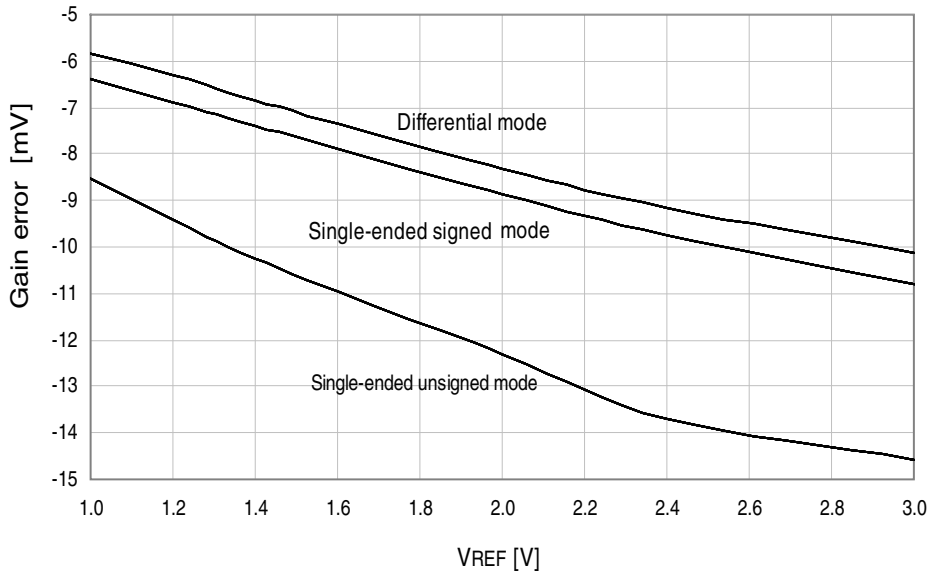
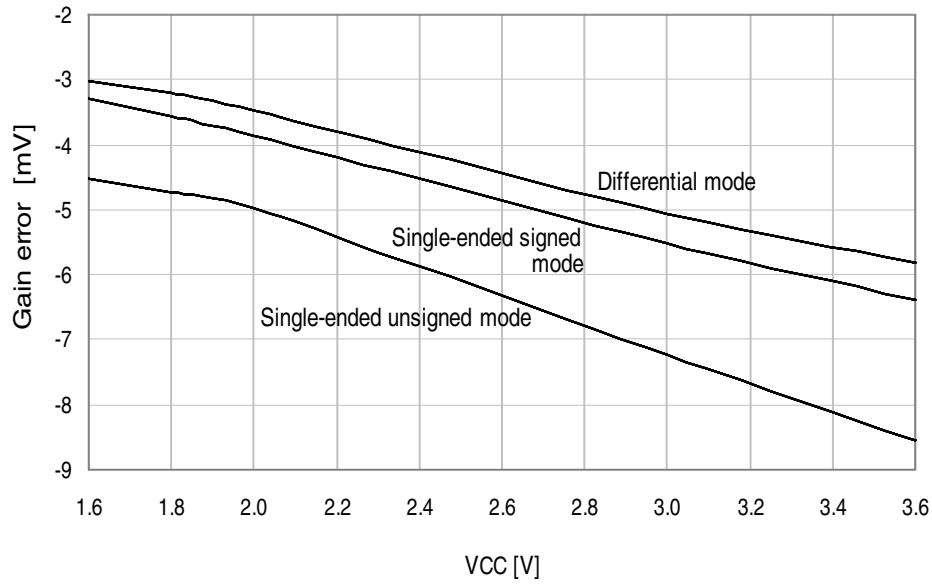


Figure 34-109. Gain Error vs. V_{CC}

T = 25°C, V_{REF} = external 1.0V, ADC sample rate = 300ksps



34.2.8.2 32.768kHz Internal Oscillator

Figure 34-126. 32.768kHz Internal Oscillator Frequency vs. Temperature

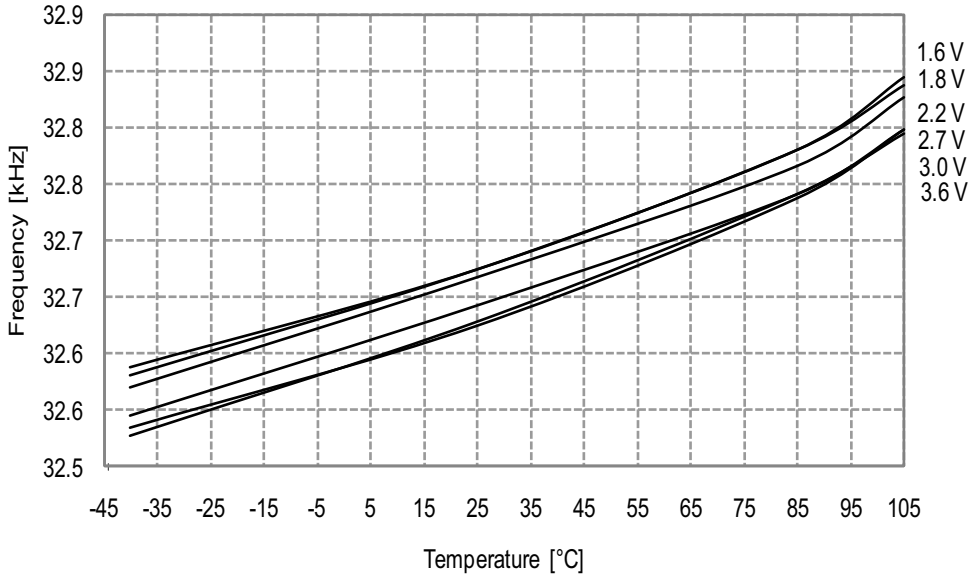


Figure 34-127. 32.768kHz Internal Oscillator Frequency vs. Calibration Value

V_{CC} = 3.0V, T = 25°C

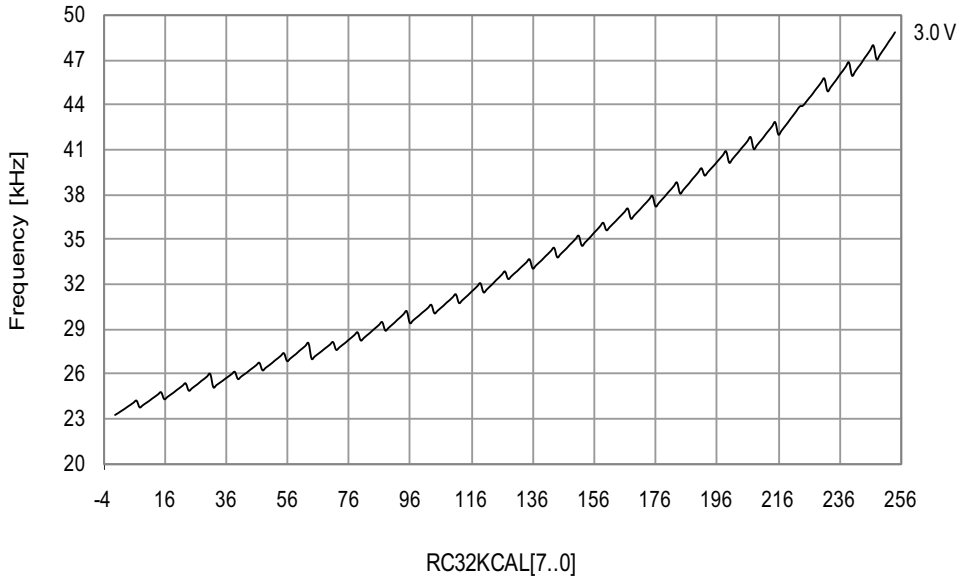


Figure 34-151. Idle Mode Supply Current vs. Frequency

f_{SYS} = 1 - 32MHz external clock, T = 25°C

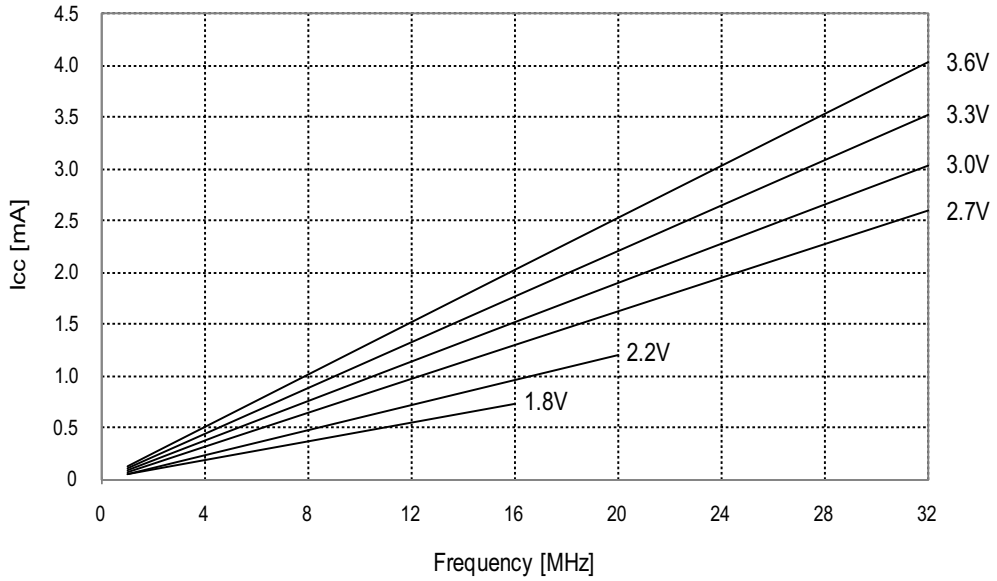


Figure 34-152. Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 32.768kHz internal oscillator

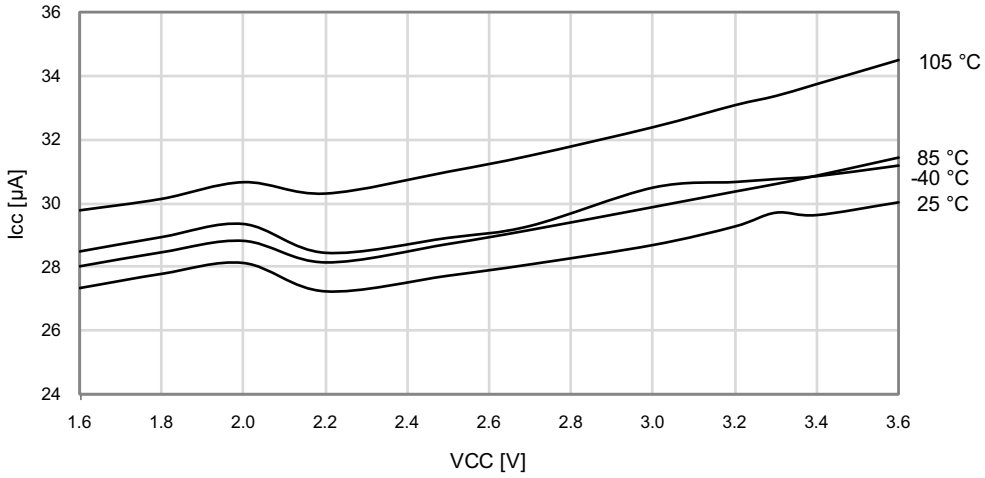


Figure 34-193. Reset Pin Pull-up Resistor Current vs. Reset Pin Voltage

V_{CC} = 3.3V

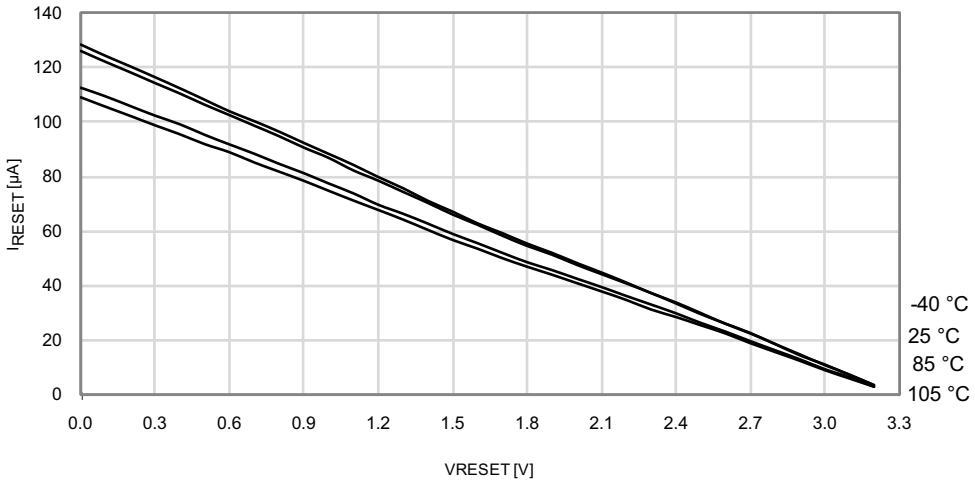


Figure 34-194. Reset Pin Input Threshold Voltage vs. V_{CC}

V_{IH} - Reset pin read as "1"

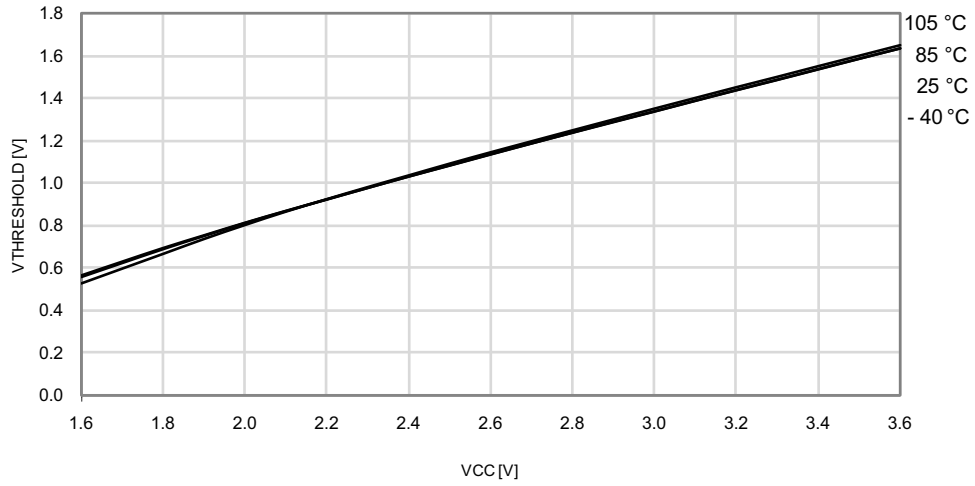
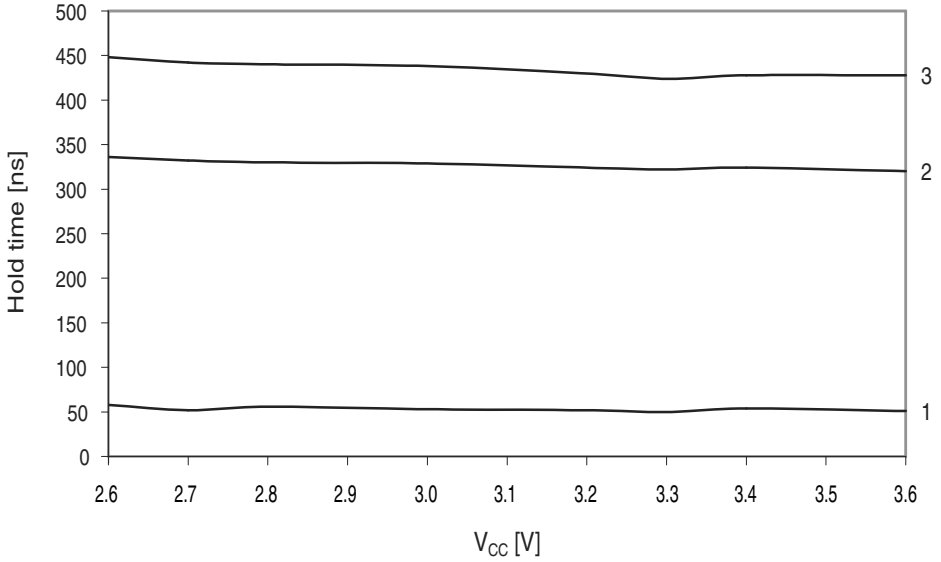


Figure 34-211. SDA Hold Time vs. Supply Voltage



34.3.10 PDI Characteristics

Figure 34-212. Maximum PDI Frequency vs. V_{CC}

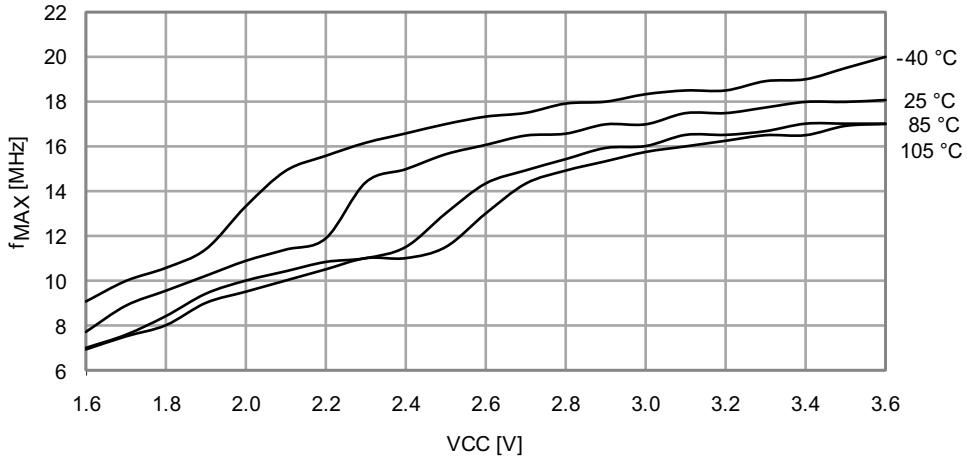


Figure 34-269. 2MHz Internal Oscillator Frequency vs. Temperature

DFLL enabled, from the 32.768kHz internal oscillator

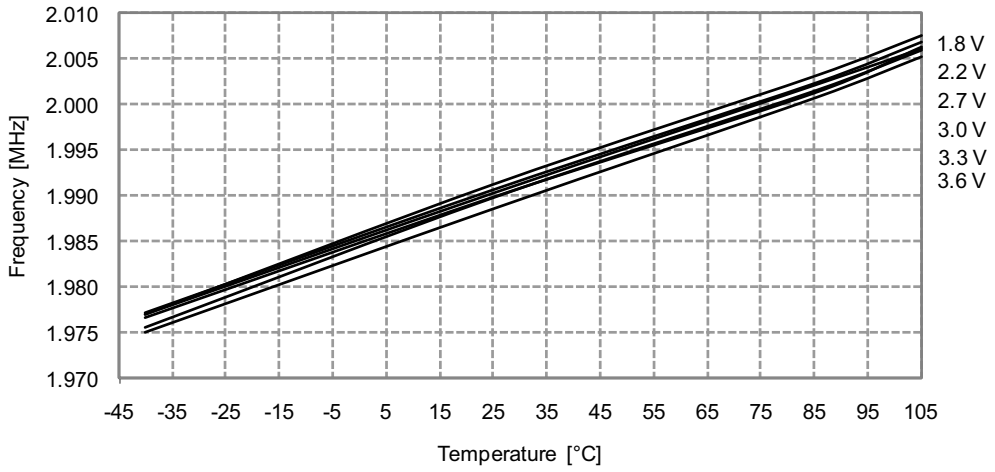


Figure 34-270. 2MHz Internal Oscillator Frequency vs. CALA Calibration Value

V_{CC} = 3V

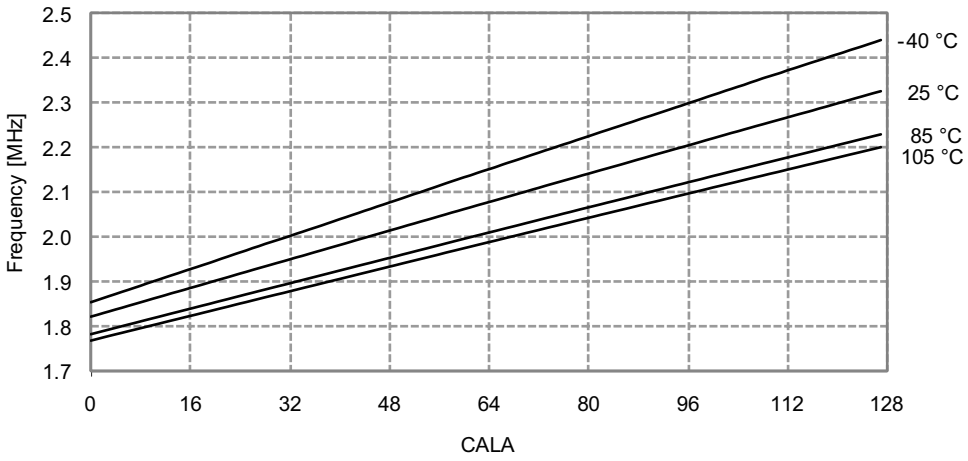
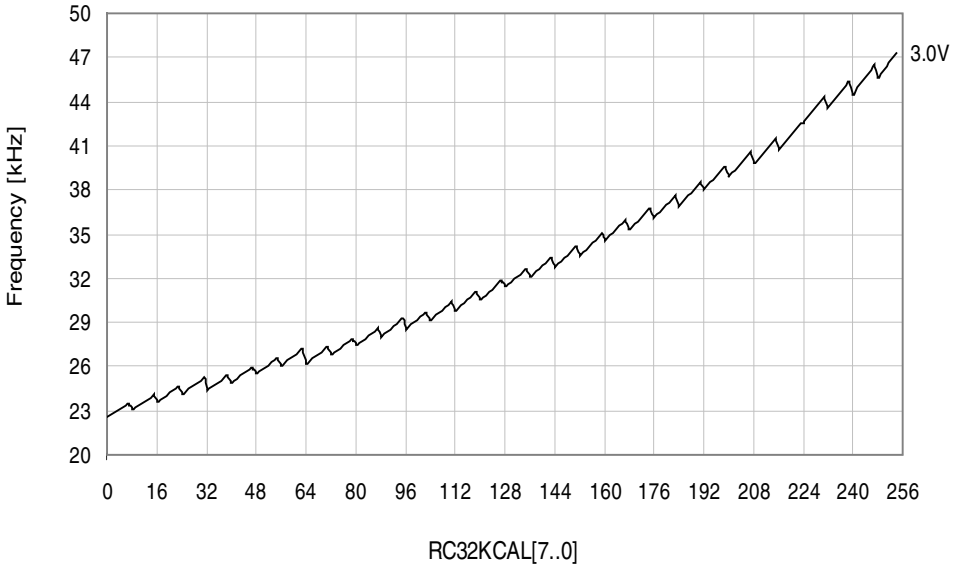


Figure 34-337. 32.768kHz Internal Oscillator Frequency vs. Calibration Value

V_{CC} = 3.0V, T = 25°C



34.5.8.3 2MHz Internal Oscillator

Figure 34-338. 2MHz Internal Oscillator Frequency vs. Temperature

DFLL disabled