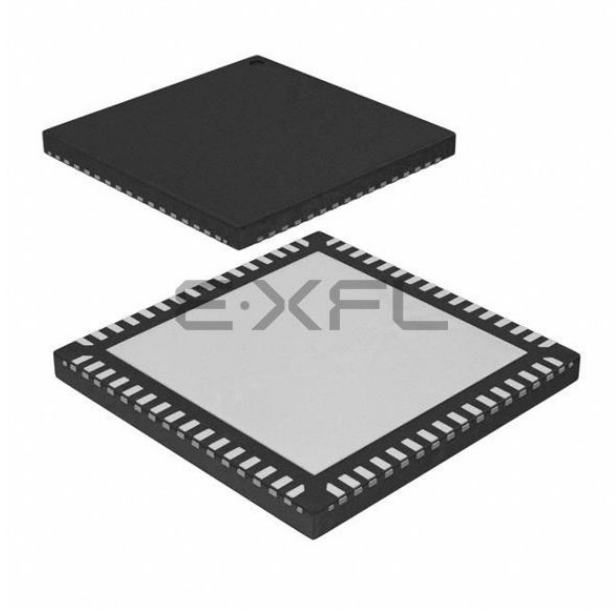

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	50
Program Memory Size	192KB (96K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega192c3-mn

8. Event System

8.1 Features

- System for direct peripheral-to-peripheral communication and signaling
- Peripherals can directly send, receive, and react to peripheral events
  - CPU independent operation
  - 100% predictable signal timing
  - Short and guaranteed response time
- Four event channels for up to four different and parallel signal routing configurations
- Events can be sent and/or used by most peripherals, clock system, and software
- Additional functions include
  - Quadrature decoders
  - Digital filtering of I/O pin state
- Works in active mode and idle sleep mode

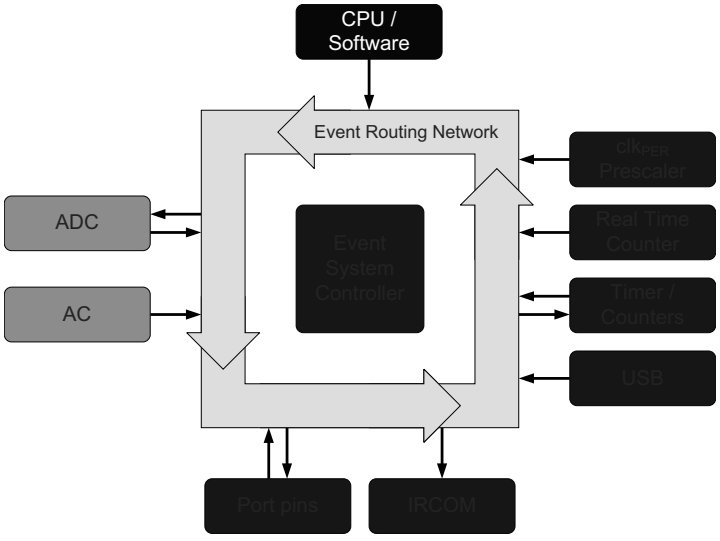
8.2 Overview

The event system enables direct peripheral-to-peripheral communication and signaling. It allows a change in one peripheral's state to automatically trigger actions in other peripherals. It is designed to provide a predictable system for short and predictable response times between peripherals. It allows for autonomous peripheral control and interaction without the use of interrupts, and CPU, and is thus a powerful tool for reducing the complexity, size and execution time of application code. It also allows for synchronized timing of actions in several peripheral modules.

A change in a peripheral's state is referred to as an event, and usually corresponds to the peripheral's interrupt conditions. Events can be directly passed to other peripherals using a dedicated routing network called the event routing network. How events are routed and used by the peripherals is configured in software.

Figure 8-1 on page 18 shows a basic diagram of all connected peripherals. The event system can directly connect together analog to digital converter, analog comparators, I/O port pins, the real-time counter, timer/counters, IR communication module (IRCOM), and USB interface. Events can also be generated from software and the peripheral clock.

Figure 8-1. Event System Overview and Connected Peripherals



The event routing network consists of four software-configurable multiplexers that control how events are routed and used. These are called event channels, and allow for up to four parallel event routing configurations. The maximum routing latency is two peripheral clock cycles. The event system works in both active mode and idle sleep mode.

18. Hi-Res – High Resolution Extension

18.1 Features

- Increases waveform generator resolution up to 8x (three bits)
- Supports frequency, single-slope PWM, and dual-slope PWM generation
- Supports the AWeX when this is used for the same timer/counter

18.2 Overview

The high-resolution (hi-res) extension can be used to increase the resolution of the waveform generation output from a timer/counter by four or eight. It can be used for a timer/counter doing frequency, single-slope PWM, or dual-slope PWM generation. It can also be used with the AWeX if this is used for the same timer/counter.

The hi-res extension uses the peripheral 4x clock (Clk_{PER4}). The system clock prescalers must be configured so the peripheral 4x clock frequency is four times higher than the peripheral and CPU clock frequency when the hi-res extension is enabled.

There is one hi-res extensions that can be enabled for timer/counters pair on PORTC. The notation of this is HIRESC.

Mnemonics	Operands	Description	Operation	Flags	#Clocks
SEN		Set Negative Flag	N ← 1	N	1
CLN		Clear Negative Flag	N ← 0	N	1
SEZ		Set Zero Flag	Z ← 1	Z	1
CLZ		Clear Zero Flag	Z ← 0	Z	1
SEI		Global Interrupt Enable	I ← 1	I	1
CLI		Global Interrupt Disable	I ← 0	I	1
SES		Set Signed Test Flag	S ← 1	S	1
CLS		Clear Signed Test Flag	S ← 0	S	1
SEV		Set Two’s Complement Overflow	V ← 1	V	1
CLV		Clear Two’s Complement Overflow	V ← 0	V	1
SET		Set T in SREG	T ← 1	T	1
CLT		Clear T in SREG	T ← 0	T	1
SEH		Set Half Carry Flag in SREG	H ← 1	H	1
CLH		Clear Half Carry Flag in SREG	H ← 0	H	1
MCU control instructions					
BREAK		Break	(See specific descr. for BREAK)	None	1
NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep)	None	1
WDR		Watchdog Reset	(see specific descr. for WDR)	None	1

Notes: 1. One extra cycle must be added when accessing internal SRAM.

33.1.5 I/O Pin Characteristics

The I/O pins complies with the JEDEC LVTTL and LVCMOS specification and the high- and low-level input and output voltage limits reflect or exceed this specification.

Table 33-7. I/O Pin Characteristics

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{OH} (1)/ I_{OL} (2)	I/O pin source/sink current			-15		15	mA
V_{IH}	High level input voltage	V_{CC} = 2.4 - 3.6V		0.7*Vcc		V_{CC}+0.5	V
		V_{CC} = 1.6 - 2.4V		0.8*V_{CC}		V_{CC}+0.5	
V_{IL}	Low level input voltage	V_{CC} = 2.4 - 3.6V		-0.5		0.3*V_{CC}	
		V_{CC} = 1.6 - 2.4V		-0.5		0.2*V_{CC}	
V_{OH}	High level output voltage	V_{CC} = 3.3V	I_{OH} = -4mA	2.6	2.9		
		V_{CC} = 3.0V	I_{OH} = -3mA	2.1	2.6		
		V_{CC} = 1.8V	I_{OH} = -1mA	1.4	1.6		
V_{OL}	Low level output voltage	V_{CC} = 3.3V	I_{OL} = 8mA		0.4	0.76	
		V_{CC} = 3.0V	I_{OL} = 5mA		0.3	0.64	
		V_{CC} = 1.8V	I_{OL} = 3mA		0.2	0.46	
I_{IN}	Input leakage current I/O pin	T = 25°C			<0.01	1.0	µA
R_P	Pull/Bus keeper resistor				25		kΩ

Notes:
1. The sum of all I_{OH} for PORTA and PORTB must not exceed 100mA.
   The sum of all I_{OH} for PORTC, PORTD, and PORTE must for each port not exceed 200mA.
   The sum of all I_{OH} for pins PF[0-5] on PORTF must not exceed 200mA.
   The sum of all I_{OL} for pins PF[6-7] on PORTF, PORTR, and PDI must not exceed 100mA.
2. The sum of all I_{OL} for PORTA and PORTB must not exceed 100mA.
   The sum of all I_{OL} for PORTC, PORTD, and PORTE must for each port not exceed 200mA.
   The sum of all I_{OL} for pins PF[0-5] on PORTF must not exceed 200mA.
   The sum of all I_{OL} for pins PF[6-7] on PORTF, PORTR, and PDI must not exceed 100mA.

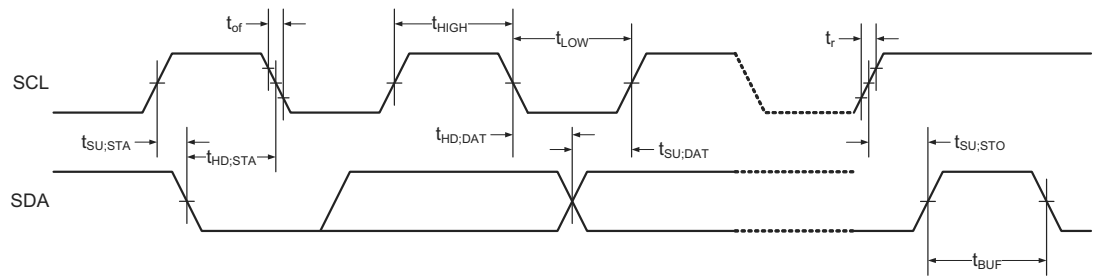
Table 33-86. SPI Timing Characteristics and Requirements

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_{SCK}	SCK period	Master		(See Table 20-3 in XMEGA C Manual)		ns
t_{SCKW}	SCK high/low width	Master		0.5*SCK		
t_{SCKR}	SCK rise time	Master		2.7		
t_{SCKF}	SCK fall time	Master		2.7		
t_{MIS}	MISO setup to SCK	Master		10		
t_{MIH}	MISO hold after SCK	Master		10		
t_{MOS}	MOSI setup SCK	Master		0.5*SCK		
t_{MOH}	MOSI hold after SCK	Master		1		
t_{SSCK}	Slave SCK period	Slave	4*t Clk_{PER}			
t_{SSCKW}	SCK high/low width	Slave	2*t Clk_{PER}			
t_{SSCKR}	SCK rise time	Slave			1600	
t_{SSCKF}	SCK fall time	Slave			1600	
t_{SIS}	MOSI setup to SCK	Slave	3			
t_{SIH}	MOSI hold after SCK	Slave	t Clk_{PER}			
t_{SSS}	$\overline{SS}$ setup to SCK	Slave	21			
t_{SSH}	$\overline{SS}$ hold after SCK	Slave	20			
t_{SOS}	MISO setup SCK	Slave		8		
t_{SOH}	MISO hold after SCK	Slave		13		
t_{SOSS}	MISO setup after $\overline{SS}$ low	Slave		11		
t_{SOSH}	MISO hold after $\overline{SS}$ high	Slave		8		

33.3.15 Two-Wire Interface Characteristics

Table 33-87 describes the requirements for devices connected to the Two-Wire Interface Bus. The Atmel AVR XMEGA Two-Wire Interface meets or exceeds these requirements under the noted conditions. Timing symbols refer to Figure 33-21.

Figure 33-21.Two-wire Interface Bus Timing



34. Typical Characteristics

34.1 Atmel ATxmega32C3

34.1.1 Current Consumption

34.1.1.1 Active Mode Supply Current

Figure 34-1. Active Supply Current vs. Frequency

f_{SYS} = 0 - 1MHz external clock, T = 25°C

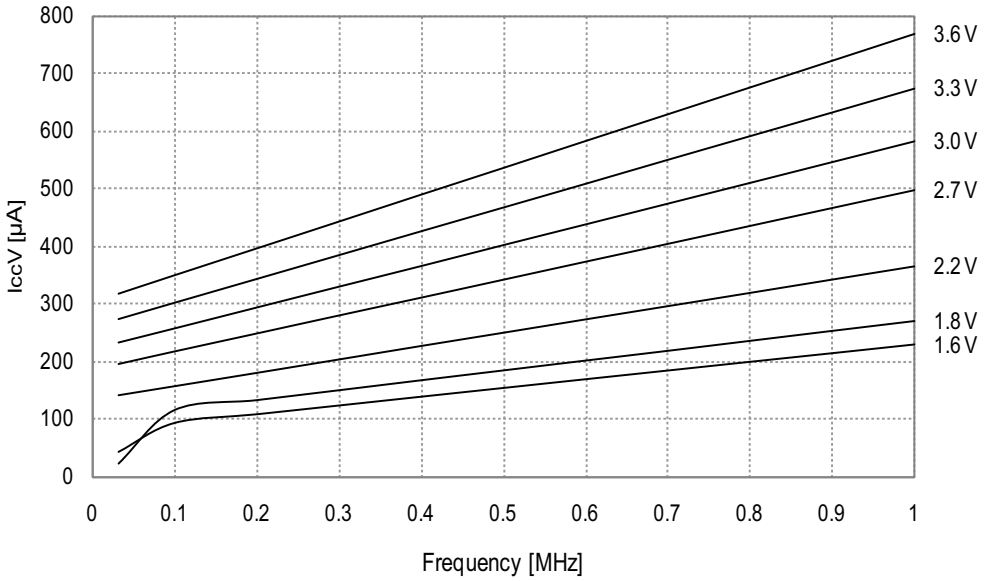


Figure 34-2. Active Supply Current vs. Frequency

f_{SYS} = 1 - 32MHz external clock, T = 25°C

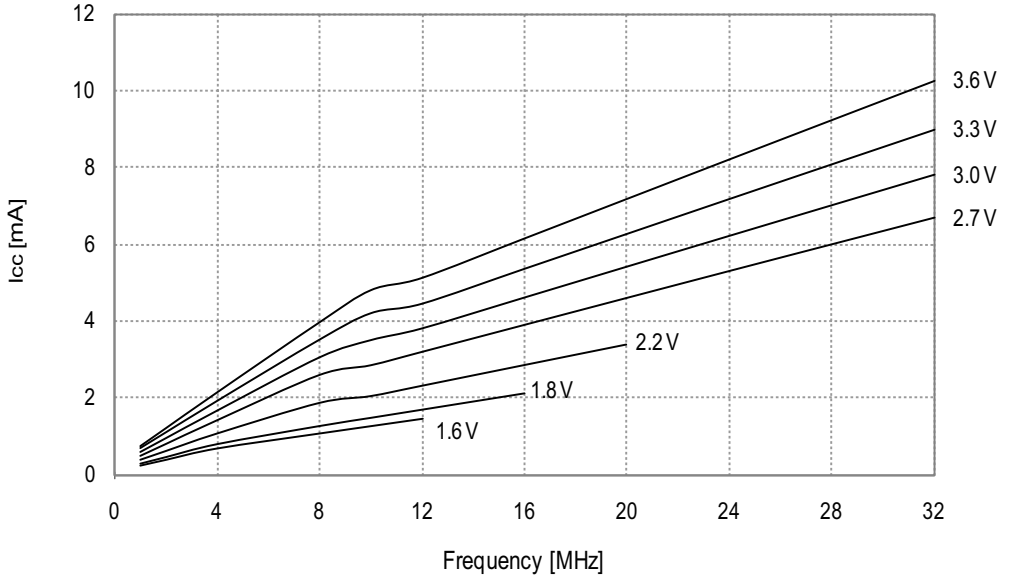
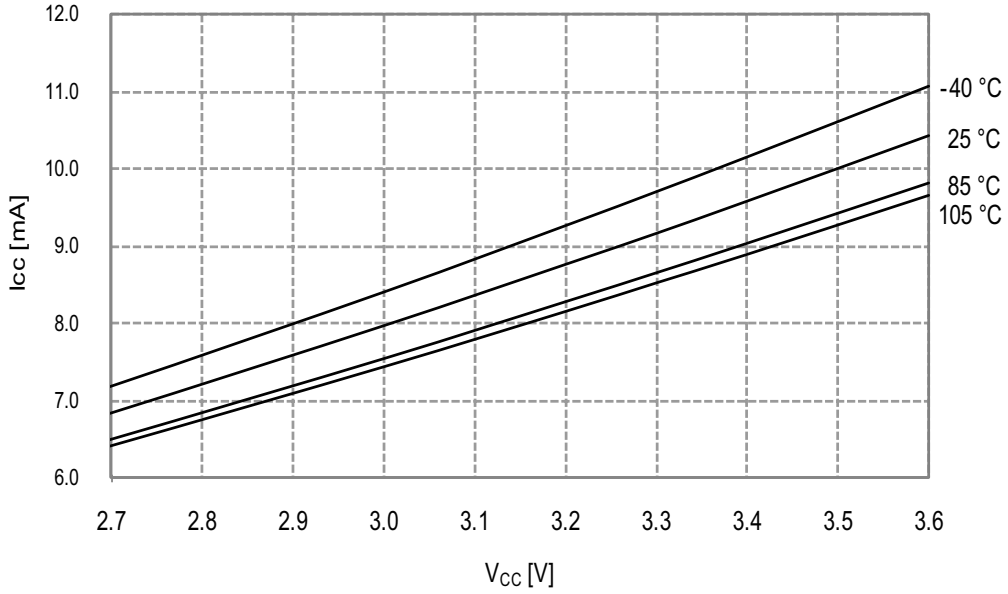


Figure 34-7. Active Mode Supply Current vs. V_{CC}

f_{SYS} = 32MHz internal oscillator



34.1.1.2 Idle Mode Supply Current

Figure 34-8. Idle Mode Supply Current vs. Frequency

f_{SYS} = 0 - 1MHz external clock, T = 25°C

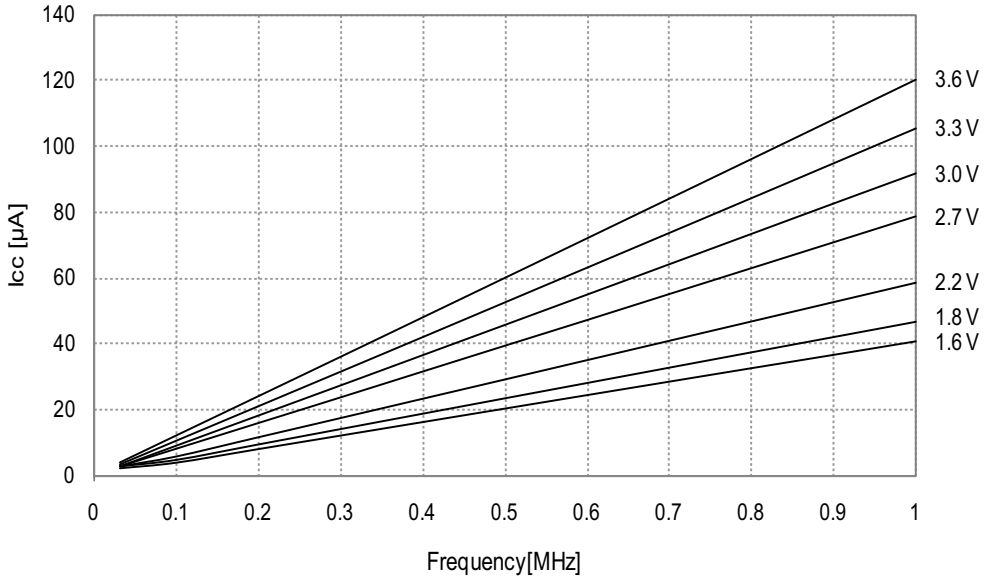


Figure 34-65. 32MHz Internal Oscillator CALA Calibration Step Size

$T = 105°C$, $V_{CC} = 3.0V$

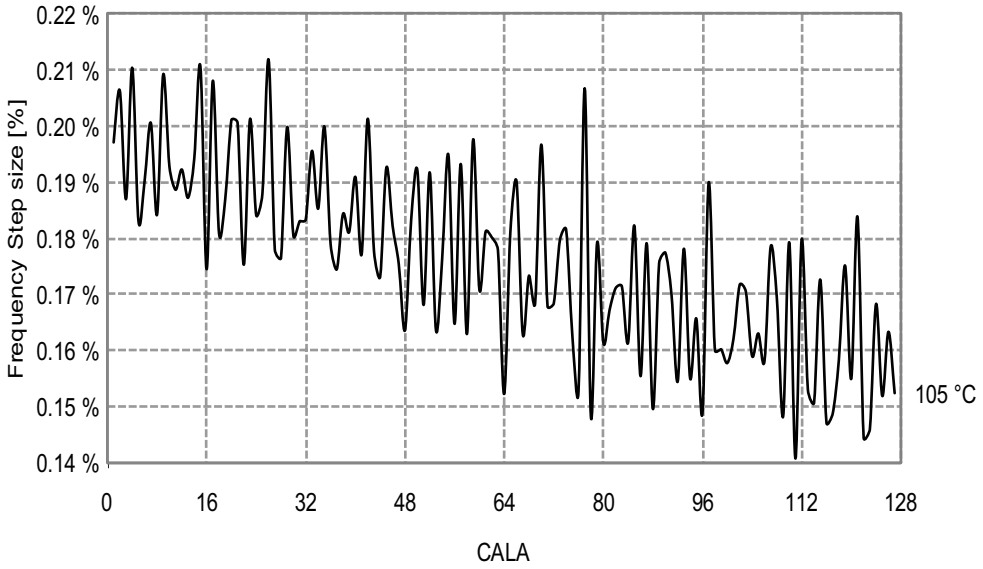
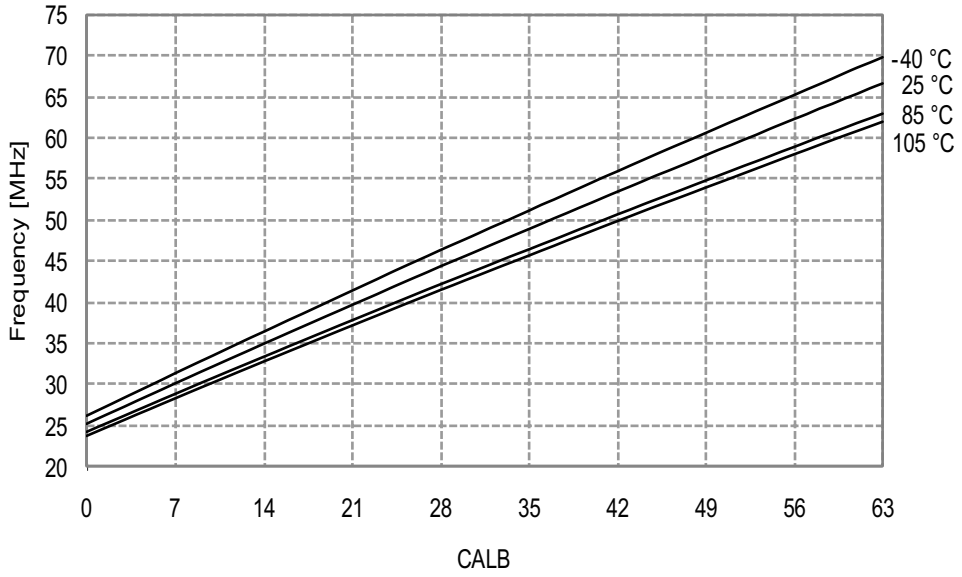


Figure 34-66. 32MHz Internal Oscillator Frequency vs. CALB Calibration Value

$V_{CC} = 3.0V$



34.2.3 ADC Characteristics

Figure 34-102. INL Error vs. External V_{REF}

T = 25°C, V_{CC} = 3.6V, external reference

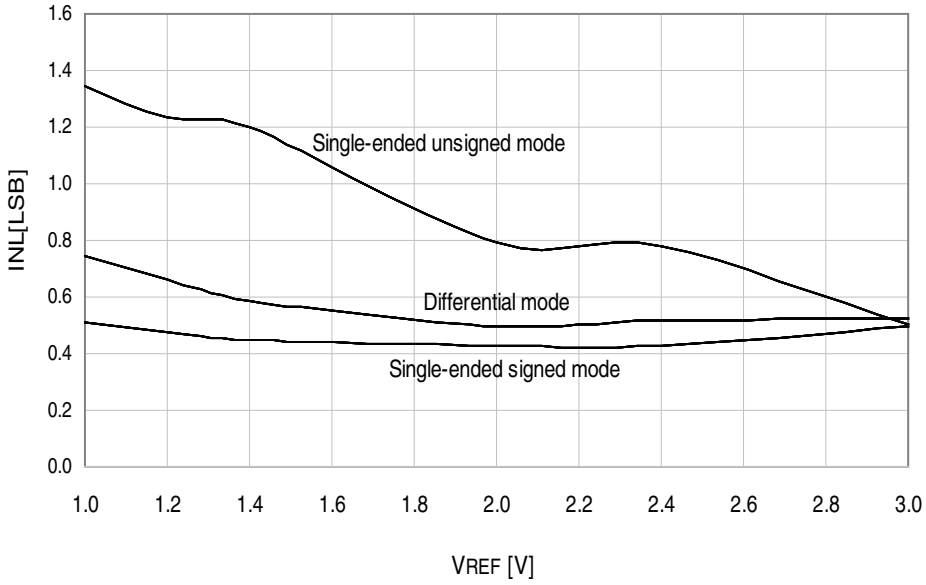


Figure 34-103. INL Error vs. Sample Rate

T = 25°C, V_{CC} = 3.6V, V_{REF} = 3.0V external

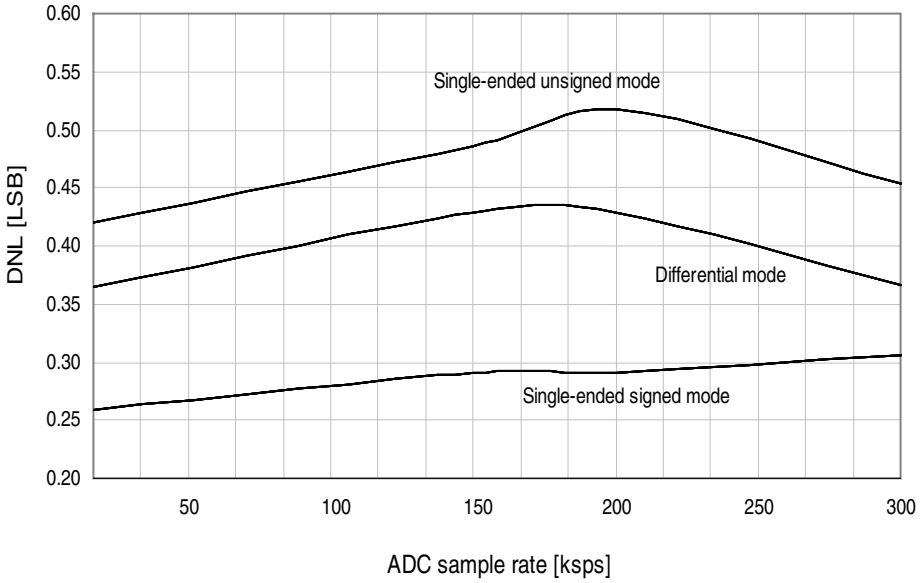
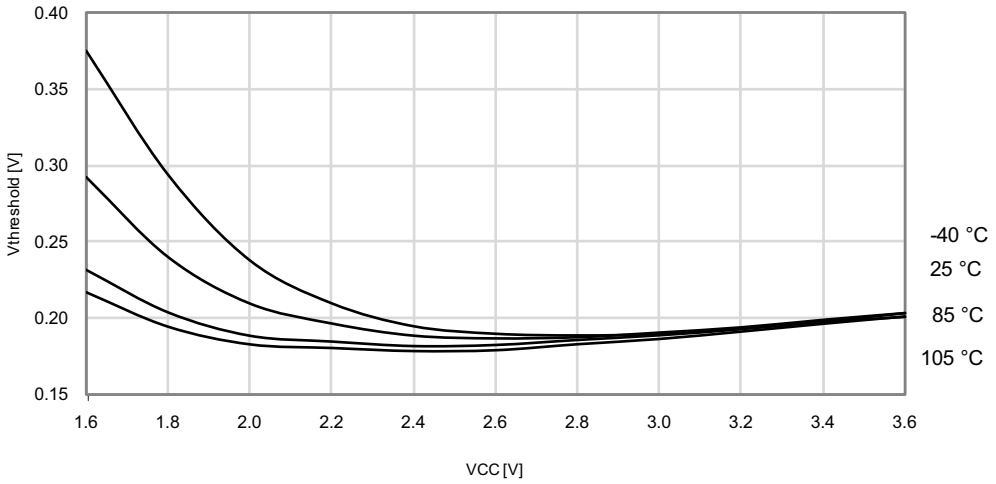


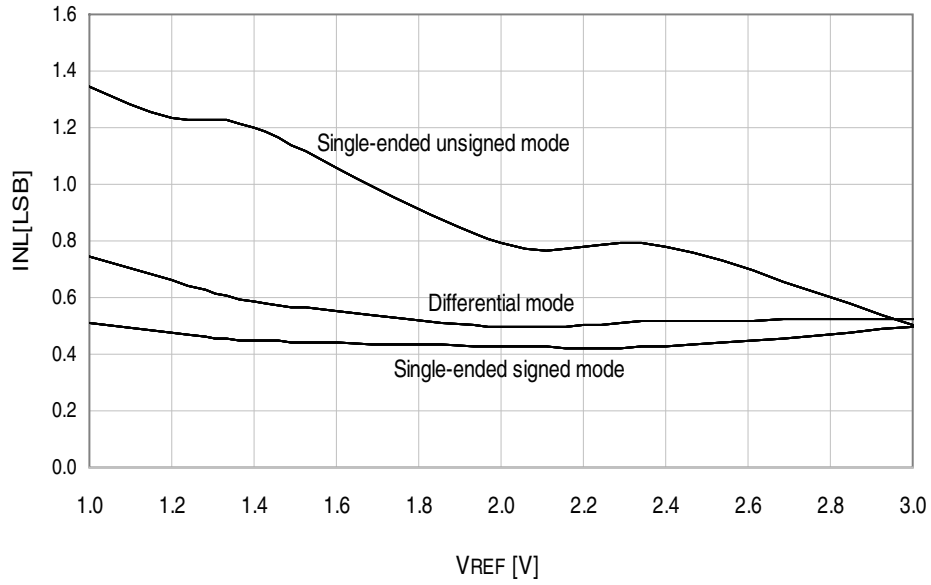
Figure 34-171. I/O Pin Input Hysteresis vs. V_{CC}



34.3.3 ADC Characteristics

Figure 34-172. INL Error vs. External V_{REF}

T = 25°C, V_{CC} = 3.6V, external reference



34.3.4 Analog Comparator Characteristics

Figure 34-183. Analog Comparator Hysteresis vs. V_{CC}

Small hysteresis

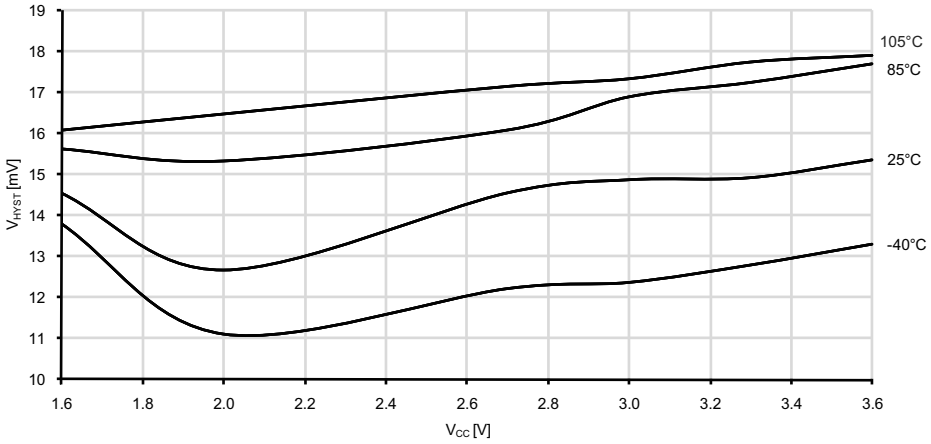


Figure 34-184. Analog Comparator Hysteresis vs. V_{CC}

Large hysteresis

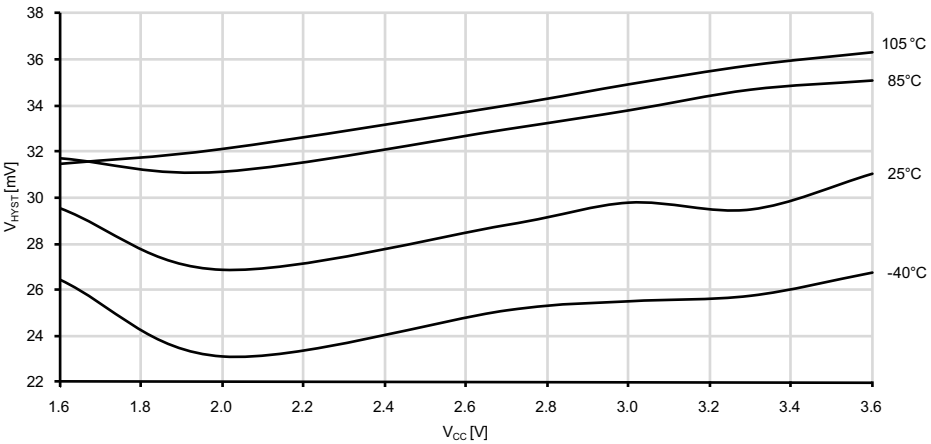


Figure 34-185. Analog Comparator Current Source vs. Calibration Value

V_{CC} = 3.0V

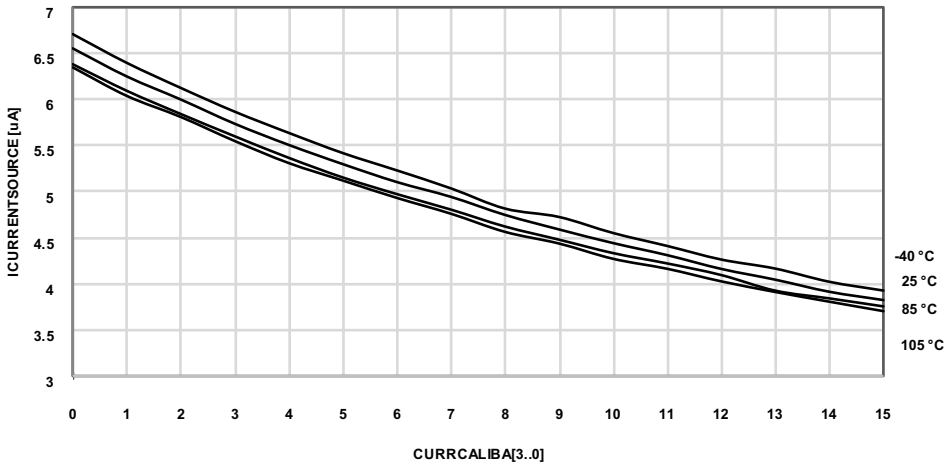
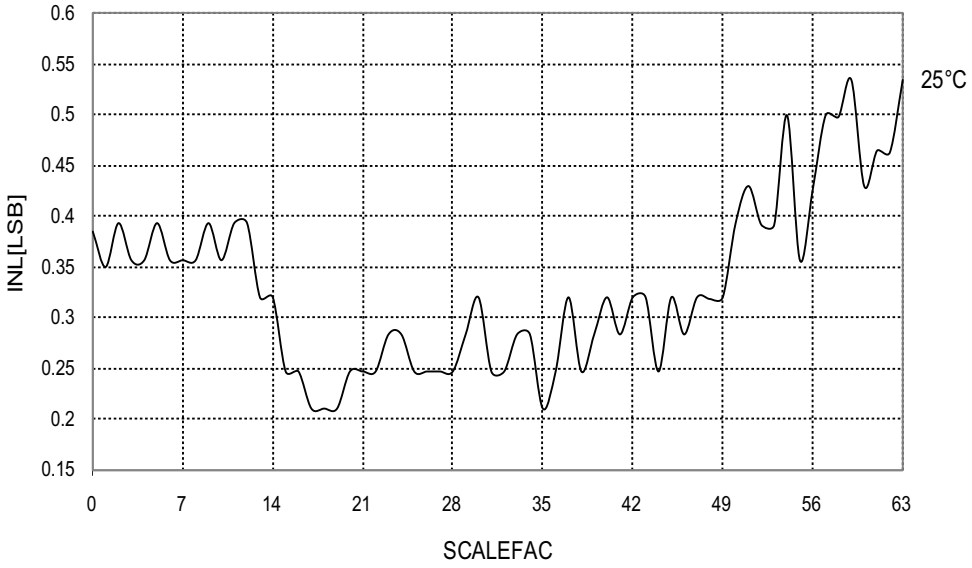


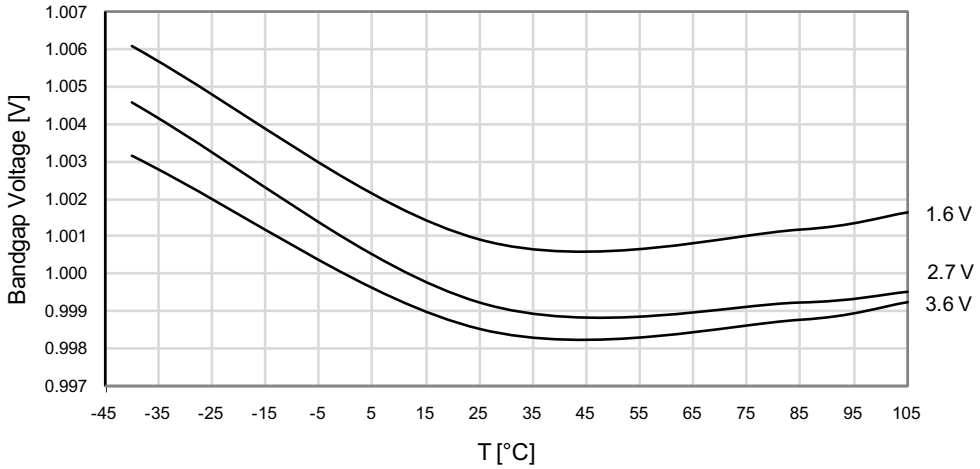
Figure 34-186. Voltage Scaler INL vs. SCALEFAC

T = 25°C, V_{CC} = 3.0V



34.3.5 Internal 1.0V Reference Characteristics

Figure 34-187. ADC Internal 1.0V Reference vs. Temperature



34.3.6 BOD Characteristics

Figure 34-188. BOD Thresholds vs. Temperature

BOD level = 1.6V

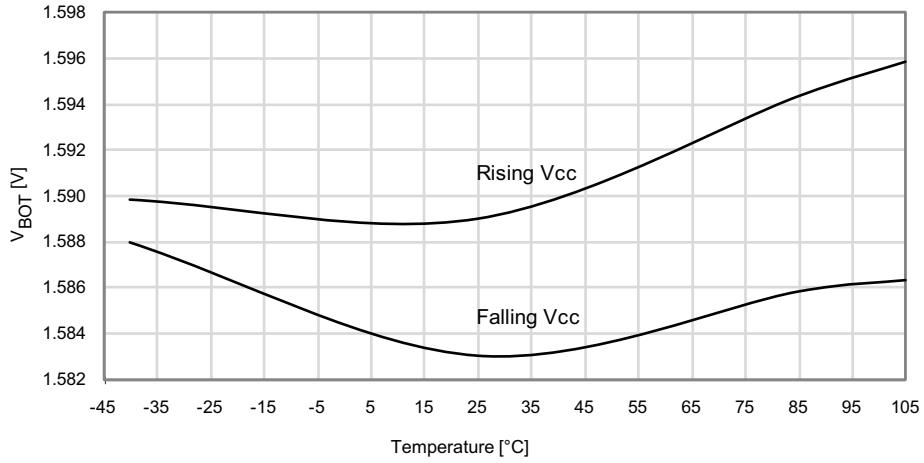
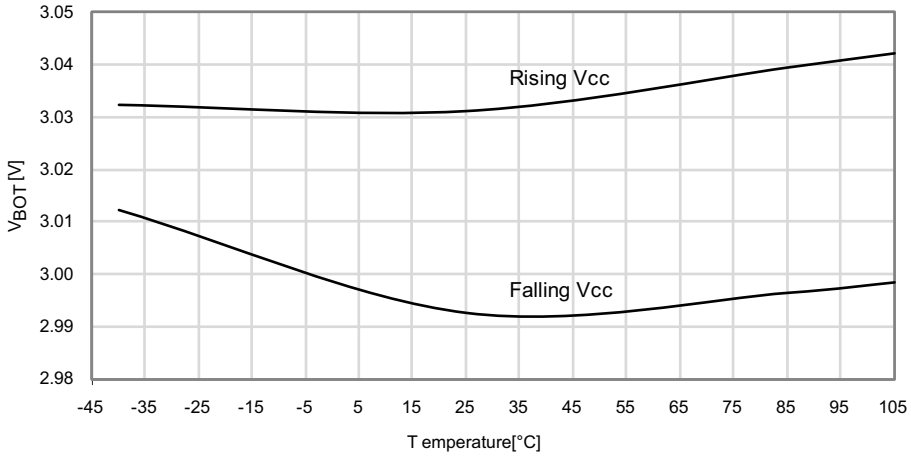


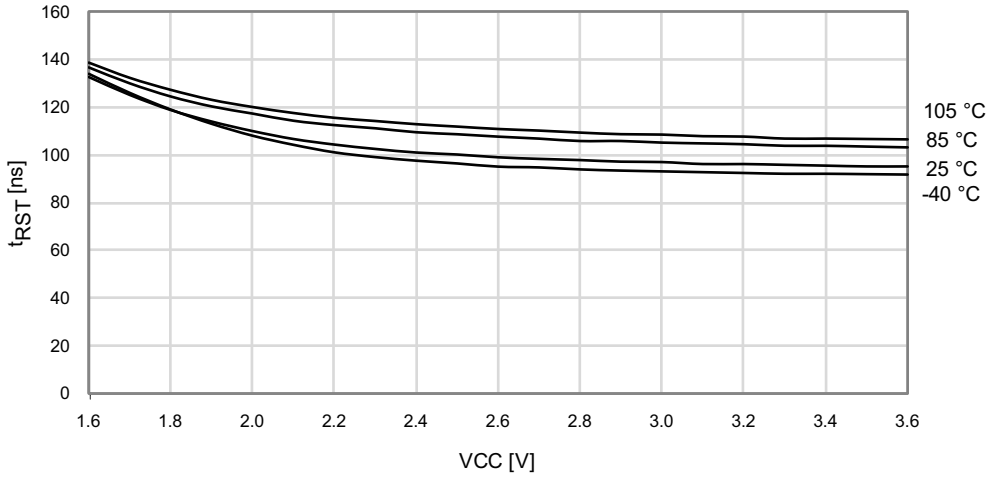
Figure 34-189. BOD Thresholds vs. Temperature

BOD level = 3.0V



34.3.7 External Reset Characteristics

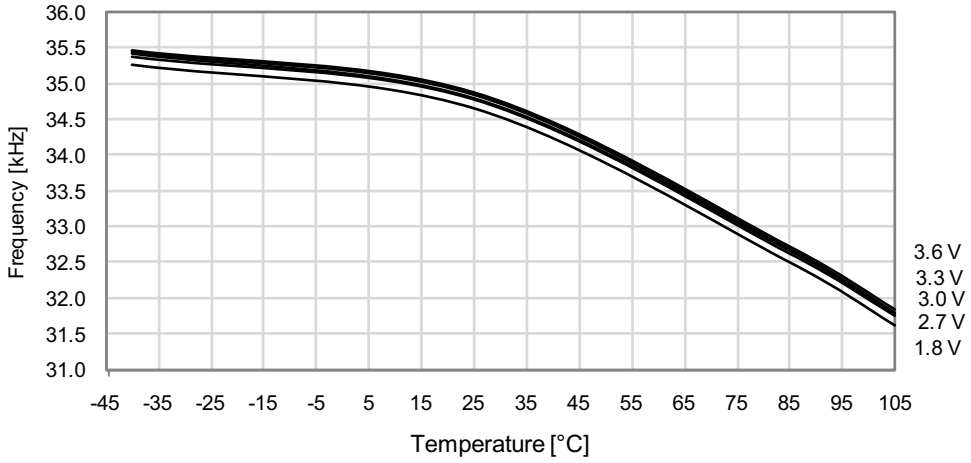
Figure 34-190. Minimum Reset Pin Pulse Width vs. V_{CC}



34.3.8 Oscillator Characteristics

34.3.8.1 Ultra Low-Power Internal Oscillator

Figure 34-195. Ultra Low-Power Internal Oscillator Frequency vs. Temperature



34.3.8.2 32.768kHz Internal Oscillator

Figure 34-196. 32.768kHz Internal Oscillator Frequency vs. Temperature

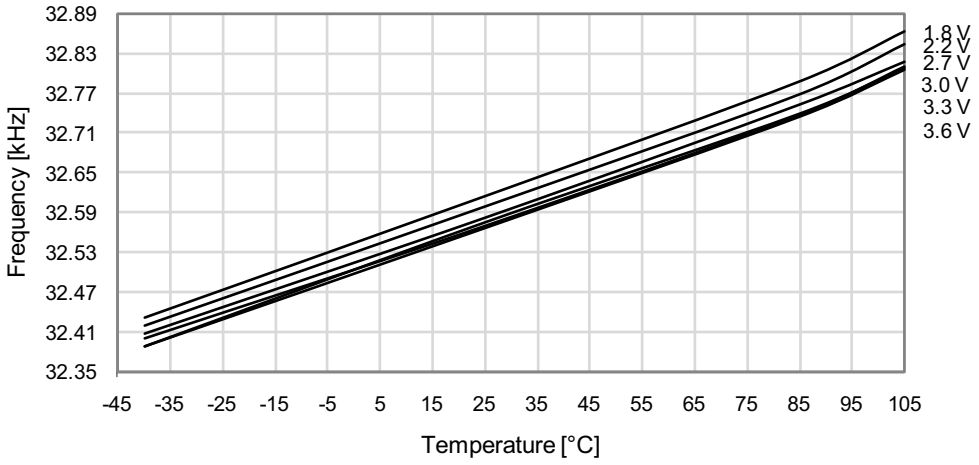


Figure 34-215. Active Mode Supply Current vs. V_{CC}

f_{SYS} = 32.768kHz internal oscillator

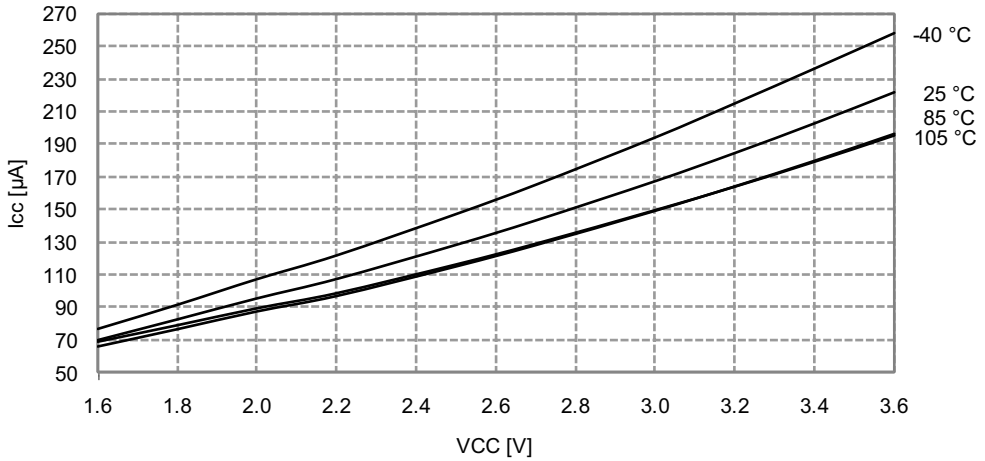


Figure 34-216. Active Mode Supply Current vs. V_{CC}

f_{SYS} = 1MHz external clock

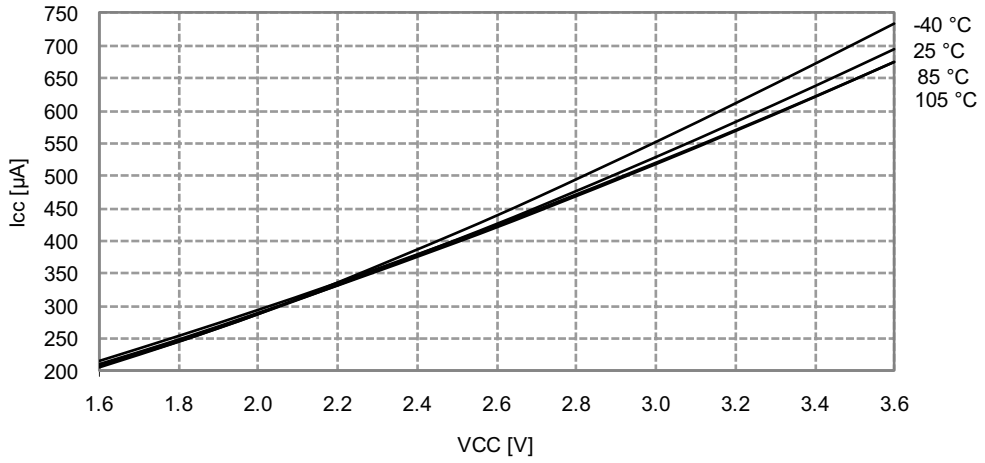


Figure 34-221. Idle Mode Supply Current vs. Frequency

f_{SYS} = 1 - 32MHz external clock, T = 25°C

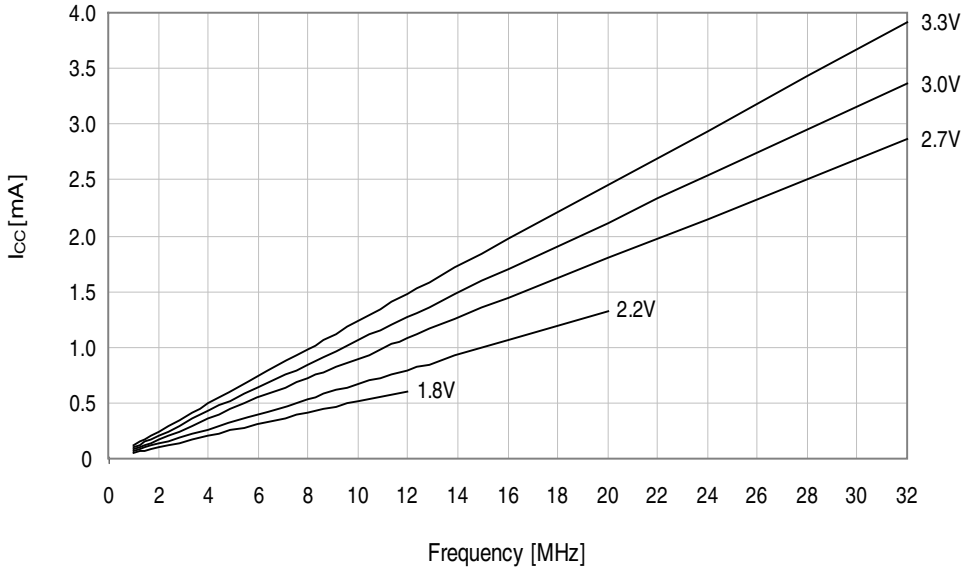


Figure 34-222. Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 32.768kHz internal oscillator

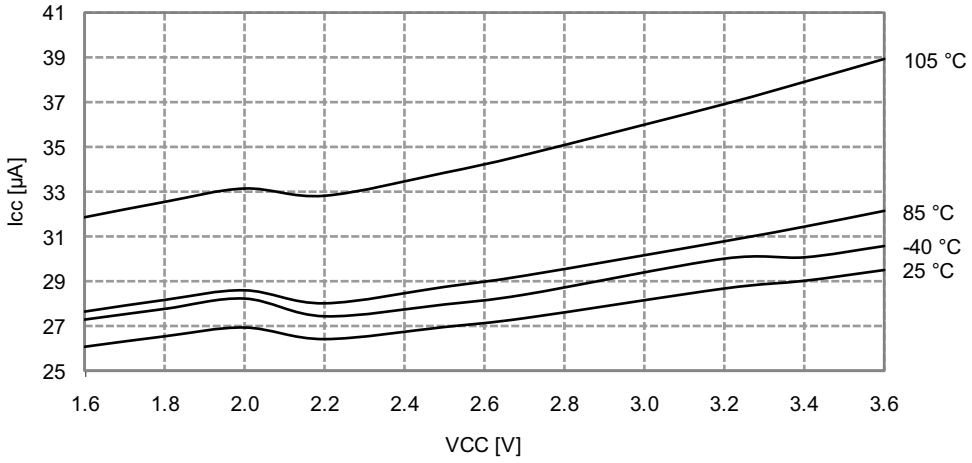


Figure 34-343. 32MHz Internal Oscillator CALA Calibration Step Size

T = -40°C, V_{CC} = 3.0V

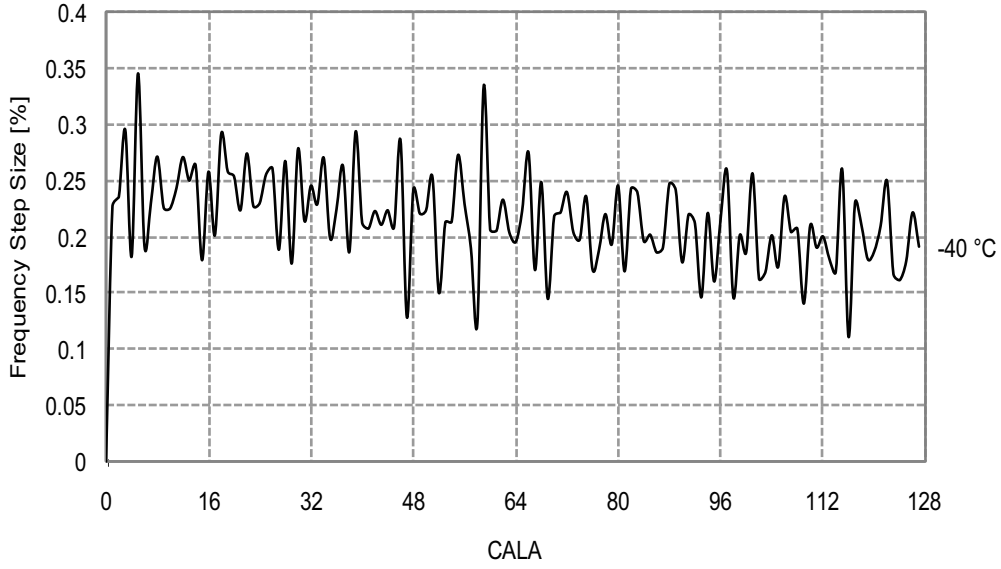
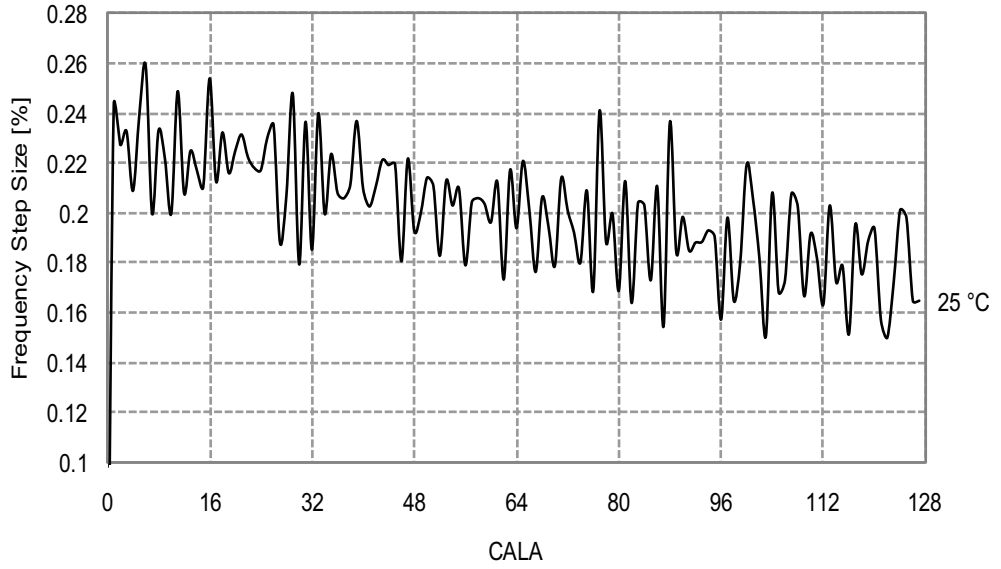


Figure 34-344. 32MHz Internal Oscillator CALA Calibration Step Size

T = 25°C, V_{CC} = 3.0V



36. Datasheet Revision History

Note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

36.1 8492G – 11/2014

1.	Updated the “Ordering Information” on page 2. Added ordering information for ATxmega32C3/64C3/128C3/192C3/256C3 @ 105°C.
2.	Updated Table 33-4 on page 67, Table 33-33 on page 86, Table 33-62 on page 105, Table 33-91 on page 124 and Table 33-120 on page 143. Added I_{CC} Power-down power consumption for T=105°C for all functions disabled and for WDT and sampled BOD enabled.
3.	Updated Table 33-17 on page 75, Table 33-46 on page 94, Table 33-75 on page 113, Table 33-104 on page 132 and Table 33-133 on page 151. Updated all tables to include values for T=85°C and T=105°C. Removed T=55°C.
4.	Updated “Bandgap and Internal 1.0V Reference Characteristics” on page 93: ● Added values of INT1V for T= 105°C, calibrated at 85°C
5.	Changed V_{CC} to AV_{CC} in Section 26. “ADC – 12-bit Analog to Digital Converter” on page 46 and Section 27. “AC – Analog Comparator” on page 48.
6.	Changed EEPROM size to 1K for 32C3 in Section 1. “Ordering Information” on page 2, in Table 7-2 on page 15 and in Table 7-3 on page 17.
7.	TWI electrical characteristics: Units of Data setup time ($t_{SU;DAT}$) changed from µs to ns in: ● ATxmega32C3: Table 33-29 on page 83 ● ATxmega64C3: Table 33-58 on page 102 ● ATxmega128C3: Table 33-87 on page 121 ● ATxmega192C3: Table 33-116 on page 140 ● ATxmega256C3: Table 33-145 on page 159
8.	“Typical Characteristics” updated with 105°C data: ● “Atmel ATxmega32C3” on page 160 ● “Atmel ATxmega64C3” on page 196 ● “Atmel ATxmega128C3” on page 232 ● “Atmel ATxmega192C3” on page 267 ● “Atmel ATxmega256C3” on page 302
9.	Corrected use of capital letters and punctuation in headings, table headings and figure titles. Added trademarks to the back side.
10.	Cross references have been corrected.

36.2 8492F – 07/2013

1.	Errata **Temperature sensor not calibrated** added to: ● ATxmega256C3 “Rev I” on page 337 ● ATxmega192C3 “Rev I” on page 338 ● ATxmega128C3 “Rev J” on page 339 ● ATxmega64C3 “Rev I” on page 340 ● ATxmega32C3 “Rev I” on page 341

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