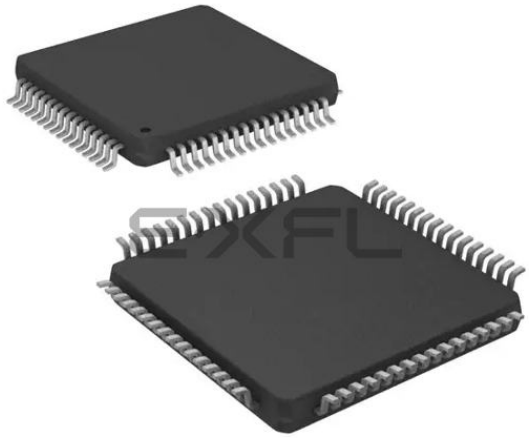

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	50
Program Memory Size	256KB (128K x 16)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega256c3-an

9. System Clock and Clock Options

9.1 Features

- Fast start-up time
- Safe run-time clock switching
- Internal oscillators:
  - 32MHz run-time calibrated and tuneable oscillator
  - 2MHz run-time calibrated oscillator
  - 32.768kHz calibrated oscillator
  - 32kHz ultra low power (ULP) oscillator with 1kHz output
- External clock options
  - 0.4MHz - 16MHz crystal oscillator
  - 32.768kHz crystal oscillator
  - External clock
- PLL with 20MHz - 128MHz output frequency
  - Internal and external clock options and 1x to 31x multiplication
  - Lock detector
- Clock prescalers with 1x to 2048x division
- Fast peripheral clocks running at two and four times the CPU clock
- Automatic run-time calibration of internal oscillators
- External oscillator and PLL lock failure detection with optional non-maskable interrupt

9.2 Overview

Atmel AVR XMEGA C3 devices have a flexible clock system supporting a large number of clock sources. It incorporates both accurate internal oscillators and external crystal oscillator and resonator support. A high-frequency phase locked loop (PLL) and clock prescalers can be used to generate a wide range of clock frequencies. A calibration feature (DFLL) is available, and can be used for automatic run-time calibration of the internal oscillators to remove frequency drift over voltage and temperature. An oscillator failure monitor can be enabled to issue a non-maskable interrupt and switch to the internal oscillator if the external oscillator or PLL fails.

When a reset occurs, all clock sources except the 32kHz ultra low power oscillator are disabled. After reset, the device will always start up running from the 2MHz internal oscillator. During normal operation, the system clock source and prescalers can be changed from software at any time.

Figure 9-1 on page 20 presents the principal clock system. Not all of the clocks need to be active at a given time. The clocks for the CPU and peripherals can be stopped using sleep modes and power reduction registers, as described in “Power Management and Sleep Modes” on page 22.

20. USB – Universal Serial Bus Interface

20.1 Features

- One USB 2.0 full speed (12Mbps) and low speed (1.5Mbps) device compliant interface
- Integrated on-chip USB transceiver, no external components needed
- 16 endpoint addresses with full endpoint flexibility for up to 31 endpoints
  - One input endpoint per endpoint address
  - One output endpoint per endpoint address
- Endpoint address transfer type selectable to
  - Control transfers
  - Interrupt transfers
  - Bulk transfers
  - Isochronous transfers
- Configurable data payload size per endpoint, up to 1023 bytes
- Endpoint configuration and data buffers located in internal SRAM
  - Configurable location for endpoint configuration data
  - Configurable location for each endpoint's data buffer
- Built-in direct memory access (DMA) to internal SRAM for:
  - Endpoint configurations
  - Reading and writing endpoint data
- Ping-pong operation for higher throughput and double buffered operation
  - Input and output endpoint data buffers used in a single direction
  - CPU can update data buffer during transfer
- Multipacket transfer for reduced interrupt load and software intervention
  - Data payload exceeding maximum packet size is transferred in one continuous transfer
  - No interrupts or software interaction on packet transaction level
- Transaction complete FIFO for workflow management when using multiple endpoints
  - Tracks all completed transactions in a first-come, first-served work queue
- Clock selection independent of system clock source and selection
- Minimum 1.5MHz CPU clock required for low speed USB operation
- Minimum 12MHz CPU clock required for full speed operation
- Connection to event system
- On chip debug possibilities during USB transactions

20.2 Overview

The USB module is a USB 2.0 full speed (12Mbps) and low speed (1.5Mbps) device compliant interface.

The USB supports 16 endpoint addresses. All endpoint addresses have one input and one output endpoint, for a total of 31 configurable endpoints and one control endpoint. Each endpoint address is fully configurable and can be configured for any of the four transfer types; control, interrupt, bulk, or isochronous. The data payload size is also selectable, and it supports data payloads up to 1023 bytes.

No dedicated memory is allocated for or included in the USB module. Internal SRAM is used to keep the configuration for each endpoint address and the data buffer for each endpoint. The memory locations used for endpoint configurations and data buffers are fully configurable. The amount of memory allocated is fully dynamic, according to the number of endpoints in use and the configuration of these. The USB module has built-in direct memory access (DMA), and will read/write data from/to the SRAM when a USB transaction takes place.

To maximize throughput, an endpoint address can be configured for ping-pong operation. When done, the input and output endpoints are both used in the same direction. The CPU can then read/write one data buffer while the USB module writes/reads the others, and vice versa. This gives double buffered communication.

22. SPI – Serial Peripheral Interface

22.1 Features

- Two Identical SPI peripherals
- Full-duplex, three-wire synchronous data transfer
- Master or slave operation
- Lsb first or msb first data transfer
- Eight programmable bit rates
- Interrupt flag at the end of transmission
- Write collision flag to indicate data collision
- Wake up from idle sleep mode
- Double speed master mode

22.2 Overview

The Serial Peripheral Interface (SPI) is a high-speed synchronous data transfer interface using three or four pins. It allows fast communication between an Atmel AVR XMEGA device and peripheral devices or between several microcontrollers. The SPI supports full-duplex communication.

A device connected to the bus must act as a master or slave. The master initiates and controls all data transactions.

PORTC and PORTD each has one SPI. Notation of these peripherals are SPIC and SPID, respectively.

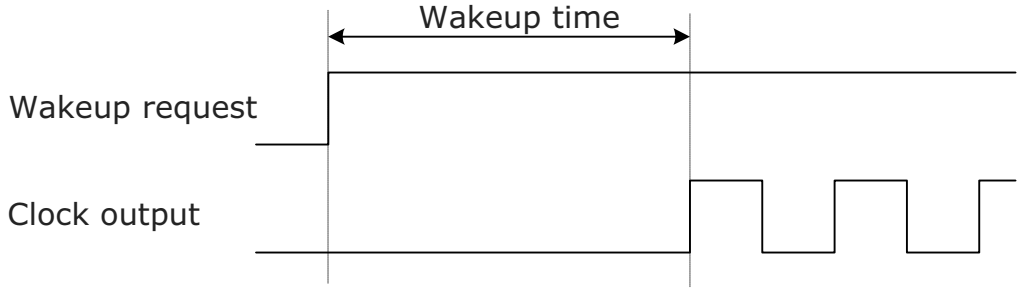
33.1.4 Wake-up Time from Sleep Modes

Table 33-6. Device Wake-up Time from Sleep Modes with Various System Clock Sources

Symbol	Parameter	Condition	Min.	Typ.(1)	Max.	Units
t_{wakeup}	Wake-up time from Idle, Standby, and Extended Standby mode	External 2MHz clock		2.0		µs
		32.768kHz internal oscillator		125		
		2MHz internal oscillator		2.0		
		32MHz internal oscillator		0.2		
	Wake-up time from Power-save and Power-down mode	External 2MHz clock		4.6		
		32.768kHz internal oscillator		330		
		2MHz internal oscillator		9.5		
		32MHz internal oscillator		5.6		

Note: 1. The wake-up time is the time from the wake-up request is given until the peripheral clock is available on pin, see Figure 33-2. All peripherals and modules start execution from the first clock cycle, expect the CPU that is halted for four clock cycles before program execution starts.

Figure 33-2. Wake-up Time Definition



33.1.13.5 Internal Phase Locked Loop (PLL) Characteristics

Table 33-23. Internal PLL Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{IN}	Input frequency	Output frequency must be within f_{OUT}	0.4		64	MHz
f_{OUT}	Output frequency(1)	V_{CC}= 1.6 - 1.8V	20		48	
		V_{CC}= 2.7 - 3.6V	20		128	
	Start-up time			25		µs
	Re-lock time			25		

Note: 1. The maximum output frequency vs. supply voltage is linear between 1.8V and 2.7V, and can never be higher than four times the maximum CPU frequency.

33.1.13.6 External Clock Characteristics

Figure 33-3. External Clock Drive Waveform

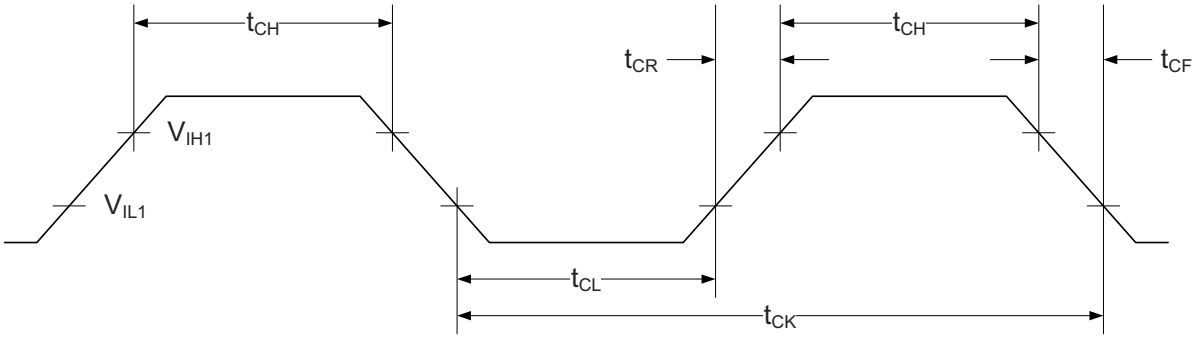


Table 33-24. External Clock used as System Clock without Prescaling

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock Frequency (1)	V_{CC} = 1.6 - 1.8V	0		12	MHz
		V_{CC} = 2.7 - 3.6V	0		32	
t_{CK}	Clock Period	V_{CC} = 1.6 - 1.8V	83.3			ns
		V_{CC} = 2.7 - 3.6V	31.5			
t_{CH}	Clock High Time	V_{CC} = 1.6 - 1.8V	30.0			
		V_{CC} = 2.7 - 3.6V	12.5			
t_{CL}	Clock Low Time	V_{CC} = 1.6 - 1.8V	30.0			
		V_{CC} = 2.7 - 3.6V	12.5			
t_{CR}	Rise Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			10	
		V_{CC} = 2.7 - 3.6V			3	
t_{CF}	Fall Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			10	
		V_{CC} = 2.7 - 3.6V			3	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Note: 1. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

33.2.5 I/O Pin Characteristics

The I/O pins complies with the JEDEC LVTTL and LVCMOS specification and the high- and low-level input and output voltage limits reflect or exceed this specification.

Table 33-36. I/O Pin Characteristics

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{OH} (1)/ I_{OL} (2)	I/O pin source/sink current			-15		15	mA
V_{IH}	High level input voltage	V_{CC} = 2.4 - 3.6V		0.7*Vcc		V_{CC}+0.5	V
		V_{CC} = 1.6 - 2.4V		0.8*V_{CC}		V_{CC}+0.5	
V_{IL}	Low level input voltage	V_{CC} = 2.4 - 3.6V		-0.5		0.3*V_{CC}	
		V_{CC} = 1.6 - 2.4V		-0.5		0.2*V_{CC}	
V_{OH}	High level output voltage	V_{CC} = 3.3V	I_{OH} = -4mA	2.6	2.9		
		V_{CC} = 3.0V	I_{OH} = -3mA	2.1	2.6		
		V_{CC} = 1.8V	I_{OH} = -1mA	1.4	1.6		
V_{OL}	Low level output voltage	V_{CC} = 3.3V	I_{OL} = 8mA		0.4	0.76	
		V_{CC} = 3.0V	I_{OL} = 5mA		0.3	0.64	
		V_{CC} = 1.8V	I_{OL} = 3mA		0.2	0.46	
I_{IN}	Input leakage current I/O pin	T = 25°C			<0.01	1.0	µA
R_P	Pull/Bus keeper resistor				25		kΩ

Notes:
1. The sum of all I_{OH} for PORTA and PORTB must not exceed 100mA.
   The sum of all I_{OH} for PORTC, PORTD, and PORTE must for each port not exceed 200mA.
   The sum of all I_{OH} for pins PF[0-5] on PORTF must not exceed 200mA.
   The sum of all I_{OL} for pins PF[6-7] on PORTF, PORTR, and PDI must not exceed 100mA.
2. The sum of all I_{OL} for PORTA and PORTB must not exceed 100mA.
   The sum of all I_{OL} for PORTC, PORTD, and PORTE must for each port not exceed 200mA.
   The sum of all I_{OL} for pins PF[0-5] on PORTF must not exceed 200mA.
   The sum of all I_{OL} for pins PF[6-7] on PORTF, PORTR, and PDI must not exceed 100mA.

33.2.11 Power-on Reset Characteristics

Table 33-45. Power-on Reset Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{POT-} (1)	POR threshold voltage falling V_{CC}	V_{CC} falls faster than 1V/ms	0.4	1.0		V
		V_{CC} falls at 1V/ms or slower	0.8	1.3		
V_{POT+}	POR threshold voltage rising V_{CC}			1.3	1.59	

Note: 1. V_{POT-} values are only valid when BOD is disabled. When BOD is enabled $V_{POT-} = V_{POT+}$.

33.2.12 Flash and EEPROM Memory Characteristics

Table 33-46. Endurance and Data Retention

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Flash	Write/Erase cycles	25°C	10K			Cycle
			85°C	10K			
			105°C	2K			
		Data retention	25°C	100			Year
			85°C	25			
			105°C	10			
	EEPROM	Write/Erase cycles	25°C	100K			Cycle
			85°C	100K			
			105°C	30K			
		Data retention	25°C	100			Year
			85°C	25			
			105°C	10			

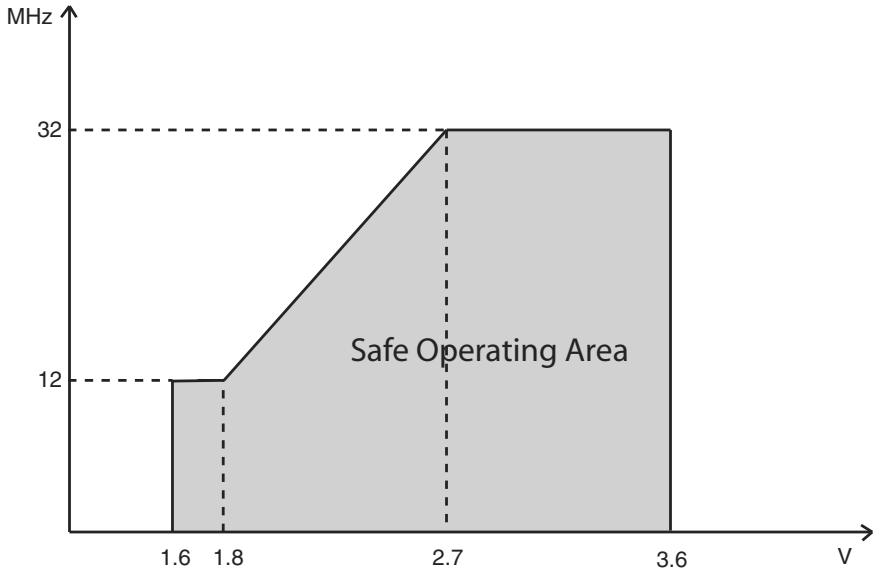
Table 33-47. Programming Time

Symbol	Parameter	Condition	Min.	Typ.(1)	Max.	Units
	Chip erase(2)	64KB Flash, EEPROM		55		ms
	Application erase	Section erase		6		
	Flash	Page erase		4		
		Page write		4		
		Atomic page erase and write		8		
	EEPROM	Page erase		4		
		Page write		4		
		Atomic page erase and write		8		

Notes: 1. Programming is timed from the 2MHz internal oscillator.
2. EEPROM is not erased if the EESAVE fuse is programmed.

The maximum CPU clock frequency depends on V_{CC}. As shown in Figure 33-15 the Frequency vs. V_{CC} curve is linear between 1.8V < V_{CC} < 2.7V.

Figure 33-15.Maximum Frequency vs. V_{CC}



33.3.4 Wake-up Time from Sleep Modes

Table 33-64. Device Wake-up Time from Sleep Modes with Various System Clock Sources

Symbol	Parameter	Condition	Min.	Typ. (1)	Max.	Units
t_{wakeup}	Wake-up time from Idle, Standby, and Extended Standby mode	External 2MHz clock		2.0		µs
		32.768kHz internal oscillator		130		
		2MHz internal oscillator		2.0		
		32MHz internal oscillator		0.2		
	Wake-up time from Power-save and Power-down mode	External 2MHz clock		4.5		
		32.768kHz internal oscillator		320		
		2MHz internal oscillator		9.0		
		32MHz internal oscillator		6.5		

Note: 1. The wake-up time is the time from the wake-up request is given until the peripheral clock is available on pin, see Figure 33-16. All peripherals and modules start execution from the first clock cycle, expect the CPU that is halted for four clock cycles before program execution starts.

Figure 33-16.Wake-up Time Definition

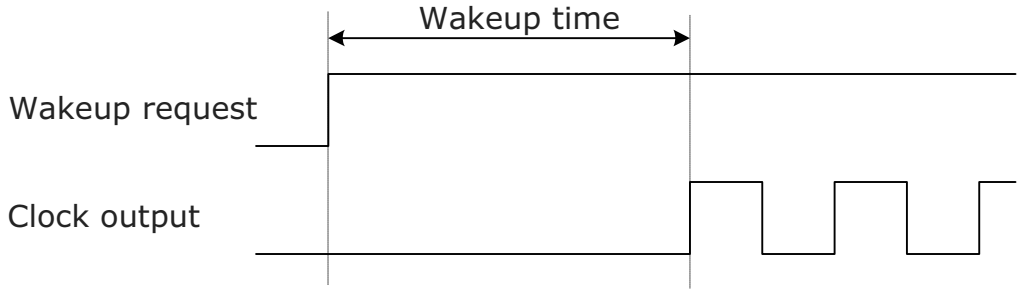


Table 33-141.External Clock with Prescaler (1) for System Clock

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock Frequency (2)	V_{CC} = 1.6 - 1.8V	0		90	MHz
		V_{CC} = 2.7 - 3.6V	0		142	
t_{CK}	Clock Period	V_{CC} = 1.6 - 1.8V	11			ns
		V_{CC} = 2.7 - 3.6V	7			
t_{CH}	Clock High Time	V_{CC} = 1.6 - 1.8V	4.5			
		V_{CC} = 2.7 - 3.6V	2.4			
t_{CL}	Clock Low Time	V_{CC} = 1.6 - 1.8V	4.5			
		V_{CC} = 2.7 - 3.6V	2.4			
t_{CR}	Rise Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			1.5	
		V_{CC} = 2.7 - 3.6V			1.0	
t_{CF}	Fall Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			1.5	
		V_{CC} = 2.7 - 3.6V			1.0	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Notes: 1. System Clock Prescalers must be set so that maximum CPU clock frequency for device is not exceeded.
2. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

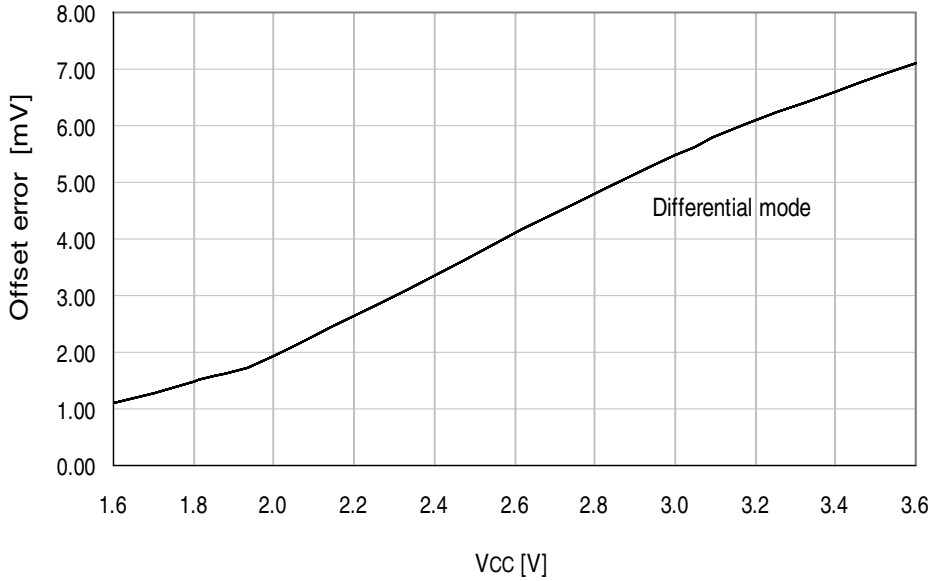
33.5.13.7 External 16MHz Crystal Oscillator and XOSC Characteristics

Table 33-142. External 16MHz Crystal Oscillator and XOSC Characteristics

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Cycle to cycle jitter	XOSCPWR=0	FRQRANGE=0		0		ns
			FRQRANGE=1, 2, or 3		0		
		XOSCPWR=1			0		
	Long term jitter	XOSCPWR=0	FRQRANGE=0		0		
			FRQRANGE=1, 2, or 3		0		
		XOSCPWR=1			0		
	Frequency error	XOSCPWR=0	FRQRANGE=0		0.03		%
			FRQRANGE=1		0.03		
			FRQRANGE=2 or 3		0.03		
		XOSCPWR=1			0.003		
	Duty cycle	XOSCPWR=0	FRQRANGE=0		50		
			FRQRANGE=1		50		
			FRQRANGE=2 or 3		50		
		XOSCPWR=1			50		

Figure 34-41. Offset Error vs. V_{CC}

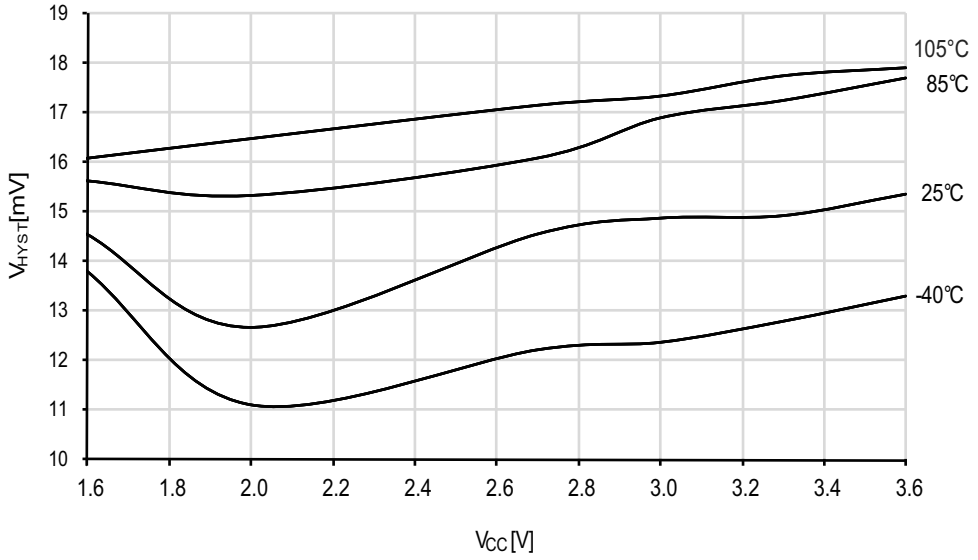
T = 25°C, V_{REF} = external 1.0V, ADC sample rate = 300ksps



34.1.4 Analog Comparator Characteristics

Figure 34-42. Analog Comparator Hysteresis vs. V_{CC}

Small hysteresis



34.1.8.2 32.768kHz Internal Oscillator

Figure 34-55. 32.768kHz Internal Oscillator Frequency vs. Temperature

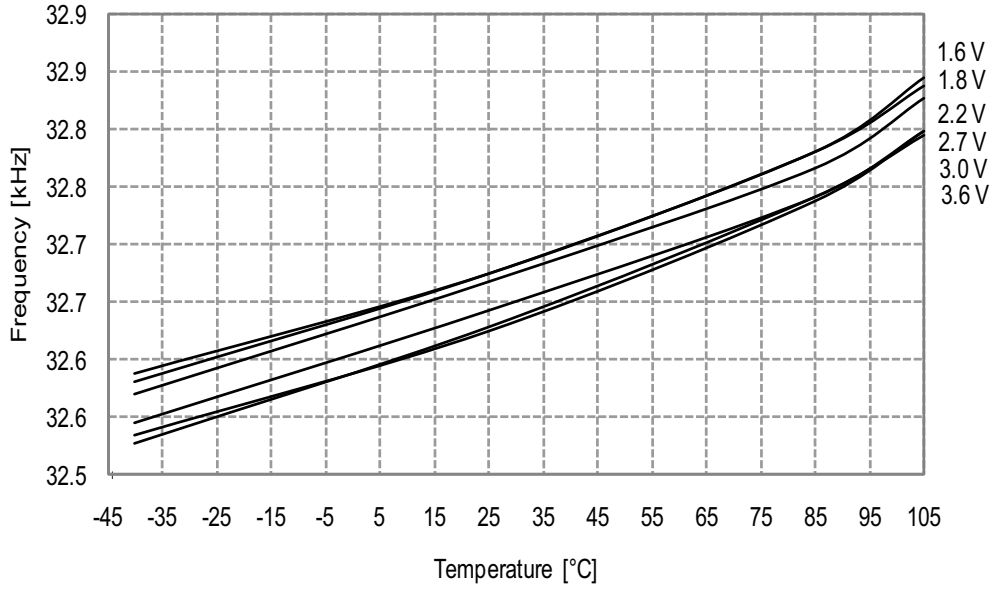


Figure 34-56. 32.768kHz Internal Oscillator Frequency vs. Calibration Value

V_{CC} = 3.0V, T = 25°C

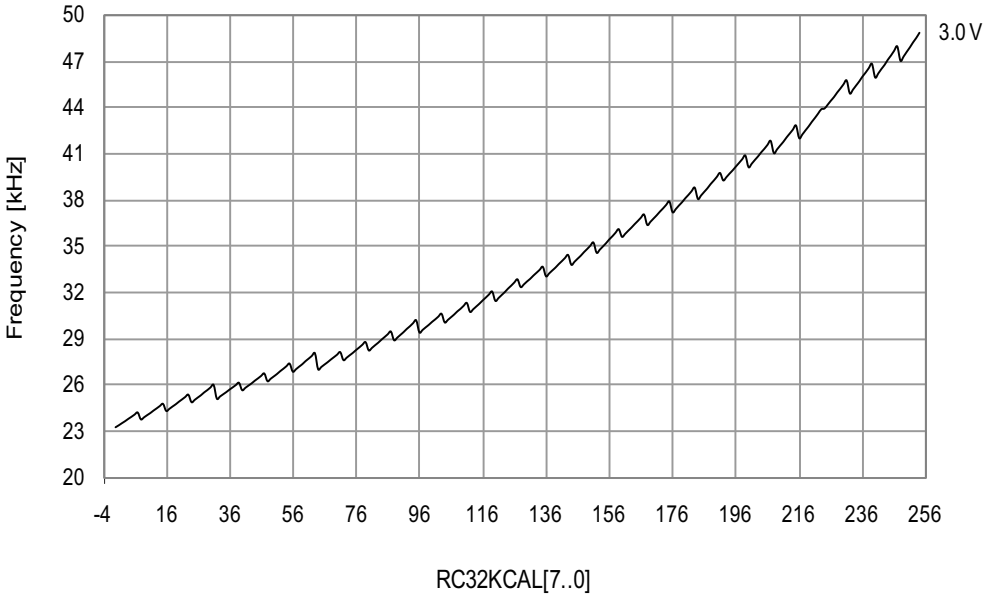
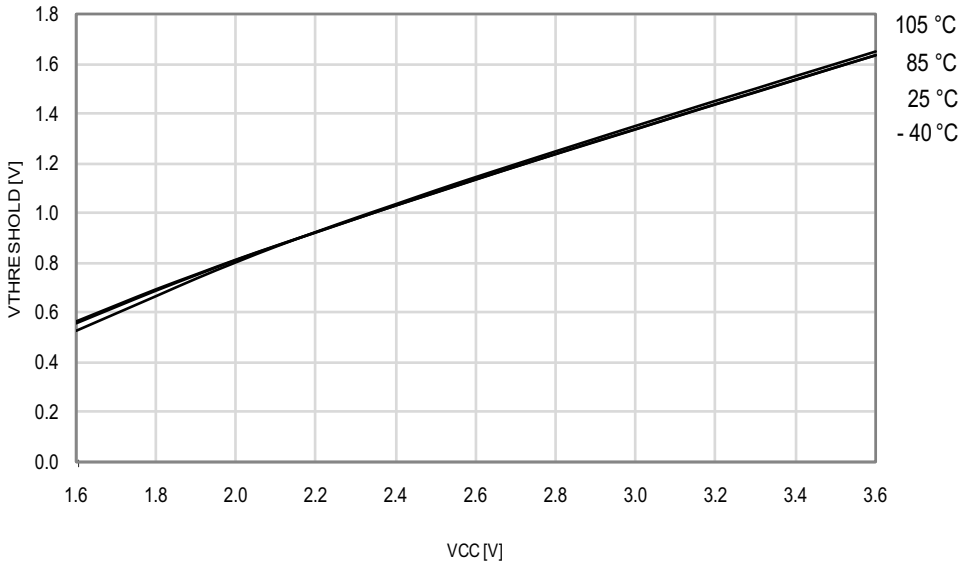


Figure 34-124. Reset Pin Input Threshold Voltage vs. V_{CC}

V_{IH} - Reset pin read as "1"



34.2.8 Oscillator Characteristics

34.2.8.1 Ultra Low-Power Internal Oscillator

Figure 34-125. Ultra Low-Power Internal Oscillator Frequency vs. Temperature

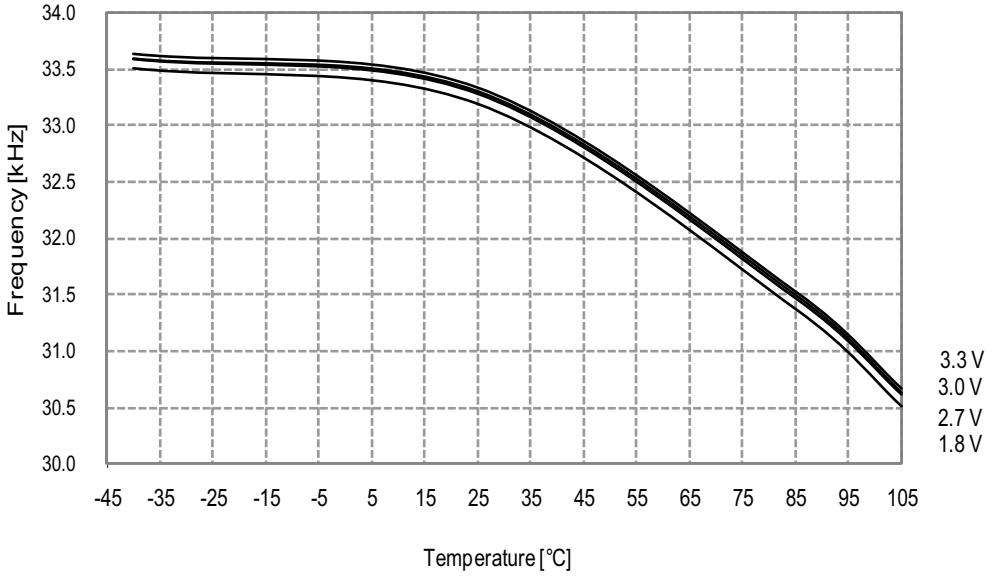


Figure 34-151. Idle Mode Supply Current vs. Frequency

f_{SYS} = 1 - 32MHz external clock, T = 25°C

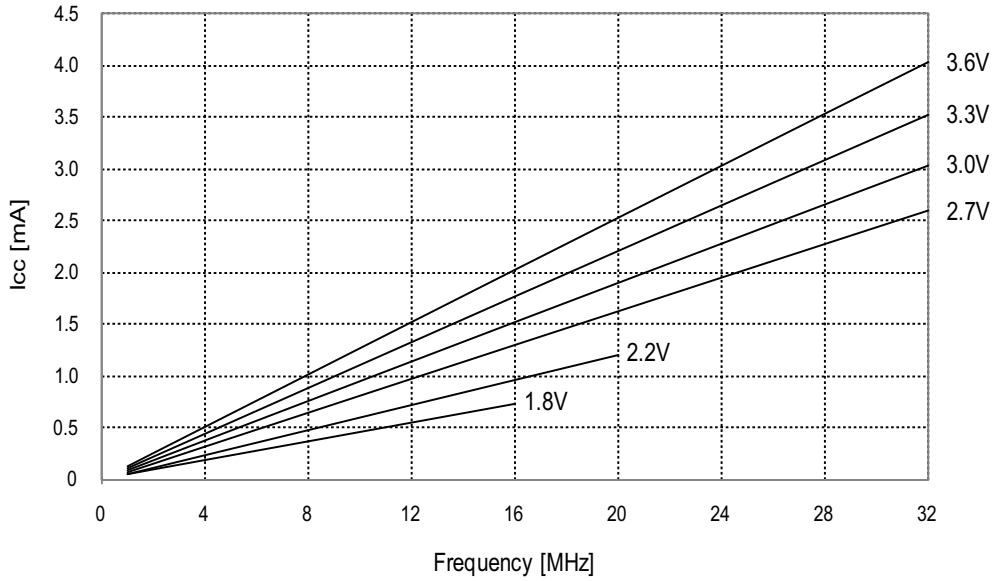


Figure 34-152. Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 32.768kHz internal oscillator

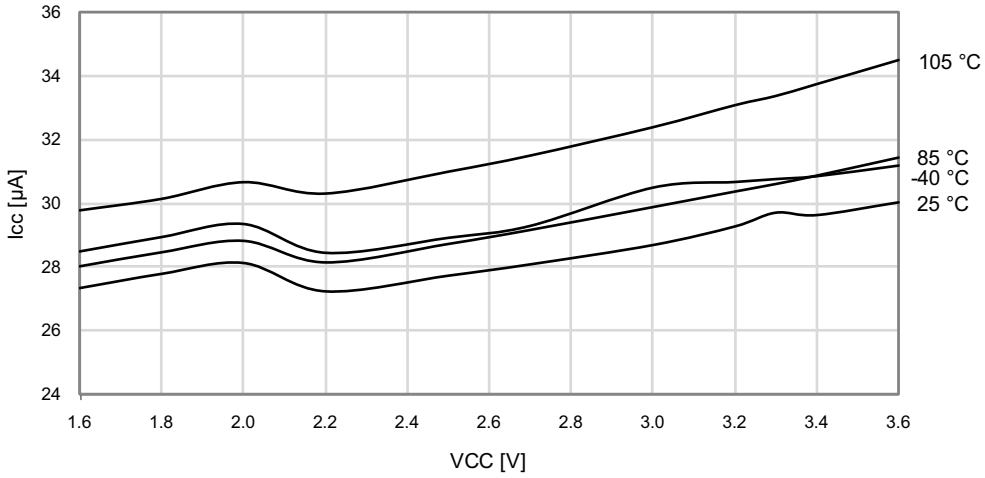
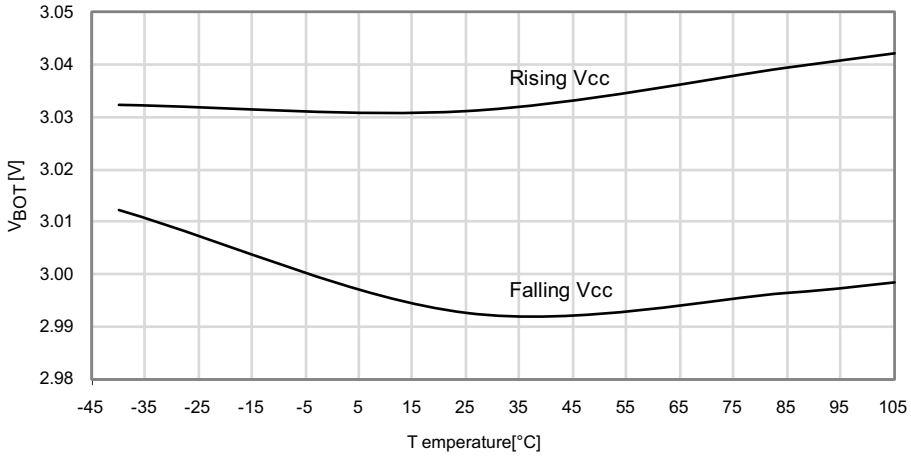


Figure 34-189. BOD Thresholds vs. Temperature

BOD level = 3.0V



34.3.7 External Reset Characteristics

Figure 34-190. Minimum Reset Pin Pulse Width vs. V_{CC}

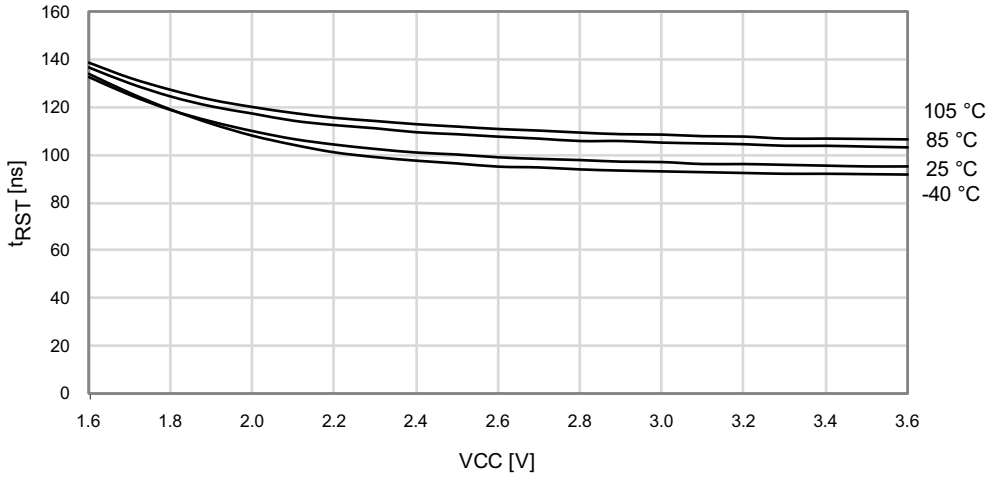


Figure 34-203. 32MHz Internal Oscillator CALA Calibration Step Size

T = -40°C, V_{CC} = 3.0V

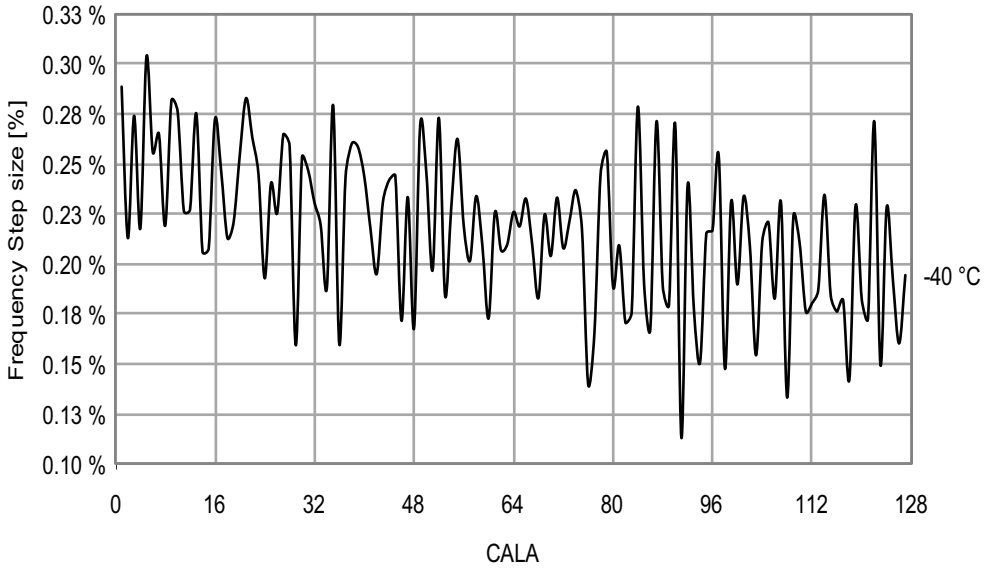


Figure 34-204. 32MHz Internal Oscillator CALA Calibration Step Size

T = 25°C, V_{CC} = 3.0V

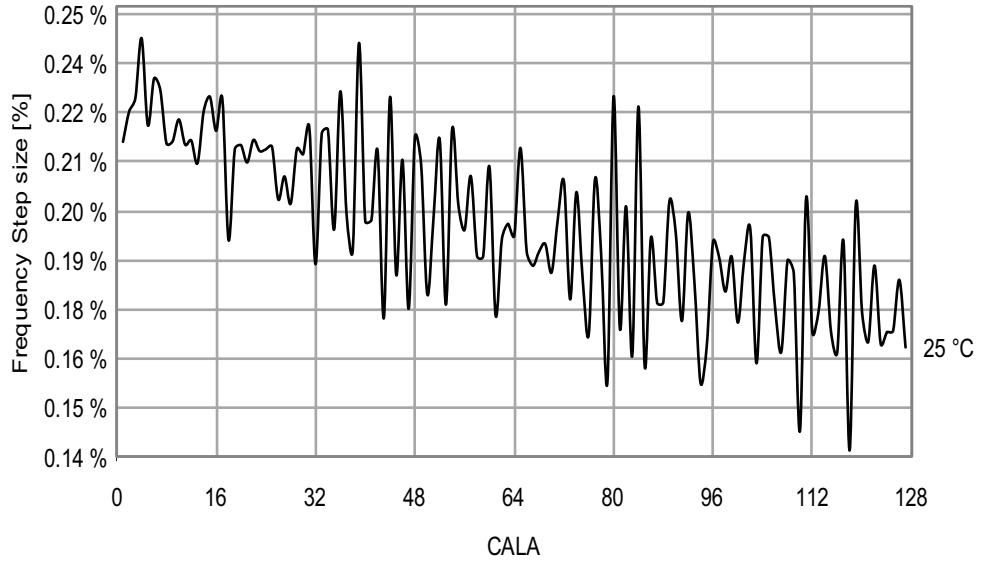


Figure 34-225. Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 32MHz internal oscillator prescaled to 8MHz

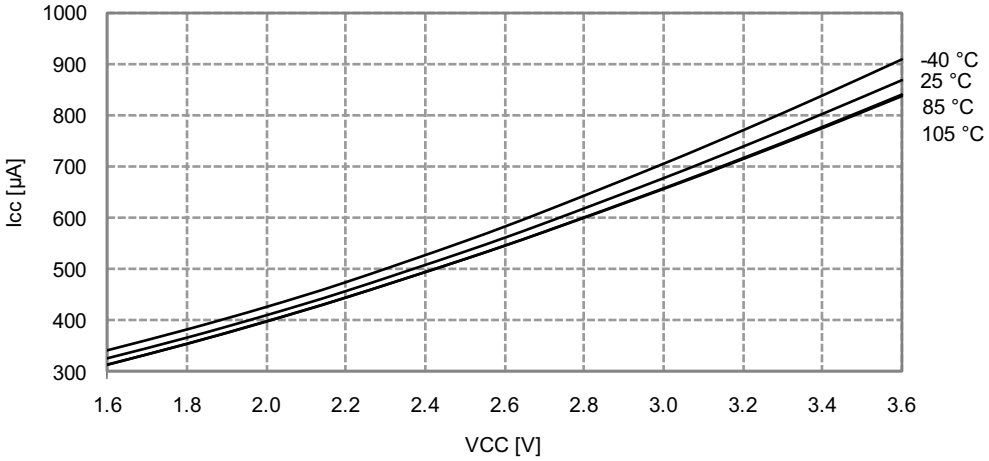


Figure 34-226. Idle Mode Current vs. V_{CC}

f_{SYS} = 32MHz internal oscillator

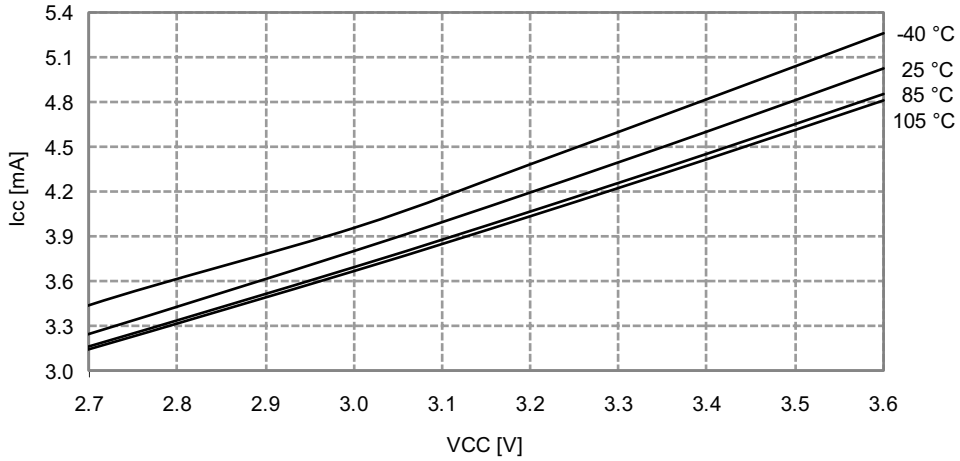


Figure 34-269. 2MHz Internal Oscillator Frequency vs. Temperature

DFLL enabled, from the 32.768kHz internal oscillator

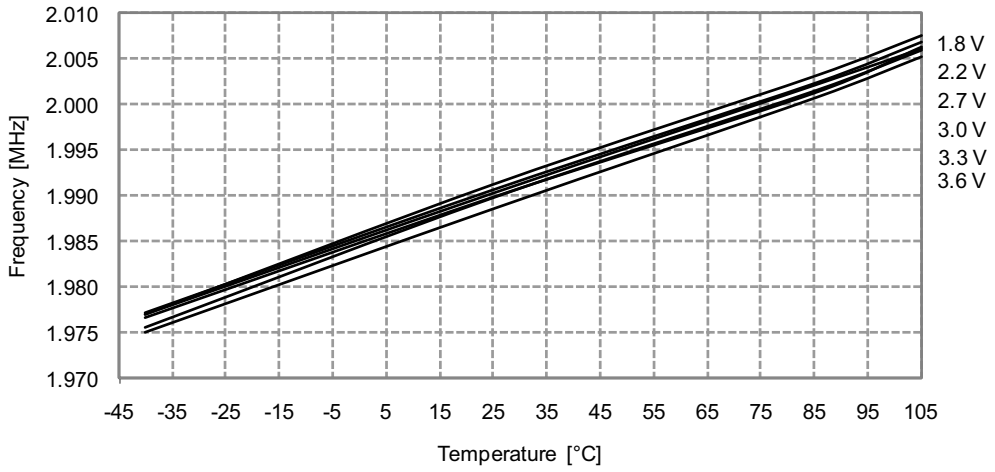


Figure 34-270. 2MHz Internal Oscillator Frequency vs. CALA Calibration Value

V_{CC} = 3V

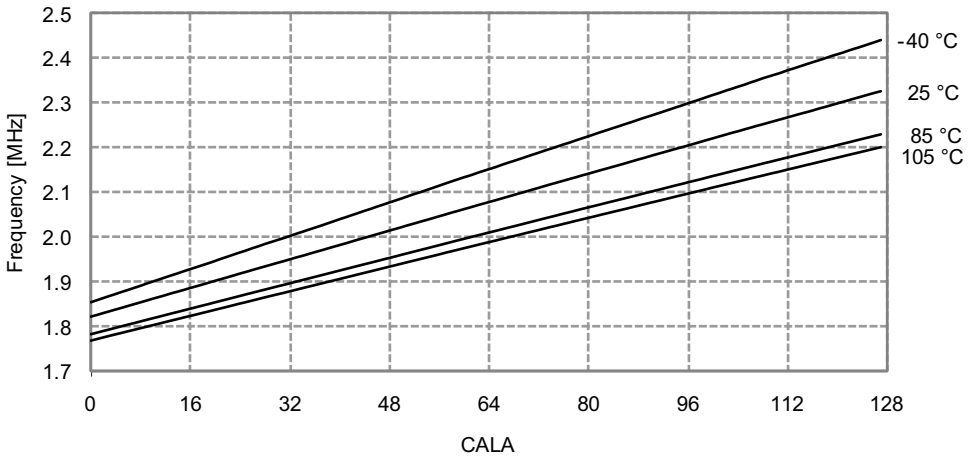


Figure 34-287. Active Mode Supply Current vs. V_{CC}

f_{SYS} = 2MHz internal oscillator

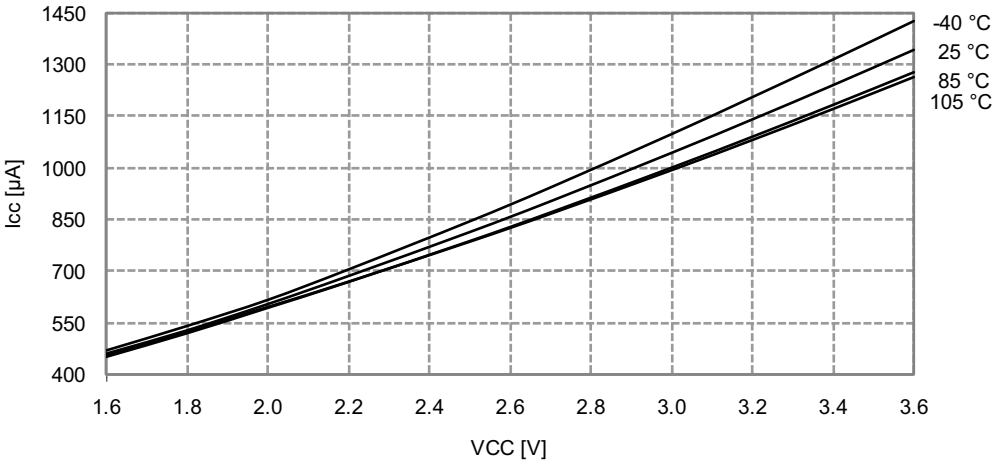


Figure 34-288. Active Mode Supply Current vs. V_{CC}

f_{SYS} = 32MHz internal oscillator prescaled to 8MHz

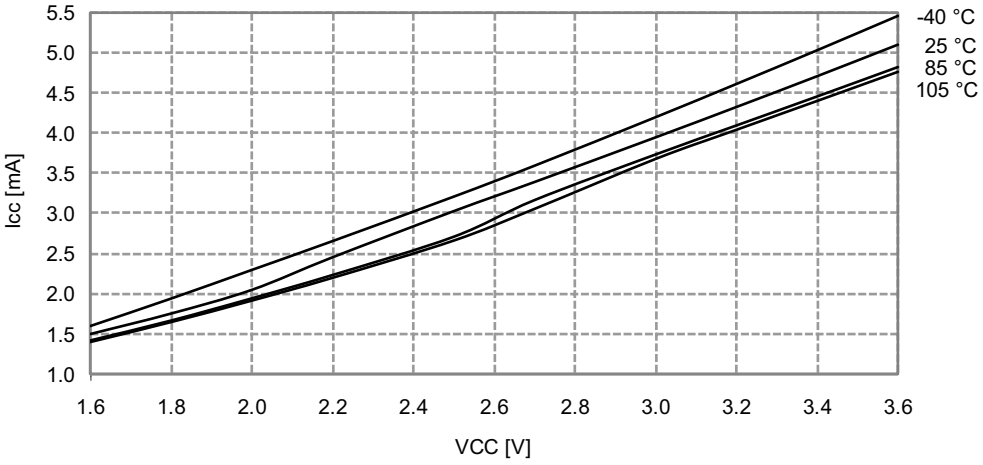


Figure 34-307. I/O Pin Output Voltage vs. Sink Current

V_{CC} = 3.0V

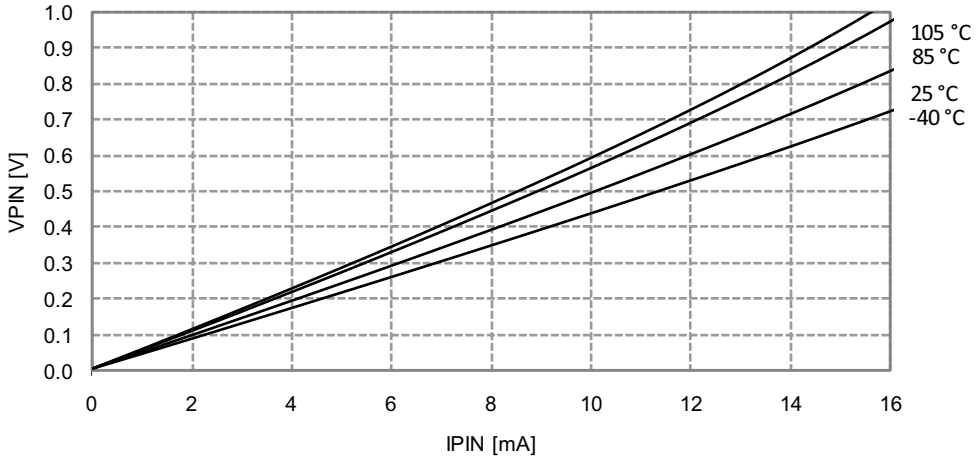


Figure 34-308. I/O Pin Output Voltage vs. Sink Current

V_{CC} = 3.3V