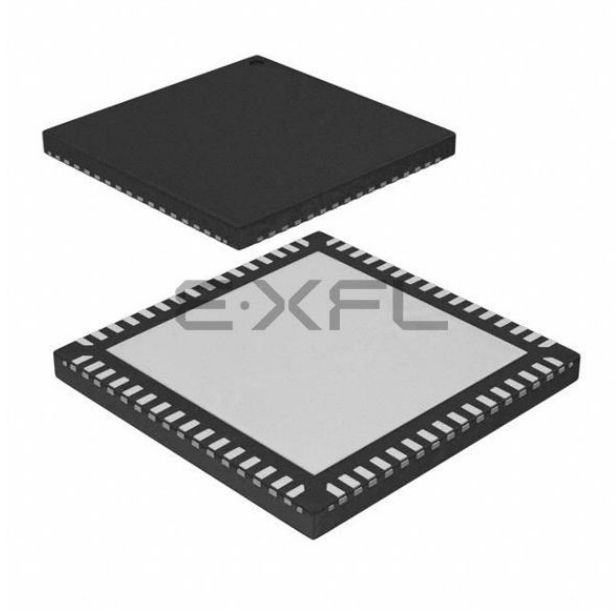

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	50
Program Memory Size	256KB (128K x 16)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega256c3-mh

Mnemonics	Operands	Description	Operation	Flags	#Clocks
RCALL	k	Relative Call Subroutine	PC ← PC + k + 1	None	2 / 3
ICALL		Indirect Call to (Z)	PC(15:0) ← Z, PC(21:16) ← 0	None	2 / 3
EICALL		Extended Indirect Call to (Z)	PC(15:0) ← Z, PC(21:16) ← EIND	None	3
CALL	k	call Subroutine	PC ← k	None	3 / 4
RET		Subroutine Return	PC ← STACK	None	4 / 5
RETI		Interrupt Return	PC ← STACK	I	4 / 5
CPSE	Rd,Rr	Compare, Skip if Equal	if (Rd = Rr) PC ← PC + 2 or 3	None	1 / 2 / 3
CP	Rd,Rr	Compare	Rd - Rr	Z,C,N,V,S,H	1
CPC	Rd,Rr	Compare with Carry	Rd - Rr - C	Z,C,N,V,S,H	1
CPI	Rd,K	Compare with Immediate	Rd - K	Z,C,N,V,S,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b) = 0) PC ← PC + 2 or 3	None	1 / 2 / 3
SBRS	Rr, b	Skip if Bit in Register Set	if (Rr(b) = 1) PC ← PC + 2 or 3	None	1 / 2 / 3
SBIC	A, b	Skip if Bit in I/O Register Cleared	if (I/O(A,b) = 0) PC ← PC + 2 or 3	None	2 / 3 / 4
SBIS	A, b	Skip if Bit in I/O Register Set	If (I/O(A,b) =1) PC ← PC + 2 or 3	None	2 / 3 / 4
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then PC ← PC + k + 1	None	1 / 2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then PC ← PC + k + 1	None	1 / 2
BREQ	k	Branch if Equal	if (Z = 1) then PC ← PC + k + 1	None	1 / 2
BRNE	k	Branch if Not Equal	if (Z = 0) then PC ← PC + k + 1	None	1 / 2
BRCS	k	Branch if Carry Set	if (C = 1) then PC ← PC + k + 1	None	1 / 2
BRCC	k	Branch if Carry Cleared	if (C = 0) then PC ← PC + k + 1	None	1 / 2
BRSH	k	Branch if Same or Higher	if (C = 0) then PC ← PC + k + 1	None	1 / 2
BRLO	k	Branch if Lower	if (C = 1) then PC ← PC + k + 1	None	1 / 2
BRMI	k	Branch if Minus	if (N = 1) then PC ← PC + k + 1	None	1 / 2
BRPL	k	Branch if Plus	if (N = 0) then PC ← PC + k + 1	None	1 / 2
BRGE	k	Branch if Greater or Equal, Signed	if (N ⊕ V= 0) then PC ← PC + k + 1	None	1 / 2
BRLT	k	Branch if Less Than, Signed	if (N ⊕ V= 1) then PC ← PC + k + 1	None	1 / 2
BRHS	k	Branch if Half Carry Flag Set	if (H = 1) then PC ← PC + k + 1	None	1 / 2
BRHC	k	Branch if Half Carry Flag Cleared	if (H = 0) then PC ← PC + k + 1	None	1 / 2
BRTS	k	Branch if T Flag Set	if (T = 1) then PC ← PC + k + 1	None	1 / 2
BRTC	k	Branch if T Flag Cleared	if (T = 0) then PC ← PC + k + 1	None	1 / 2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then PC ← PC + k + 1	None	1 / 2
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then PC ← PC + k + 1	None	1 / 2
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then PC ← PC + k + 1	None	1 / 2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then PC ← PC + k + 1	None	1 / 2
Data transfer instructions					
MOV	Rd, Rr	Copy Register	Rd ← Rr	None	1

33.2.11 Power-on Reset Characteristics

Table 33-45. Power-on Reset Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{POT-} (1)	POR threshold voltage falling V_{CC}	V_{CC} falls faster than 1V/ms	0.4	1.0		V
		V_{CC} falls at 1V/ms or slower	0.8	1.3		
V_{POT+}	POR threshold voltage rising V_{CC}			1.3	1.59	

Note: 1. V_{POT-} values are only valid when BOD is disabled. When BOD is enabled $V_{POT-} = V_{POT+}$.

33.2.12 Flash and EEPROM Memory Characteristics

Table 33-46. Endurance and Data Retention

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Flash	Write/Erase cycles	25°C	10K			Cycle
			85°C	10K			
			105°C	2K			
		Data retention	25°C	100			Year
			85°C	25			
			105°C	10			
	EEPROM	Write/Erase cycles	25°C	100K			Cycle
			85°C	100K			
			105°C	30K			
		Data retention	25°C	100			Year
			85°C	25			
			105°C	10			

Table 33-47. Programming Time

Symbol	Parameter	Condition	Min.	Typ.(1)	Max.	Units
	Chip erase(2)	64KB Flash, EEPROM		55		ms
	Application erase	Section erase		6		
	Flash	Page erase		4		
		Page write		4		
		Atomic page erase and write		8		
	EEPROM	Page erase		4		
		Page write		4		
		Atomic page erase and write		8		

Notes: 1. Programming is timed from the 2MHz internal oscillator.
2. EEPROM is not erased if the EESAVE fuse is programmed.

The maximum CPU clock frequency depends on V_{CC}. As shown in Figure 33-15 the Frequency vs. V_{CC} curve is linear between 1.8V < V_{CC} < 2.7V.

Figure 33-15.Maximum Frequency vs. V_{CC}

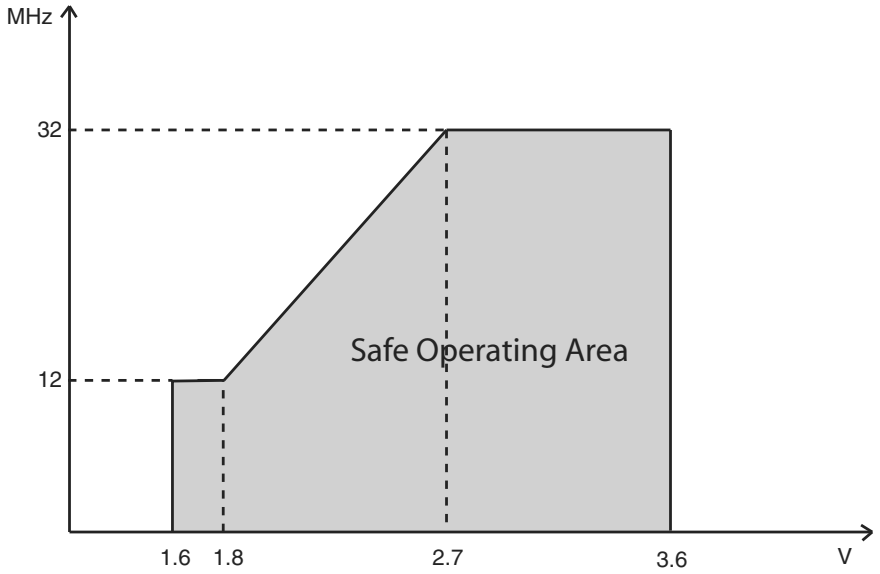


Table 33-63. Current Consumption for Modules and Peripherals

Symbol	Parameter	Condition [1]		Min.	Typ.	Max.	Units
I_{CC}	ULP oscillator				0.9		µA
	32.768kHz int. oscillator				26		
	2MHz int. oscillator				79		
		DFLL enabled with 32.768kHz int. osc. as reference			110		
	32MHz int. oscillator				245		
		DFLL enabled with 32.768kHz int. osc. as reference			415		
	PLL	20x multiplication factor, 32MHz int. osc. DIV4 as reference			305		
	Watchdog timer				1.0		
	BOD	Continuous mode			138		
		Sampled mode, includes ULP oscillator			1.4		
	Internal 1.0V reference				185		
	Temperature sensor				173		
	ADC	16ksps V_{REF} = Ext. ref.			1.3		mA
			CURRLIMIT = LOW		1.15		
			CURRLIMIT = MEDIUM		1.0		
			CURRLIMIT = HIGH		0.9		
		75ksps V_{REF} = Ext. ref.	CURRLIMIT = LOW		1.7		
		300ksps V_{REF} = Ext. ref.			3.1		
	USART	Rx and Tx enabled, 9600 BAUD			7.5		µA
	Flash memory and EEPROM programming				4		mA

Note: 1. All parameters measured as the difference in current consumption between module enabled and disabled. All data at V_{CC} = 3.0V, Clk_{SYS} = 1MHz external clock without prescaling, T = 25°C unless other conditions are given.

33.3.8 Bandgap and Internal 1.0V Reference Characteristics

Table 33-71. Bandgap and Internal 1.0V Reference Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Startup time	As reference for ADC		1 Clk_{PER} + 2.5µs		µs
		As input voltage to ADC and AC		1.5		
	Bandgap voltage			1.1		V
INT1V	Internal 1.00V reference	T= 85°C, after calibration	0.99	1.0	1.01	
	Variation over voltage and temperature	Calibrated at T= 85°C		1		%

33.3.9 Brownout Detection Characteristics

Table 33-72. Brownout Detection Characteristics(1)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{BOT}	BOD level 0 falling V_{CC}		1.40	1.60	1.70	V
	BOD level 1 falling V_{CC}			1.8		
	BOD level 2 falling V_{CC}			2.0		
	BOD level 3 falling V_{CC}			2.2		
	BOD level 4 falling V_{CC}			2.4		
	BOD level 5 falling V_{CC}			2.6		
	BOD level 6 falling V_{CC}			2.8		
	BOD level 7 falling V_{CC}			3.0		
t_{BOD}	Detection time	Continuous mode		0.4		µs
		Sampled mode		1000		
V_{HYST}	Hysteresis			1.0		%

Note: 1. BOD is calibrated at 85°C within BOD level 0 values, and BOD level 0 is the default level.

33.3.10 External Reset Characteristics

Table 33-73. External Reset Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_{EXT}	Minimum reset pulse width		1000	100		ns
V_{RST}	Reset threshold voltage	V_{CC} = 2.7 - 3.6V		0.45*V_{CC}		V
		V_{CC} = 1.6 - 2.7V		0.45*V_{CC}		
R_{RST}	Reset pin Pull-up Resistor			27		kΩ

33.4.3 Current Consumption

Table 33-91. Current Consumption for Active Mode and Sleep Mode

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{CC}	Active power consumption(1)	32kHz, Ext. Clk	V_{CC} = 1.8V		60		µA
			V_{CC} = 3.0V		140		
		1MHz, Ext. Clk	V_{CC} = 1.8V		245		
			V_{CC} = 3.0V		550		
		2MHz, Ext. Clk	V_{CC} = 1.8V		440	700	
			V_{CC} = 3.0V		0.9	1.5	mA
		32MHz, Ext. Clk			9.0	15	
	Idle power consumption(2)	32kHz, Ext. Clk	V_{CC} = 1.8V		3.0		µA
			V_{CC} = 3.0V		3.5		
		1MHz, Ext. Clk	V_{CC} = 1.8V		55		
			V_{CC} = 3.0V		110		
		2MHz, Ext. Clk	V_{CC} = 1.8V		105	350	
			V_{CC} = 3.0V		215	650	
		32MHz, Ext. Clk			3.4	8.0	mA
	Power-down power consumption	T = 25°C	V_{CC} = 3.0V		0.1	1.0	µA
		T = 85°C			3.5	6.0	
		T = 105°C			10.0	15	
		WDT and sampled BOD enabled, T = 25°C	V_{CC} = 3.0V		1.5	2.0	
		WDT and sampled BOD enabled, T = 85°C			5.8	10	
		WDT and sampled BOD enabled, T = 105°C			12	20	
	Power-save power consumption(3)	RTC from ULP clock, WDT and sampled BOD enabled, T = 25°C	V_{CC} = 1.8V		1.3		
			V_{CC} = 3.0V		1.4		
		RTC from 1.024kHz low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.7	2.0	
			V_{CC} = 3.0V		0.8	2.0	
		RTC from low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.9	3.0	
			V_{CC} = 3.0V		1.1	3.0	
	Reset power consumption	Current through $\overline{\text{RESET}}$ pin substracted	V_{CC} = 3.0V		170		

Notes:
1. All Power Reduction Registers set including FPRM and EPRM.
2. All Power Reduction Registers set without FPRM and EPRM.
3. Maximum limits are based on characterization, and not tested in production.

33.5.5 I/O Pin Characteristics

The I/O pins complies with the JEDEC LVTTL and LVCMOS specification and the high- and low-level input and output voltage limits reflect or exceed this specification.

Table 33-123. I/O Pin Characteristics

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{OH} (1)/ I_{OL} (2)	I/O pin source/sink current			-15		15	mA
V_{IH}	High level input voltage	V_{CC} = 2.4 - 3.6V		0.7*Vcc		V_{CC}+0.5	V
		V_{CC} = 1.6 - 2.4V		0.8*V_{CC}		V_{CC}+0.5	
V_{IL}	Low level input voltage	V_{CC} = 2.4 - 3.6V		-0.5		0.3*V_{CC}	
		V_{CC} = 1.6 - 2.4V		-0.5		0.2*V_{CC}	
V_{OH}	High level output voltage	V_{CC} = 3.3V	I_{OH} = -4mA	2.6	2.9		
		V_{CC} = 3.0V	I_{OH} = -3mA	2.1	2.6		
		V_{CC} = 1.8V	I_{OH} = -1mA	1.4	1.6		
V_{OL}	Low level output voltage	V_{CC} = 3.3V	I_{OL} = 8mA		0.4	0.76	
		V_{CC} = 3.0V	I_{OL} = 5mA		0.3	0.64	
		V_{CC} = 1.8V	I_{OL} = 3mA		0.2	0.46	
I_{IN}	Input leakage current I/O pin	T = 25°C			<0.01	1.0	µA
R_P	Pull/Bus keeper resistor				25		kΩ

Notes:
1. The sum of all I_{OH} for PORTA and PORTB must not exceed 100mA.
   The sum of all I_{OH} for PORTC, PORTD, and PORTE must for each port not exceed 200mA.
   The sum of all I_{OH} for pins PF[0-5] on PORTF must not exceed 200mA.
   The sum of all I_{OL} for pins PF[6-7] on PORTF, PORTR, and PDI must not exceed 100mA.
2. The sum of all I_{OL} for PORTA and PORTB must not exceed 100mA.
   The sum of all I_{OL} for PORTC, PORTD, and PORTE must for each port not exceed 200mA.
   The sum of all I_{OL} for pins PF[0-5] on PORTF must not exceed 200mA.
   The sum of all I_{OL} for pins PF[6-7] on PORTF, PORTR, and PDI must not exceed 100mA.

Table 33-145.Two-wire Interface Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input high voltage		0.7*V_{CC}		V_{CC}+0.5	V
V_{IL}	Input low voltage		-0.5		0.3*V_{CC}	
V_{hys}	Hysteresis of Schmitt trigger inputs		0.05V_{CC} (1)			
V_{OL}	Output low voltage	3mA, sink current	0		0.4	
t_r	Rise time for both SDA and SCL		20+0.1C_b (1)(2)		300	ns
t_{of}	Output fall time from V_{IHmin} to V_{ILmax}	10pF < C_b < 400pF (2)	20+0.1C_b (1)(2)		250	
t_{SP}	Spikes suppressed by input filter		0		50	
I_I	Input current for each I/O Pin	0.1V_{CC} < V_I < 0.9V_{CC}	-10		10	µA
C_I	Capacitance for each I/O Pin				10	pF
f_{SCL}	SCL clock frequency	f_{PER} (3) >max(10f_{SCL}, 250kHz)	0		400	kHz
R_P	Value of pull-up resistor	f_{SCL} ≤ 100kHz	$\frac{V_{CC}-0.4V}{3mA}$		$\frac{100ns}{C_b}$	Ω
		f_{SCL} > 100kHz			$\frac{300ns}{C_b}$	
$t_{HD;STA}$	Hold time (repeated) START condition	f_{SCL} ≤ 100kHz	4.0			µs
		f_{SCL} > 100kHz	0.6			
t_{LOW}	Low period of SCL clock	f_{SCL} ≤ 100kHz	4.7			
		f_{SCL} > 100kHz	1.3			
t_{HIGH}	High period of SCL clock	f_{SCL} ≤ 100kHz	4.0			
		f_{SCL} > 100kHz	0.6			
$t_{SU;STA}$	Setup time for a repeated START condition	f_{SCL} ≤ 100kHz	4.7			
		f_{SCL} > 100kHz	0.6			
$t_{HD;DAT}$	Data hold time	f_{SCL} ≤ 100kHz	0		3.45	
		f_{SCL} > 100kHz	0		0.9	
$t_{SU;DAT}$	Data setup time	f_{SCL} ≤ 100kHz	250			ns
		f_{SCL} > 100kHz	100			
$t_{SU;STO}$	Setup time for STOP condition	f_{SCL} ≤ 100kHz	4.0			µs
		f_{SCL} > 100kHz	0.6			
t_{BUF}	Bus free time between a STOP and START condition	f_{SCL} ≤ 100kHz	4.7			
		f_{SCL} > 100kHz	1.3			

Notes:
1. Required only for f_{SCL} > 100kHz.
2. C_b = Capacitance of one bus line in pF.
3. f_{PER} = Peripheral clock frequency.

Figure 34-3. Active Mode Supply Current vs. V_{CC}

f_{SYS} = 32.768kHz internal oscillator

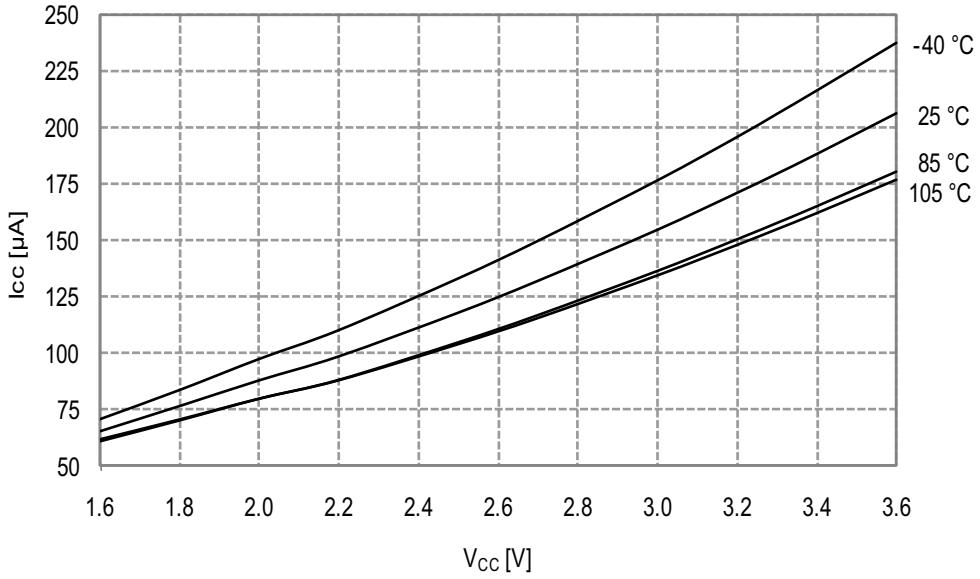


Figure 34-4. Active Mode Supply Current vs. V_{CC}

f_{SYS} = 1MHz external clock

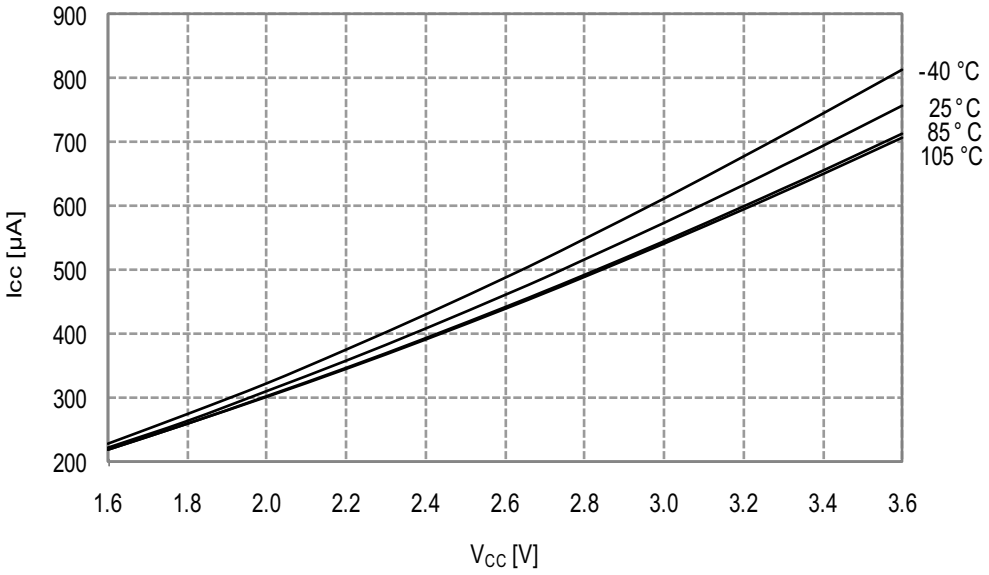


Figure 34-11. Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 1MHz external clock

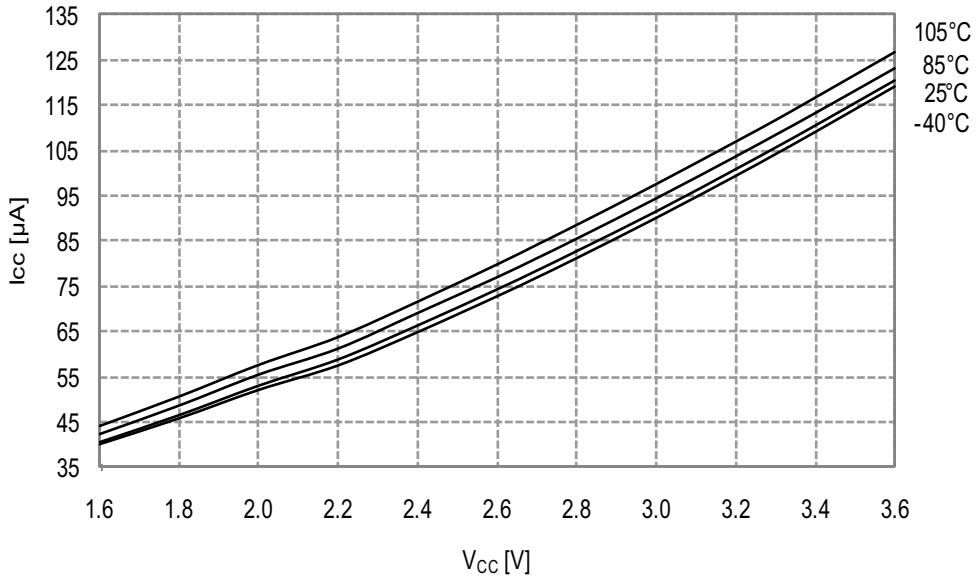


Figure 34-12. Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 2MHz internal oscillator

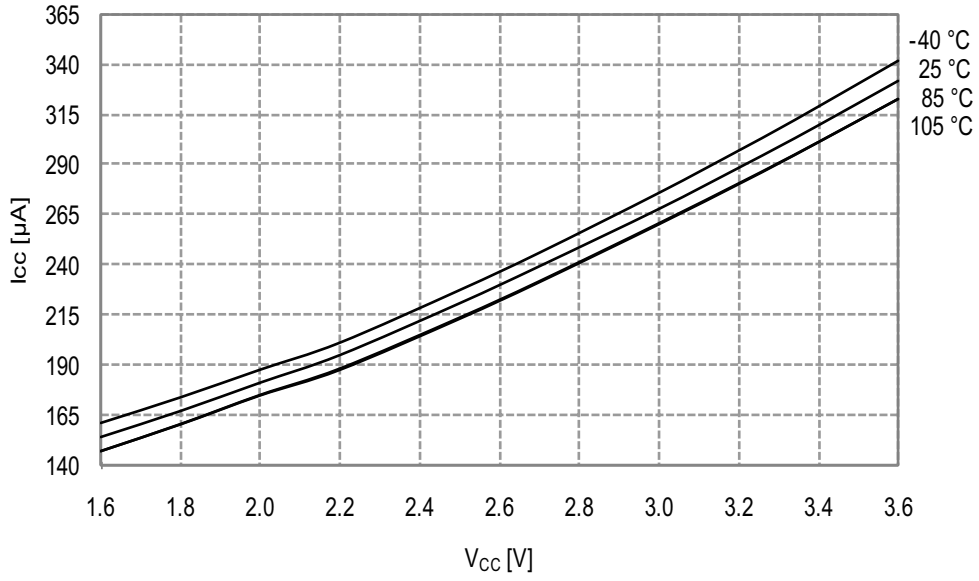


Figure 34-39. Offset Error vs. V_{REF}

T = 25°C, V_{CC} = 3.6V, ADC sample rate = 300ksps

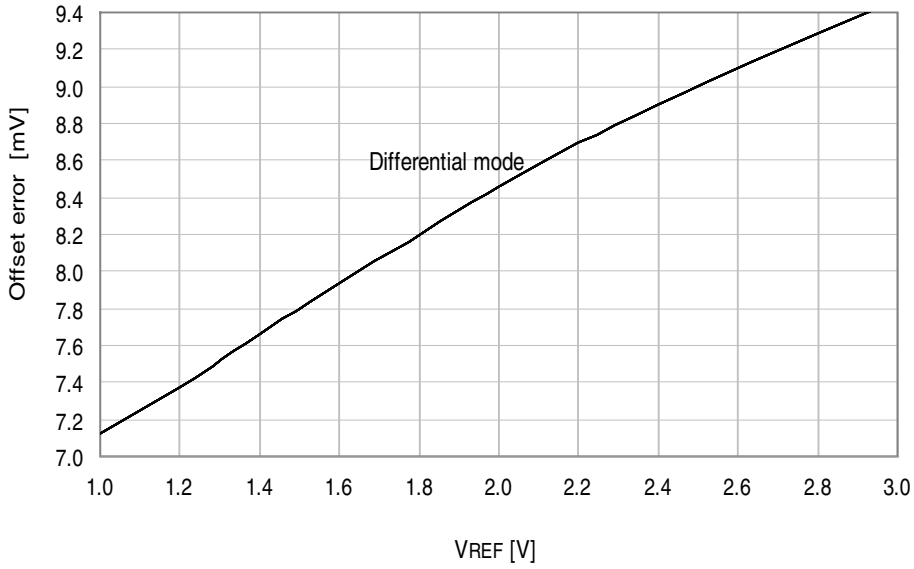


Figure 34-40. Gain Error vs. Temperature

V_{CC} = 3.0V, V_{REF} = external 2.0V

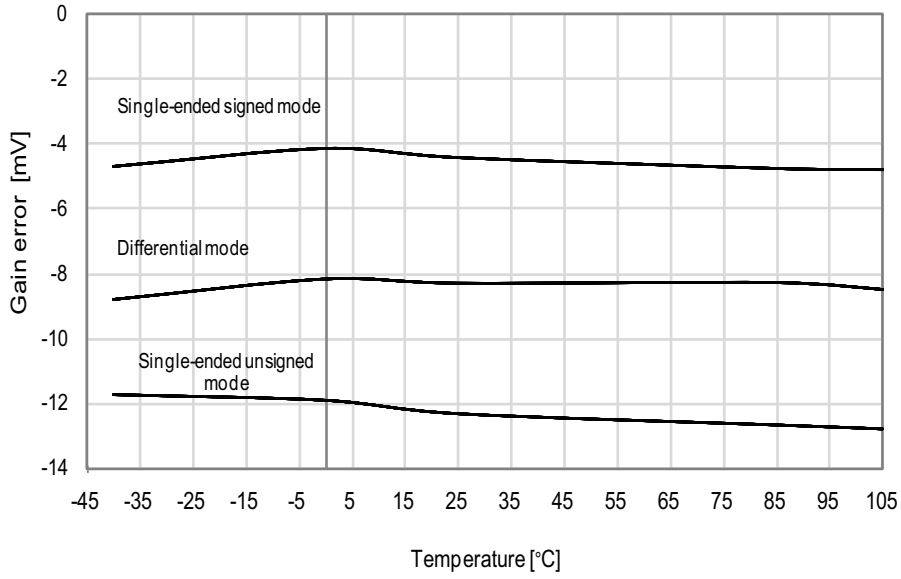


Figure 34-94. I/O Pin Output Voltage vs. Source Current

V_{CC} = 3.0V

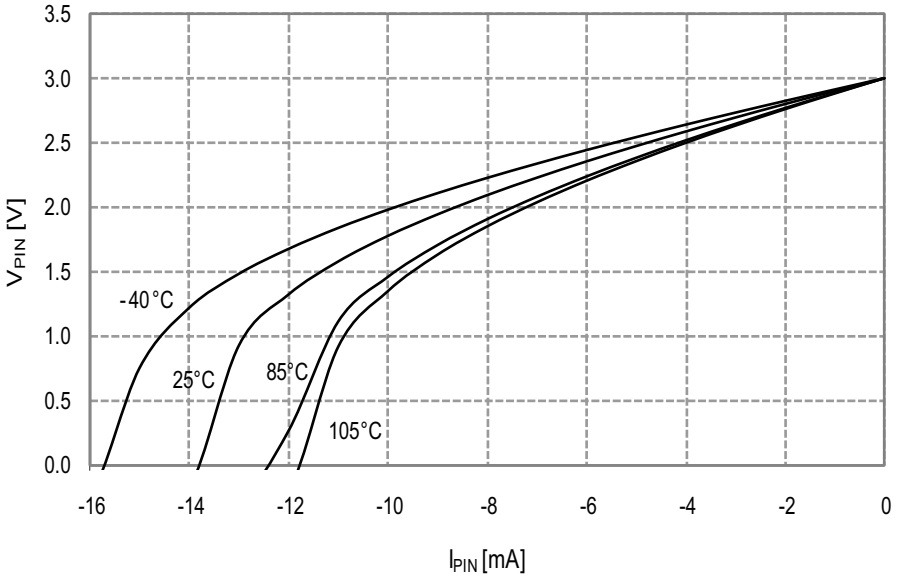


Figure 34-95. I/O Pin Output Voltage vs. Source Current

V_{CC} = 3.3V

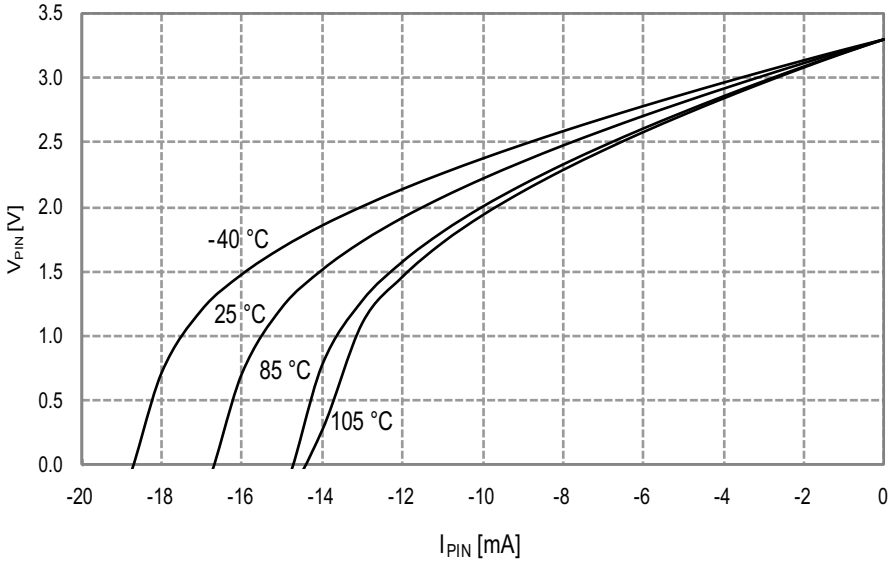


Figure 34-108. Gain Error vs. V_{REF}

T = 25°C, V_{CC} = 3.6V, ADC sample rate = 300ksps

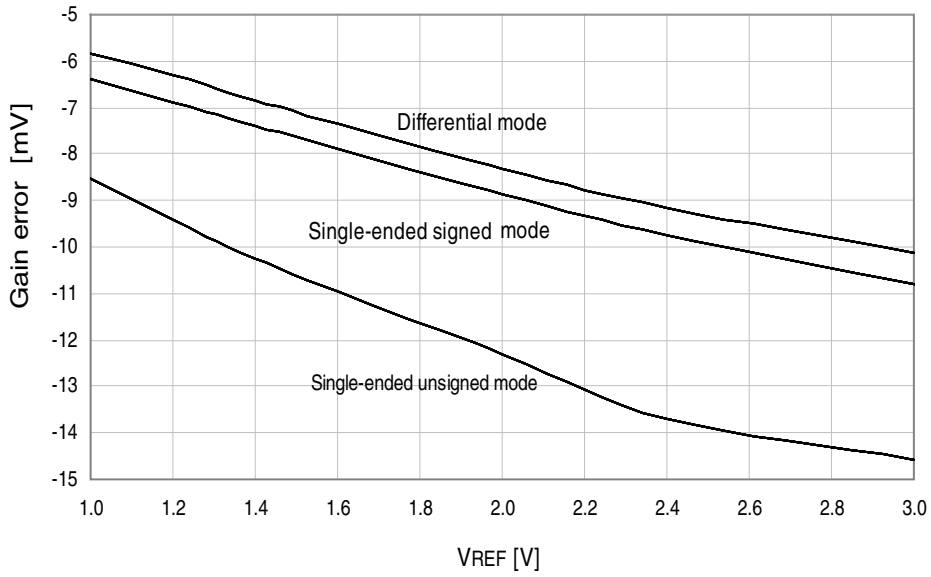


Figure 34-109. Gain Error vs. V_{CC}

T = 25°C, V_{REF} = external 1.0V, ADC sample rate = 300ksps

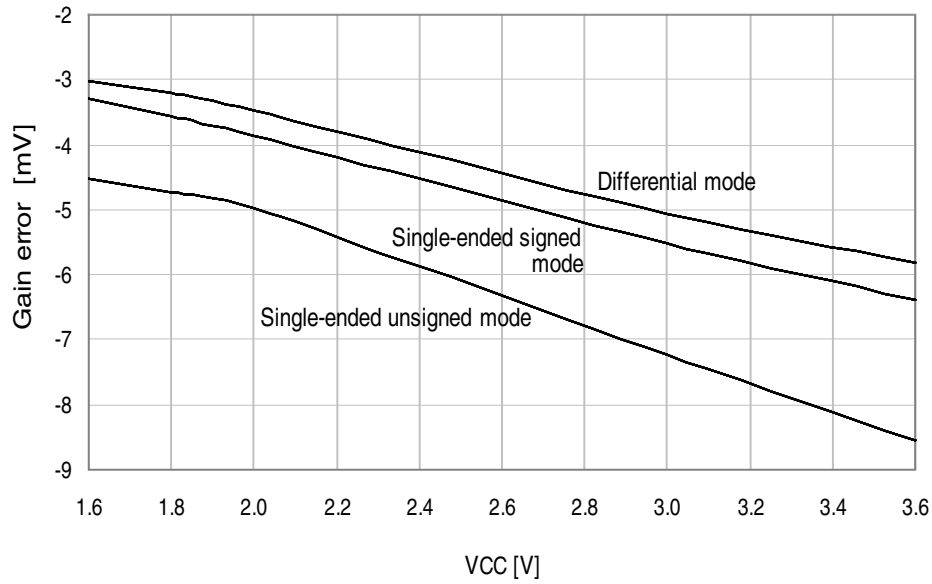


Figure 34-136. 32MHz Internal Oscillator CALA Calibration Step Size

T = 105°C, V_{CC}=3.0V

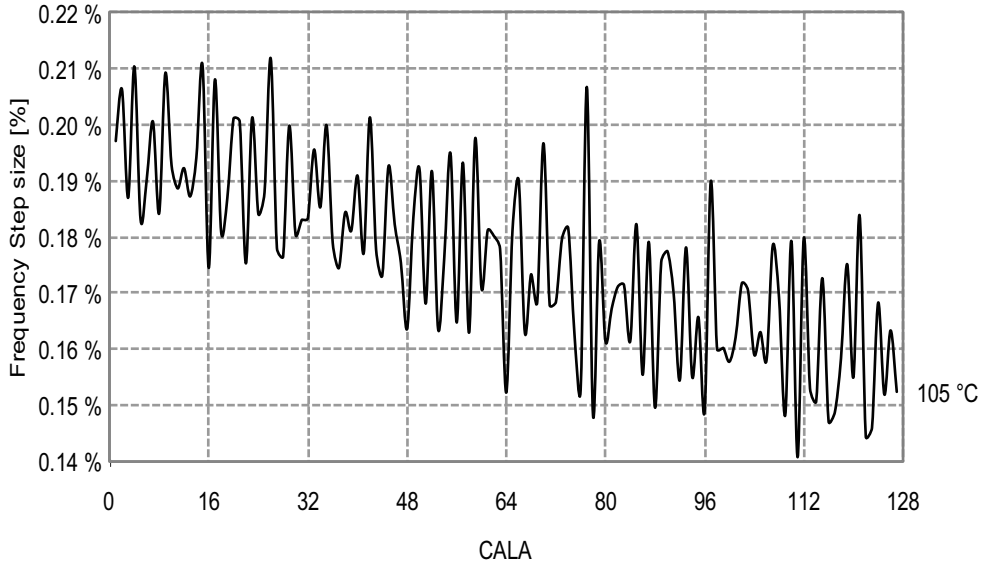


Figure 34-137. 32MHz Internal Oscillator Frequency vs. CALB Calibration Value

V_{CC} = 3.0V

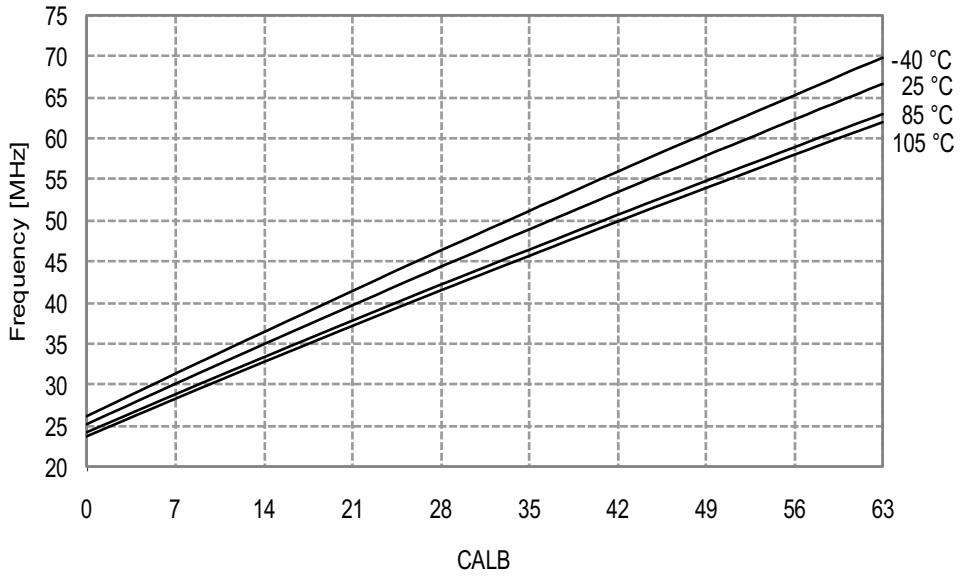


Figure 34-167. I/O Pin Output Voltage vs. Sink Current

V_{CC} = 3.0V

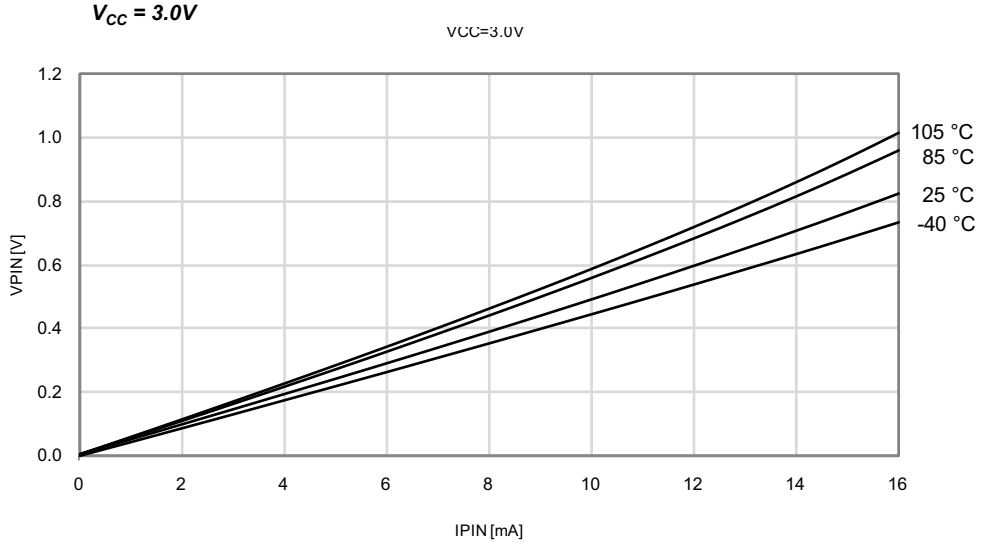
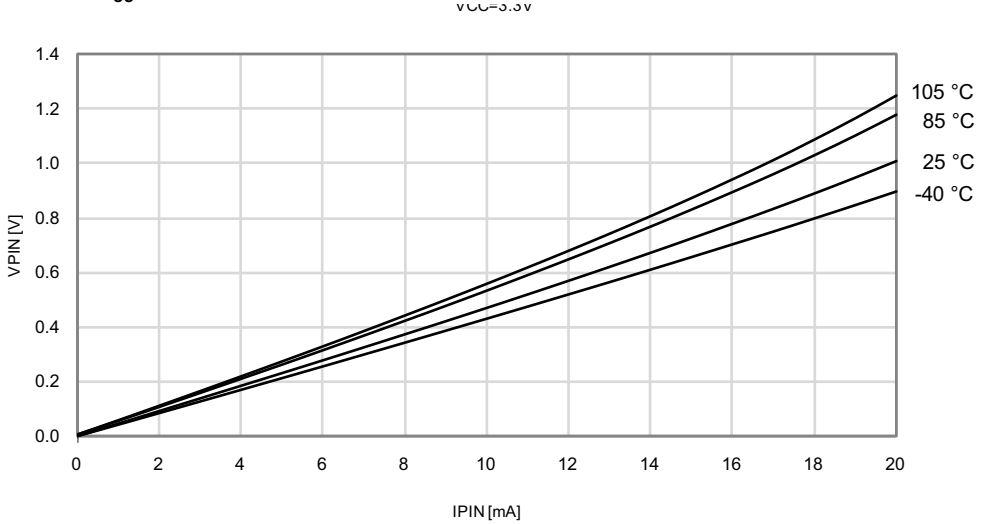


Figure 34-168. I/O Pin Output Voltage vs. Sink Current

V_{CC} = 3.3V



34.3.4 Analog Comparator Characteristics

Figure 34-183. Analog Comparator Hysteresis vs. V_{CC}

Small hysteresis

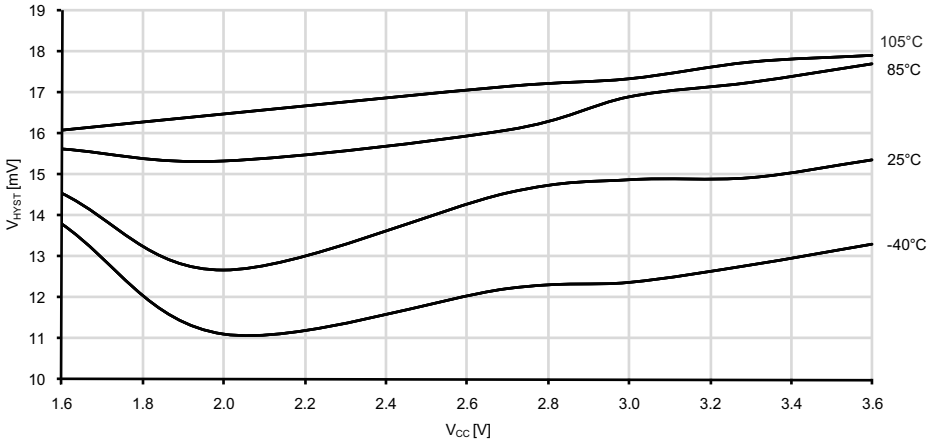


Figure 34-184. Analog Comparator Hysteresis vs. V_{CC}

Large hysteresis

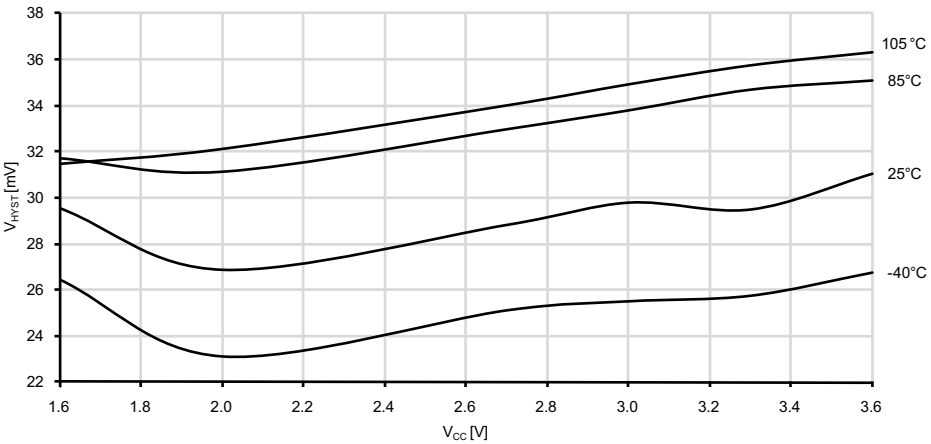


Figure 34-319. Gain Error vs. V_{CC}

T = 25°C, V_{REF} = external 1.0V, ADC sample rate = 300ksps

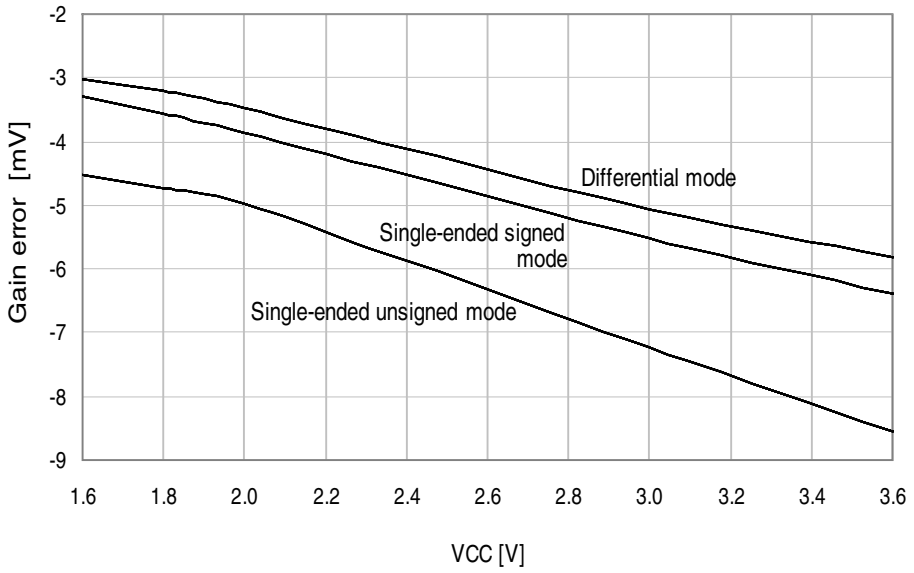


Figure 34-320. Offset Error vs. V_{REF}

T = 25°C, V_{CC} = 3.6V, ADC sample rate = 300ksps

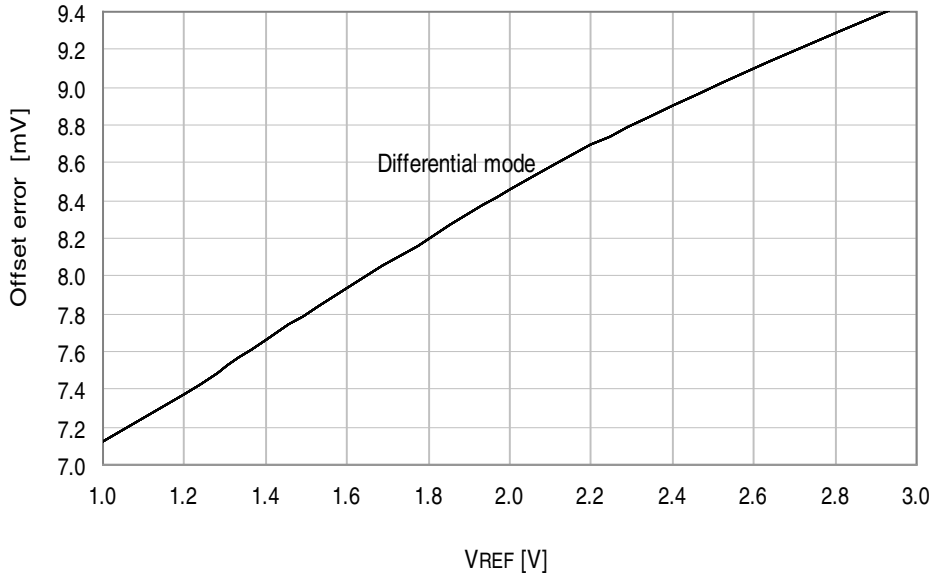
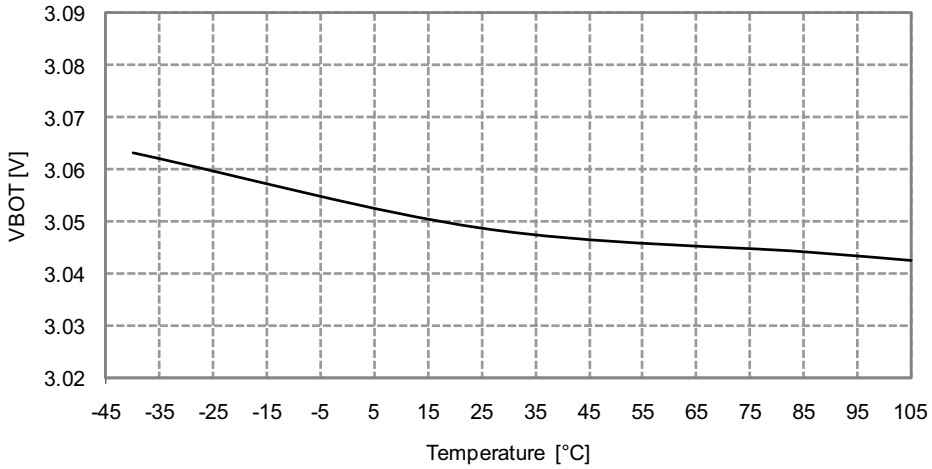


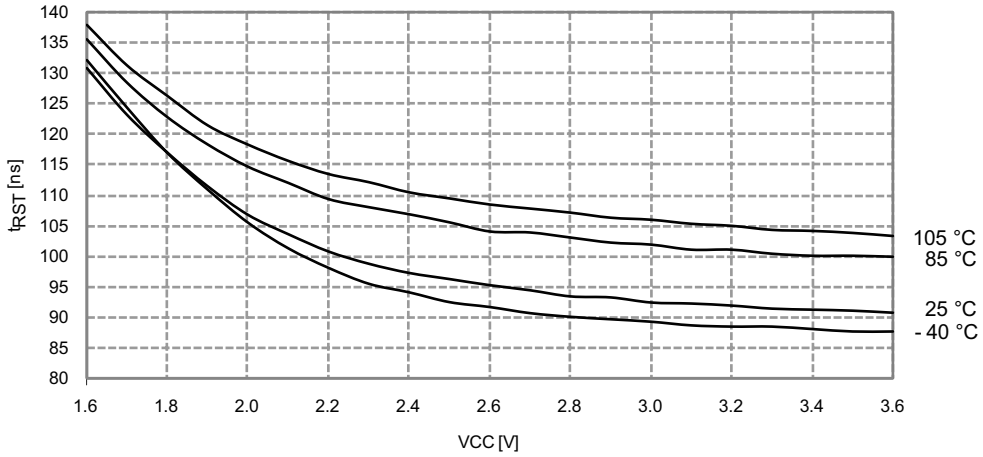
Figure 34-329. BOD Thresholds vs. Temperature

BOD level = 3.0V



34.5.7 External Reset Characteristics

Figure 34-330. Minimum Reset Pin Pulse Width vs. V_{CC}



34.5.8.4 32MHz Internal Oscillator

Figure 34-341. 32MHz Internal Oscillator Frequency vs. Temperature

DFLL disabled

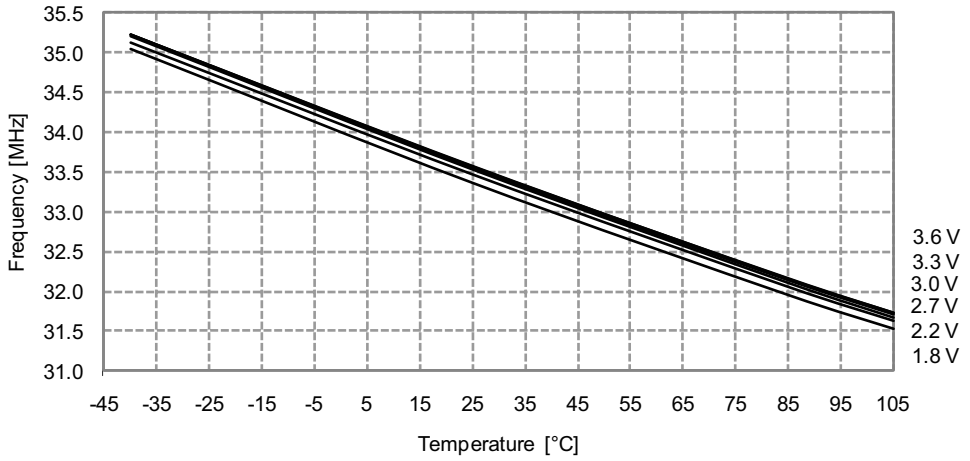
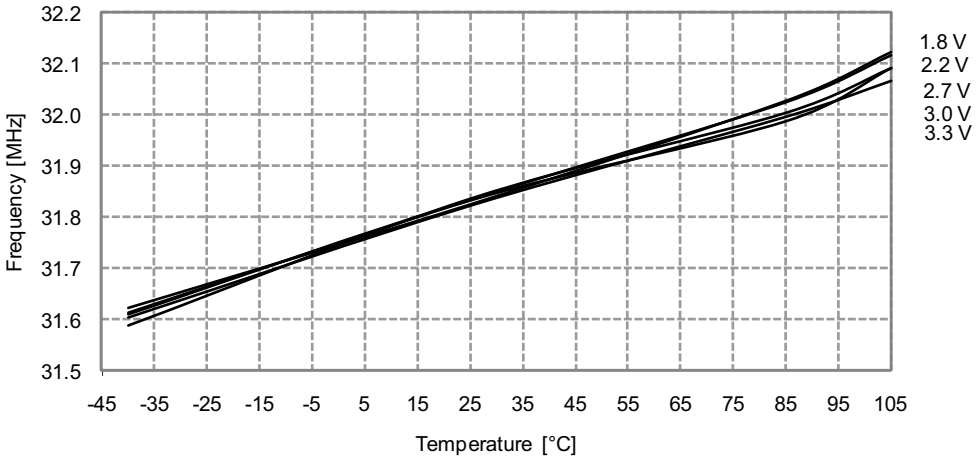


Figure 34-342. 32MHz Internal Oscillator Frequency vs. Temperature

DFLL enabled, from the 32.768kHz internal oscillator



36.3 8492E – 05/2013

1.	ATxmega32C3 and ATxmega128C3 changed status from preliminary to complete.
2.	Updated “Ordering Information” on page 2. Removed PA and PJ package references. Added 64M package reference.
3.	Updated “Packaging Information” on page 63. Removed the packaging 64PA and 64PJ. Added the packaging 64M.
4.	Updated “Errata” on page 337. Added “Rev A - H: not sampled” for ATxmega32C3, ATxmega64C3, ATxmega192C3 and ATxmega256C3. Added “Rev A - I: not sampled” for ATxmega128C3 and added rev J to ATxmega128C3.

36.4 8492D – 02/2013

1.	Added ATxmega32C3 device.
2.	Added ATxmega32C3 “Ordering Information” on page 2.
3.	Updated Figure 2-1 on page 4. Pin 15 and pin 25 are VCC and not VDD.
4.	Updated Figure 7-1 on page 13, ATxmega32C3 “Flash Program Memory (hexadecimal address)” .
5.	Updated Figure 7-2 on page 15, ATxmega32C3 “Data Memory Map (hexadecimal address)” .
6.	Updated Table 7-1 on page 14, ATxmega32C3 “Device ID Bytes” .
7.	Updated Table 7-2 on page 16 and Table 7-3 on page 17.
8.	Updated I/O Ports’ “Features” on page 29 and “Overview” on page 29. Removed “Optional slew rate control” as this option is not present on XMEGA C devices.
9.	Updated Figure 27-1 on page 49, “Analog Comparator Overview” .
10.	Added “Electrical Characteristics” for “Atmel ATxmega32C3” on page 65.
12.	Added “Electrical Characteristics” for “Atmel ATxmega128C3” on page 103.
11.	Added “Typical Characteristics” for “Atmel ATxmega32C3” on page 160.
13.	Added “Typical Characteristics” for “Atmel ATxmega128C3” on page 232.
14.	Updated “Errata” on page 337. Added Errata on all rev I: AC system status flags are only valid if AC-system is enabled.

36.5 8492C – 07/2012

1.	Added “Electrical Characteristics” for “Atmel ATxmega64C3” on page 84.
2.	Removed DMA from all “Electrical Characteristics” .
3.	“Accuracy” added to: Table 33-51 on page 95; Table 33-80 on page 114; Table 33-109 on page 133 and Table 33-138 on page 152.
4.	Added “Typical Characteristics” for “Atmel ATxmega64C3” on page 196.
5.	Updated the whole datasheet using the Atmel new datasheet template.

36.6 8492B – 03/2012

1.	Updated “Electrical Characteristics” on page 65.
2.	Added “Typical Characteristics” on page 160.