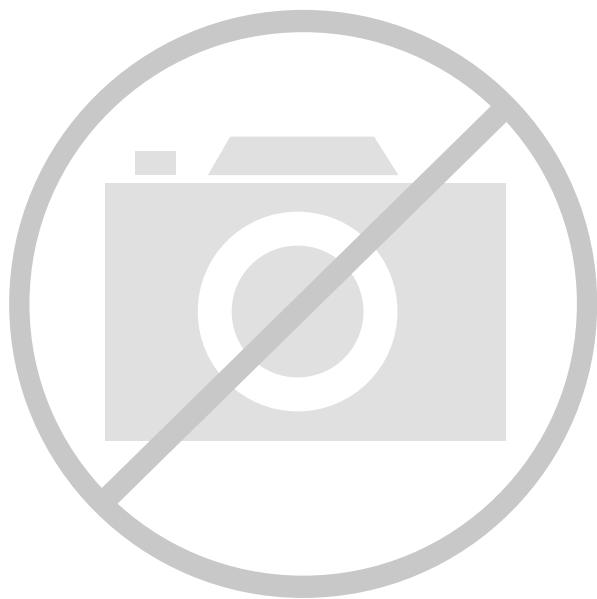




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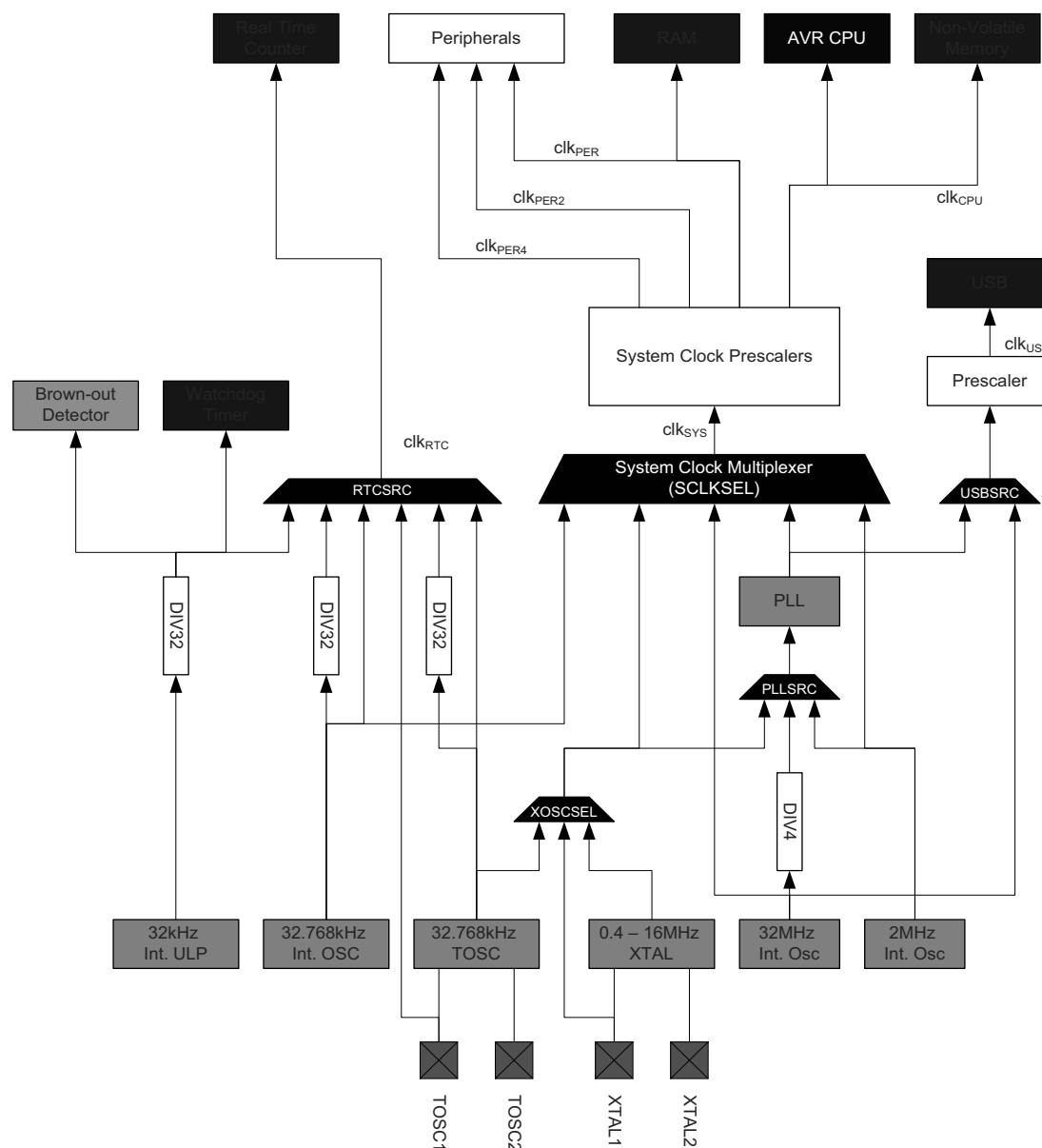
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I ² C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	50
Program Memory Size	256KB (128K x 16)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega256c3-mn

Figure 9-1. The Clock System, Clock Sources, and Clock Distribution



9.3 Clock Sources

The clock sources are divided in two main groups: internal oscillators and external clock sources. Most of the clock sources can be directly enabled and disabled from software, while others are automatically enabled or disabled, depending on peripheral settings. After reset, the device starts up running from the 2MHz internal oscillator. The other clock sources, DFLLs, and PLL, are turned off by default.

The internal oscillators do not require any external components to run. For details on characteristics and accuracy of the internal oscillators, refer to the device datasheet.

9.3.1 32kHz Ultra Low Power Internal Oscillator

This oscillator provides an approximate 32kHz clock. The 32kHz ultra low power (ULP) internal oscillator is a very low power clock source, and it is not designed for high accuracy. The oscillator employs a built-in prescaler that provides a

10. Power Management and Sleep Modes

10.1 Features

- Power management for adjusting power consumption and functions
- Five sleep modes
 - Idle
 - Power down
 - Power save
 - Standby
 - Extended standby
- Power reduction register to disable clock and turn off unused peripherals in active and idle modes

10.2 Overview

Various sleep modes and clock gating are provided in order to tailor power consumption to application requirements. This enables the Atmel AVR XMEGA microcontroller to stop unused modules to save power.

All sleep modes are available and can be entered from active mode. In active mode, the CPU is executing application code. When the device enters sleep mode, program execution is stopped and interrupts or a reset is used to wake the device again. The application code decides which sleep mode to enter and when. Interrupts from enabled peripherals and all enabled reset sources can restore the microcontroller from sleep to active mode.

In addition, power reduction registers provide a method to stop the clock to individual peripherals from software. When this is done, the current state of the peripheral is frozen, and there is no power consumption from that peripheral. This reduces the power consumption in active mode and idle sleep modes and enables much more fine-tuned power management than sleep modes alone.

10.3 Sleep Modes

Sleep modes are used to shut down modules and clock domains in the microcontroller in order to save power. XMEGA microcontrollers have five different sleep modes tuned to match the typical functional stages during application execution. A dedicated sleep instruction (SLEEP) is available to enter sleep mode. Interrupts are used to wake the device from sleep, and the available interrupt wake-up sources are dependent on the configured sleep mode. When an enabled interrupt occurs, the device will wake up and execute the interrupt service routine before continuing normal program execution from the first instruction after the SLEEP instruction. If other, higher priority interrupts are pending when the wake-up occurs, their interrupt service routines will be executed according to their priority before the interrupt service routine for the wake-up interrupt is executed. After wake-up, the CPU is halted for four cycles before execution starts.

The content of the register file, SRAM and registers are kept during sleep. If a reset occurs during sleep, the device will reset, start up, and execute from the reset vector.

10.3.1 Idle Mode

In idle mode the CPU and nonvolatile memory are stopped (note that any ongoing programming will be completed), but all peripherals, including the interrupt controller, and event system are kept running. Any enabled interrupt will wake the device.

10.3.2 Power-down Mode

In power-down mode, all clocks, including the real-time counter clock source, are stopped. This allows operation only of asynchronous modules that do not require a running clock. The only interrupts that can wake up the MCU are the two-wire interface address match interrupt, asynchronous port interrupts, and the USB resume interrupt.

22. SPI – Serial Peripheral Interface

22.1 Features

- Two identical SPI peripherals
- Full-duplex, three-wire synchronous data transfer
- Master or slave operation
- Lsb first or msb first data transfer
- Eight programmable bit rates
- Interrupt flag at the end of transmission
- Write collision flag to indicate data collision
- Wake up from idle sleep mode
- Double speed master mode

22.2 Overview

The Serial Peripheral Interface (SPI) is a high-speed synchronous data transfer interface using three or four pins. It allows fast communication between an Atmel AVR XMEGA device and peripheral devices or between several microcontrollers. The SPI supports full-duplex communication.

A device connected to the bus must act as a master or slave. The master initiates and controls all data transactions. PORTC and PORTD each has one SPI. Notation of these peripherals are SPIC and SPID, respectively.

28. Programming and Debugging

28.1 Features

- Programming
 - External programming through PDI interface
 - Minimal protocol overhead for fast operation
 - Built-in error detection and handling for reliable operation
 - Boot loader support for programming through any communication interface
- Debugging
 - Nonintrusive, real-time, on-chip debug system
 - No software or hardware resources required from device except pin connection
 - Program flow control
 - Go, Stop, Reset, Step Into, Step Over, Step Out, Run-to-Cursor
 - Unlimited number of user program breakpoints
 - Unlimited number of user data breakpoints, break on:
 - Data location read, write, or both read and write
 - Data location content equal or not equal to a value
 - Data location content is greater or smaller than a value
 - Data location content is within or outside a range
 - No limitation on device clock frequency
- Program and Debug Interface (PDI)
 - Two-pin interface for external programming and debugging
 - Uses the Reset pin and a dedicated pin
 - No I/O pins required during programming or debugging

28.2 Overview

The Program and Debug Interface (PDI) is an Atmel proprietary interface for external programming and on-chip debugging of a device.

The PDI supports fast programming of nonvolatile memory (NVM) spaces; flash, EEPROM, fuses, lock bits, and the user signature row.

Debug is supported through an on-chip debug system that offers nonintrusive, real-time debug. It does not require any software or hardware resources except for the device pin connection. Using the Atmel tool chain, it offers complete program flow control and support for an unlimited number of program and complex data breakpoints. Application debug can be done from a C or other high-level language source code level, as well as from an assembler and disassembler level.

Programming and debugging can be done through the PDI physical layer. This is a two-pin interface that uses the Reset pin for the clock input (PDI_CLK) and one other dedicated pin for data input and output (PDI_DATA). Any external programmer or on-chip debugger/emulator can be directly connected to this interface.

29.2 Alternate Pin Functions

The tables below show the primary/default function for each pin on a port in the first column, the pin number in the second column, and then all alternate pin functions in the remaining columns. The head row shows what peripheral that enable and use the alternate pin functions.

For better flexibility, some alternate functions also have selectable pin locations for their functions, this is noted under the first table where this apply.

Table 29-1. Port A - Alternate Functions

PORT A	PIN #	INTERRUPT	ADCA POS/ GAINPOS	ADCA NEG	ADCA GAINNEG	ACA POS	ACA NEG	ACA OUT	REFA
GND	60								
AVCC	61								
PA0	62	SYNC	ADC0	ADC0		AC0	AC0		AREFA
PA1	63	SYNC	ADC1	ADC1		AC1	AC1		
PA2	64	SYNC/ASYNC	ADC2	ADC2		AC2			
PA3	1	SYNC	ADC3	ADC3		AC3	AC3		
PA4	2	SYNC	ADC4		ADC4	AC4			
PA5	3	SYNC	ADC5		ADC5	AC5	AC5		
PA6	4	SYNC	ADC6		ADC6	AC6		AC1OUT	
PA7	5	SYNC	ADC7		ADC7		AC7	AC0OUT	

Table 29-2. Port B - Alternate Functions

PORT B	PIN #	INTERRUPT	ADCA POS	REFB
PB0	6	SYNC	ADC8	AREFB
PB1	6	SYNC	ADC9	
PB2	8	SYNC/ASYNC	ADC10	
PB3	9	SYNC	ADC11	
PB4	10	SYNC	ADC12	
PB5	11	SYNC	ADC13	
PB6	12	SYNC	ADC14	
PB7	13	SYNC	ADC15	
GND	14			
VCC	15			

Table 33-25. External Clock with Prescaler ⁽¹⁾ for System Clock

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
1/t _{CK}	Clock Frequency ⁽²⁾	V _{CC} = 1.6 - 1.8V	0		90	MHz
		V _{CC} = 2.7 - 3.6V	0		142	
t _{CK}	Clock Period	V _{CC} = 1.6 - 1.8V	11			ns
		V _{CC} = 2.7 - 3.6V	7			
t _{CH}	Clock High Time	V _{CC} = 1.6 - 1.8V	4.5			
		V _{CC} = 2.7 - 3.6V	2.4			
t _{CL}	Clock Low Time	V _{CC} = 1.6 - 1.8V	4.5			
		V _{CC} = 2.7 - 3.6V	2.4			
t _{CR}	Rise Time (for maximum frequency)	V _{CC} = 1.6 - 1.8V			1.5	
		V _{CC} = 2.7 - 3.6V			1.0	
t _{CF}	Fall Time (for maximum frequency)	V _{CC} = 1.6 - 1.8V			1.5	
		V _{CC} = 2.7 - 3.6V			1.0	
Δt _{CK}	Change in period from one clock cycle to the next				10	%

Notes: 1. System Clock Prescalers must be set so that maximum CPU clock frequency for device is not exceeded.
2. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

33.1.13.7 External 16MHz Crystal Oscillator and XOSC Characteristics

Table 33-26. External 16MHz Crystal Oscillator and XOSC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Cycle to cycle jitter	XOSCPWR=0	FRQRANGE=0	0		ns
			FRQRANGE=1, 2, or 3	0		
		XOSCPWR=1		0		
	Long term jitter	XOSCPWR=0	FRQRANGE=0	0		
			FRQRANGE=1, 2, or 3	0		
		XOSCPWR=1		0		
	Frequency error	XOSCPWR=0	FRQRANGE=0	0.03		%
			FRQRANGE=1	0.03		
			FRQRANGE=2 or 3	0.03		
		XOSCPWR=1		0.003		
	Duty cycle	XOSCPWR=0	FRQRANGE=0	50		
			FRQRANGE=1	50		
			FRQRANGE=2 or 3	50		
		XOSCPWR=1		50		

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
R _Q	Negative impedance ⁽¹⁾	XOSCPWR=0, FRQRANGE=0	0.4MHz resonator, CL=100pF		44k		Ω
			1MHz crystal, CL=20pF		67k		
			2MHz crystal, CL=20pF		67k		
		XOSCPWR=0, FRQRANGE=1, CL=20pF	2MHz crystal		82k		
			8MHz crystal		1500		
			9MHz crystal		1500		
		XOSCPWR=0, FRQRANGE=2, CL=20pF	8MHz crystal		2700		
			9MHz crystal		2700		
			12MHz crystal		1000		
		XOSCPWR=0, FRQRANGE=3, CL=20pF	9MHz crystal		3600		
			12MHz crystal		1300		
			16MHz crystal		590		
		XOSCPWR=1, FRQRANGE=0, CL=20pF	9MHz crystal		390		
			12MHz crystal		50		
			16MHz crystal		10		
		XOSCPWR=1, FRQRANGE=1, CL=20pF	9MHz crystal		1500		
			12MHz crystal		650		
			16MHz crystal		270		
		XOSCPWR=1, FRQRANGE=2, CL=20pF	12MHz crystal		1000		
			16MHz crystal		440		
		XOSCPWR=1, FRQRANGE=3, CL=20pF	12MHz crystal		1300		
			16MHz crystal		590		
	ESR	SF = safety factor				min(R _Q)/SF	kΩ
	Start-up time	XOSCPWR=0, FRQRANGE=0	0.4MHz resonator, CL=100pF		1.0		ms
		XOSCPWR=0, FRQRANGE=1	2MHz crystal, CL=20pF		2.6		
		XOSCPWR=0, FRQRANGE=2	8MHz crystal, CL=20pF		0.8		
		XOSCPWR=0, FRQRANGE=3	12MHz crystal, CL=20pF		1.0		
		XOSCPWR=1, FRQRANGE=3	16MHz crystal, CL=20pF		1.4		

33.2.13.5 Internal Phase Locked Loop (PLL) Characteristics

Table 33-52. Internal PLL Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{IN}	Input frequency	Output frequency must be within f_{OUT}	0.4		64	MHz
f_{OUT}	Output frequency ⁽¹⁾	$V_{CC} = 1.6 - 1.8V$	20		48	
		$V_{CC} = 2.7 - 3.6V$	20		128	
	Start-up time			25		μs
	Re-lock time			25		

Note: 1. The maximum output frequency vs. supply voltage is linear between 1.8V and 2.7V, and can never be higher than four times the maximum CPU frequency.

33.2.13.6 External Clock Characteristics

Figure 33-10. External Clock Drive Waveform

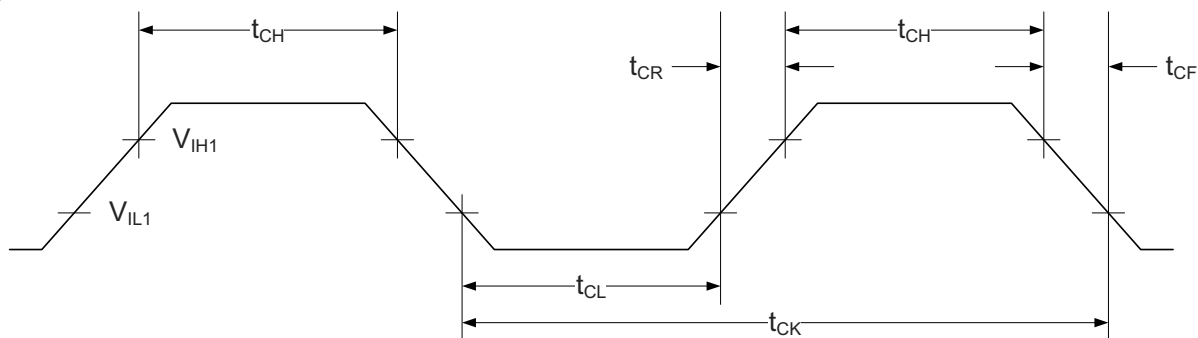


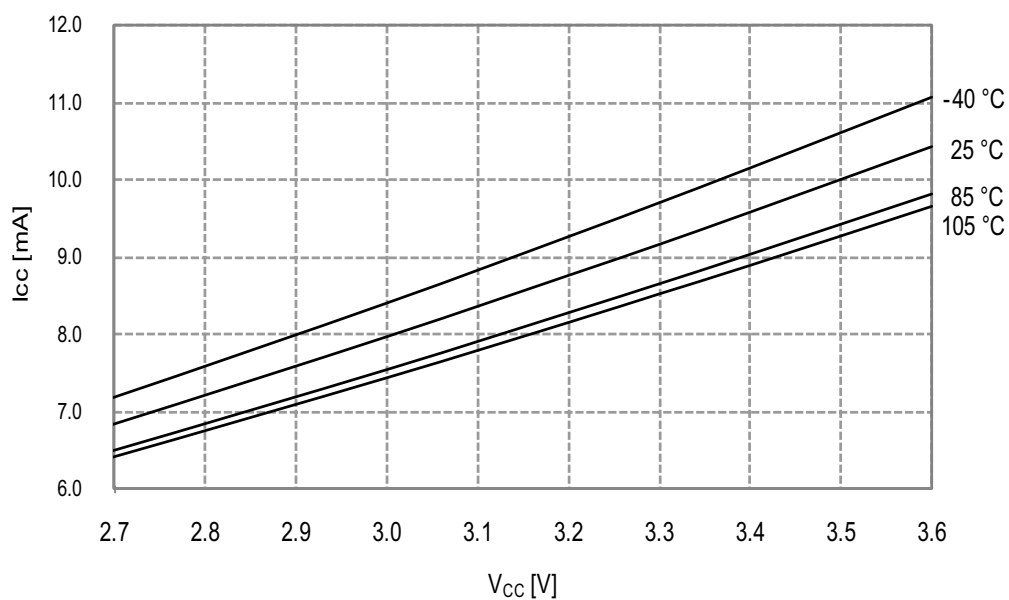
Table 33-53. External Clock used as System Clock without Prescaling

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock Frequency ⁽¹⁾	$V_{CC} = 1.6 - 1.8V$	0		12	MHz
		$V_{CC} = 2.7 - 3.6V$	0		32	
t_{CK}	Clock Period	$V_{CC} = 1.6 - 1.8V$	83.3			ns
		$V_{CC} = 2.7 - 3.6V$	31.5			
t_{CH}	Clock High Time	$V_{CC} = 1.6 - 1.8V$	30.0			
		$V_{CC} = 2.7 - 3.6V$	12.5			
t_{CL}	Clock Low Time	$V_{CC} = 1.6 - 1.8V$	30.0			
		$V_{CC} = 2.7 - 3.6V$	12.5			
t_{CR}	Rise Time (for maximum frequency)	$V_{CC} = 1.6 - 1.8V$			10	
		$V_{CC} = 2.7 - 3.6V$			3	
t_{CF}	Fall Time (for maximum frequency)	$V_{CC} = 1.6 - 1.8V$			10	
		$V_{CC} = 2.7 - 3.6V$			3	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Note: 1. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

Figure 34-7. Active Mode Supply Current vs. V_{CC}

$f_{SYS} = 32\text{MHz}$ internal oscillator



34.1.1.2 Idle Mode Supply Current

Figure 34-8. Idle Mode Supply Current vs. Frequency

$f_{SYS} = 0 - 1\text{MHz}$ external clock, $T = 25\text{ }^{\circ}\text{C}$

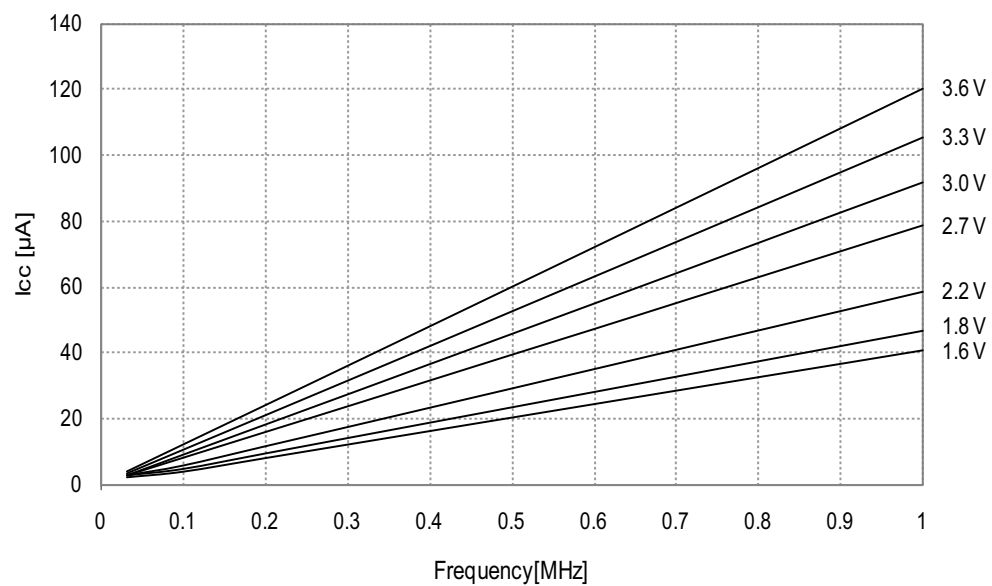
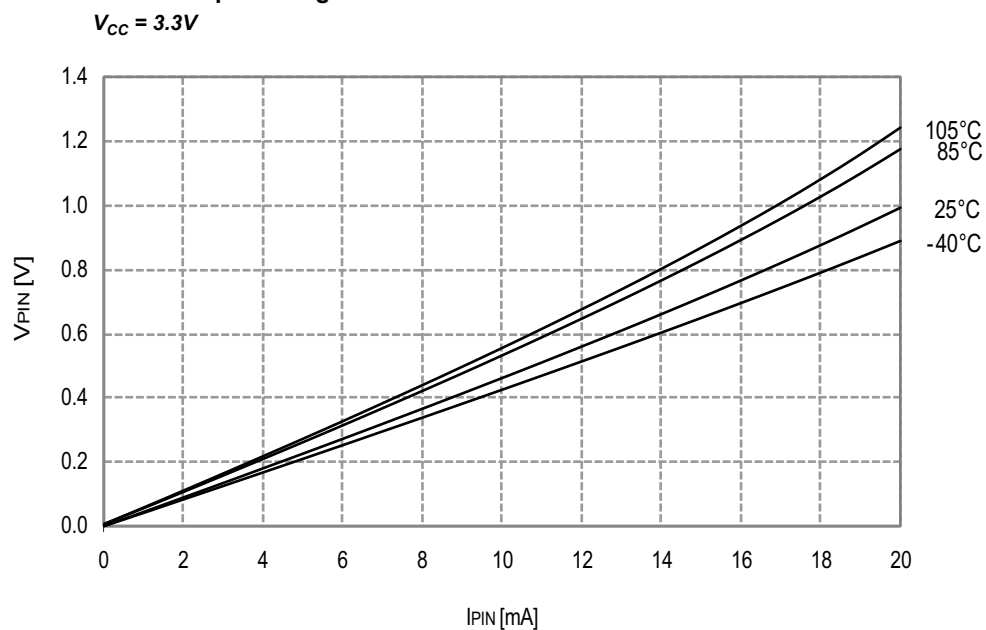


Figure 34-27. I/O Pin Output Voltage vs. Sink Current



34.1.2.3 Thresholds and Hysteresis

Figure 34-28. I/O Pin Input Threshold Voltage vs. V_{CC}

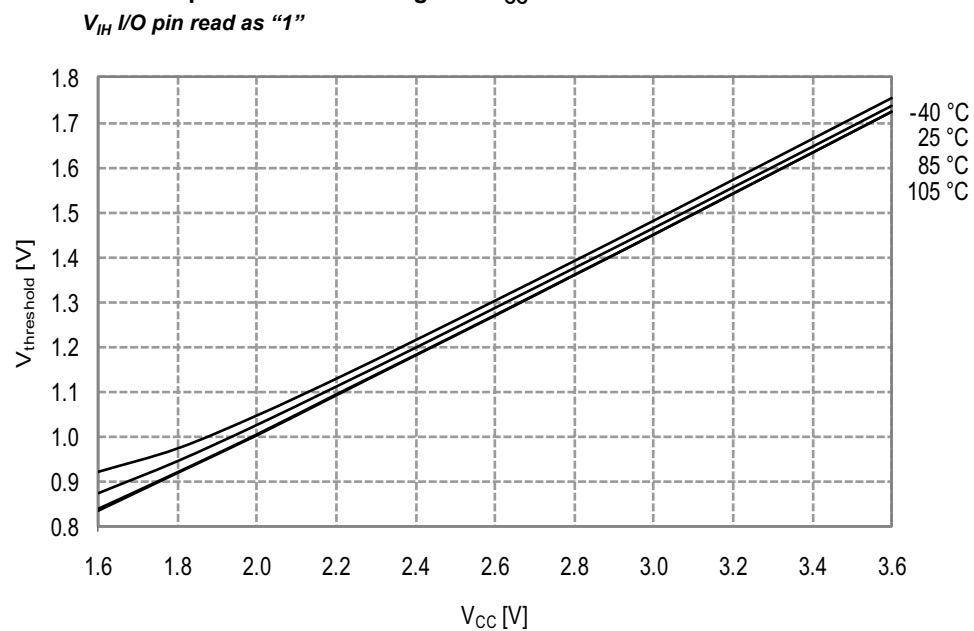


Figure 34-43. Analog Comparator Hysteresis vs. V_{CC}
Large hysteresis

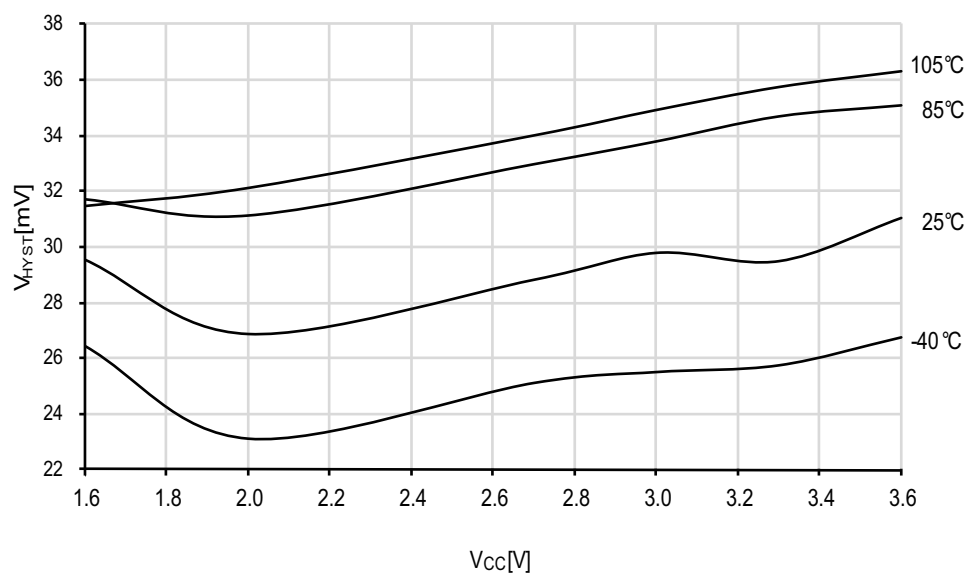
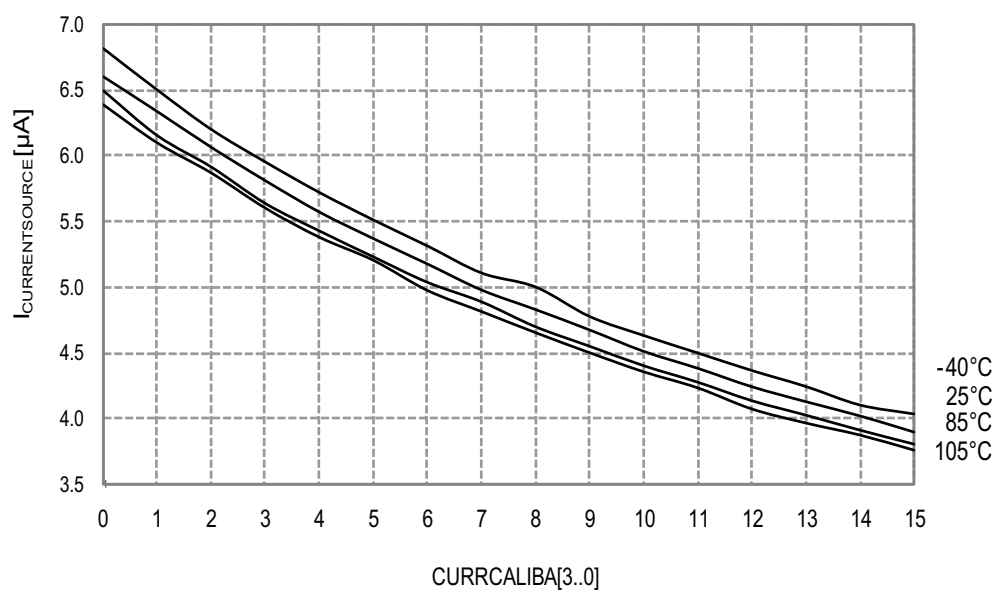


Figure 34-44. Analog Comparator Current Source vs. Calibration Value
 $V_{CC} = 3.0V$



34.2 Atmel ATxmega64C3

34.2.1 Current Consumption

34.2.1.1 Active Mode Supply Current

Figure 34-72.Active Supply Current vs. Frequency

$f_{\text{SYS}} = 0 - 1\text{MHz}$ external clock, $T = 25^{\circ}\text{C}$

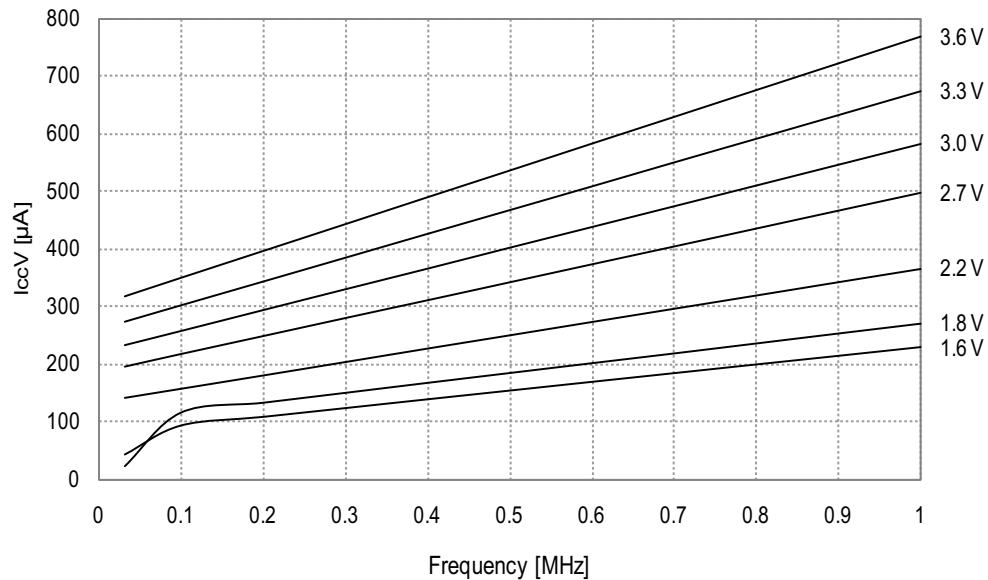


Figure 34-73.Active Supply Current vs. Frequency

$f_{\text{SYS}} = 1 - 32\text{MHz}$ external clock, $T = 25^{\circ}\text{C}$

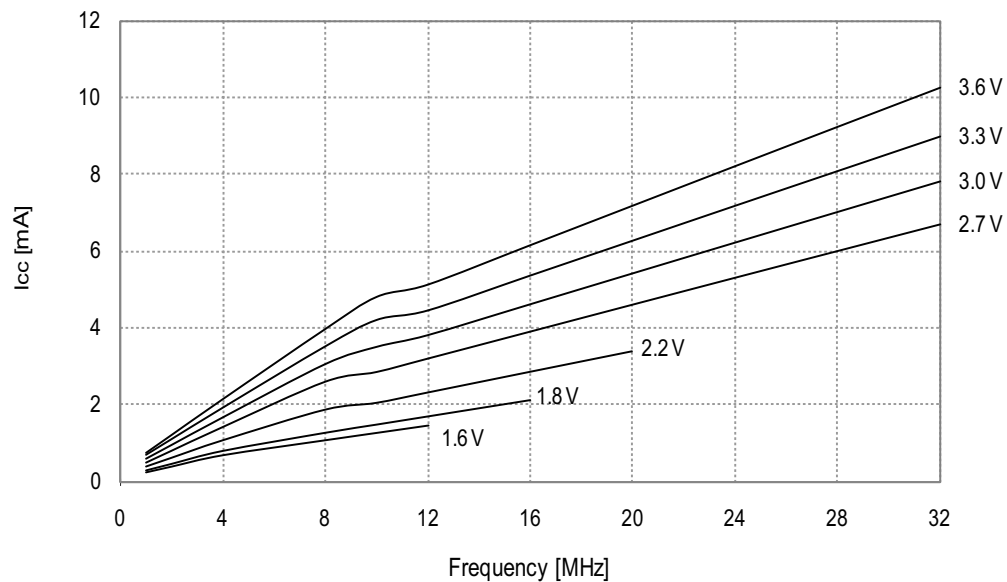
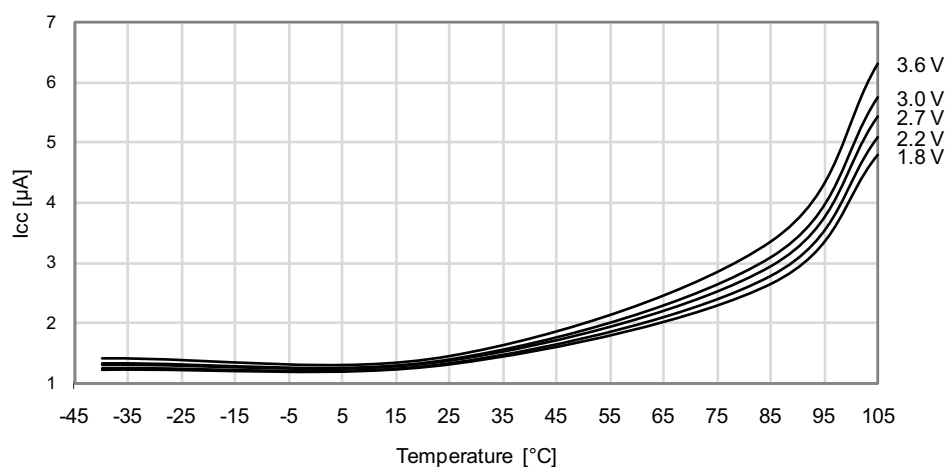


Figure 34-159. Power-down Mode Supply Current vs. Temperature
Watchdog and sampled BOD enabled and running from internal ULP oscillator



34.3.2 I/O Pin Characteristics

34.3.2.1 Pull-up

Figure 34-160. I/O Pin Pull-up Resistor Current vs. Input Voltage
 $V_{CC} = 1.8V$

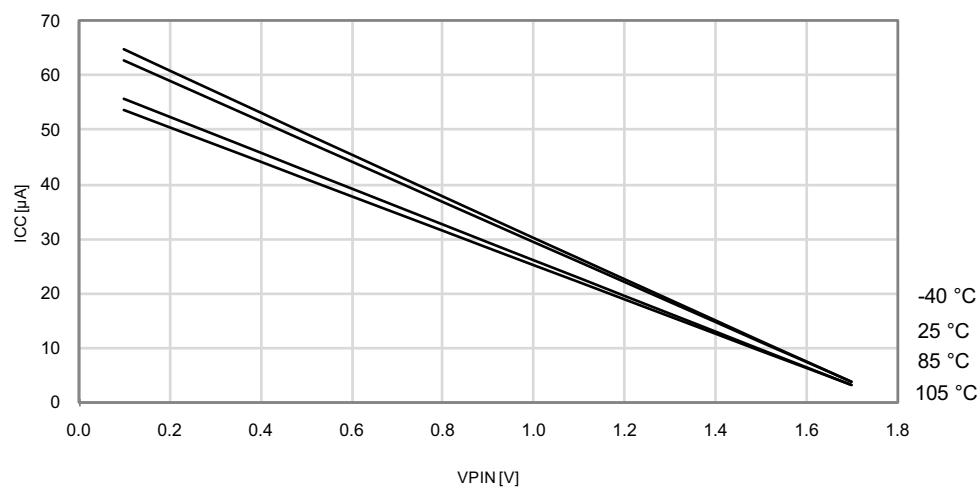
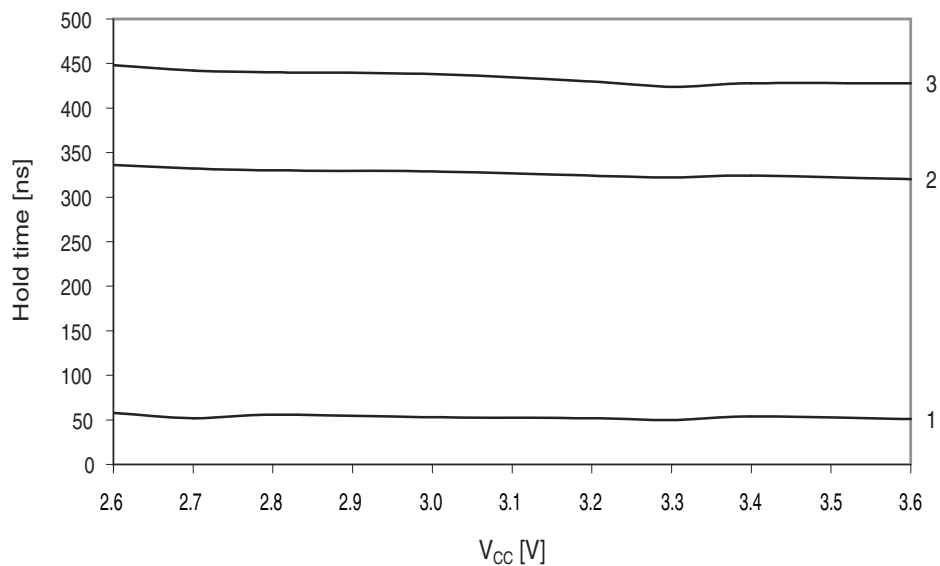


Figure 34-211. SDA Hold Time vs. Supply Voltage



34.3.10 PDI Characteristics

Figure 34-212. Maximum PDI Frequency vs. V_{CC}

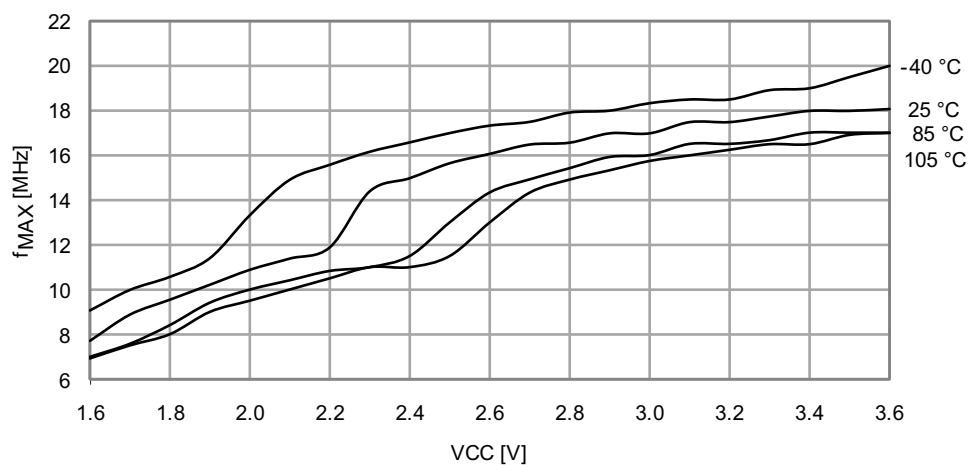


Figure 34-221. Idle Mode Supply Current vs. Frequency

$f_{\text{SYS}} = 1 - 32\text{MHz}$ external clock, $T = 25^\circ\text{C}$

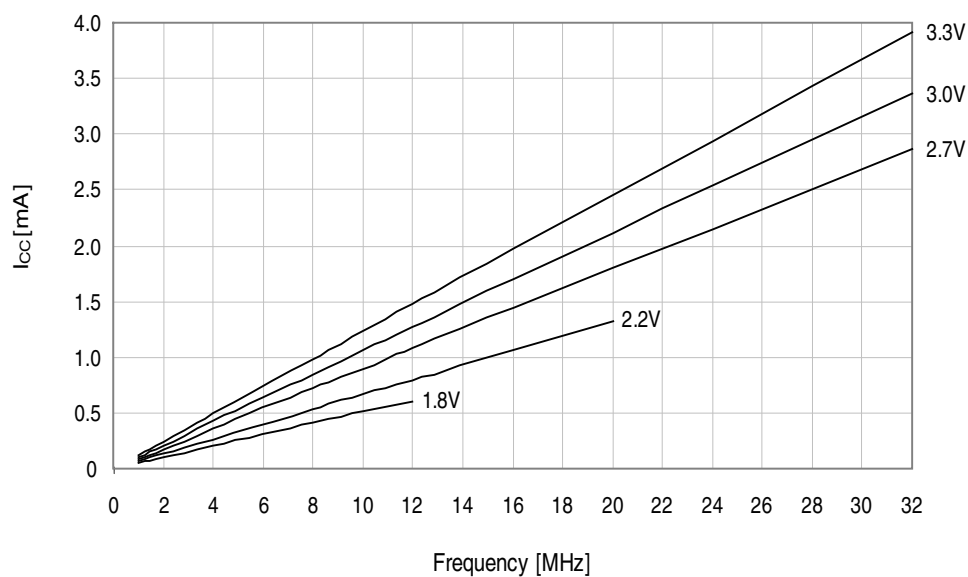
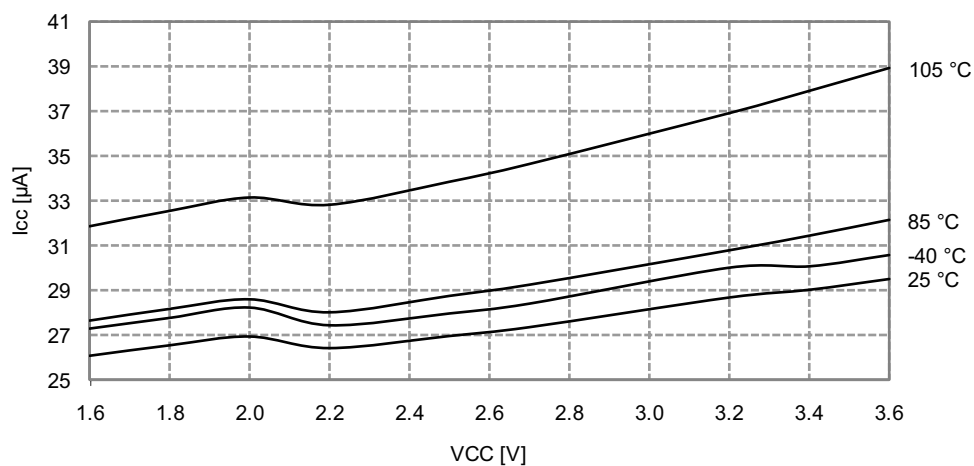


Figure 34-222. Idle Mode Supply Current vs. V_{CC}

$f_{\text{SYS}} = 32.768\text{kHz}$ internal oscillator



34.4.2.3 Thresholds and Hysteresis

Figure 34-239. I/O Pin Input Threshold Voltage vs. V_{CC}
 V_{IH} I/O pin read as “1”

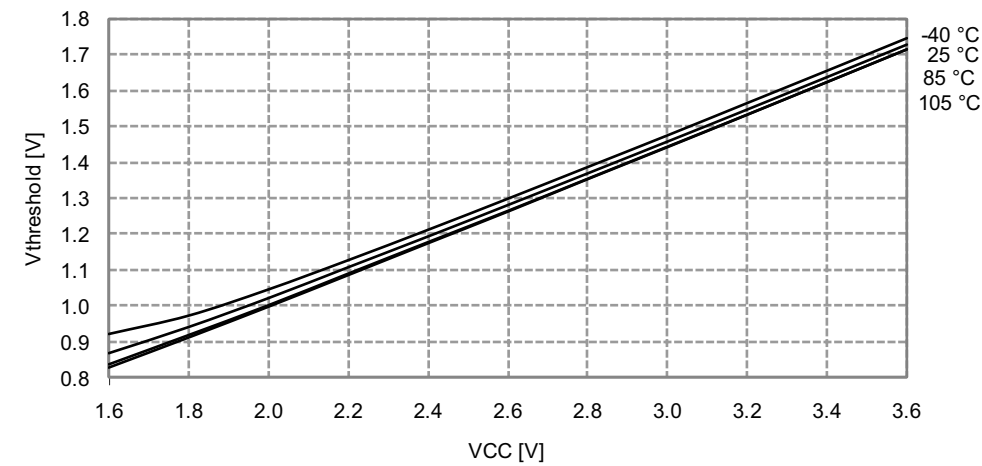


Figure 34-240. I/O Pin Input Threshold Voltage vs. V_{CC}
 V_{IL} I/O pin read as “0”

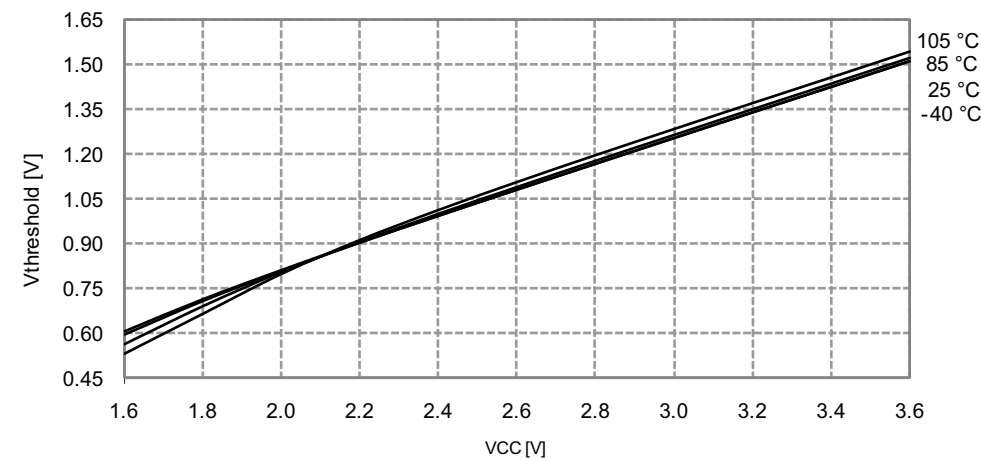
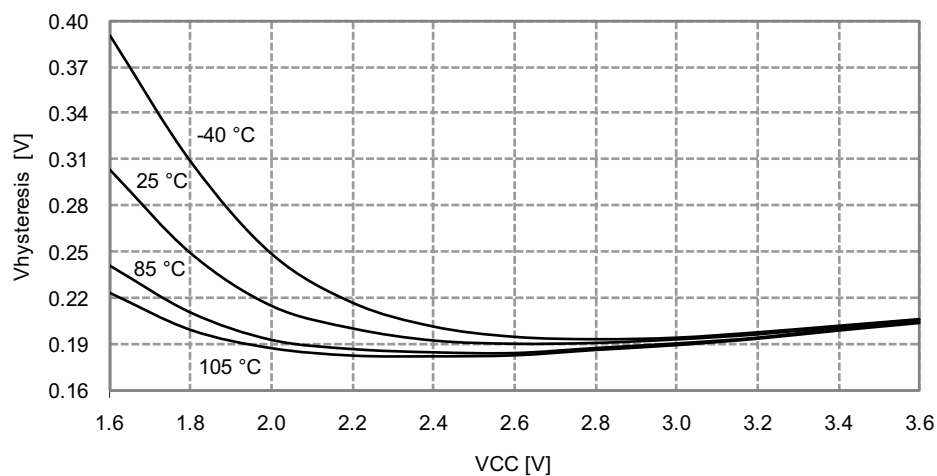


Figure 34-241. I/O Pin Input Hysteresis vs. V_{CC}



34.4.3 ADC Characteristics

Figure 34-242. INL Error vs. External V_{REF}
 $T = 25^{\circ}\text{C}$, $V_{CC} = 3.6\text{V}$, external reference

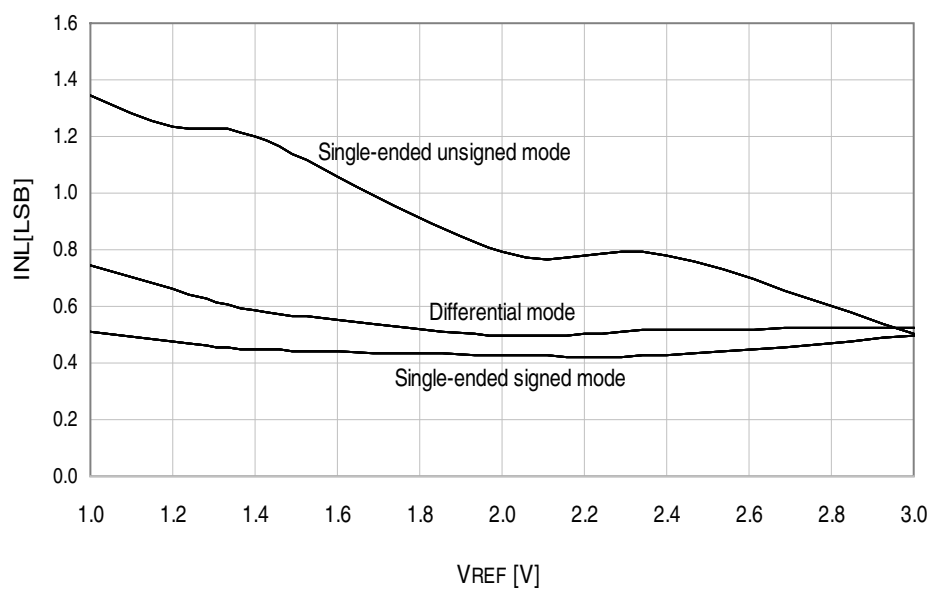


Figure 34-285. Active Mode Supply Current vs. V_{CC}

$f_{SYS} = 32.768\text{kHz}$ internal oscillator

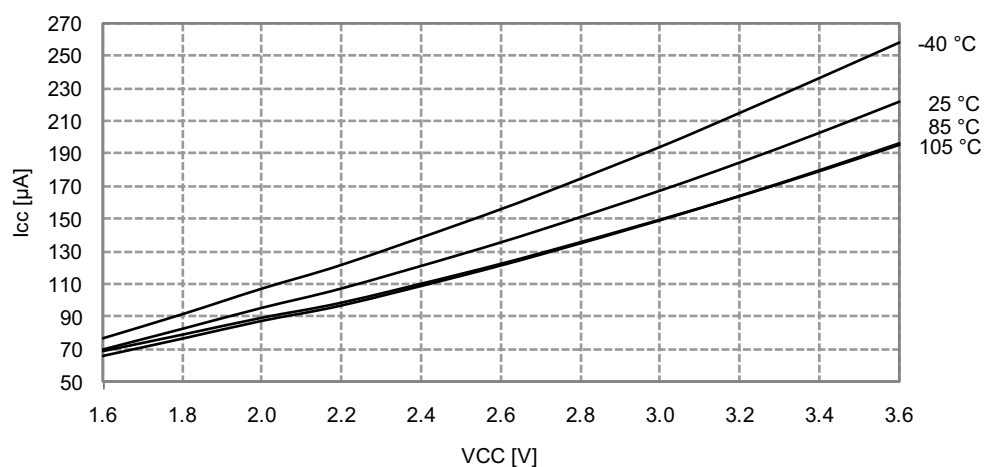


Figure 34-286. Active Mode Supply Current vs. V_{CC}

$f_{SYS} = 1\text{MHz}$ external clock

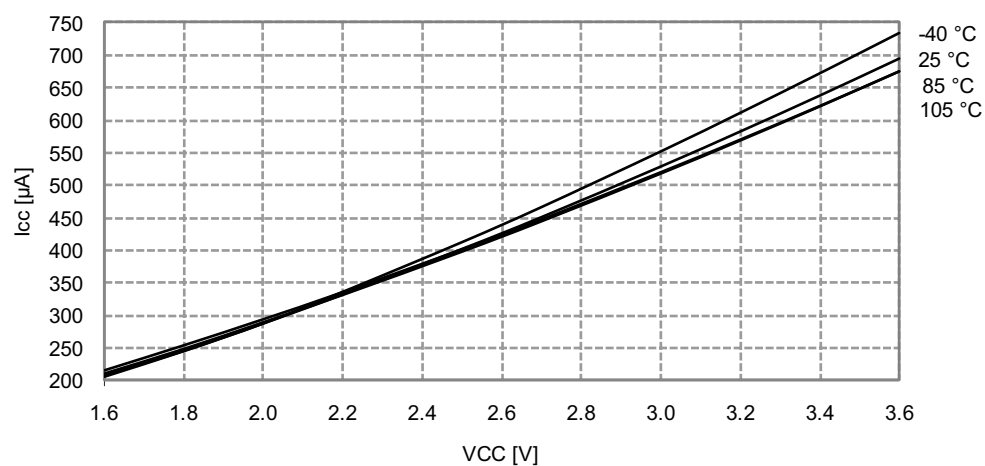
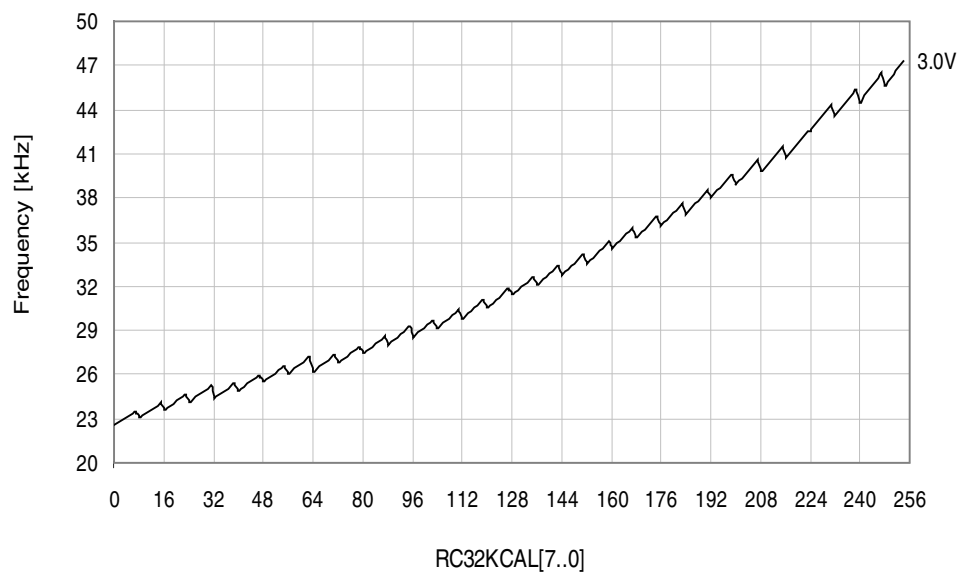


Figure 34-337. 32.768kHz Internal Oscillator Frequency vs. Calibration Value

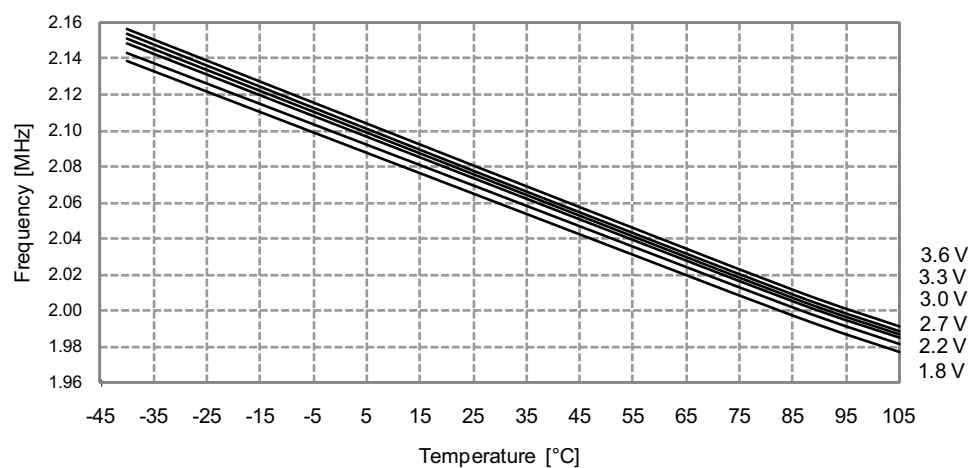
$V_{CC} = 3.0V$, $T = 25^{\circ}C$



34.5.8.3 2MHz Internal Oscillator

Figure 34-338. 2MHz Internal Oscillator Frequency vs. Temperature

DFLL disabled



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