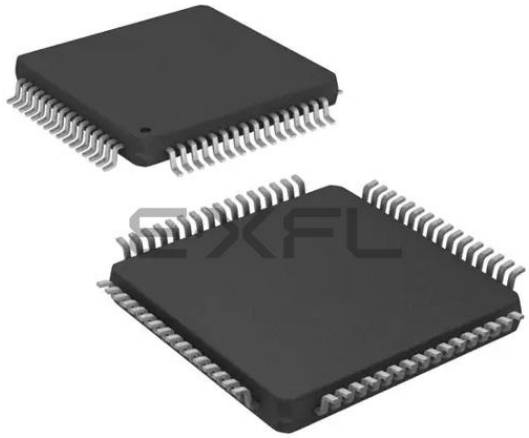

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	50
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega32c3-anr

The production signature row also contains an ID that identifies each microcontroller device type and a serial number for each manufactured device. The serial number consists of the production lot number, wafer number, and wafer coordinates for the device. The device ID for the available devices is shown in Table 7-1.

The production signature row cannot be written or erased, but it can be read from application software and external programmers.

Table 7-1. Device ID Bytes

Device	Device ID bytes		
	Byte 2	Byte 1	Byte 0
ATxmega32C3	49	95	1E
ATxmega64C3	49	96	1E
ATxmega128C3	52	97	1E
ATxmega192C3	51	97	1E
ATxmega256C3	46	98	1E

7.3.5 User Signature Row

The user signature row is a separate memory section that is fully accessible (read and write) from application software and external programmers. It is one flash page in size, and is meant for static user parameter storage, such as calibration data, custom serial number, identification numbers, random number seeds, etc. This section is not erased by chip erase commands that erase the flash, and requires a dedicated erase command. This ensures parameter storage during multiple program/erase operations and on-chip debug sessions.

7.4 Fuses and Lock Bits

The fuses are used to configure important system functions, and can only be written from an external programmer. The application software can read the fuses. The fuses are used to configure reset sources such as brownout detector and watchdog, and startup configuration.

The lock bits are used to set protection levels for the different flash sections (that is, if read and/or write access should be blocked). Lock bits can be written by external programmers and application software, but only to stricter protection levels. Chip erase is the only way to erase the lock bits. To ensure that flash contents are protected even during chip erase, the lock bits are erased after the rest of the flash memory has been erased.

An unprogrammed fuse or lock bit will have the value one, while a programmed fuse or lock bit will have the value zero.

Both fuses and lock bits are reprogrammable like the flash program memory.

7.5 Data Memory

The data memory contains the I/O memory, internal SRAM, optionally memory mapped EEPROM, and external memory if available. The data memory is organized as one continuous memory section, see Figure 7-2 on page 15. To simplify development, I/O Memory, EEPROM, and SRAM will always have the same start addresses for all Atmel AVR XMEGA devices.

Mnemonics	Operands	Description	Operation	Flags	#Clocks
MOVW	Rd, Rr	Copy Register Pair	Rd+1:Rd ← Rr+1:Rr	None	1
LDI	Rd, K	Load Immediate	Rd ← K	None	1
LDS	Rd, k	Load Direct from data space	Rd ← (k)	None	2 (1)
LD	Rd, X	Load Indirect	Rd ← (X)	None	1 (1)
LD	Rd, X+	Load Indirect and Post-Increment	Rd ← (X) X ← X + 1	None	1 (1)
LD	Rd, -X	Load Indirect and Pre-Decrement	X ← X - 1, ← X - 1 Rd ← (X) ← (X)	None	2 (1)
LD	Rd, Y	Load Indirect	Rd ← (Y) ← (Y)	None	1 (1)
LD	Rd, Y+	Load Indirect and Post-Increment	Rd ← (Y) Y ← Y + 1	None	1 (1)
LD	Rd, -Y	Load Indirect and Pre-Decrement	Y ← Y - 1 Rd ← (Y)	None	2 (1)
LDD	Rd, Y+q	Load Indirect with Displacement	Rd ← (Y + q)	None	2 (1)
LD	Rd, Z	Load Indirect	Rd ← (Z)	None	1 (1)
LD	Rd, Z+	Load Indirect and Post-Increment	Rd ← (Z), Z ← Z+1	None	1 (1)
LD	Rd, -Z	Load Indirect and Pre-Decrement	Z ← Z - 1, Rd ← (Z)	None	2 (1)
LDD	Rd, Z+q	Load Indirect with Displacement	Rd ← (Z + q)	None	2 (1)
STS	k, Rr	Store Direct to Data Space	(k) ← Rd	None	2
ST	X, Rr	Store Indirect	(X) ← Rr	None	1
ST	X+, Rr	Store Indirect and Post-Increment	(X) ← Rr, X ← X + 1	None	1
ST	-X, Rr	Store Indirect and Pre-Decrement	X ← X - 1, (X) ← Rr	None	2
ST	Y, Rr	Store Indirect	(Y) ← Rr	None	1
ST	Y+, Rr	Store Indirect and Post-Increment	(Y) ← Rr, Y ← Y + 1	None	1
ST	-Y, Rr	Store Indirect and Pre-Decrement	Y ← Y - 1, (Y) ← Rr	None	2
STD	Y+q, Rr	Store Indirect with Displacement	(Y + q) ← Rr	None	2
ST	Z, Rr	Store Indirect	(Z) ← Rr	None	1
ST	Z+, Rr	Store Indirect and Post-Increment	(Z) ← Rr Z ← Z + 1	None	1
ST	-Z, Rr	Store Indirect and Pre-Decrement	Z ← Z - 1	None	2
STD	Z+q,Rr	Store Indirect with Displacement	(Z + q) ← Rr	None	2
LPM		Load Program Memory	R0 ← (Z)	None	3
LPM	Rd, Z	Load Program Memory	Rd ← (Z)	None	3
LPM	Rd, Z+	Load Program Memory and Post-Increment	Rd ← (Z), Z ← Z + 1	None	3
ELPM		Extended Load Program Memory	R0 ← (RAMPZ:Z)	None	3

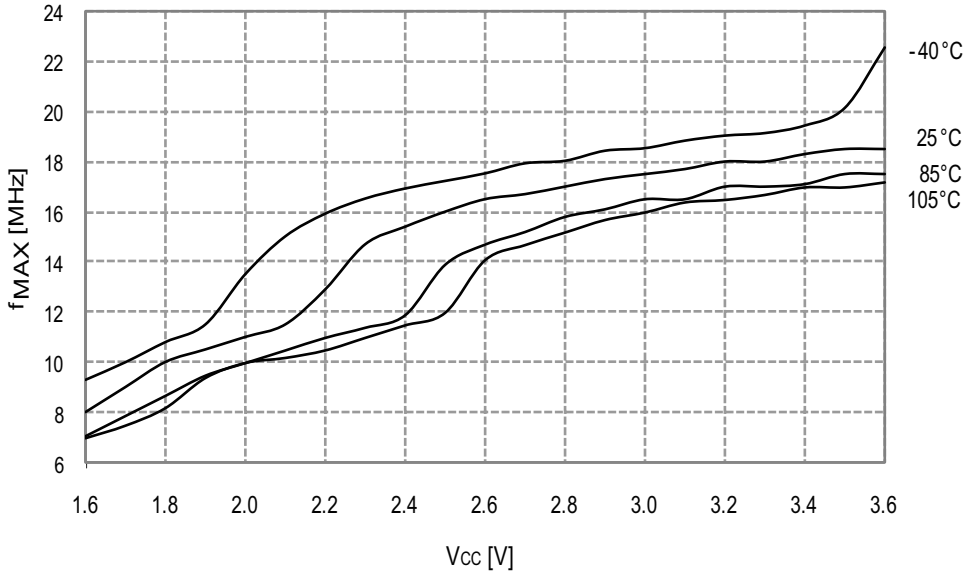
Table 33-34. Current Consumption for Modules and Peripherals

Symbol	Parameter	Condition[1]		Min.	Typ.	Max.	Units
I_{CC}	ULP oscillator				0.9		µA
	32.768kHz int. oscillator				29		
	2MHz int. oscillator				82		
		DFLL enabled with 32.768kHz int. osc. as reference			114		
	32MHz int. oscillator				250		
		DFLL enabled with 32.768kHz int. osc. as reference			400		
	PLL	20x multiplication factor, 32MHz int. osc. DIV4 as reference			300		
	Watchdog timer				1.0		
	BOD	Continuous mode			140		
		Sampled mode, includes ULP oscillator			1.4		
	Internal 1.0V reference				180		
	Temperature sensor				175		
	ADC	16ksps V_{REF} = Ext. ref.			1.23		mA
			CURRLIMIT = LOW		1.1		
			CURRLIMIT = MEDIUM		0.98		
			CURRLIMIT = HIGH		0.87		
		75ksps V_{REF} = Ext. ref.	CURRLIMIT = LOW		1.7		
		300ksps V_{REF} = Ext. ref.			3.1		
	USART	Rx and Tx enabled, 9600 BAUD			9.7		µA
	Flash memory and EEPROM programming				5		mA

Note: 1. All parameters measured as the difference in current consumption between module enabled and disabled. All data at V_{CC} = 3.0V, Clk_{SYS} = 1MHz external clock without prescaling, T = 25°C unless other conditions are given.

34.1.10 PDI Characteristics

Figure 34-71. Maximum PDI Frequency vs. V_{CC}



34.2 Atmel ATxmega64C3

34.2.1 Current Consumption

34.2.1.1 Active Mode Supply Current

Figure 34-72.Active Supply Current vs. Frequency

f_{SYS} = 0 - 1MHz external clock, T = 25°C

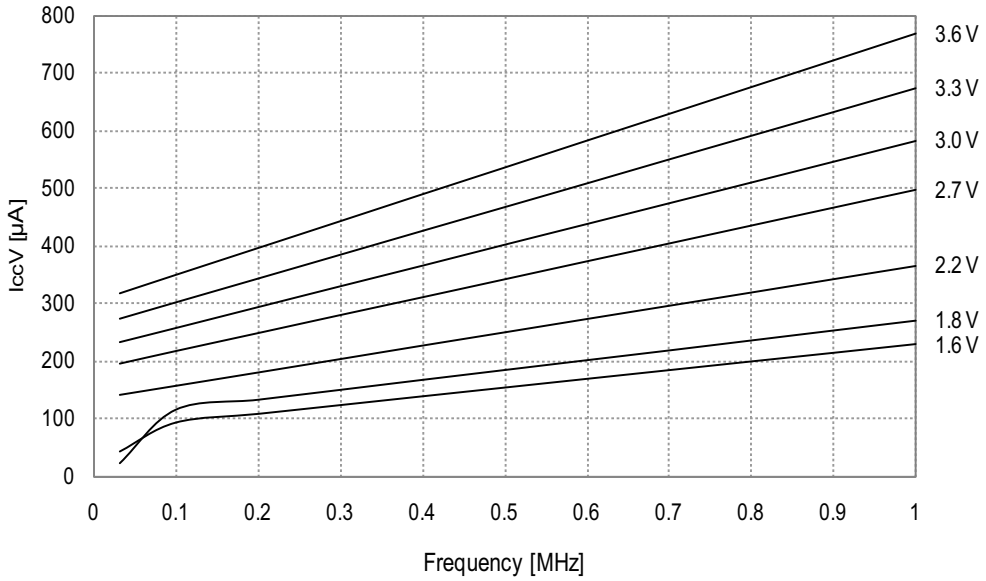


Figure 34-73.Active Supply Current vs. Frequency

f_{SYS} = 1 - 32MHz external clock, T = 25°C

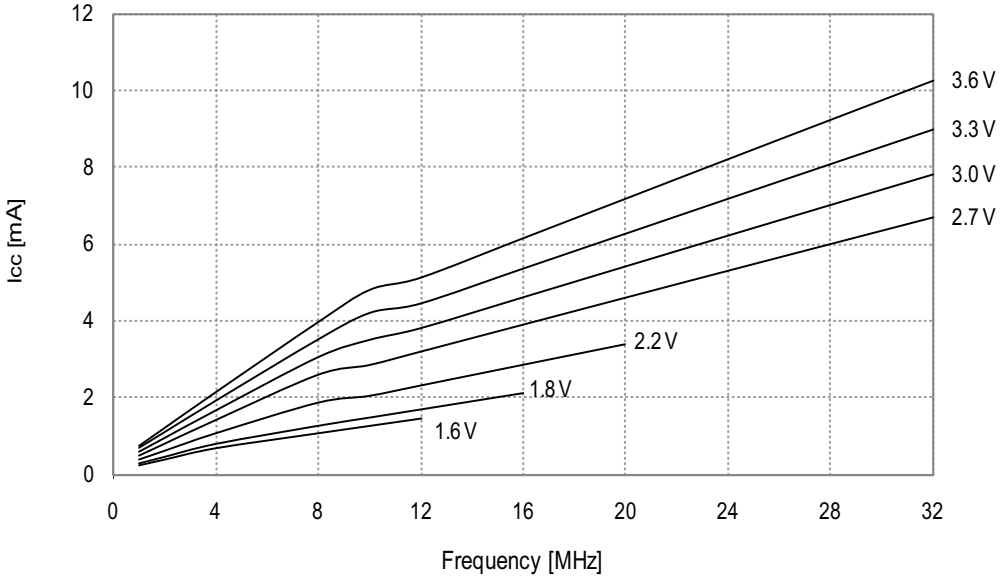
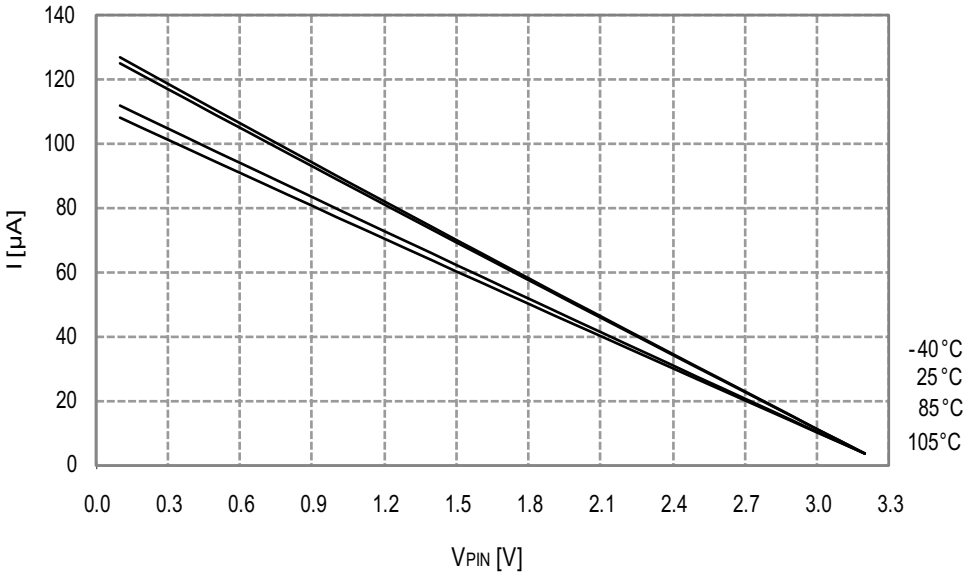


Figure 34-92. I/O Pin Pull-up Resistor Current vs. Input Voltage

V_{CC} = 3.3V



34.2.2.2 Output Voltage vs. Sink/Source Current

Figure 34-93. I/O Pin Output Voltage vs. Source Current

V_{CC} = 1.8V

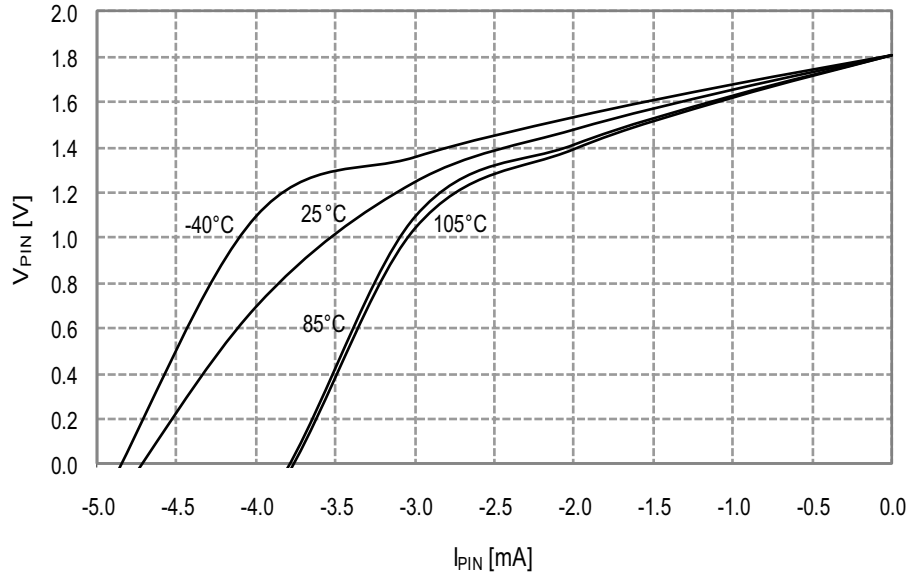
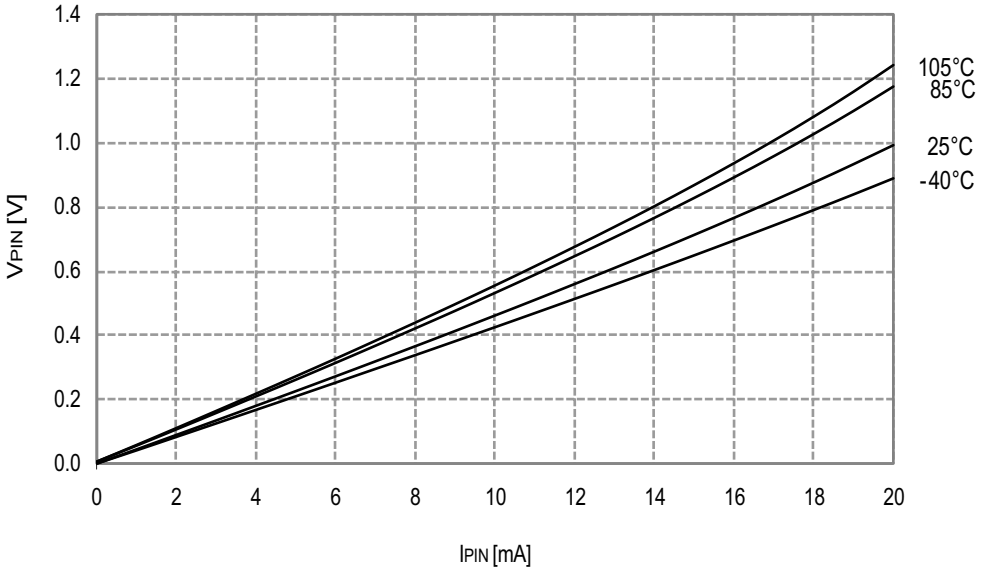


Figure 34-98. I/O Pin Output Voltage vs. Sink Current

V_{CC} = 3.3V



34.2.2.3 Thresholds and Hysteresis

Figure 34-99. I/O Pin Input Threshold Voltage vs. V_{CC}

V_{IH} I/O pin read as "1"

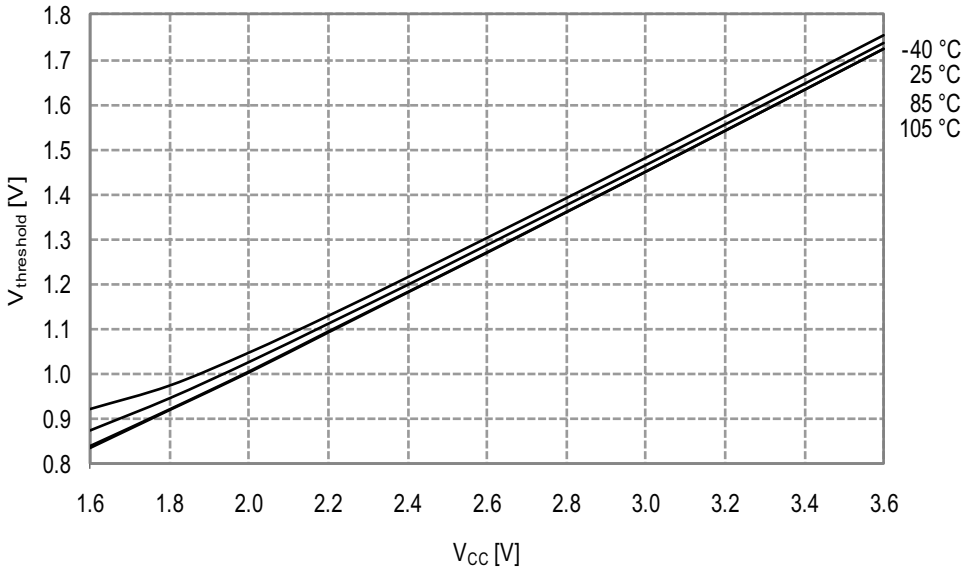


Figure 34-114. Analog Comparator Hysteresis vs. V_{CC}

Large hysteresis

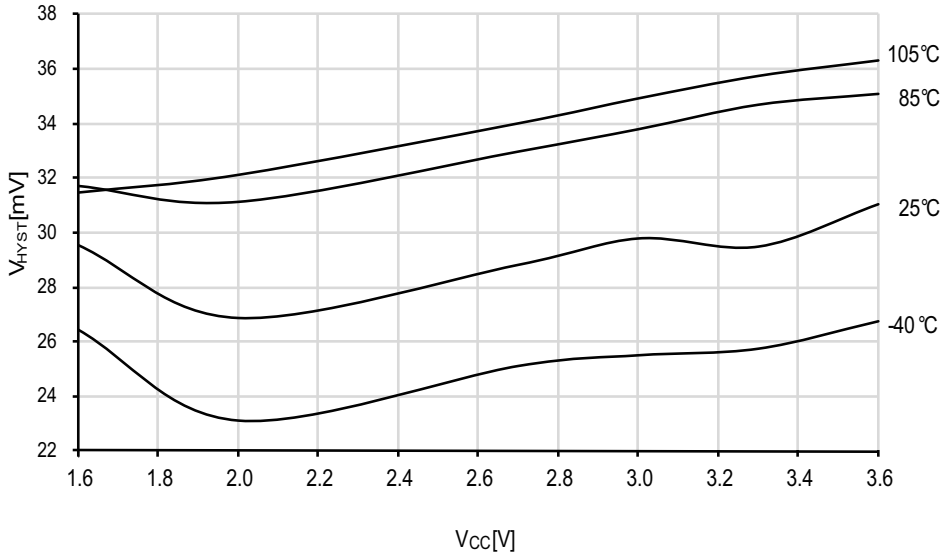


Figure 34-115. Analog Comparator Current Source vs. Calibration Value

V_{CC} = 3.0V

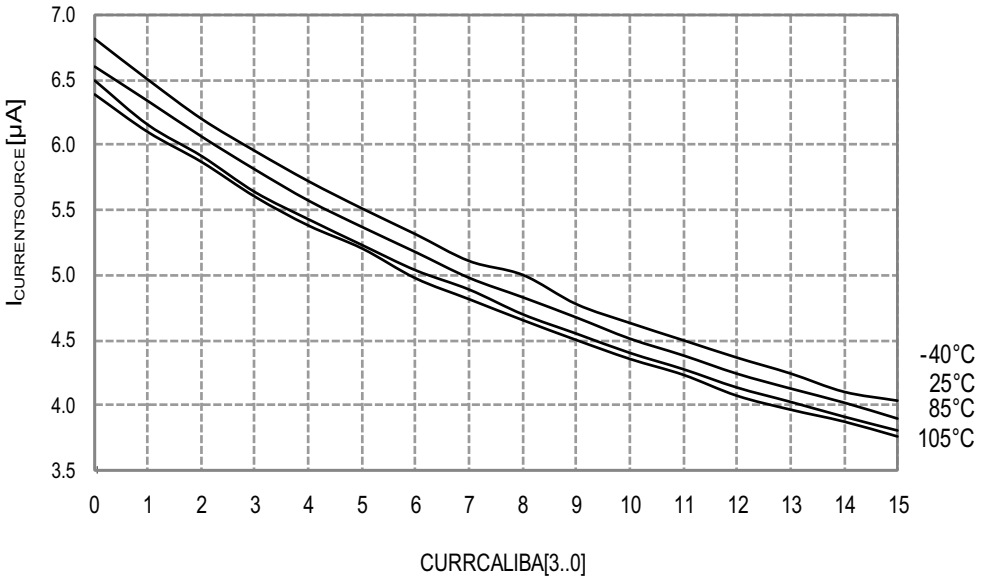
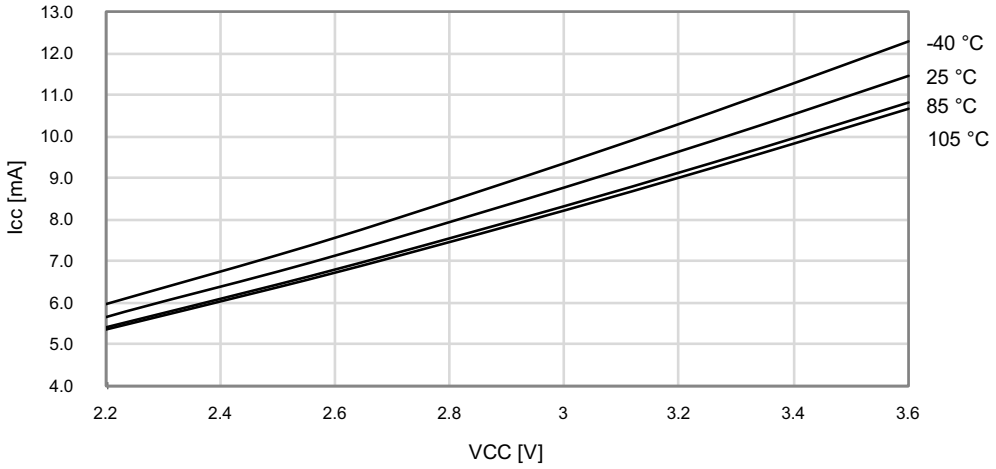


Figure 34-149. Active Mode Supply Current vs. V_{CC}

f_{SYS} = 32MHz internal oscillator



34.3.1.2 Idle Mode Supply Current

Figure 34-150. Idle Mode Supply Current vs. Frequency

f_{SYS} = 0 - 1MHz external clock, T = 25°C

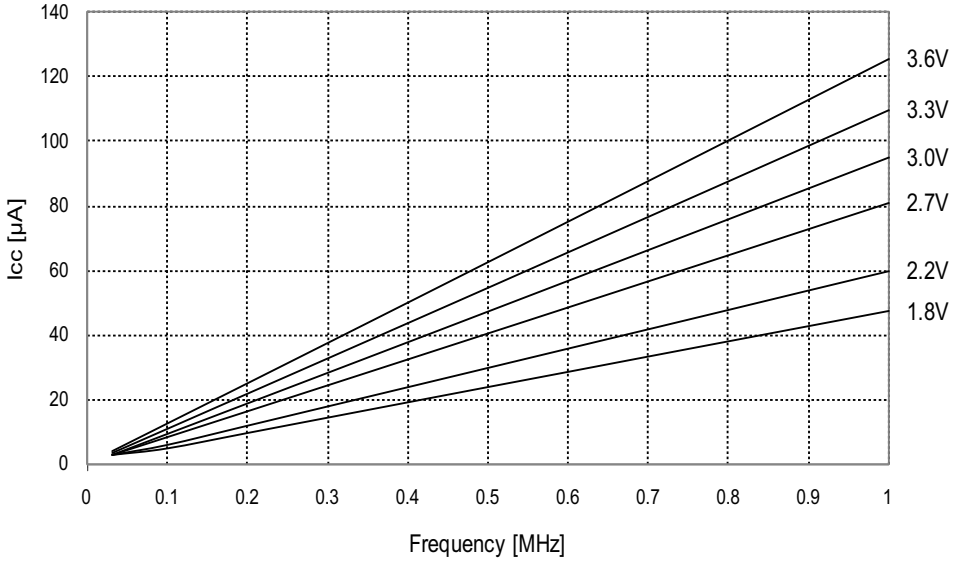


Figure 34-181. Gain Error vs. Temperature

V_{CC} = 3.0V, V_{REF} = external 2.0V

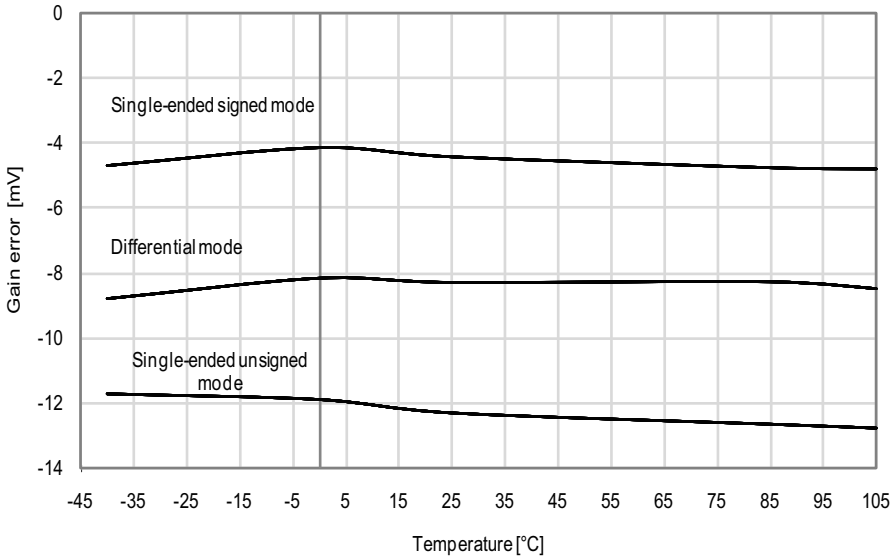


Figure 34-182. Offset Error vs. V_{CC}

T = 25°C, V_{REF} = external 1.0V, ADC sample rate = 300ksps

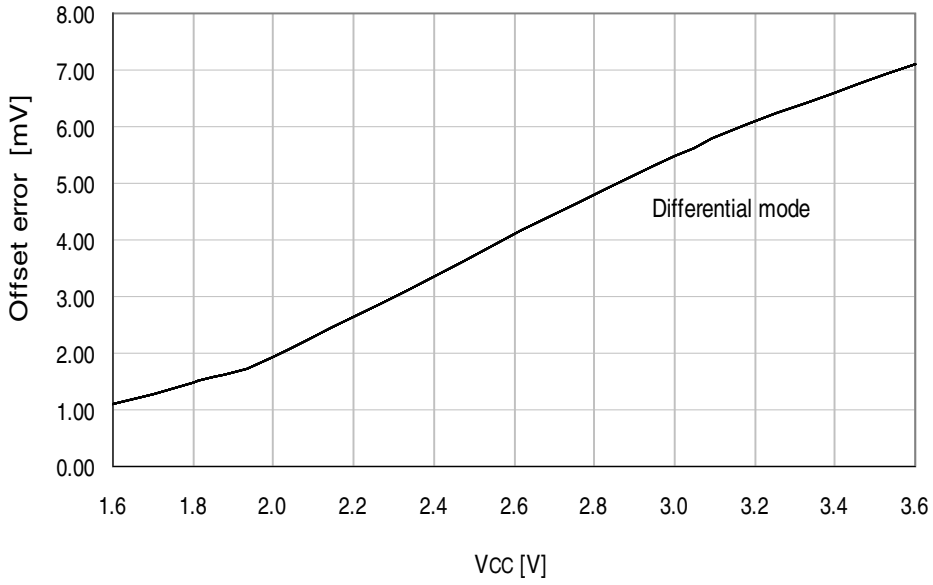
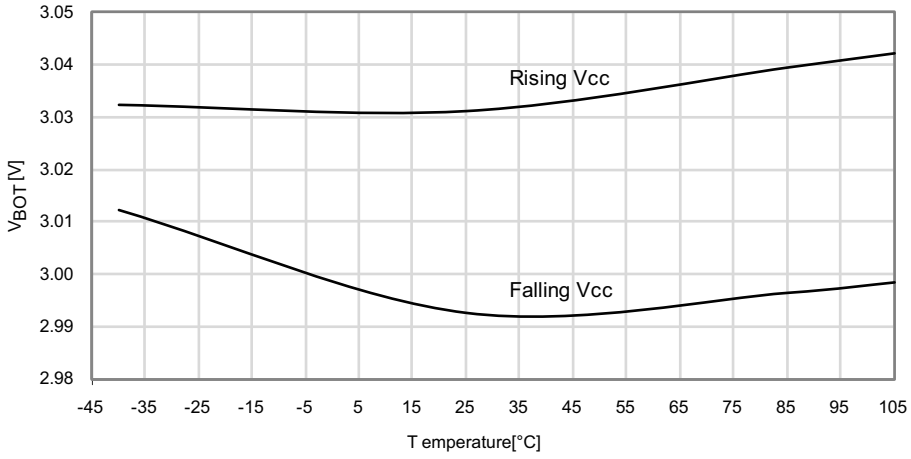


Figure 34-189. BOD Thresholds vs. Temperature

BOD level = 3.0V



34.3.7 External Reset Characteristics

Figure 34-190. Minimum Reset Pin Pulse Width vs. V_{CC}

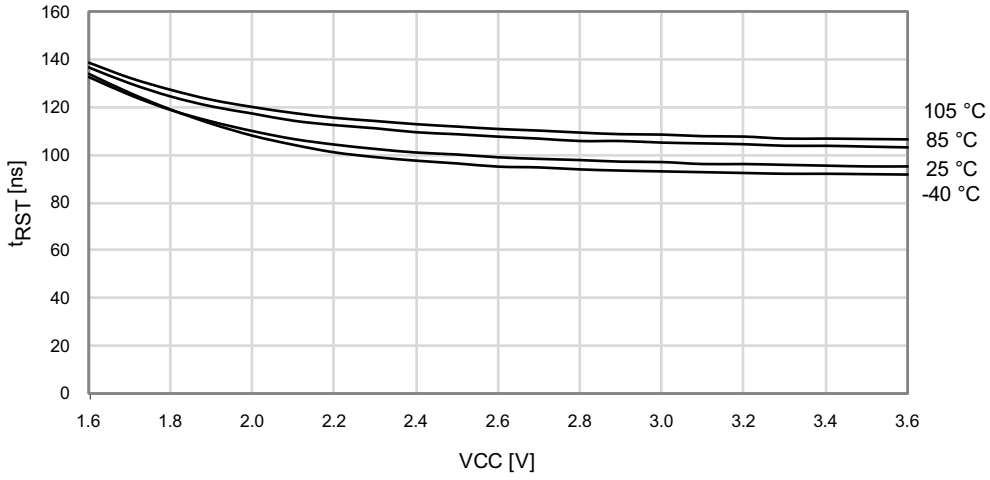
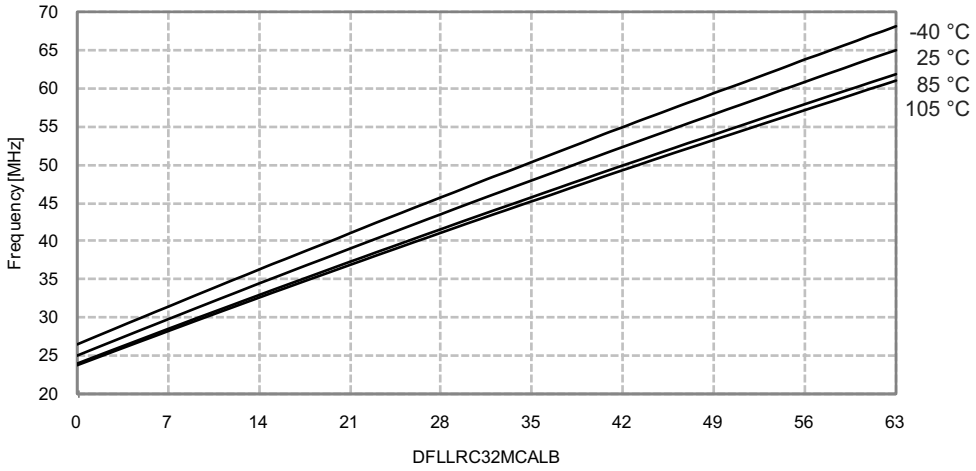


Figure 34-207. 32MHz Internal Oscillator Frequency vs. CALB Calibration Value

V_{CC} = 3.0V



34.3.8.5 32MHz Internal Oscillator Calibrated to 48MHz

Figure 34-208. 48MHz Internal Oscillator Frequency vs. Temperature

DFLL disabled

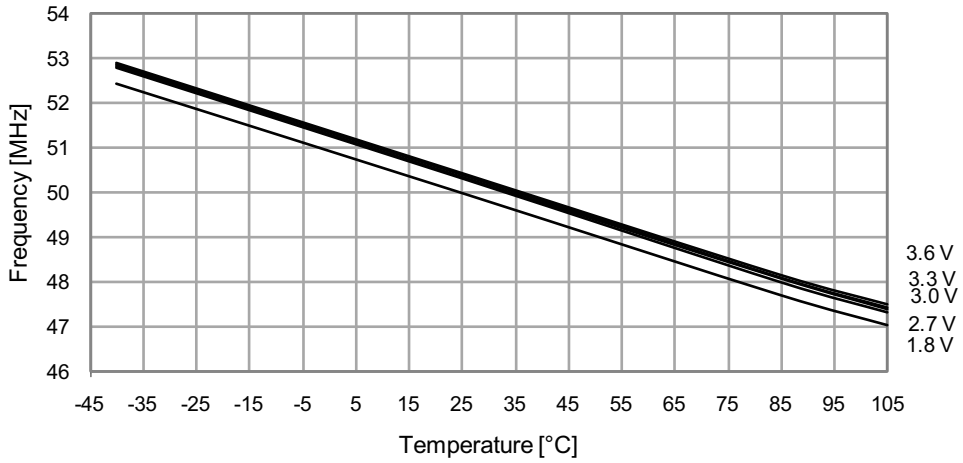
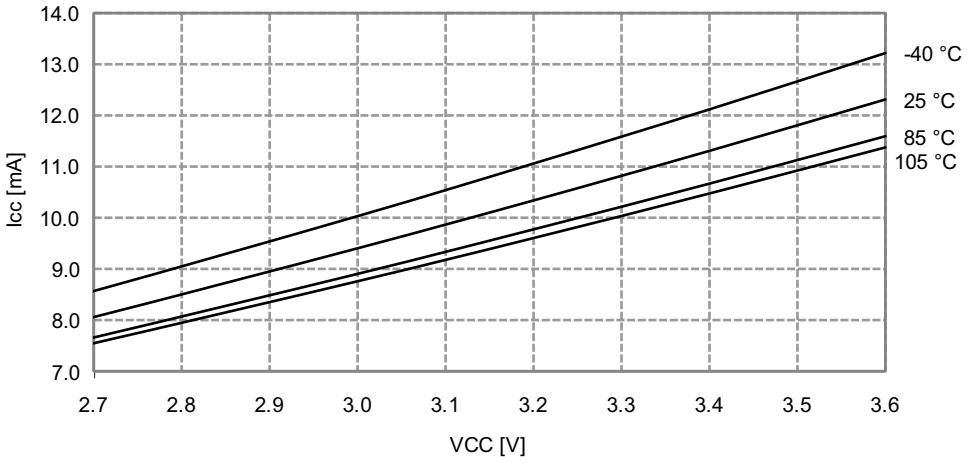


Figure 34-219. Active Mode Supply Current vs. V_{CC}

f_{SYS} = 32MHz internal oscillator



34.4.1.2 Idle Mode Supply Current

Figure 34-220. Idle Mode Supply Current vs. Frequency

f_{SYS} = 0 - 1MHz external clock, T = 25°C

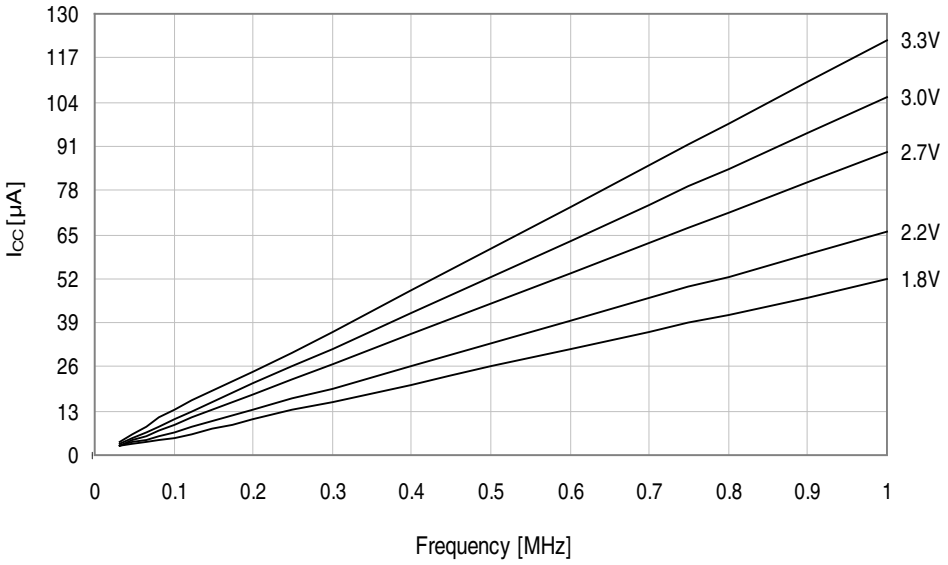


Figure 34-237. I/O Pin Output Voltage vs. Sink Current

V_{CC} = 3.0V

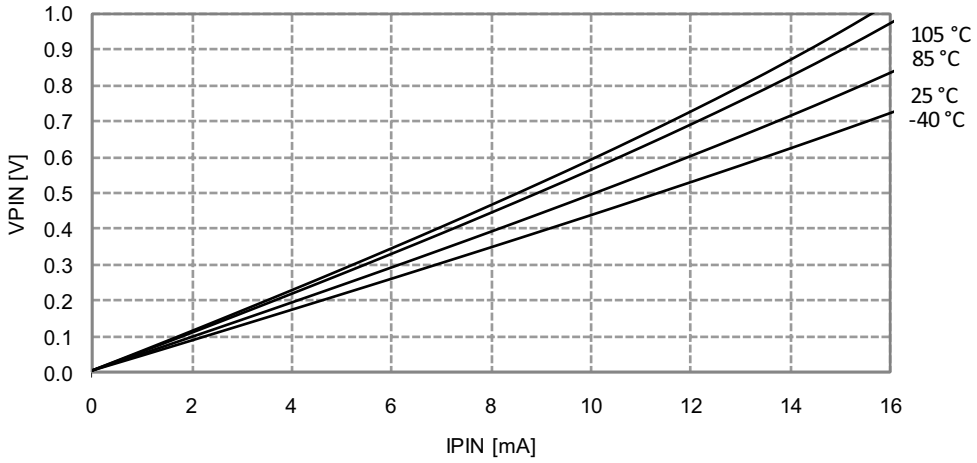


Figure 34-238. I/O Pin Output Voltage vs. Sink Current

V_{CC} = 3.3V

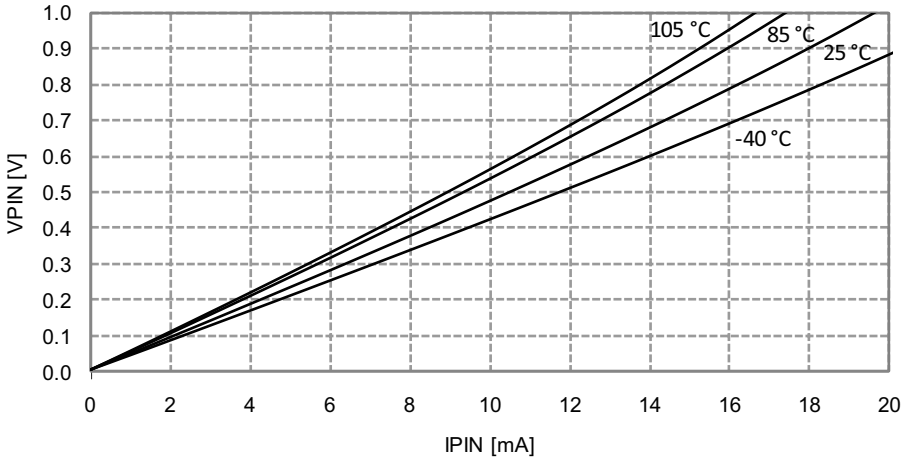


Figure 34-255. Analog Comparator Current Source vs. Calibration Value

V_{CC} = 3.0V

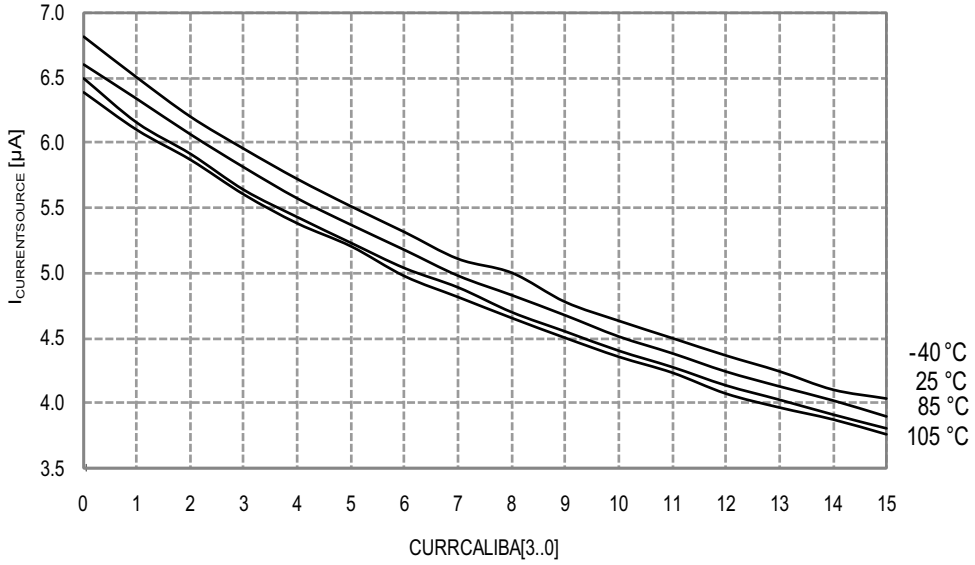


Figure 34-256. Voltage Scaler INL vs. SCALEFAC

T = 25°C, V_{CC} = 3.0V

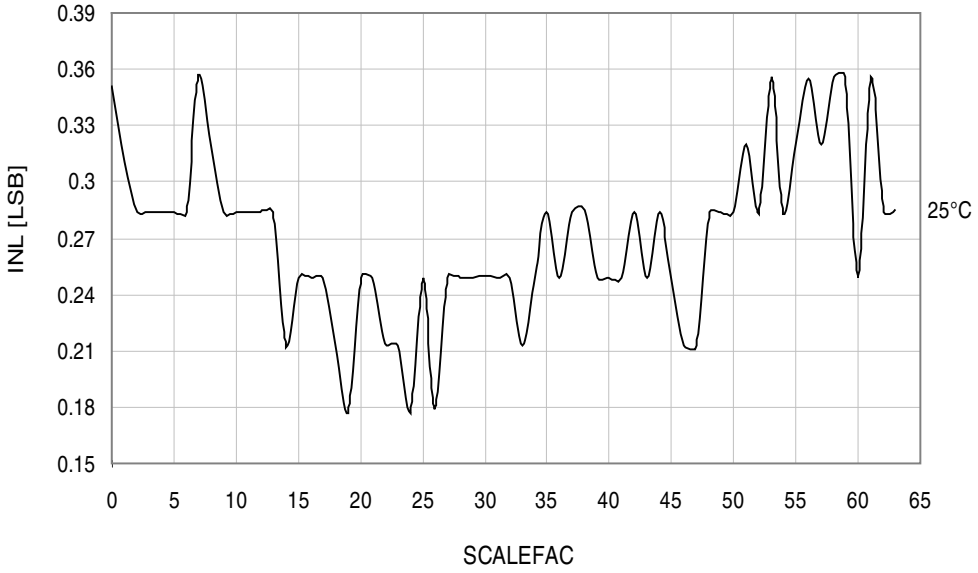


Figure 34-263. Reset Pin Pull-up Resistor Current vs. Reset Pin Voltage

V_{CC} = 3.3V

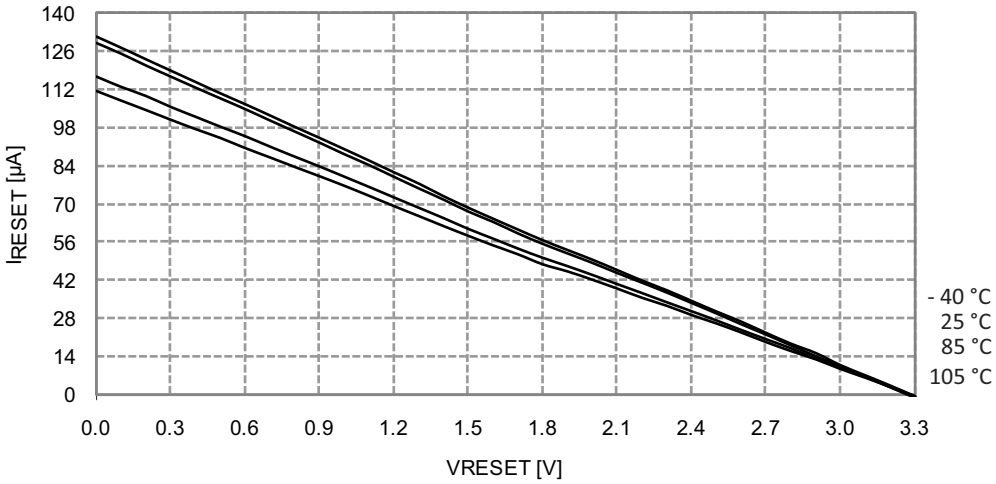
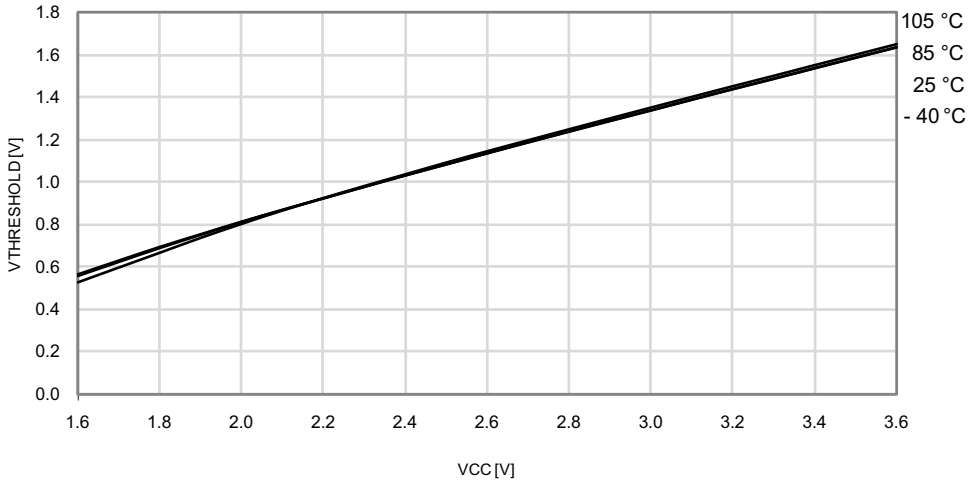


Figure 34-264. Reset Pin Input Threshold Voltage vs. V_{CC}

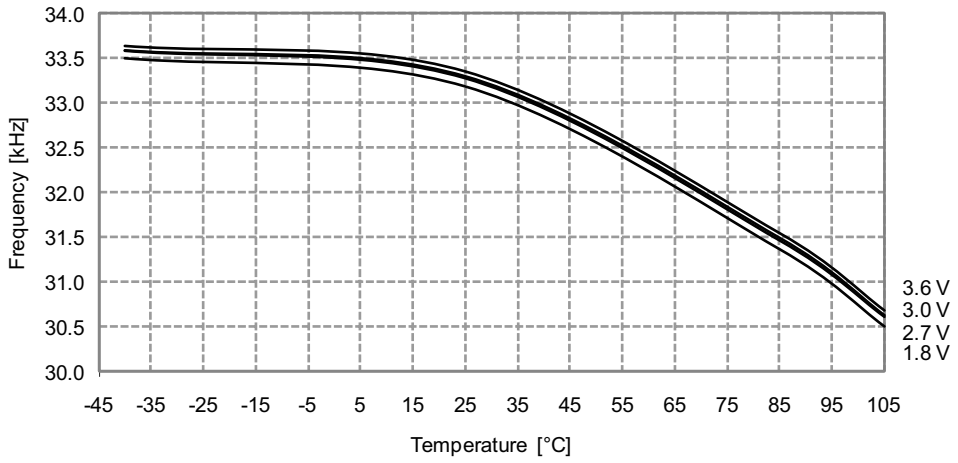
V_{IH} - Reset pin read as "1"



34.4.8 Oscillator Characteristics

34.4.8.1 Ultra Low-Power Internal Oscillator

Figure 34-265. Ultra Low-Power Internal Oscillator Frequency vs. Temperature



34.4.8.2 32.768kHz Internal Oscillator

Figure 34-266. 32.768kHz Internal Oscillator Frequency vs. Temperature

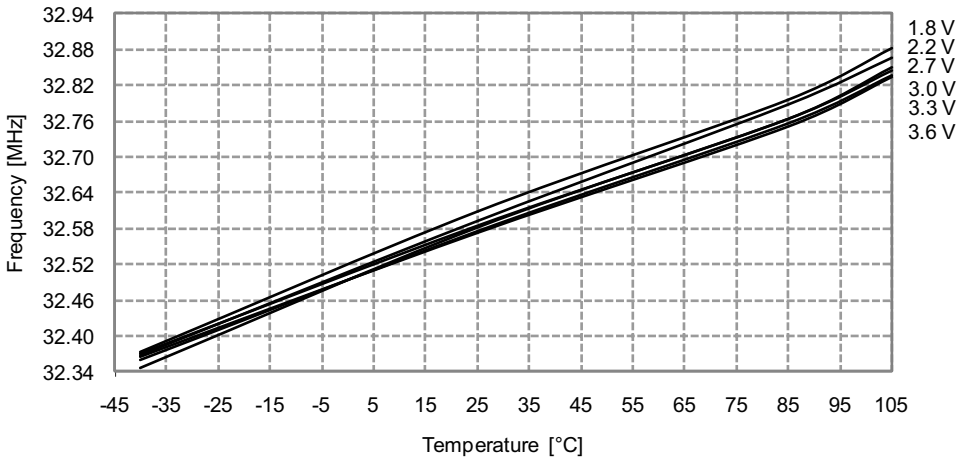


Figure 34-291. Idle Mode Supply Current vs. Frequency

f_{SYS} = 1 - 32MHz external clock, T = 25°C

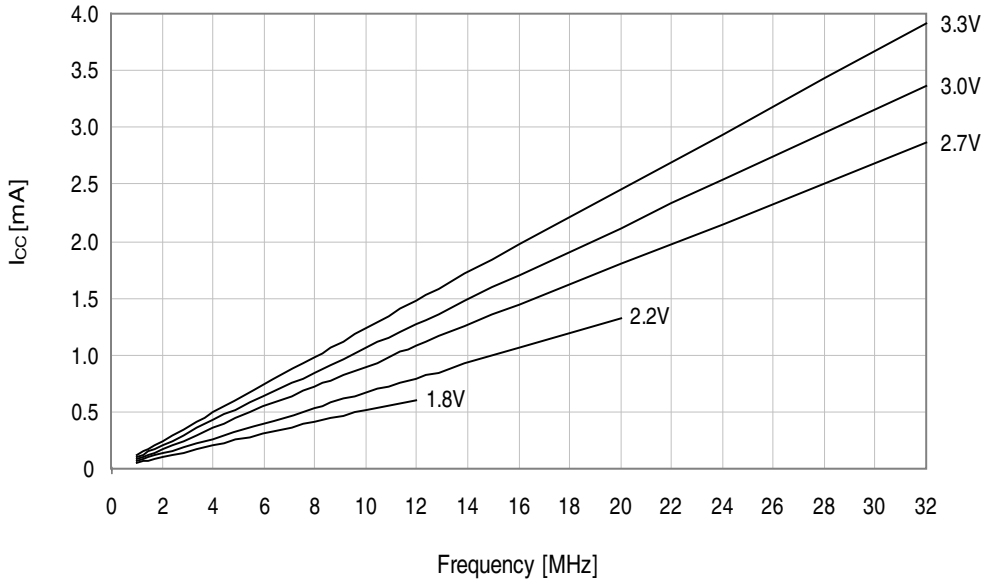
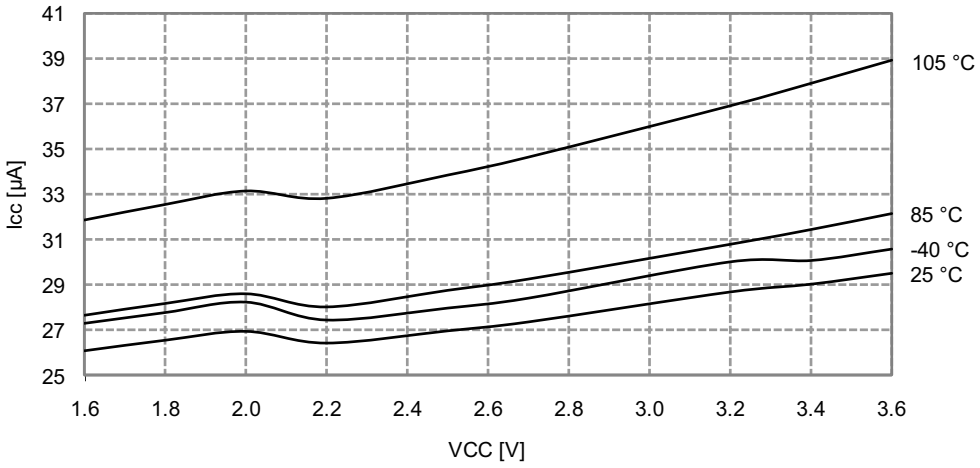


Figure 34-292. Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 32.768kHz internal oscillator



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Atmel Corporation 1600 Technology Drive, San Jose, CA 95110 USA **T:** (+1)(408) 441.0311 **F:** (+1)(408) 436.4200 | **www.atmel.com**