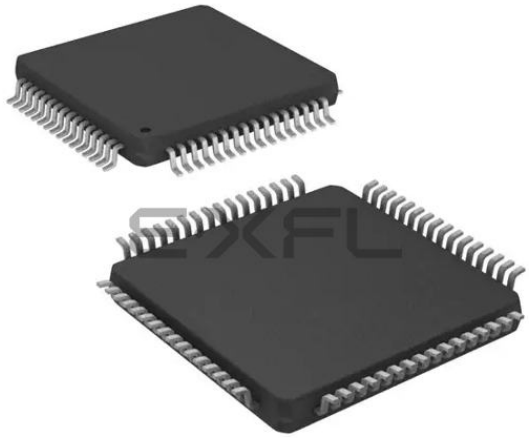

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	50
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega64c3-anr

The production signature row also contains an ID that identifies each microcontroller device type and a serial number for each manufactured device. The serial number consists of the production lot number, wafer number, and wafer coordinates for the device. The device ID for the available devices is shown in Table 7-1.

The production signature row cannot be written or erased, but it can be read from application software and external programmers.

Table 7-1. Device ID Bytes

Device	Device ID bytes		
	Byte 2	Byte 1	Byte 0
ATxmega32C3	49	95	1E
ATxmega64C3	49	96	1E
ATxmega128C3	52	97	1E
ATxmega192C3	51	97	1E
ATxmega256C3	46	98	1E

7.3.5 User Signature Row

The user signature row is a separate memory section that is fully accessible (read and write) from application software and external programmers. It is one flash page in size, and is meant for static user parameter storage, such as calibration data, custom serial number, identification numbers, random number seeds, etc. This section is not erased by chip erase commands that erase the flash, and requires a dedicated erase command. This ensures parameter storage during multiple program/erase operations and on-chip debug sessions.

7.4 Fuses and Lock Bits

The fuses are used to configure important system functions, and can only be written from an external programmer. The application software can read the fuses. The fuses are used to configure reset sources such as brownout detector and watchdog, and startup configuration.

The lock bits are used to set protection levels for the different flash sections (that is, if read and/or write access should be blocked). Lock bits can be written by external programmers and application software, but only to stricter protection levels. Chip erase is the only way to erase the lock bits. To ensure that flash contents are protected even during chip erase, the lock bits are erased after the rest of the flash memory has been erased.

An unprogrammed fuse or lock bit will have the value one, while a programmed fuse or lock bit will have the value zero.

Both fuses and lock bits are reprogrammable like the flash program memory.

7.5 Data Memory

The data memory contains the I/O memory, internal SRAM, optionally memory mapped EEPROM, and external memory if available. The data memory is organized as one continuous memory section, see Figure 7-2 on page 15. To simplify development, I/O Memory, EEPROM, and SRAM will always have the same start addresses for all Atmel AVR XMEGA devices.

16. TC2 – Timer/Counter Type 2

16.1 Features

- Eight eight-bit timer/counters
  - Four Low-byte timer/counter
  - Four High-byte timer/counter
- Up to eight compare channels in each Timer/Counter 2
  - Four compare channels for the low-byte timer/counter
  - Four compare channels for the high-byte timer/counter
- Waveform generation
  - Single slope pulse width modulation
- Timer underflow interrupts/events
- One compare match interrupt/event per compare channel for the low-byte timer/counter
- Can be used with the event system for count control

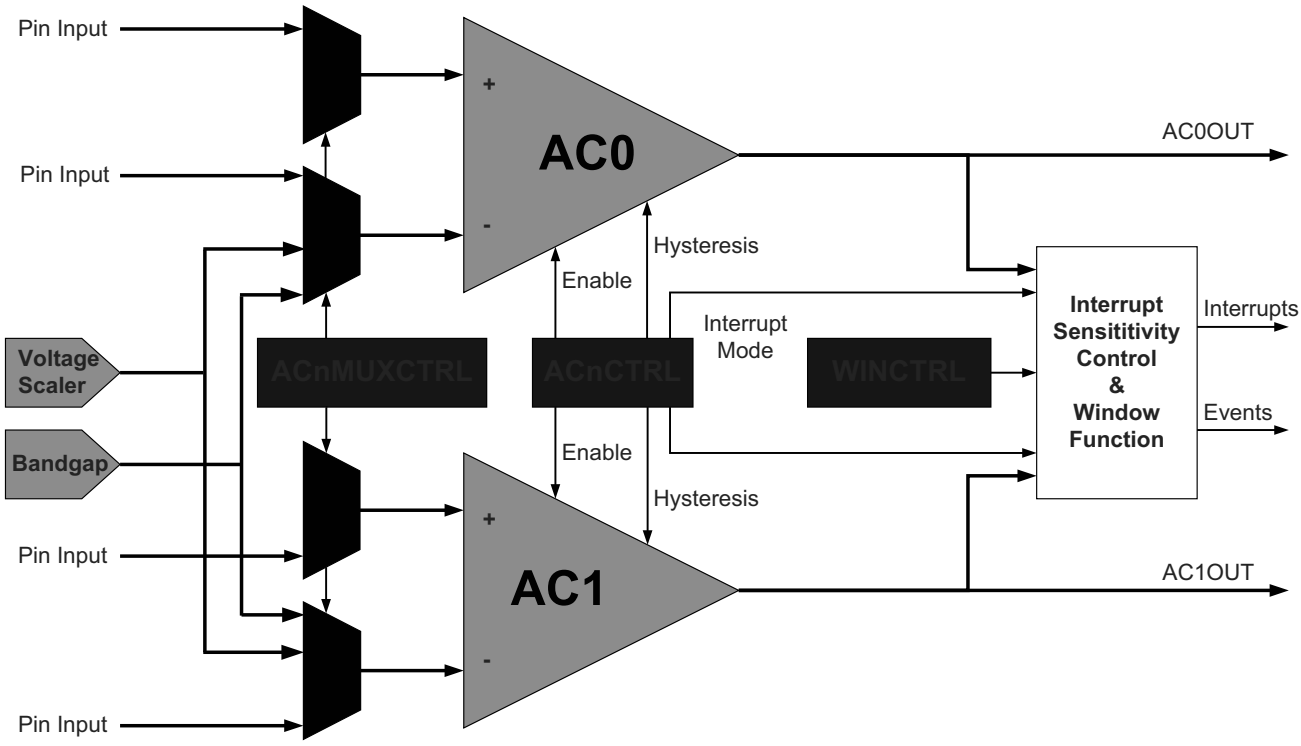
16.2 Overview

There are four Timer/Counter 2. These are realized when a Timer/Counter 0 is set in split mode. It is then a system of two eight-bit timer/counters, each with four compare channels. This results in eight configurable pulse width modulation (PWM) channels with individually controlled duty cycles, and is intended for applications that require a high number of PWM channels.

The two eight-bit timer/counters in this system are referred to as the low-byte timer/counter and high-byte timer/counter, respectively. The difference between them is that only the low-byte timer/counter can be used to generate compare match interrupts and events. The two eight-bit timer/counters have a shared clock source and separate period and compare settings. They can be clocked and timed from the peripheral clock, with optional prescaling, or from the event system. The counters are always counting down.

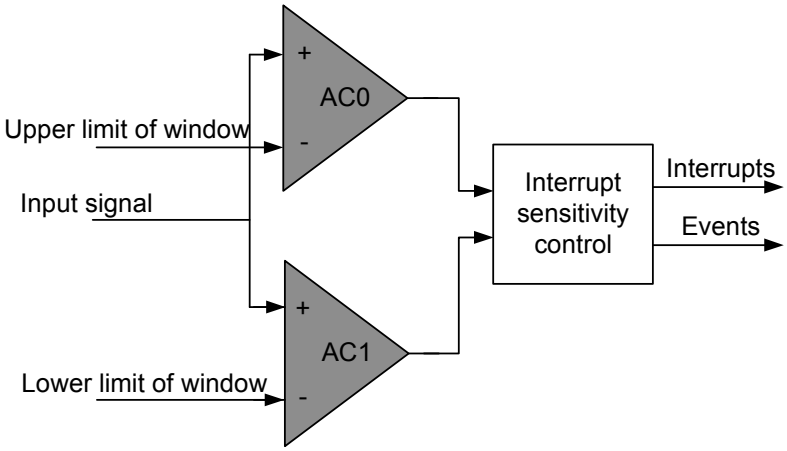
PORTC, PORTD, PORTE, and PORTF each has one Timer/Counter 2. Notation of these are TCC2 (Time/Counter C2), TCD2, TCE2, and TCF2, respectively.

Figure 27-1. Analog Comparator Overview



The window function is realized by connecting the external inputs of the two analog comparators in a pair as shown in Figure 27-2.

Figure 27-2. Analog Comparator Window Function



29.2 Alternate Pin Functions

The tables below show the primary/default function for each pin on a port in the first column, the pin number in the second column, and then all alternate pin functions in the remaining columns. The head row shows what peripheral that enable and use the alternate pin functions.

For better flexibility, some alternate functions also have selectable pin locations for their functions, this is noted under the first table where this apply.

Table 29-1. Port A - Alternate Functions

PORT A	PIN #	INTERRUPT	ADCA POS/ GAINPOS	ADCA NEG	ADCA GAINNEG	ACA POS	ACA NEG	ACA OUT	REFA
GND	60								
AVCC	61								
PA0	62	SYNC	ADC0	ADC0		AC0	AC0		AREFA
PA1	63	SYNC	ADC1	ADC1		AC1	AC1		
PA2	64	SYNC/ASYNC	ADC2	ADC2		AC2			
PA3	1	SYNC	ADC3	ADC3		AC3	AC3		
PA4	2	SYNC	ADC4		ADC4	AC4			
PA5	3	SYNC	ADC5		ADC5	AC5	AC5		
PA6	4	SYNC	ADC6		ADC6	AC6		AC1OUT	
PA7	5	SYNC	ADC7		ADC7		AC7	AC0OUT	

Table 29-2. Port B - Alternate Functions

PORT B	PIN #	INTERRUPT	ADCA POS	REFB
PB0	6	SYNC	ADC8	AREFB
PB1	6	SYNC	ADC9	
PB2	8	SYNC/ASYNC	ADC10	
PB3	9	SYNC	ADC11	
PB4	10	SYNC	ADC12	
PB5	11	SYNC	ADC13	
PB6	12	SYNC	ADC14	
PB7	13	SYNC	ADC15	
GND	14			
VCC	15			

33.2.13 Clock and Oscillator Characteristics

33.2.13.1 Calibrated 32.768kHz Internal Oscillator Characteristics

Table 33-48. 32.768kHz Internal Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency			32.768		kHz
	Factory calibration accuracy	T = 85°C, V_{CC} = 3.0V	-0.5		0.5	%
	User calibration accuracy		-0.5		0.5	

33.2.13.2 Calibrated 2MHz RC Internal Oscillator Characteristics

Table 33-49. 2MHz Internal Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	1.8	2.0	2.2	MHz
	Factory calibrated frequency			2.0		
	Factory calibration accuracy	T = 85°C, V_{CC}= 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	
	DFLL calibration stepsize			0.18		

33.2.13.3 Calibrated and Tunable 32MHz Internal Oscillator Characteristics

Table 33-50. 32MHz Internal Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	30	32	55	MHz
	Factory calibrated frequency			32		
	Factory calibration accuracy	T = 85°C, V_{CC}= 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	
	DFLL calibration step size			0.19		

33.2.13.4 32kHz Internal ULP Oscillator Characteristics

Table 33-51. 32kHz Internal ULP Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Factory calibrated frequency			32		kHz
	Factory calibration accuracy	T = 85°C, V_{CC}= 3.0V	-12		12	%
	Accuracy		-30		30	

Table 33-63. Current Consumption for Modules and Peripherals

Symbol	Parameter	Condition [1]		Min.	Typ.	Max.	Units
I_{CC}	ULP oscillator				0.9		µA
	32.768kHz int. oscillator				26		
	2MHz int. oscillator				79		
		DFLL enabled with 32.768kHz int. osc. as reference			110		
	32MHz int. oscillator				245		
		DFLL enabled with 32.768kHz int. osc. as reference			415		
	PLL	20x multiplication factor, 32MHz int. osc. DIV4 as reference			305		
	Watchdog timer				1.0		
	BOD	Continuous mode			138		
		Sampled mode, includes ULP oscillator			1.4		
	Internal 1.0V reference				185		
	Temperature sensor				173		
	ADC	16ksps V_{REF} = Ext. ref.			1.3		mA
			CURRLIMIT = LOW		1.15		
			CURRLIMIT = MEDIUM		1.0		
			CURRLIMIT = HIGH		0.9		
		75ksps V_{REF} = Ext. ref.	CURRLIMIT = LOW		1.7		
		300ksps V_{REF} = Ext. ref.			3.1		
	USART	Rx and Tx enabled, 9600 BAUD			7.5		µA
	Flash memory and EEPROM programming				4		mA

Note: 1. All parameters measured as the difference in current consumption between module enabled and disabled. All data at V_{CC} = 3.0V, Clk_{SYS} = 1MHz external clock without prescaling, T = 25°C unless other conditions are given.

The maximum CPU clock frequency depends on V_{CC}. As shown in Figure 33-22 the Frequency vs. V_{CC} curve is linear between $1.8V < V_{CC} < 2.7V$.

Figure 33-22.Maximum Frequency vs. V_{CC}

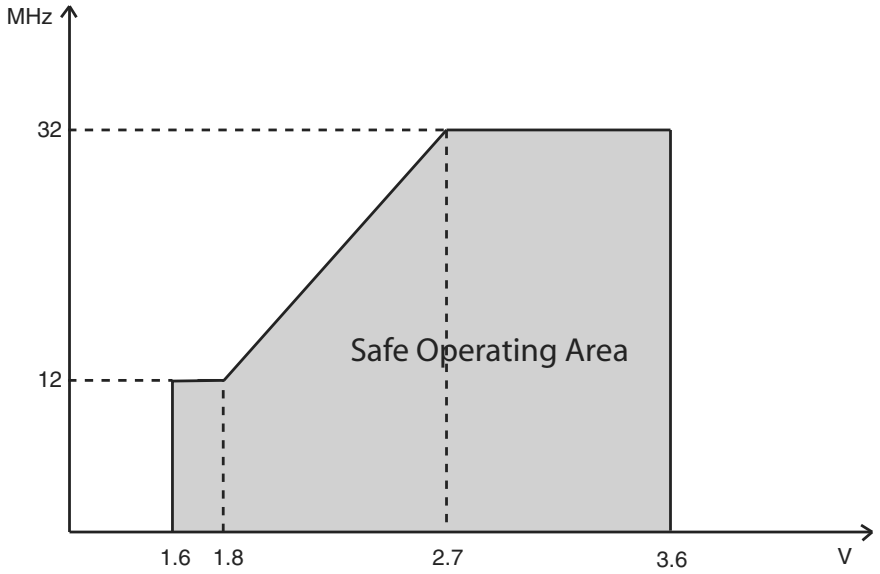


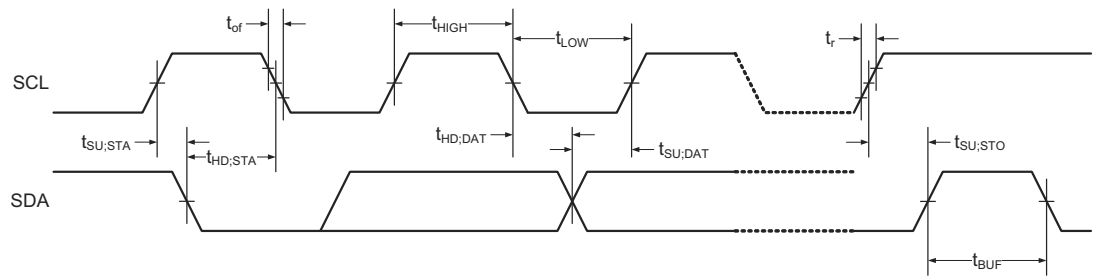
Table 33-115.SPI Timing Characteristics and Requirements

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_{SCK}	SCK period	Master		(See Table 20-3 in XMEGA C Manual)		ns
t_{SCKW}	SCK high/low width	Master		0.5*SCK		
t_{SCKR}	SCK rise time	Master		2.7		
t_{SCKF}	SCK fall time	Master		2.7		
t_{MIS}	MISO setup to SCK	Master		10		
t_{MIH}	MISO hold after SCK	Master		10		
t_{MOS}	MOSI setup SCK	Master		0.5*SCK		
t_{MOH}	MOSI hold after SCK	Master		1		
t_{SSCK}	Slave SCK period	Slave	4*t Clk_{PER}			
t_{SSCKW}	SCK high/low width	Slave	2*t Clk_{PER}			
t_{SSCKR}	SCK rise time	Slave			1600	
t_{SSCKF}	SCK fall time	Slave			1600	
t_{SIS}	MOSI setup to SCK	Slave	3			
t_{SIH}	MOSI hold after SCK	Slave	t Clk_{PER}			
t_{SSS}	$\overline{SS}$ setup to SCK	Slave	21			
t_{SSH}	$\overline{SS}$ hold after SCK	Slave	20			
t_{SOS}	MISO setup SCK	Slave		8		
t_{SOH}	MISO hold after SCK	Slave		13		
t_{SOSS}	MISO setup after $\overline{SS}$ low	Slave		11		
t_{SOSH}	MISO hold after $\overline{SS}$ high	Slave		8		

33.4.15 Two-Wire Interface Characteristics

Table 33-116 describes the requirements for devices connected to the Two-Wire Interface Bus. The Atmel AVR XMEGA Two-Wire Interface meets or exceeds these requirements under the noted conditions. Timing symbols refer to Figure 33-28.

Figure 33-28.Two-wire Interface Bus Timing



Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
R_Q	Negative impedance[1]	XOSCPWR=0, FRQRANGE=0	0.4MHz resonator, CL=100pF		44k		Ω
			1MHz crystal, CL=20pF		67k		
			2MHz crystal, CL=20pF		67k		
		XOSCPWR=0, FRQRANGE=1, CL=20pF	2MHz crystal		82k		
			8MHz crystal		1500		
			9MHz crystal		1500		
		XOSCPWR=0, FRQRANGE=2, CL=20pF	8MHz crystal		2700		
			9MHz crystal		2700		
			12MHz crystal		1000		
		XOSCPWR=0, FRQRANGE=3, CL=20pF	9MHz crystal		3600		
			12MHz crystal		1300		
			16MHz crystal		590		
		XOSCPWR=1, FRQRANGE=0, CL=20pF	9MHz crystal		390		
			12MHz crystal		50		
			16MHz crystal		10		
		XOSCPWR=1, FRQRANGE=1, CL=20pF	9MHz crystal		1500		
			12MHz crystal		650		
			16MHz crystal		270		
		XOSCPWR=1, FRQRANGE=2, CL=20pF	12MHz crystal		1000		
			16MHz crystal		440		
		XOSCPWR=1, FRQRANGE=3, CL=20pF	12MHz crystal		1300		
			16MHz crystal		590		
	ESR	SF = safety factor				min(R_Q)/SF	kΩ
	Startup time	XOSCPWR=0, FRQRANGE=0	0.4MHz resonator, CL=100pF		1.0		ms
		XOSCPWR=0, FRQRANGE=1	2MHz crystal, CL=20pF		2.6		
		XOSCPWR=0, FRQRANGE=2	8MHz crystal, CL=20pF		0.8		
		XOSCPWR=0, FRQRANGE=3	12MHz crystal, CL=20pF		1.0		
		XOSCPWR=1, FRQRANGE=3	16MHz crystal, CL=20pF		1.4		

Figure 34-11. Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 1MHz external clock

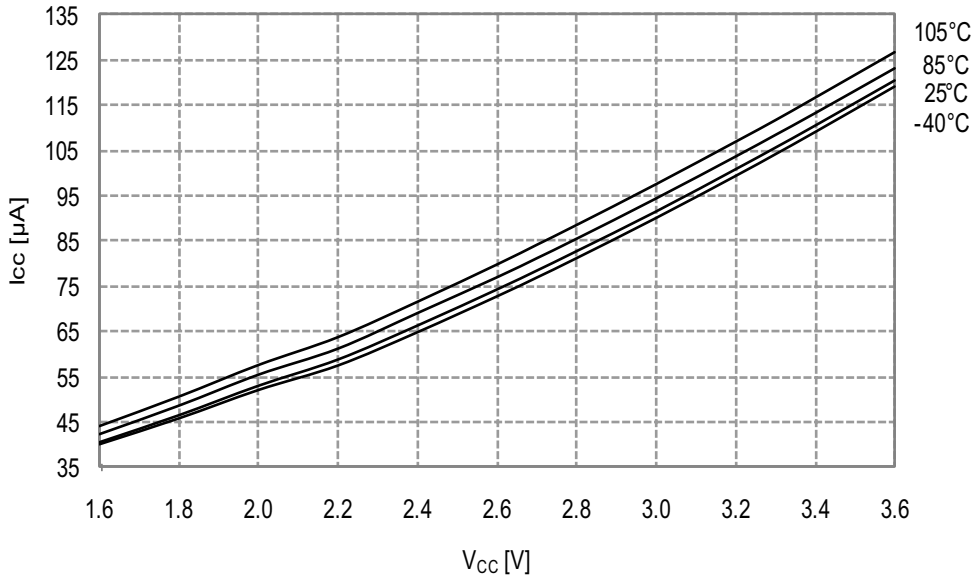


Figure 34-12. Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 2MHz internal oscillator

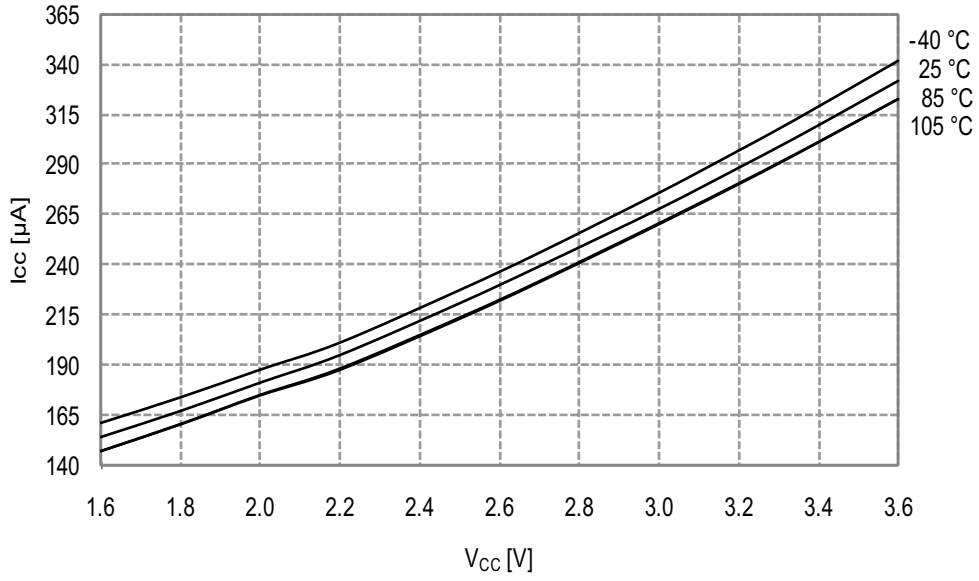
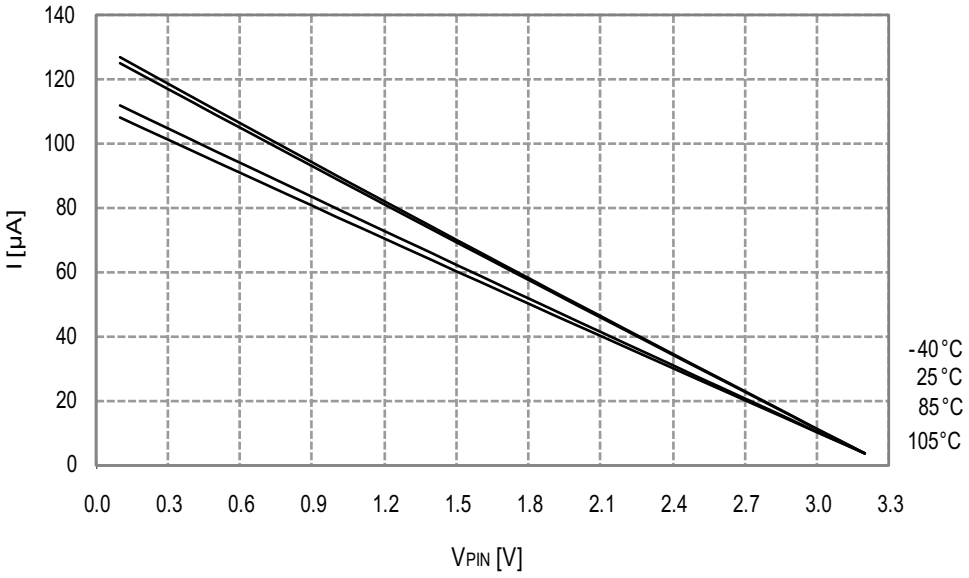


Figure 34-21. I/O Pin Pull-up Resistor Current vs. Input Voltage

V_{CC} = 3.3V



34.1.2.2 Output Voltage vs. Sink/Source Current

Figure 34-22. I/O Pin Output Voltage vs. Source Current

V_{CC} = 1.8V

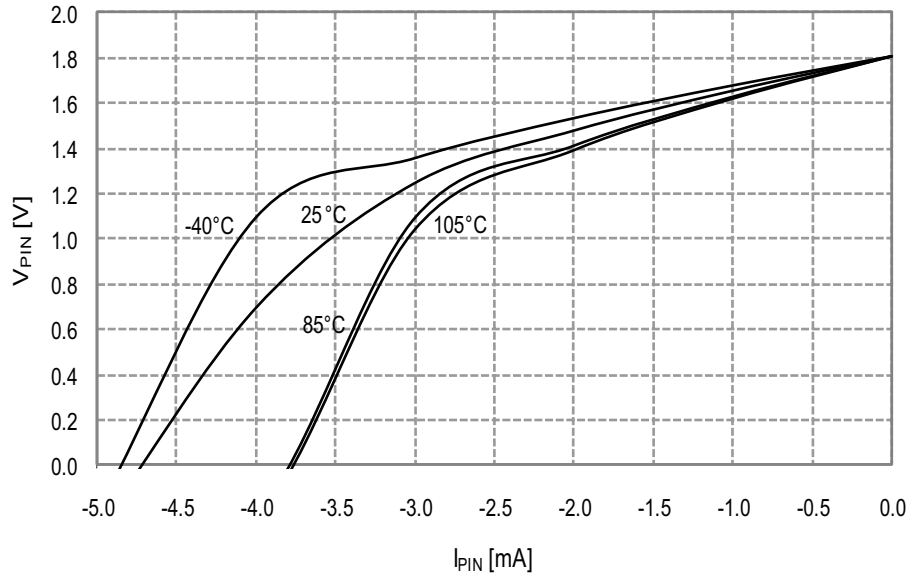
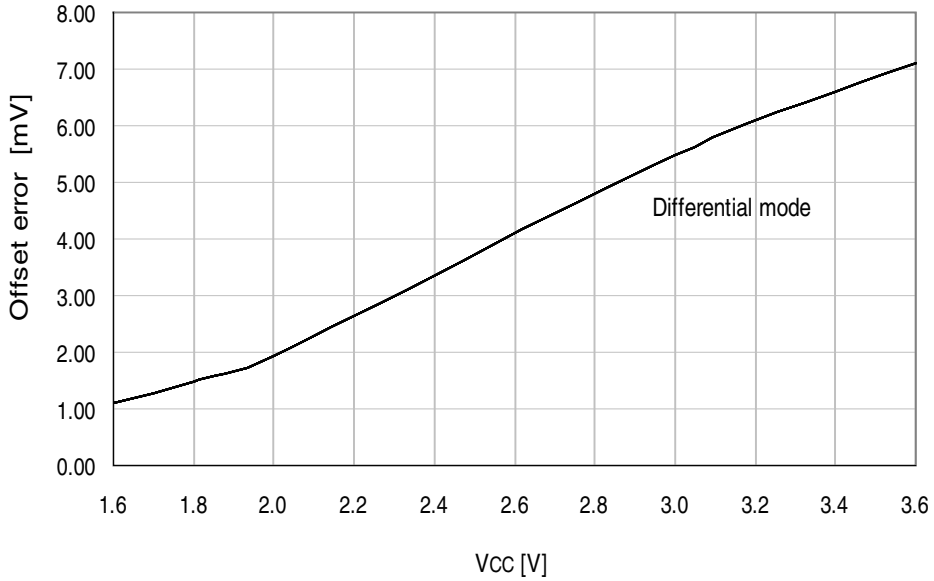


Figure 34-41. Offset Error vs. V_{CC}

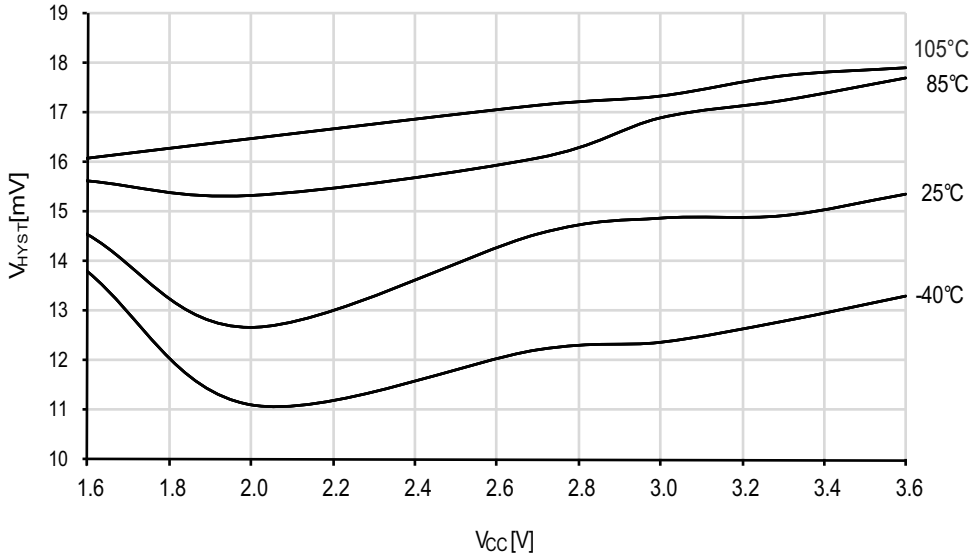
T = 25°C, V_{REF} = external 1.0V, ADC sample rate = 300ksps



34.1.4 Analog Comparator Characteristics

Figure 34-42. Analog Comparator Hysteresis vs. V_{CC}

Small hysteresis



34.3.2.3 Thresholds and Hysteresis

Figure 34-169. I/O Pin Input Threshold Voltage vs. V_{CC}

V_{IH} I/O pin read as "1"

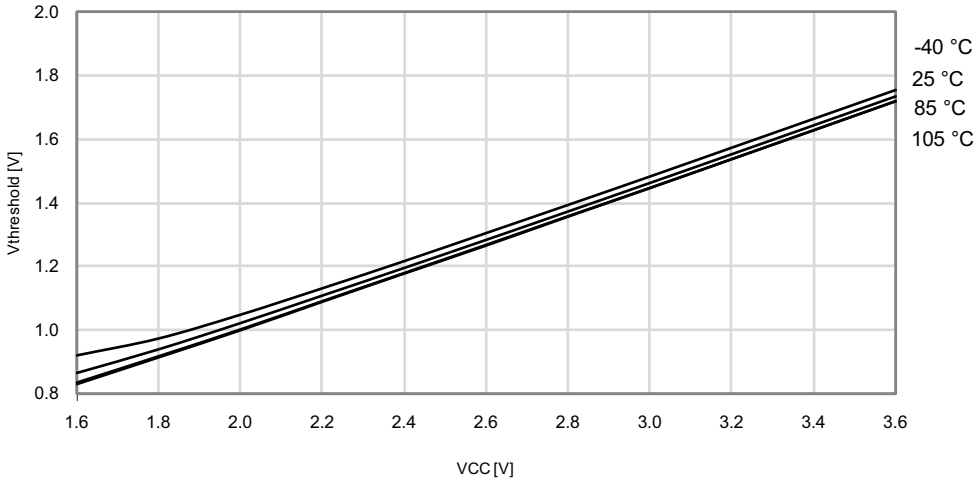


Figure 34-170. I/O Pin Input Threshold Voltage vs. V_{CC}

V_{IL} I/O pin read as "0"

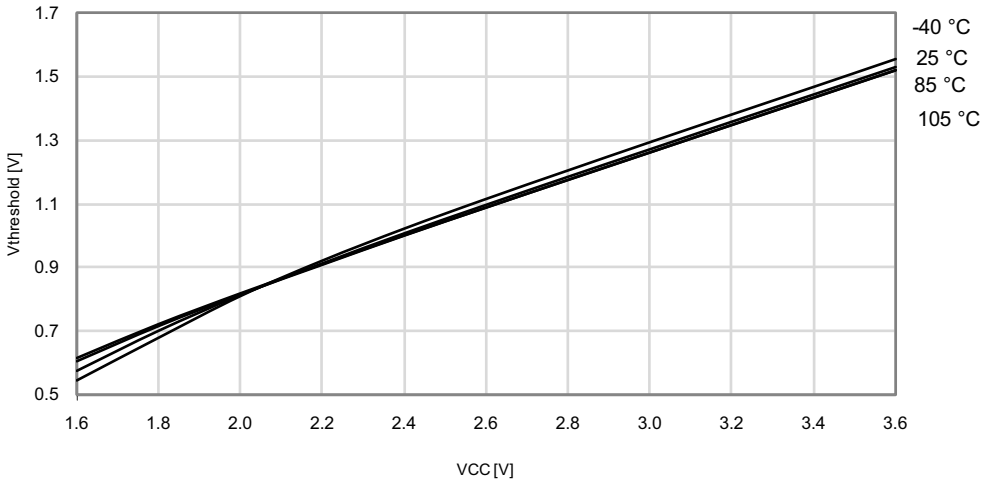


Figure 34-179. Gain Error vs. V_{CC}

T = 25°C, V_{REF} = external 1.0V, ADC sample rate = 300ksps

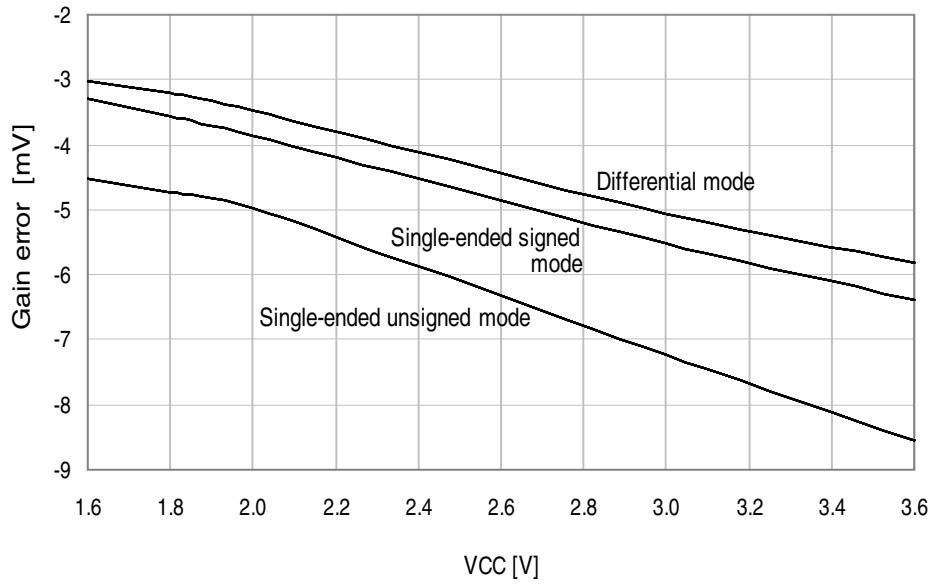


Figure 34-180. Offset Error vs. V_{REF}

T = 25°C, V_{CC} = 3.6V, ADC sample rate = 300ksps

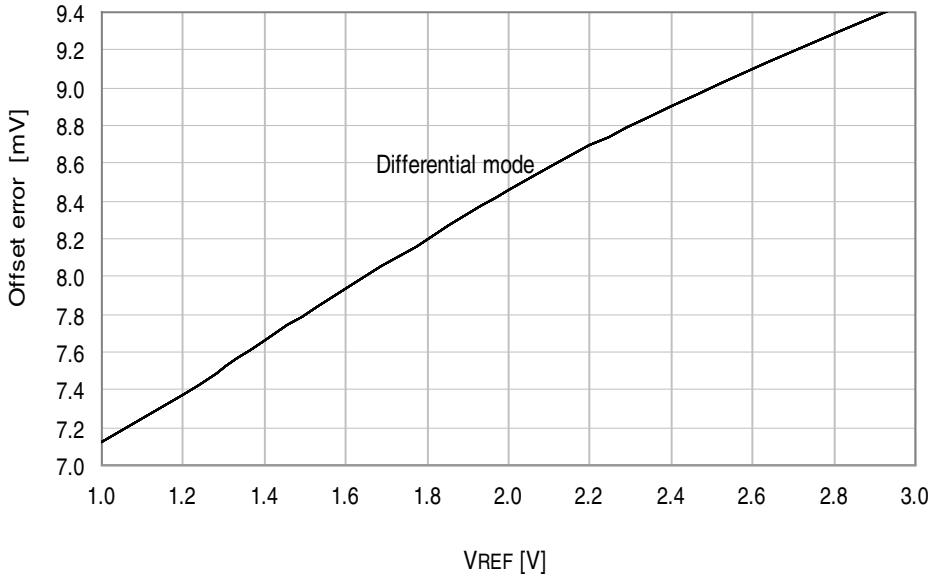


Figure 34-225. Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 32MHz internal oscillator prescaled to 8MHz

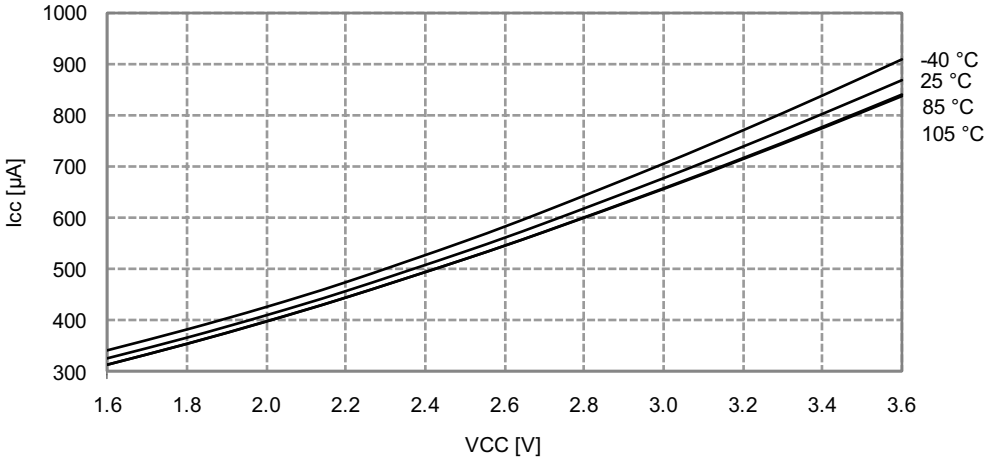


Figure 34-226. Idle Mode Current vs. V_{CC}

f_{SYS} = 32MHz internal oscillator

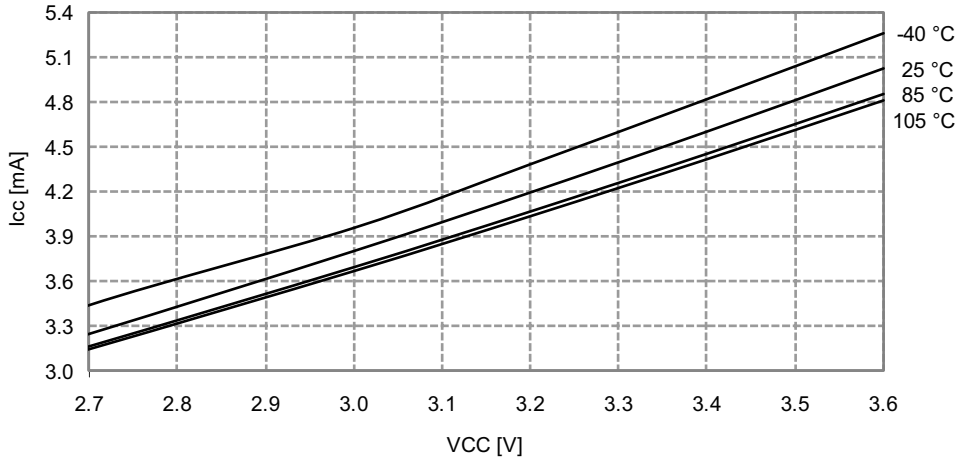


Figure 34-235. I/O Pin Output Voltage vs. Source Current

V_{CC} = 3.3V

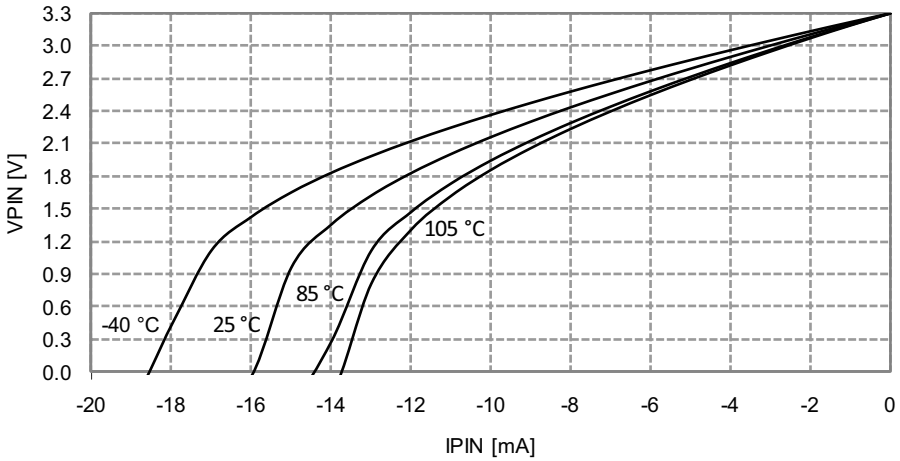


Figure 34-236. I/O Pin Output Voltage vs. Sink Current

V_{CC} = 1.8V

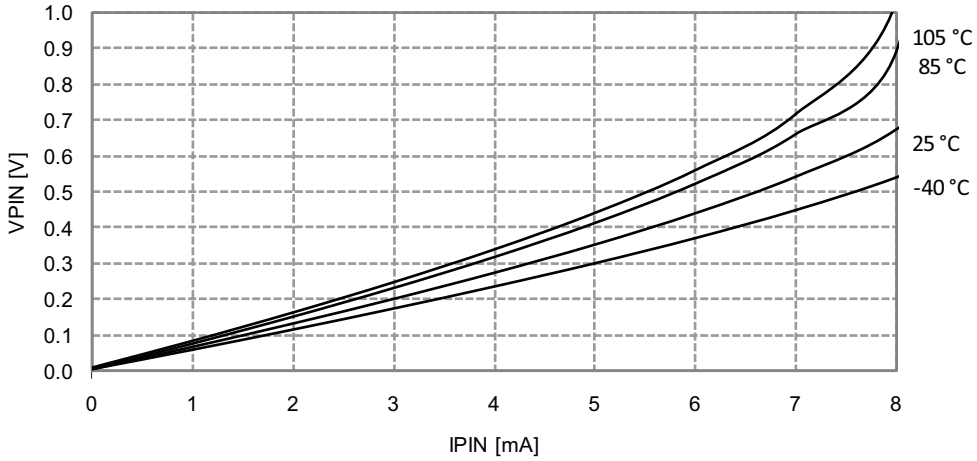
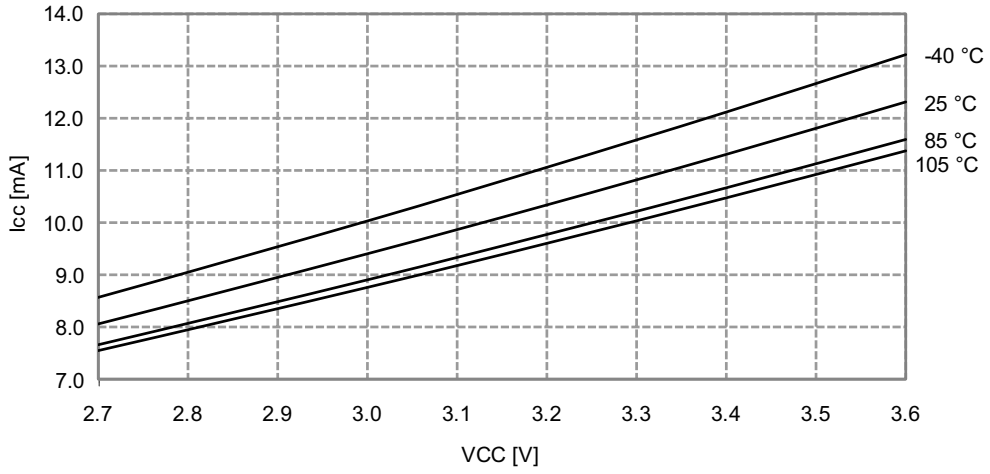


Figure 34-289. Active Mode Supply Current vs. V_{CC}

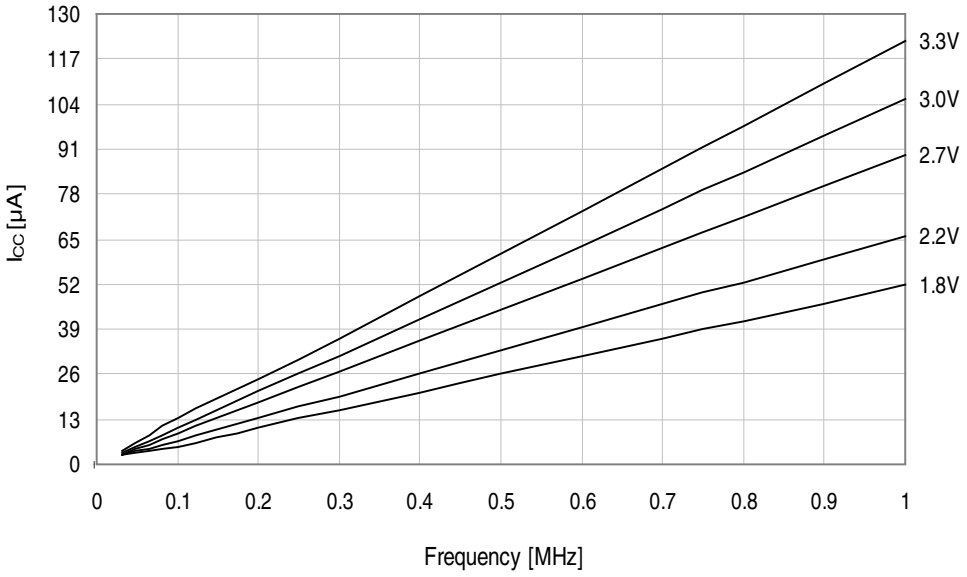
f_{SYS} = 32MHz internal oscillator



34.5.1.2 Idle Mode Supply Current

Figure 34-290. Idle Mode Supply Current vs. Frequency

f_{SYS} = 0 - 1MHz external clock, T = 25°C



34.5.2.2 Output Voltage vs. Sink/Source Current

Figure 34-303. I/O Pin Output Voltage vs. Source Current

V_{CC} = 1.8V

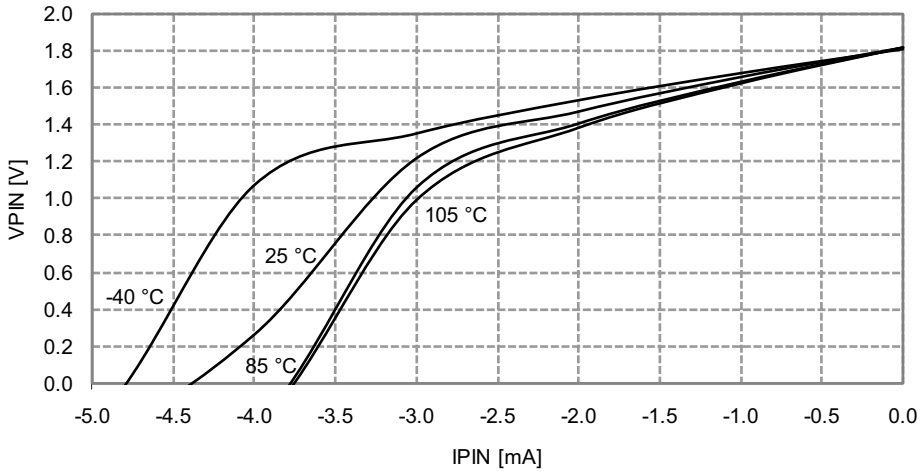


Figure 34-304. I/O Pin Output Voltage vs. Source Current

V_{CC} = 3.0V

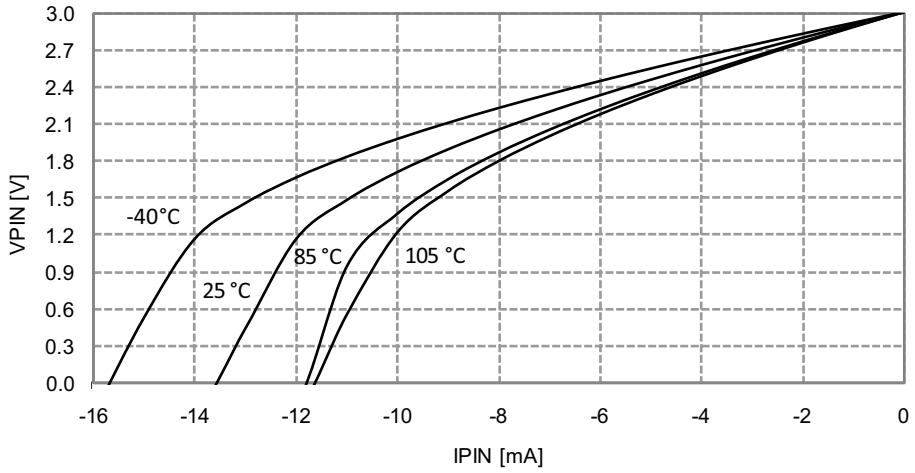


Figure 34-319. Gain Error vs. V_{CC}

T = 25°C, V_{REF} = external 1.0V, ADC sample rate = 300ksps

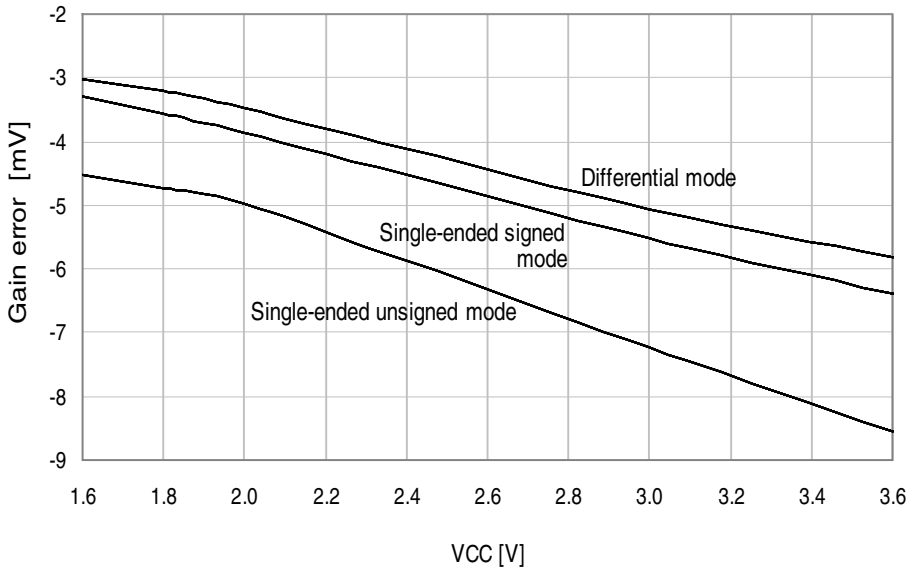


Figure 34-320. Offset Error vs. V_{REF}

T = 25°C, V_{CC} = 3.6V, ADC sample rate = 300ksps

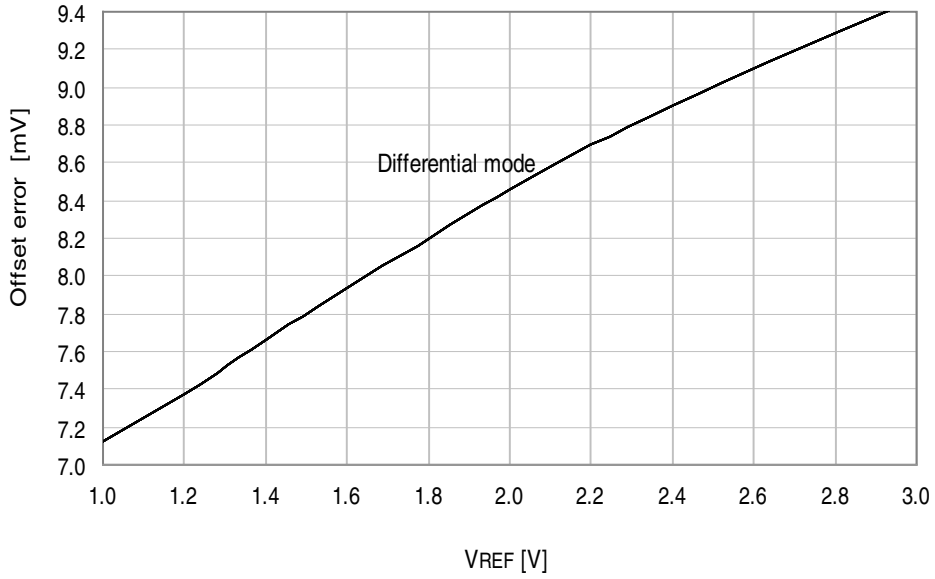


Figure 34-325. Analog Comparator Current Source vs. Calibration Value

V_{CC} = 3.0V

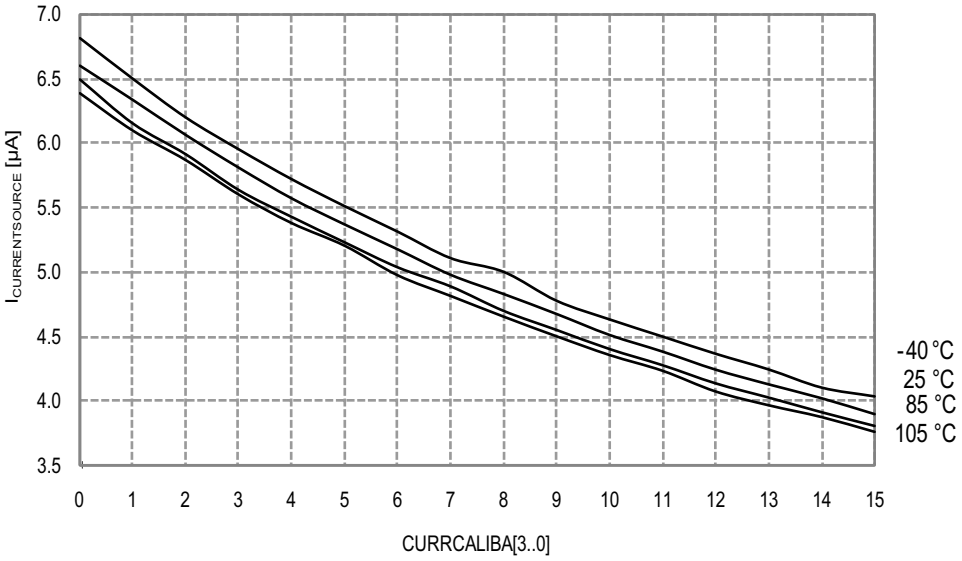


Figure 34-326. Voltage Scaler INL vs. SCALEFAC

T = 25°C, V_{CC} = 3.0V