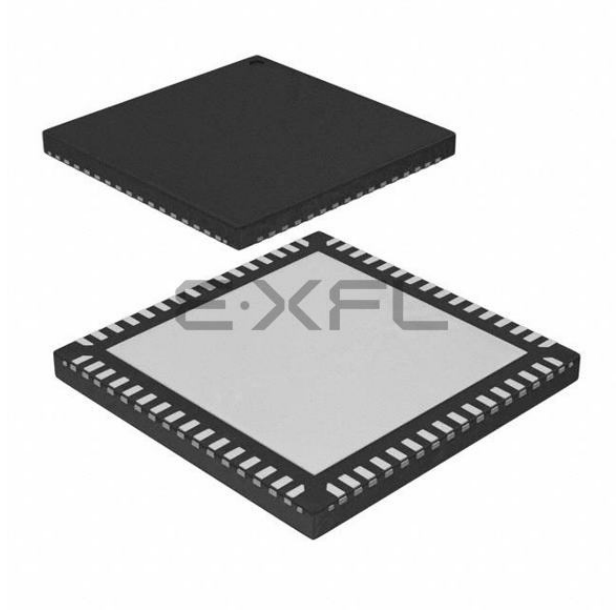


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	50
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega64c3-mn

3. Overview

The Atmel AVR XMEGA is a family of low power, high performance, and peripheral rich 8/16-bit microcontrollers based on the AVR enhanced RISC architecture. By executing instructions in a single clock cycle, the AVR XMEGA devices achieve CPU throughput approaching one million instructions per second (MIPS) per megahertz, allowing the system designer to optimize power consumption versus processing speed.

The AVR CPU combines a rich instruction set with 32 general purpose working registers. All 32 registers are directly connected to the arithmetic logic unit (ALU), allowing two independent registers to be accessed in a single instruction, executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs many times faster than conventional single-accumulator or CISC based microcontrollers.

The XMEGA C3 devices provide the following features: in-system programmable flash with read-while-write capabilities; internal EEPROM and SRAM; four-channel event system and programmable multilevel interrupt controller, 50 general purpose I/O lines, 16-bit real-time counter (RTC); five, 16-bit timer/counters with compare and PWM channels; three USARTs; two two-wire serial interfaces (TWIs); one full speed USB 2.0 interface; two serial peripheral interfaces (SPIs); one sixteen-channel, 12-bit ADC with programmable gain; two analog comparators (ACs) with window mode; programmable watchdog timer with separate internal oscillator; accurate internal oscillators with PLL and prescaler; and programmable brown-out detection.

The program and debug interface (PDI), a fast, two-pin interface for programming and debugging, is available.

The XMEGA C3 devices have five software selectable power saving modes. The idle mode stops the CPU while allowing the SRAM, event system, interrupt controller, and all peripherals to continue functioning. The power-down mode saves the SRAM and register contents, but stops the oscillators, disabling all other functions until the next TWI, USB resume, or pin-change interrupt, or reset. In power-save mode, the asynchronous real-time counter continues to run, allowing the application to maintain a timer base while the rest of the device is sleeping. In standby mode, the external crystal oscillator keeps running while the rest of the device is sleeping. This allows very fast startup from the external crystal, combined with low power consumption. In extended standby mode, both the main oscillator and the asynchronous timer continue to run. To further reduce power consumption, the peripheral clock to each individual peripheral can optionally be stopped in active mode and idle sleep mode.

Atmel offers a free QTouch library for embedding capacitive touch buttons, sliders and wheels functionality into AVR microcontrollers.

The devices are manufactured using Atmel high-density, nonvolatile memory technology. The program flash memory can be reprogrammed in-system through the PDI. A boot loader running in the device can use any interface to download the application program to the flash memory. The boot loader software in the boot flash section will continue to run while the application flash section is updated, providing true read-while-write operation. By combining an 8/16-bit RISC CPU with in-system, self-programmable flash, the AVR XMEGA is a powerful microcontroller family that provides a highly flexible and cost effective solution for many embedded applications.

All Atmel AVR XMEGA devices are supported with a full suite of program and system development tools, including: C compilers, macro assemblers, program debugger/simulators, programmers, and evaluation kits.

Mnemonics	Operands	Description	Operation	Flags	#Clocks
SEN		Set Negative Flag	N ← 1	N	1
CLN		Clear Negative Flag	N ← 0	N	1
SEZ		Set Zero Flag	Z ← 1	Z	1
CLZ		Clear Zero Flag	Z ← 0	Z	1
SEI		Global Interrupt Enable	I ← 1	I	1
CLI		Global Interrupt Disable	I ← 0	I	1
SES		Set Signed Test Flag	S ← 1	S	1
CLS		Clear Signed Test Flag	S ← 0	S	1
SEV		Set Two’s Complement Overflow	V ← 1	V	1
CLV		Clear Two’s Complement Overflow	V ← 0	V	1
SET		Set T in SREG	T ← 1	T	1
CLT		Clear T in SREG	T ← 0	T	1
SEH		Set Half Carry Flag in SREG	H ← 1	H	1
CLH		Clear Half Carry Flag in SREG	H ← 0	H	1
MCU control instructions					
BREAK		Break	(See specific descr. for BREAK)	None	1
NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep)	None	1
WDR		Watchdog Reset	(see specific descr. for WDR)	None	1

Notes: 1. One extra cycle must be added when accessing internal SRAM.

33.2.13.5 Internal Phase Locked Loop (PLL) Characteristics

Table 33-52. Internal PLL Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{IN}	Input frequency	Output frequency must be within f_{OUT}	0.4		64	MHz
f_{OUT}	Output frequency (1)	V_{CC}= 1.6 - 1.8V	20		48	
		V_{CC}= 2.7 - 3.6V	20		128	
	Start-up time			25		µs
	Re-lock time			25		

Note: 1. The maximum output frequency vs. supply voltage is linear between 1.8V and 2.7V, and can never be higher than four times the maximum CPU frequency.

33.2.13.6 External Clock Characteristics

Figure 33-10.External Clock Drive Waveform

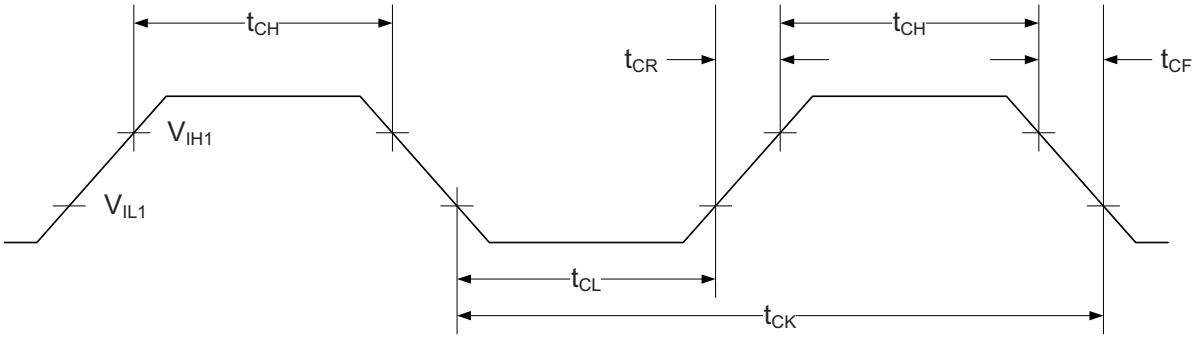


Table 33-53. External Clock used as System Clock without Prescaling

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock Frequency (1)	V_{CC} = 1.6 - 1.8V	0		12	MHz
		V_{CC} = 2.7 - 3.6V	0		32	
t_{CK}	Clock Period	V_{CC} = 1.6 - 1.8V	83.3			ns
		V_{CC} = 2.7 - 3.6V	31.5			
t_{CH}	Clock High Time	V_{CC} = 1.6 - 1.8V	30.0			
		V_{CC} = 2.7 - 3.6V	12.5			
t_{CL}	Clock Low Time	V_{CC} = 1.6 - 1.8V	30.0			
		V_{CC} = 2.7 - 3.6V	12.5			
t_{CR}	Rise Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			10	
		V_{CC} = 2.7 - 3.6V			3	
t_{CF}	Fall Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			10	
		V_{CC} = 2.7 - 3.6V			3	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Note: 1. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

33.4.3 Current Consumption

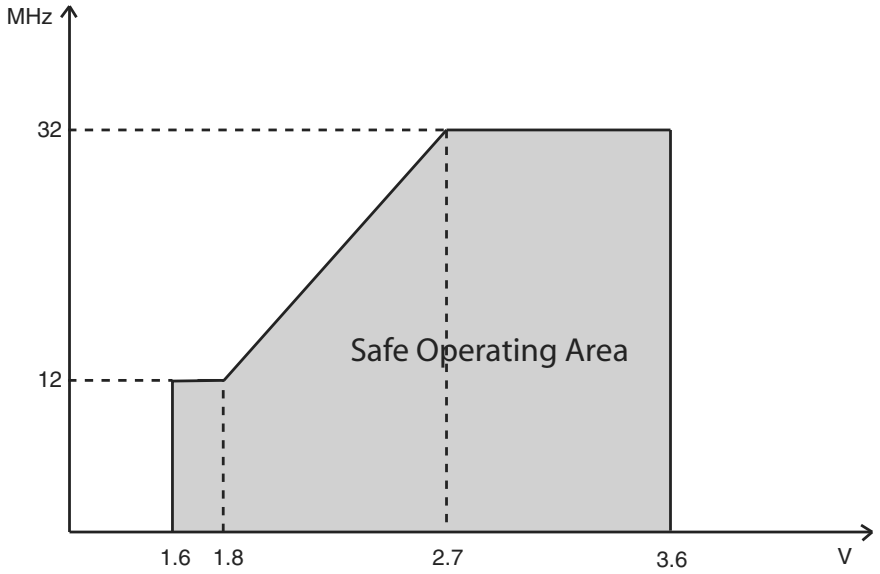
Table 33-91. Current Consumption for Active Mode and Sleep Mode

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{CC}	Active power consumption(1)	32kHz, Ext. Clk	V_{CC} = 1.8V		60		µA
			V_{CC} = 3.0V		140		
		1MHz, Ext. Clk	V_{CC} = 1.8V		245		
			V_{CC} = 3.0V		550		
		2MHz, Ext. Clk	V_{CC} = 1.8V		440	700	
			V_{CC} = 3.0V		0.9	1.5	mA
		32MHz, Ext. Clk			9.0	15	
	Idle power consumption(2)	32kHz, Ext. Clk	V_{CC} = 1.8V		3.0		µA
			V_{CC} = 3.0V		3.5		
		1MHz, Ext. Clk	V_{CC} = 1.8V		55		
			V_{CC} = 3.0V		110		
		2MHz, Ext. Clk	V_{CC} = 1.8V		105	350	
			V_{CC} = 3.0V		215	650	
		32MHz, Ext. Clk			3.4	8.0	mA
	Power-down power consumption	T = 25°C	V_{CC} = 3.0V		0.1	1.0	µA
		T = 85°C			3.5	6.0	
		T = 105°C			10.0	15	
		WDT and sampled BOD enabled, T = 25°C	V_{CC} = 3.0V		1.5	2.0	
		WDT and sampled BOD enabled, T = 85°C			5.8	10	
		WDT and sampled BOD enabled, T = 105°C			12	20	
	Power-save power consumption(3)	RTC from ULP clock, WDT and sampled BOD enabled, T = 25°C	V_{CC} = 1.8V		1.3		
			V_{CC} = 3.0V		1.4		
		RTC from 1.024kHz low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.7	2.0	
			V_{CC} = 3.0V		0.8	2.0	
		RTC from low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.9	3.0	
			V_{CC} = 3.0V		1.1	3.0	
	Reset power consumption	Current through $\overline{\text{RESET}}$ pin substracted	V_{CC} = 3.0V		170		

Notes:
1. All Power Reduction Registers set including FPRM and EPRM.
2. All Power Reduction Registers set without FPRM and EPRM.
3. Maximum limits are based on characterization, and not tested in production.

The maximum CPU clock frequency depends on V_{CC}. As shown in Figure 33-29 the Frequency vs. V_{CC} curve is linear between 1.8V < V_{CC} < 2.7V.

Figure 33-29.Maximum Frequency vs. V_{CC}



33.5.6 ADC Characteristics

Table 33-124. Power Supply, Reference, and Input Range

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
AV_{CC}	Analog supply voltage		V_{CC}- 0.3		V_{CC}+ 0.3	V
V_{REF}	Reference voltage		1		AV_{CC}- 0.6	
R_{in}	Input resistance	Switched			4.5	kΩ
C_{in}	Input capacitance	Switched			5	pF
R_{AREF}	Reference input resistance	(leakage only)		>10		MΩ
C_{AREF}	Reference input capacitance	Static load		7		pF
Vin	Input range		0		V_{REF}	V
	Conversion range	Differential mode, Vinp - Vinn	$-V_{REF}$		V_{REF}	
	Conversion range	Single ended unsigned mode, Vinp	-ΔV		V_{REF}-ΔV	
ΔV	Fixed offset voltage			200		lsb

Table 33-125.Clock and Timing

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{ADC}	ADC Clock frequency	Maximum is 1/4 of peripheral clock frequency	100		1800	kHz
		Measuring internal signals	100		125	
f_{ClkADC}	Sample rate		16		300	ksps
f_{ADC}	Sample rate	Current limitation (CURRLIMIT) off	16		300	
		CURRLIMIT = LOW	16		250	
		CURRLIMIT = MEDIUM	16		150	
		CURRLIMIT = HIGH	16		50	
	Sampling time	Configurable in steps of 1/2 Clk_{ADC} cycles up to 32 Clk_{ADC} cycles	0.28		320	µs
	Conversion time (latency)	(RES+2)/2+1+ GAIN RES (Resolution) = 8 or 12, GAIN=0 to 3	5.5		10	Clk_{ADC} cycles
	Start-up time	ADC clock cycles		12	24	
	ADC settling time	After changing reference or input mode		7	7	

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
R_Q	Negative impedance[1]	XOSCPWR=0, FRQRANGE=0	0.4MHz resonator, CL=100pF		44k		Ω
			1MHz crystal, CL=20pF		67k		
			2MHz crystal, CL=20pF		67k		
		XOSCPWR=0, FRQRANGE=1, CL=20pF	2MHz crystal		82k		
			8MHz crystal		1500		
			9MHz crystal		1500		
		XOSCPWR=0, FRQRANGE=2, CL=20pF	8MHz crystal		2700		
			9MHz crystal		2700		
			12MHz crystal		1000		
		XOSCPWR=0, FRQRANGE=3, CL=20pF	9MHz crystal		3600		
			12MHz crystal		1300		
			16MHz crystal		590		
		XOSCPWR=1, FRQRANGE=0, CL=20pF	9MHz crystal		390		
			12MHz crystal		50		
			16MHz crystal		10		
		XOSCPWR=1, FRQRANGE=1, CL=20pF	9MHz crystal		1500		
			12MHz crystal		650		
			16MHz crystal		270		
		XOSCPWR=1, FRQRANGE=2, CL=20pF	12MHz crystal		1000		
			16MHz crystal		440		
		XOSCPWR=1, FRQRANGE=3, CL=20pF	12MHz crystal		1300		
			16MHz crystal		590		
	ESR	SF = safety factor				min(R_Q)/SF	kΩ
	Startup time	XOSCPWR=0, FRQRANGE=0	0.4MHz resonator, CL=100pF		1.0		ms
		XOSCPWR=0, FRQRANGE=1	2MHz crystal, CL=20pF		2.6		
		XOSCPWR=0, FRQRANGE=2	8MHz crystal, CL=20pF		0.8		
		XOSCPWR=0, FRQRANGE=3	12MHz crystal, CL=20pF		1.0		
		XOSCPWR=1, FRQRANGE=3	16MHz crystal, CL=20pF		1.4		

Table 33-145.Two-wire Interface Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input high voltage		0.7*V_{CC}		V_{CC}+0.5	V
V_{IL}	Input low voltage		-0.5		0.3*V_{CC}	
V_{hys}	Hysteresis of Schmitt trigger inputs		0.05V_{CC} (1)			
V_{OL}	Output low voltage	3mA, sink current	0		0.4	
t_r	Rise time for both SDA and SCL		20+0.1C_b (1)(2)		300	ns
t_{of}	Output fall time from V_{IHmin} to V_{ILmax}	10pF < C_b < 400pF (2)	20+0.1C_b (1)(2)		250	
t_{SP}	Spikes suppressed by input filter		0		50	
I_I	Input current for each I/O Pin	0.1V_{CC} < V_I < 0.9V_{CC}	-10		10	µA
C_I	Capacitance for each I/O Pin				10	pF
f_{SCL}	SCL clock frequency	f_{PER} (3) >max(10f_{SCL}, 250kHz)	0		400	kHz
R_P	Value of pull-up resistor	f_{SCL} ≤ 100kHz	$\frac{V_{CC}-0.4V}{3mA}$		$\frac{100ns}{C_b}$	Ω
		f_{SCL} > 100kHz			$\frac{300ns}{C_b}$	
$t_{HD;STA}$	Hold time (repeated) START condition	f_{SCL} ≤ 100kHz	4.0			µs
		f_{SCL} > 100kHz	0.6			
t_{LOW}	Low period of SCL clock	f_{SCL} ≤ 100kHz	4.7			
		f_{SCL} > 100kHz	1.3			
t_{HIGH}	High period of SCL clock	f_{SCL} ≤ 100kHz	4.0			
		f_{SCL} > 100kHz	0.6			
$t_{SU;STA}$	Setup time for a repeated START condition	f_{SCL} ≤ 100kHz	4.7			
		f_{SCL} > 100kHz	0.6			
$t_{HD;DAT}$	Data hold time	f_{SCL} ≤ 100kHz	0		3.45	
		f_{SCL} > 100kHz	0		0.9	
$t_{SU;DAT}$	Data setup time	f_{SCL} ≤ 100kHz	250			ns
		f_{SCL} > 100kHz	100			
$t_{SU;STO}$	Setup time for STOP condition	f_{SCL} ≤ 100kHz	4.0			µs
		f_{SCL} > 100kHz	0.6			
t_{BUF}	Bus free time between a STOP and START condition	f_{SCL} ≤ 100kHz	4.7			
		f_{SCL} > 100kHz	1.3			

Notes:
1. Required only for f_{SCL} > 100kHz.
2. C_b = Capacitance of one bus line in pF.
3. f_{PER} = Peripheral clock frequency.

Figure 34-13. Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 32MHz internal oscillator prescaled to 8MHz

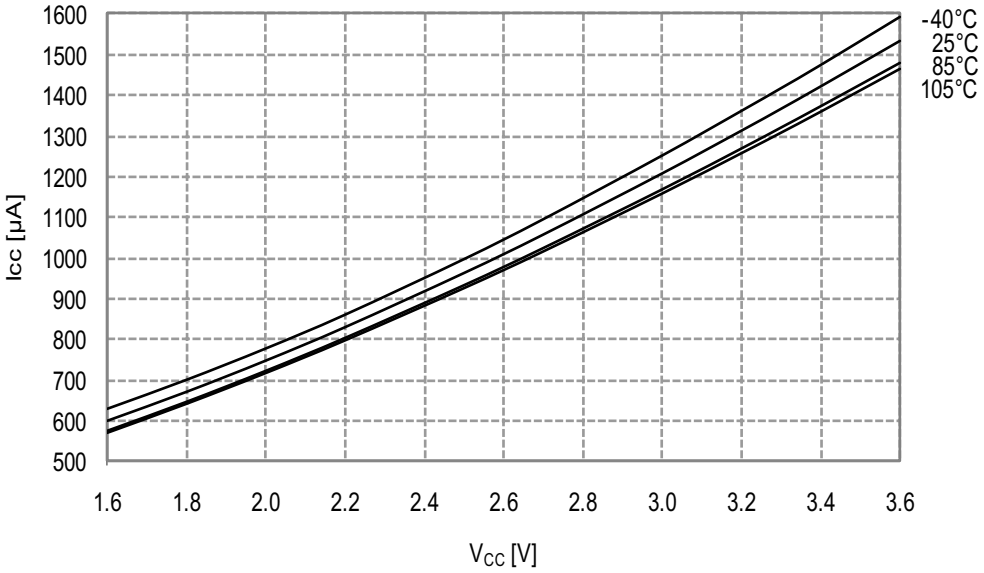


Figure 34-14. Idle Mode Current vs. V_{CC}

f_{SYS} = 32MHz internal oscillator

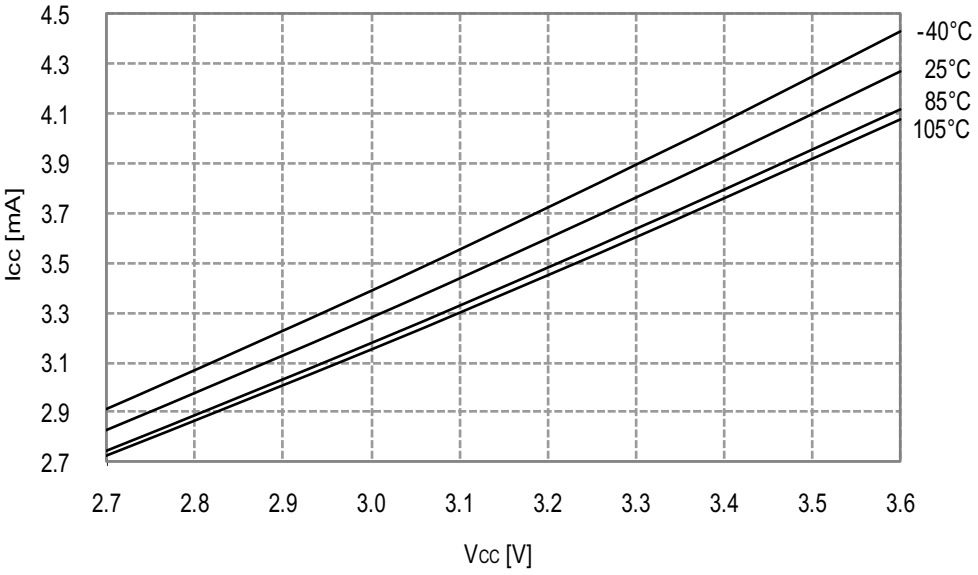


Figure 34-17. Power-down Mode Supply Current vs. Temperature

All functions disabled

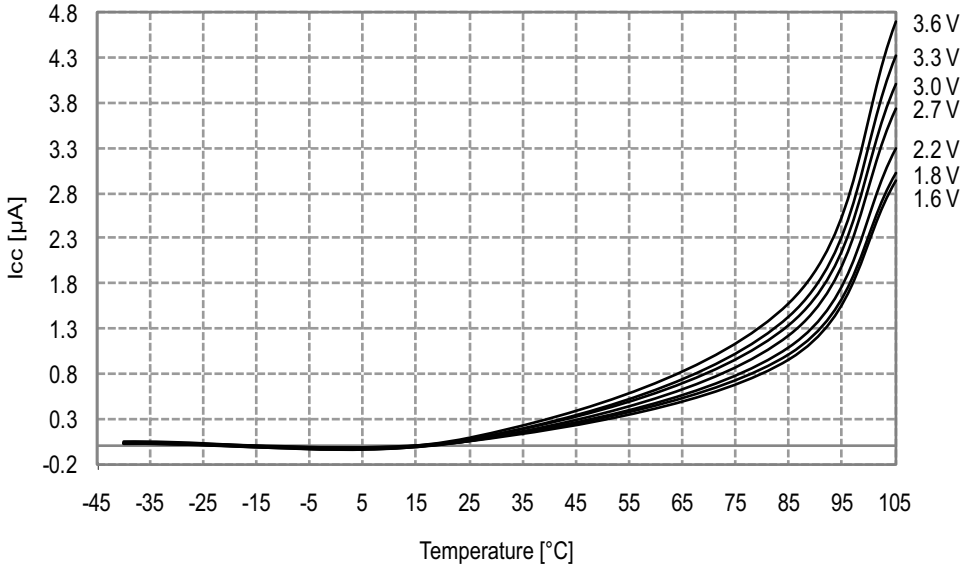


Figure 34-18. Power-down Mode Supply Current vs. Temperature

Watchdog and sampled BOD enabled and running from internal ULP oscillator

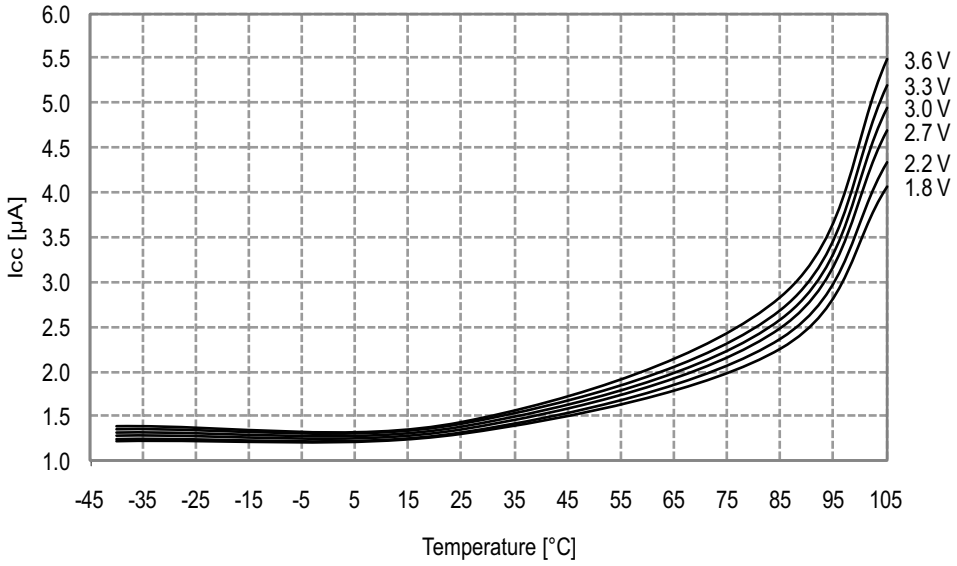


Figure 34-100. I/O Pin Input Threshold Voltage vs. V_{CC}

V_{IL} I/O pin read as "0"

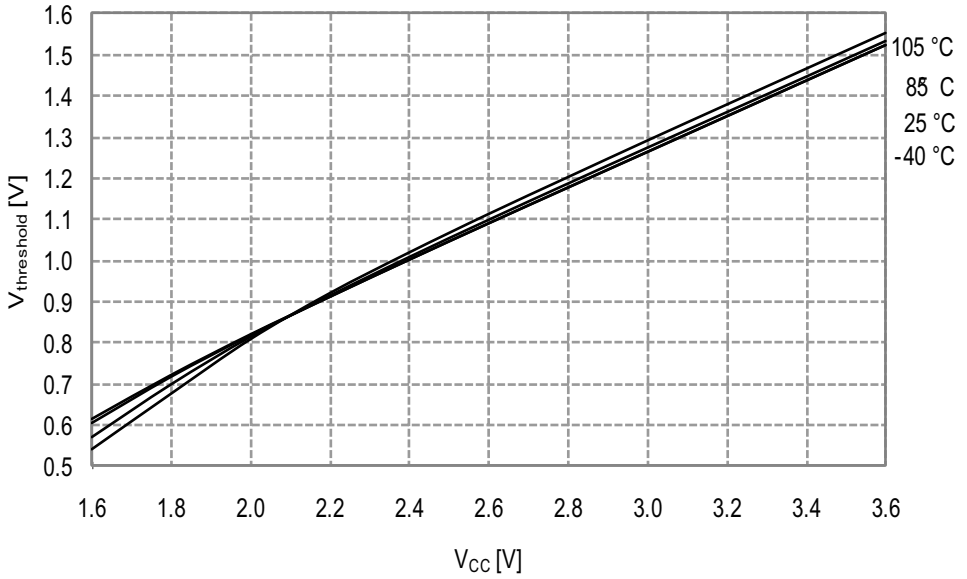


Figure 34-101. I/O Pin Input Hysteresis vs. V_{CC}

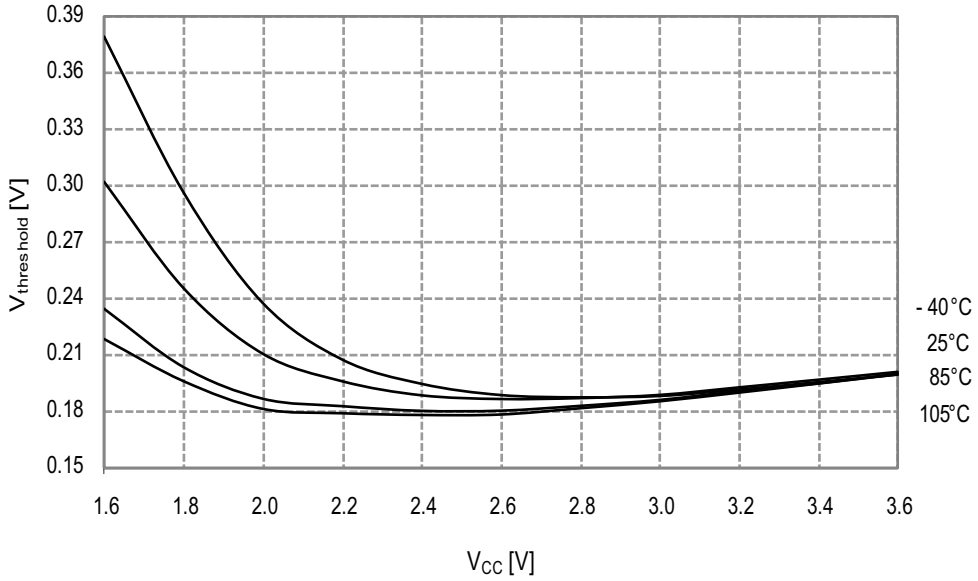


Figure 34-104. INL Error vs. Input Code

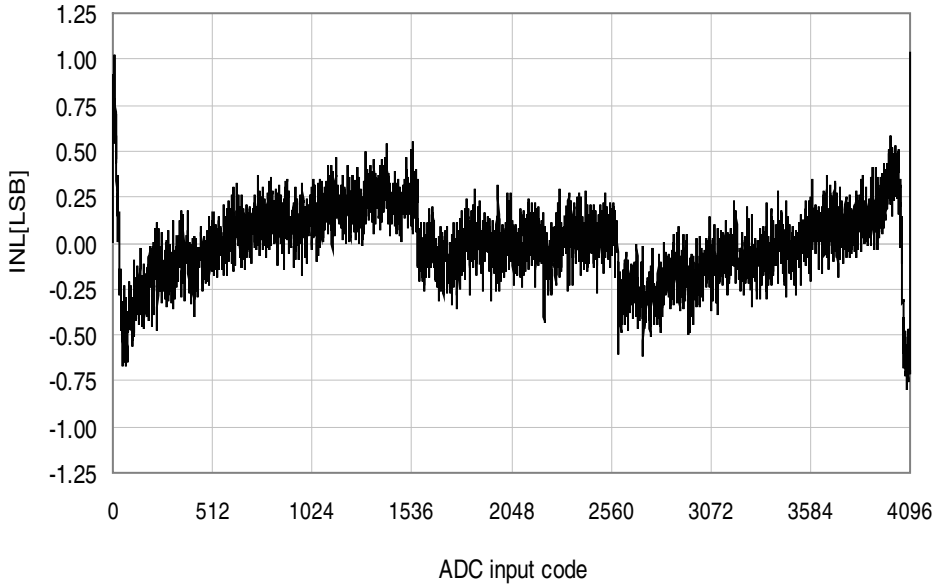


Figure 34-105. DNL Error vs. External V_{REF}

T = 25°C, V_{CC} = 3.6V, external reference

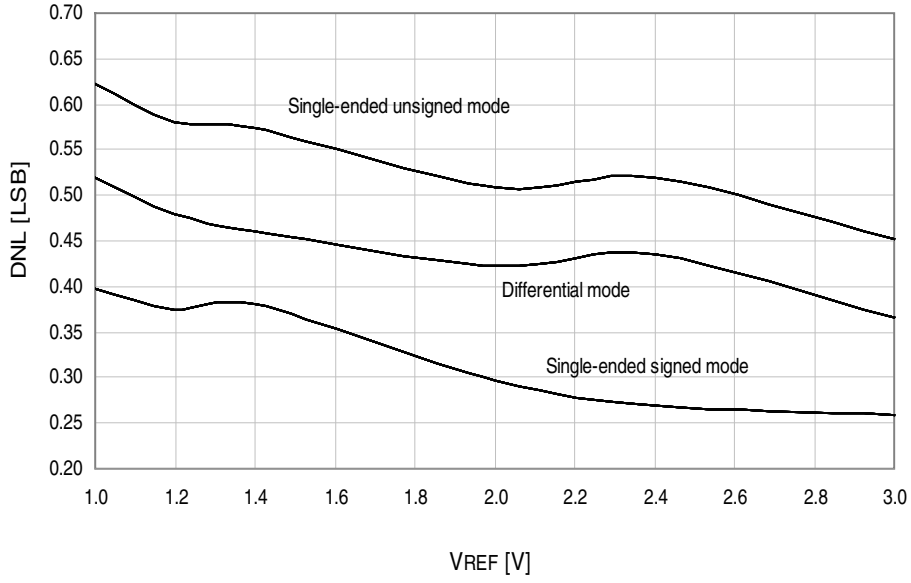


Figure 34-106. DNL Error vs. Sample Rate

T = 25°C, V_{CC} = 3.6V, V_{REF} = 3.0V external

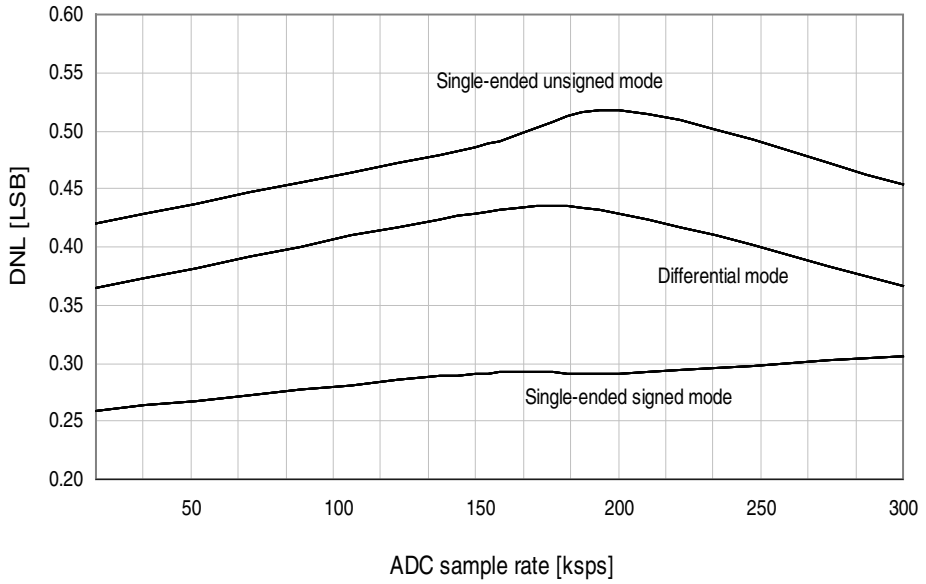


Figure 34-107. DNL Error vs. Input Code

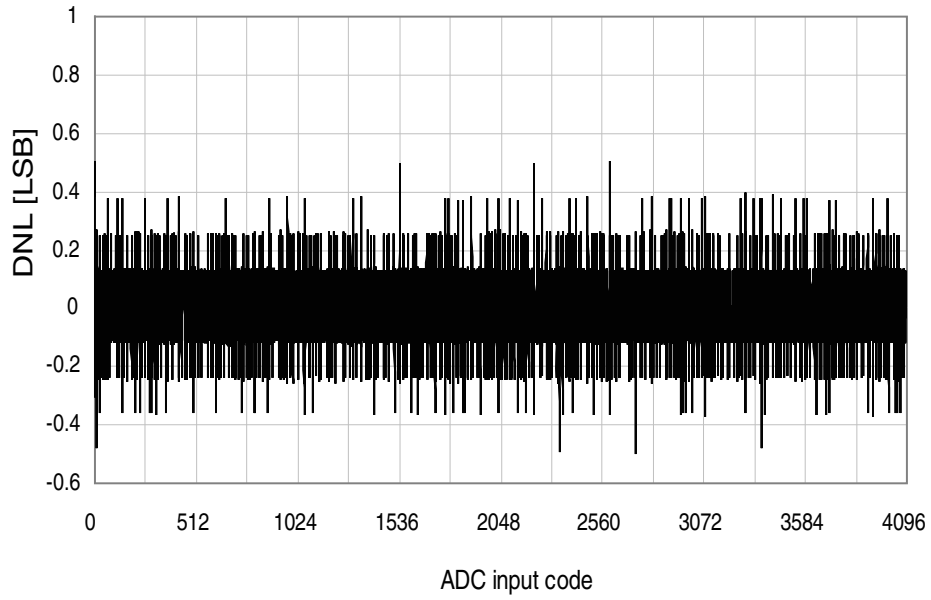
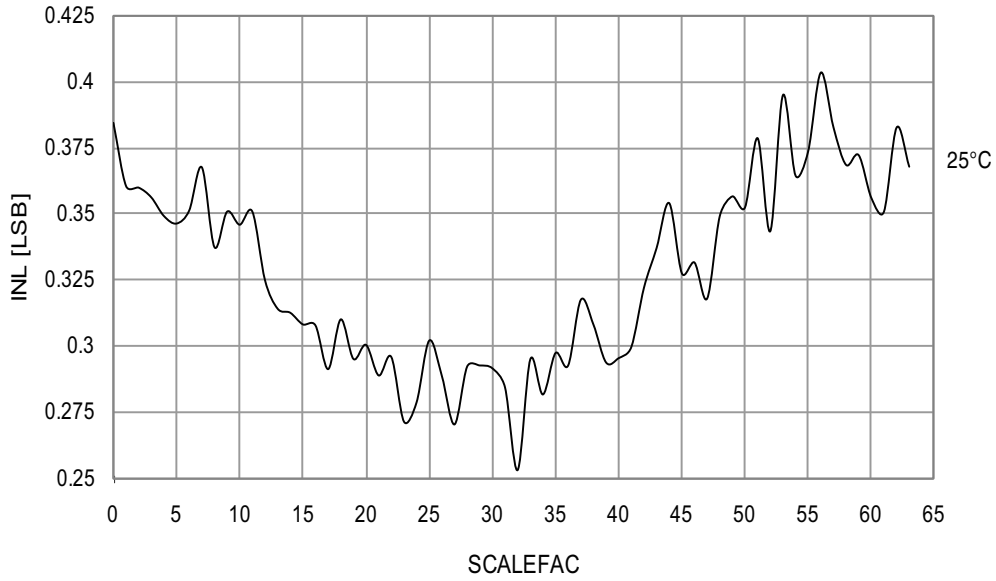


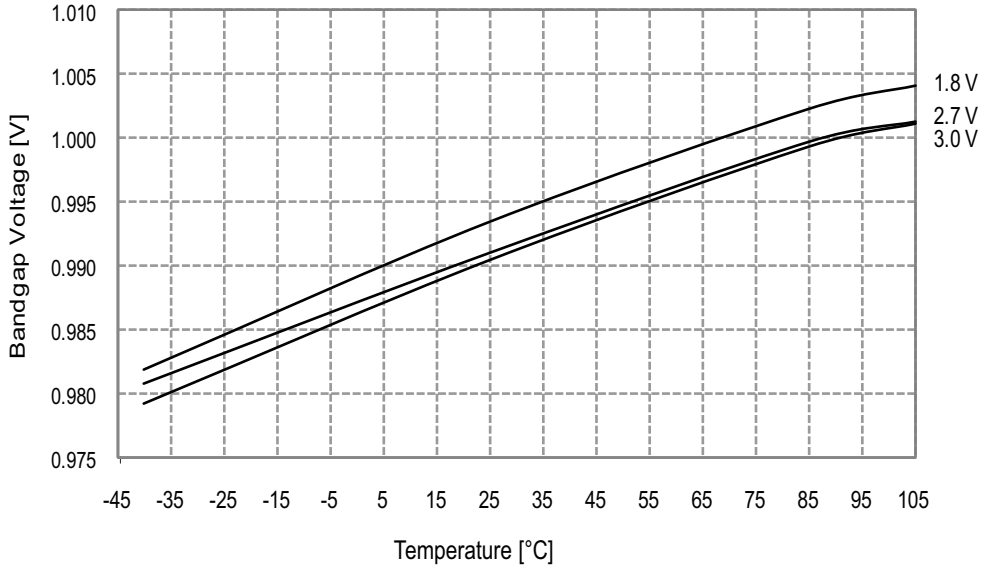
Figure 34-116. Voltage Scaler INL vs. SCALEFAC

T = 25°C, V_{CC} = 3.0V



34.2.5 Internal 1.0V Reference Characteristics

Figure 34-117. ADC Internal 1.0V Reference vs. Temperature



34.2.6 BOD Characteristics

Figure 34-118. BOD Thresholds vs. Temperature

BOD level = 1.6V

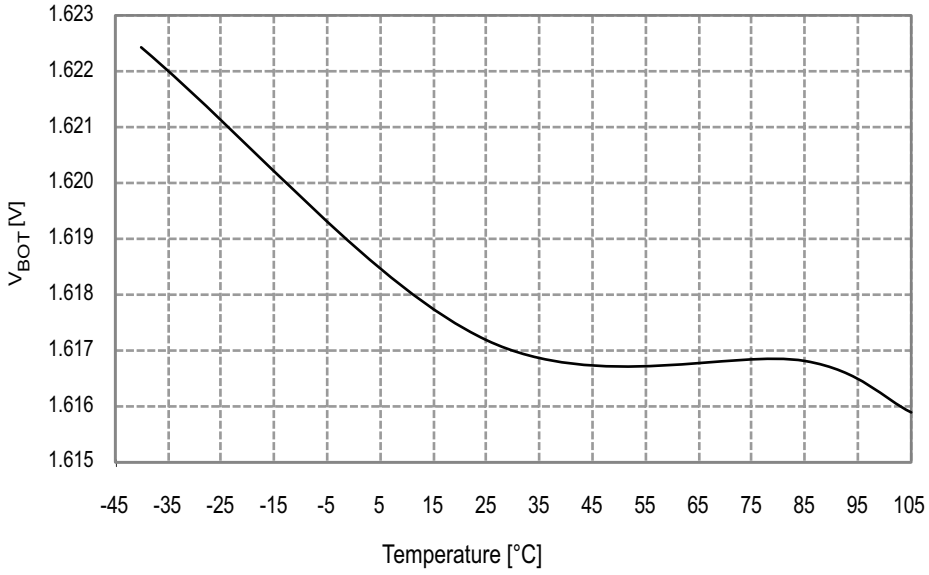


Figure 34-119. BOD Thresholds vs. Temperature

BOD level = 3.0V

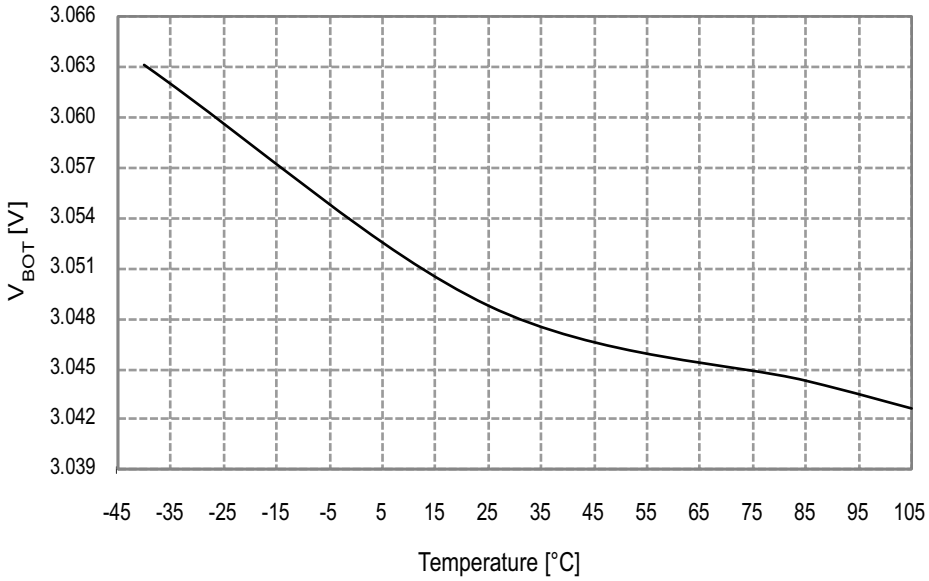


Figure 34-225. Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 32MHz internal oscillator prescaled to 8MHz

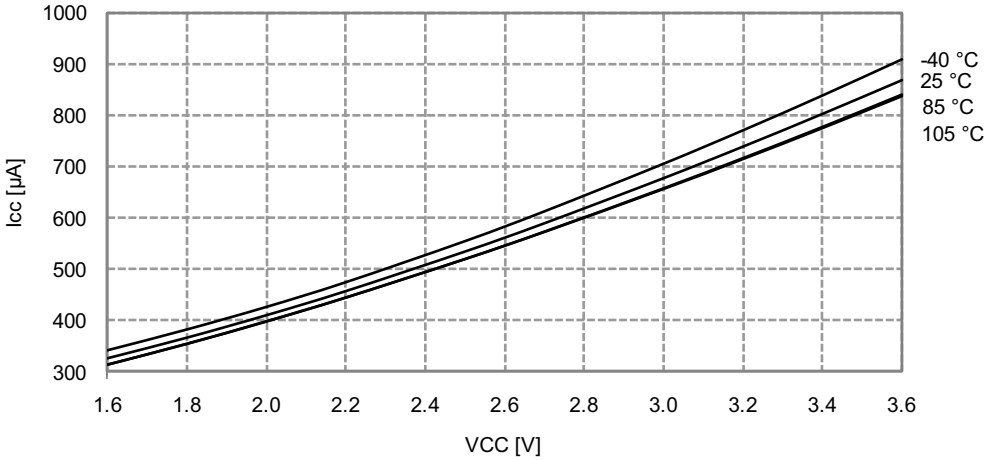


Figure 34-226. Idle Mode Current vs. V_{CC}

f_{SYS} = 32MHz internal oscillator

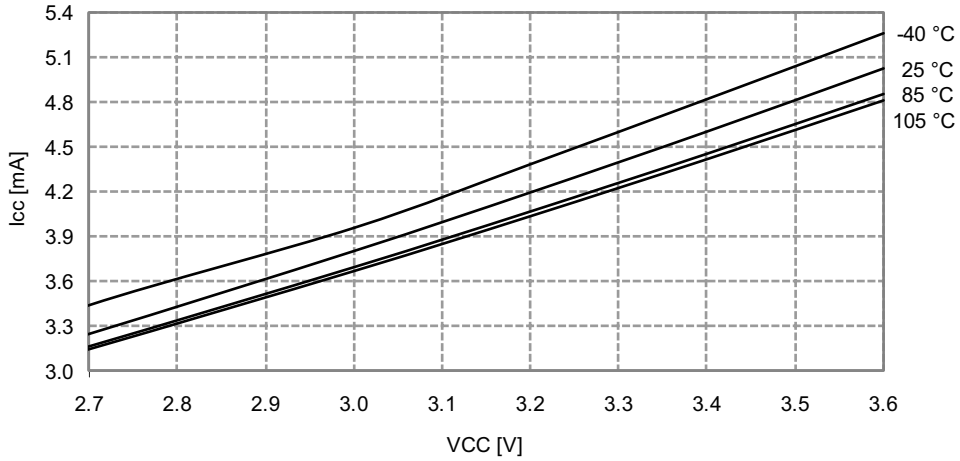


Figure 34-269. 2MHz Internal Oscillator Frequency vs. Temperature

DFLL enabled, from the 32.768kHz internal oscillator

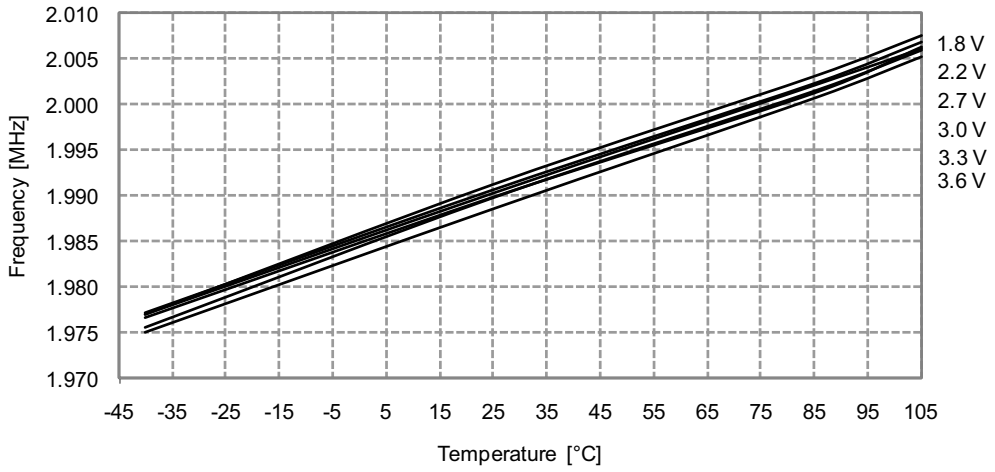


Figure 34-270. 2MHz Internal Oscillator Frequency vs. CALA Calibration Value

V_{CC} = 3V

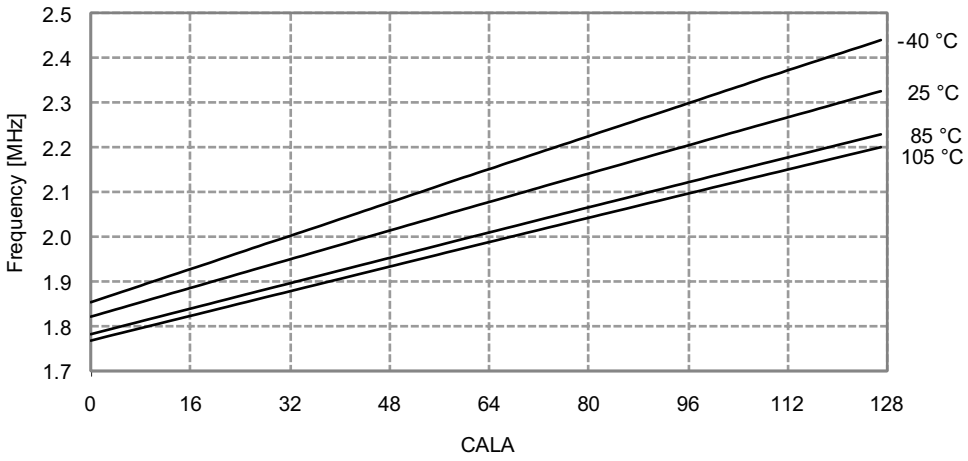


Figure 34-275. 32MHz Internal Oscillator CALA Calibration Step Size

T = 85°C, V_{CC} = 3.0V

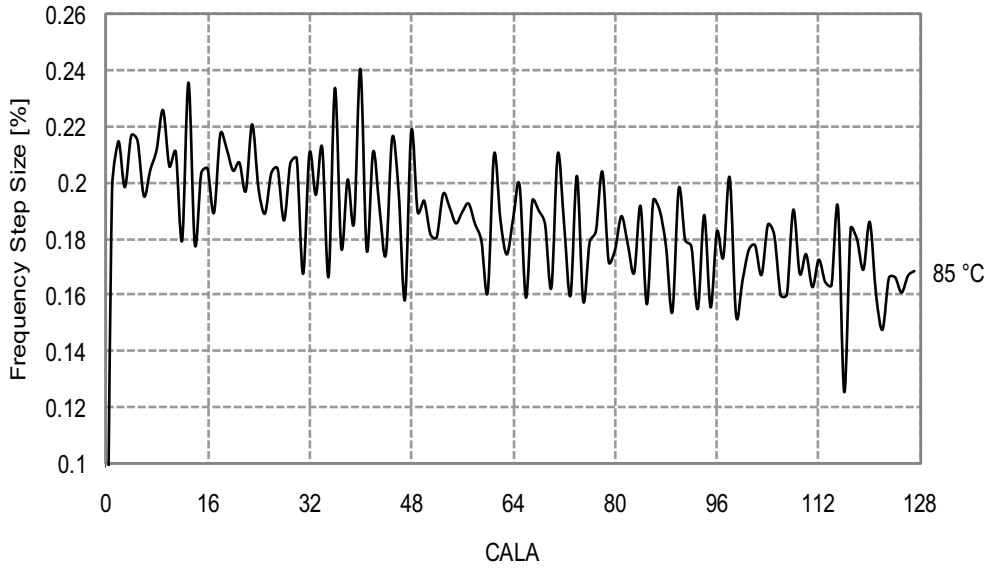


Figure 34-276. 32MHz Internal Oscillator CALA Calibration Step Size

T = 105°C, V_{CC} = 3.0V