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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | M16C/60 |
| Core Size | 16-Bit |
| Speed | 32MHz |
| Connectivity | EBI/EMI, I²C, SIO, UART/USART |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 85 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 8K x 8 |
| RAM Size | 12K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | A/D 26x10b; D/A 2x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-BQFP |
| Supplier Device Package | 100-QFP (14x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f36506dfa-u0 |

## 1.3 Product List

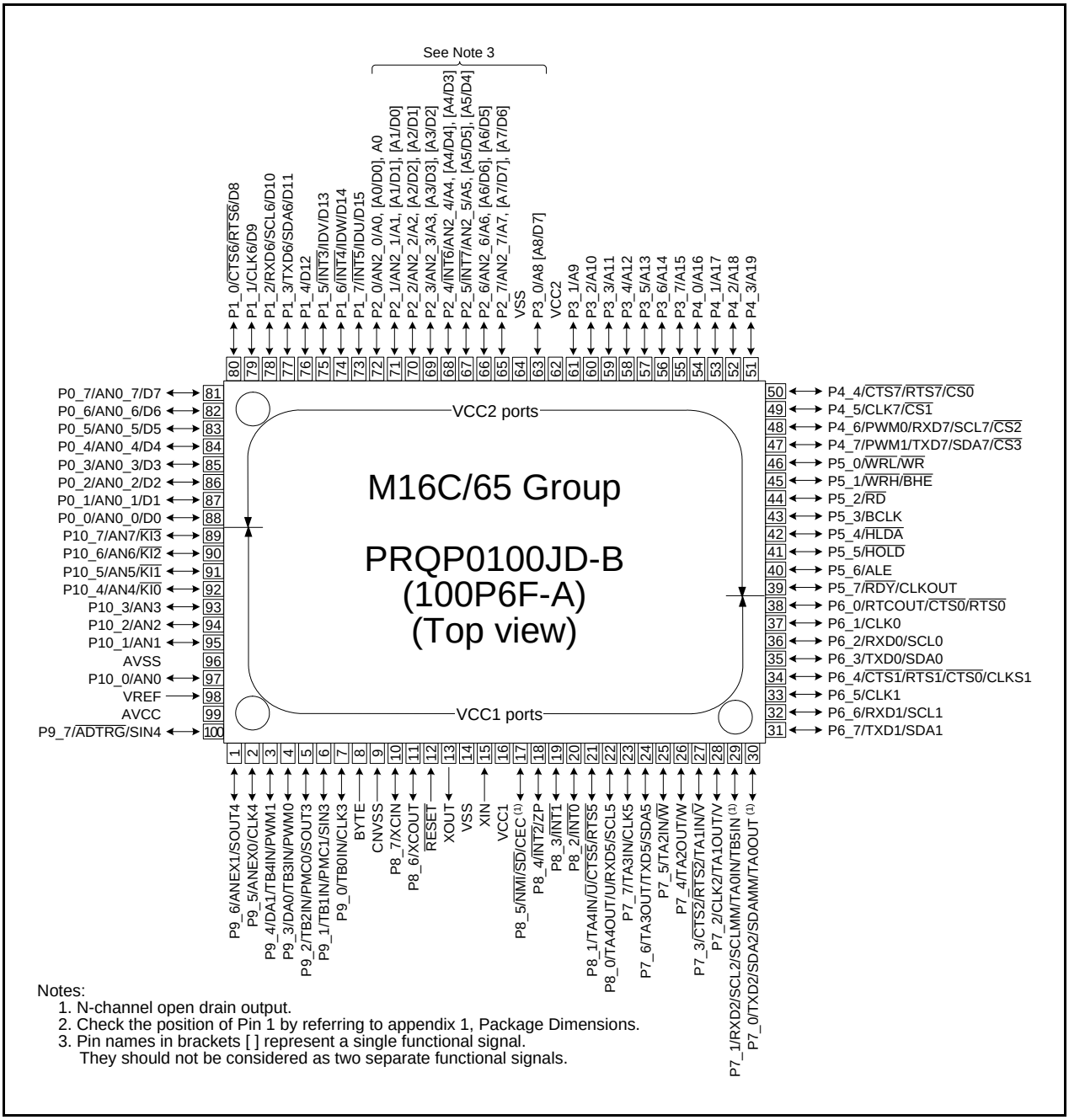
Table 1.5 and Table 1.6 list product information. Figure 1.1 shows the Part No., with Memory Size and Package, and Figure 1.2 shows the Marking Diagram (Top View).

**Table 1.5 Product List (1/2)** As of July 2012

| Part No. | ROM Capacity | | | RAM Capacity | Package Code | Remarks |
|---|---|---|---|---|---|---|
| | Program ROM 1 | Program ROM 2 | Data flash | | | |
| R5F36506NFA | 128 KB | 16 KB | 4 KB × 2 blocks | 12 KB | PRQP0100JD-B | Operating temperature -20°C to 85°C |
| R5F36506NFB | | | | | PLQP0100KB-A | |
| R5F36506DFA | | | | | PRQP0100JD-B | Operating temperature -40°C to 85°C |
| R5F36506DFB | | | | | PLQP0100KB-A | |
| R5F3651ENFC | 256 KB | 16 KB | 4 KB × 2 blocks | 20 KB | PLQP0128KB-A | Operating temperature -20°C to 85°C |
| R5F3650ENFA | | | | | PRQP0100JD-B | |
| R5F3650ENFB | | | | | PLQP0100KB-A | |
| R5F3651EDFC | | | | | PLQP0128KB-A | Operating temperature -40°C to 85°C |
| R5F3650EDFA | | | | | PRQP0100JD-B | |
| R5F3650EDFB | | | | | PLQP0100KB-A | |
| R5F3651KNFC | 384 KB | 16 KB | 4 KB × 2 blocks | 31 KB | PLQP0128KB-A | Operating temperature -20°C to 85°C |
| R5F3650KNFA | | | | | PRQP0100JD-B | |
| R5F3650KNFB | | | | | PLQP0100KB-A | |
| R5F3651KDFC | | | | | PLQP0128KB-A | Operating temperature -40°C to 85°C |
| R5F3650KDFA | | | | | PRQP0100JD-B | |
| R5F3650KDFB | | | | | PLQP0100KB-A | |
| R5F3651MNFC | 512 KB | 16 KB | 4 KB × 2 blocks | 31 KB | PLQP0128KB-A | Operating temperature -20°C to 85°C |
| R5F3650MNFA | | | | | PRQP0100JD-B | |
| R5F3650MNFB | | | | | PLQP0100KB-A | |
| R5F3651MDFC | | | | | PLQP0128KB-A | Operating temperature -40°C to 85°C |
| R5F3650MDFA | | | | | PRQP0100JD-B | |
| R5F3650MDFB | | | | | PLQP0100KB-A | |
| R5F3651NNFC | 512 KB | 16 KB | 4 KB × 2 blocks | 47 KB | PLQP0128KB-A | Operating temperature -20°C to 85°C |
| R5F3650NNFA | | | | | PRQP0100JD-B | |
| R5F3650NNFB | | | | | PLQP0100KB-A | |
| R5F3651NDFC | | | | | PLQP0128KB-A | Operating temperature -40°C to 85°C |
| R5F3650NDFA | | | | | PRQP0100JD-B | |
| R5F3650NDFB | | | | | PLQP0100KB-A | |
| R5F3651RNFC | 640 KB | 16 KB | 4 KB × 2 blocks | 47 KB | PLQP0128KB-A | Operating temperature -20°C to 85°C |
| R5F3650RNFA | | | | | PRQP0100JD-B | |
| R5F3650RNFB | | | | | PLQP0100KB-A | |
| R5F3651RDFC | | | | | PLQP0128KB-A | Operating temperature -40°C to 85°C |
| R5F3650RDFA | | | | | PRQP0100JD-B | |
| R5F3650RDFB | | | | | PLQP0100KB-A | |

(D): Under development
(P): Planning

Previous package codes are as follows:
PLQP0128KB-A: 128P6Q-A
PRQP0100JD-B: 100P6F-A
PLQP0100KB-A: 100P6Q-A




Notes:
1. N-channel open drain output.
2. Check the position of Pin 1 by referring to appendix 1, Package Dimensions.
3. Pin names in brackets [ ] represent a single functional signal.
They should not be considered as two separate functional signals.

**Figure 1.6 Pin Assignment for the 100-Pin Package**

**Table 1.15 Pin Functions for the 100-Pin Package (1/3)**

| Signal Name | Pin Name | I/O | Power Supply | Description |
|---|---|---|---|---|
| Power supply input | VCC1, VCC2, VSS | I | - | Apply 2.7 to 5.5 V to pins VCC1 and VCC2 (VCC1 ≥ VCC2) and 0 V to the VSS pin. |
| Analog power supply input | AVCC, AVSS | I | VCC1 | This is the power supply for the A/D and D/A converters. Connect the AVCC pin to VCC1, and connect the AVSS pin to VSS. |
| Reset input | $\overline{\text{RESET}}$ | I | VCC1 | Driving this pin low resets the MCU. |
| CNVSS | CNVSS | I | VCC1 | Input pin to switch processor modes. After a reset, to start operating in single-chip mode, connect the CNVSS pin to VSS via a resistor. To start operating in microprocessor mode, connect the pin to VCC1. |
| External data bus width select input | BYTE | I | VCC1 | Input pin to select the data bus of the external area. The data bus is 16 bits when it is low, and 8 bits when it is high. This pin must be fixed either high or low. Connect the BYTE pin to VSS in single-chip mode. |
| Bus control pins | D0 to D7 | I/O | VCC2 | Inputs or outputs data (D0 to D7) while accessing an external area with a separate bus. |
| | D8 to D15 | I/O | VCC2 | Inputs or outputs data (D8 to D15) while accessing an external area with a 16-bit separate bus. |
| | A0 to A19 | O | VCC2 | Outputs address bits A0 to A19. |
| | A0/D0 to A7/D7 | I/O | VCC2 | Inputs or outputs data (D0 to D7) and outputs address bits (A0 to A7) by timesharing, while accessing an external area with an 8-bit multiplexed bus. |
| | A1/D0 to A8/D7 | I/O | VCC2 | Inputs or outputs data (D0 to D7) and outputs address bits (A1 to A8) by timesharing, while accessing an external area with a 16-bit multiplexed bus. |
| | $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$ | O | VCC2 | Outputs chip-select signals $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$ to specify an external area. |
| | $\overline{\text{WRL}}$/$\overline{\text{WR}}$<br>$\overline{\text{WRH}}$/$\overline{\text{BHE}}$<br>$\overline{\text{RD}}$ | O | VCC2 | Outputs $\overline{\text{WRL}}$, $\overline{\text{WRH}}$, ($\overline{\text{WR}}$, $\overline{\text{BHE}}$), and $\overline{\text{RD}}$ signals. $\overline{\text{WRL}}$ and $\overline{\text{WRH}}$ can be switched with $\overline{\text{BHE}}$ and $\overline{\text{WR}}$.<br>• $\overline{\text{WRL}}$, $\overline{\text{WRH}}$, and $\overline{\text{RD}}$ selected<br>If the external data bus is 16 bits, data is written to an even address in an external area when $\overline{\text{WRL}}$ is driven low. Data is written to an odd address when $\overline{\text{WRH}}$ is driven low. Data is read when $\overline{\text{RD}}$ is driven low.<br>• $\overline{\text{WR}}$, $\overline{\text{BHE}}$, and $\overline{\text{RD}}$ selected<br>Data is written to an external area when $\overline{\text{WR}}$ is driven low. Data in an external area is read when $\overline{\text{RD}}$ is driven low. An odd address is accessed when $\overline{\text{BHE}}$ is driven low. Select $\overline{\text{WR}}$, $\overline{\text{BHE}}$, and $\overline{\text{RD}}$ when using an 8-bit external data bus. |
| | ALE | O | VCC2 | Outputs an ALE signal to latch the address. |
| | $\overline{\text{HOLD}}$ | I | VCC2 | $\overline{\text{HOLD}}$ input is unavailable. Connect the $\overline{\text{HOLD}}$ pin to VCC2 via a resistor (pull-up). |
| | $\overline{\text{HLDA}}$ | O | VCC2 | In a hold state, $\overline{\text{HLDA}}$ outputs a low-level signal. |
| | $\overline{\text{RDY}}$ | I | VCC2 | The MCU bus is placed in a wait state while the $\overline{\text{RDY}}$ pin is driven low. |

Power supply: VCC2 is used to supply power to the external bus associated pins. The dual power supply configuration allows VCC2 to interface at a different voltage than VCC1.

### 2.8.7 Interrupt Enable Flag (I Flag)

The I flag enables maskable interrupts.
Maskable interrupts are disabled when the I flag is 0, and enabled when it is 1. The I flag becomes 0 when an interrupt request is accepted.

### 2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is 0. USP is selected when the U flag is 1.
The U flag becomes 0 when a hardware interrupt request is accepted, or the INT instruction of software interrupt number 0 to 31 is executed.

### 2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from 0 to 7.
If a requested interrupt has higher priority than IPL, the interrupt request is enabled.

### 2.8.10 Reserved Areas

Only set these bits to 0. The read value is undefined.

# 4. Special Function Registers (SFRs)

## 4.1 SFRs

An SFR is a control register for a peripheral function.

**Table 4.1 SFR Information (1)** (1)

| Address | Register | Symbol | Reset Value |
|---|---|---|---|
| 0000h | | | |
| 0001h | | | |
| 0002h | | | |
| 0003h | | | |
| 0004h | Processor Mode Register 0 | PM0 | 0000 0000b (CNVSS pin is low) 0000 0011b (CNVSS pin is high) (2) |
| 0005h | Processor Mode Register 1 | PM1 | 0000 1000b |
| 0006h | System Clock Control Register 0 | CM0 | 0100 1000b |
| 0007h | System Clock Control Register 1 | CM1 | 0010 0000b |
| 0008h | Chip Select Control Register | CSR | 01h |
| 0009h | External Area Recovery Cycle Control Register | EWR | XXXX XX00b |
| 000Ah | Protect Register | PRCR | 00h |
| 000Bh | Data Bank Register | DBR | 00h |
| 000Ch | Oscillation Stop Detection Register | CM2 | 0X00 0010b (3) |
| 000Dh | | | |
| 000Eh | | | |
| 000Fh | | | |
| 0010h | Program 2 Area Control Register | PRG2C | XXXX XX00b |
| 0011h | External Area Wait Control Expansion Register | EWC | 00h |
| 0012h | Peripheral Clock Select Register | PCLKR | 0000 0011b |
| 0013h | | | |
| 0014h | | | |
| 0015h | Clock Prescaler Reset Flag | CPSRF | 0XXX XXXXb |
| 0016h | | | |
| 0017h | | | |
| 0018h | Reset Source Determine Register | RSTFR | XX00 001Xb (hardware reset) (4) |
| 0019h | Voltage Detector 2 Flag Register | VCR1 | 0000 1000b (5) |
| 001Ah | Voltage Detector Operation Enable Register | VCR2 | 00h (5) |
| 001Bh | Chip Select Expansion Control Register | CSE | 00h |
| 001Ch | PLL Control Register 0 | PLC0 | 0X01 X010b |
| 001Dh | | | |
| 001Eh | Processor Mode Register 2 | PM2 | XX00 0X01b |
| 001Fh | | | |

X: Undefined

Notes:
1. The blank areas are reserved. No access is allowed.
2. Software reset, watchdog timer reset, oscillator stop detect reset, voltage monitor 1 reset, and voltage monitor 2 reset do not affect the following bits: bits PM01 and PM00 in the PM0 register.
3. Oscillator stop detect reset does not affect bits CM20, CM21, and CM27.
4. The state of bits in the RSTFR register depends on the reset type.
5. This is the reset value after hardware reset. Refer to the explanation of each register for details.

**Table 4.3 SFR Information (3)** (1)

| Address | Register | Symbol | Reset Value |
|---|---|---|---|
| 0040h | | | |
| 0041h | | | |
| 0042h | $\overline{\text{INT7}}$ Interrupt Control Register | INT7IC | XX00 X000b |
| 0043h | $\overline{\text{INT6}}$ Interrupt Control Register | INT6IC | XX00 X000b |
| 0044h | $\overline{\text{INT3}}$ Interrupt Control Register | INT3IC | XX00 X000b |
| 0045h | Timer B5 Interrupt Control Register | TB5IC | XXXX X000b |
| 0046h | Timer B4 Interrupt Control Register<br>UART1 Bus Collision Detection Interrupt Control Register | TB4IC<br>U1BCNIC | XXXX X000b |
| 0047h | Timer B3 Interrupt Control Register<br>UART0 Bus Collision Detection Interrupt Control Register | TB3IC<br>U0BCNIC | XXXX X000b |
| 0048h | SI/O4 Interrupt Control Register<br>$\overline{\text{INT5}}$ Interrupt Control Register | S4IC<br>INT5IC | XX00 X000b |
| 0049h | SI/O3 Interrupt Control Register<br>$\overline{\text{INT4}}$ Interrupt Control Register | S3IC<br>INT4IC | XX00 X000b |
| 004Ah | UART2 Bus Collision Detection Interrupt Control Register | BCNIC | XXXX X000b |
| 004Bh | DMA0 Interrupt Control Register | DM0IC | XXXX X000b |
| 004Ch | DMA1 Interrupt Control Register | DM1IC | XXXX X000b |
| 004Dh | Key Input Interrupt Control Register | KUPIC | XXXX X000b |
| 004Eh | A/D Conversion Interrupt Control Register | ADIC | XXXX X000b |
| 004Fh | UART2 Transmit Interrupt Control Register | S2TIC | XXXX X000b |
| 0050h | UART2 Receive Interrupt Control Register | S2RIC | XXXX X000b |
| 0051h | UART0 Transmit Interrupt Control Register | S0TIC | XXXX X000b |
| 0052h | UART0 Receive Interrupt Control Register | S0RIC | XXXX X000b |
| 0053h | UART1 Transmit Interrupt Control Register | S1TIC | XXXX X000b |
| 0054h | UART1 Receive Interrupt Control Register | S1RIC | XXXX X000b |
| 0055h | Timer A0 Interrupt Control Register | TA0IC | XXXX X000b |
| 0056h | Timer A1 Interrupt Control Register | TA1IC | XXXX X000b |
| 0057h | Timer A2 Interrupt Control Register | TA2IC | XXXX X000b |
| 0058h | Timer A3 Interrupt Control Register | TA3IC | XXXX X000b |
| 0059h | Timer A4 Interrupt Control Register | TA4IC | XXXX X000b |
| 005Ah | Timer B0 Interrupt Control Register | TB0IC | XXXX X000b |
| 005Bh | Timer B1 Interrupt Control Register | TB1IC | XXXX X000b |
| 005Ch | Timer B2 Interrupt Control Register | TB2IC | XXXX X000b |
| 005Dh | $\overline{\text{INT0}}$ Interrupt Control Register | INT0IC | XX00 X000b |
| 005Eh | $\overline{\text{INT1}}$ Interrupt Control Register | INT1IC | XX00 X000b |
| 005Fh | $\overline{\text{INT2}}$ Interrupt Control Register | INT2IC | XX00 X000b |

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

**Table 4.5 SFR Information (5)** (1)

| Address | Register | Symbol | Reset Value |
|---|---|---|---|
| 0180h | DMA0 Source Pointer | SAR0 | XXh |
| 0181h | | | XXh |
| 0182h | | | 0Xh |
| 0183h | | | |
| 0184h | DMA0 Destination Pointer | DAR0 | XXh |
| 0185h | | | XXh |
| 0186h | | | 0Xh |
| 0187h | | | |
| 0188h | DMA0 Transfer Counter | TCR0 | XXh |
| 0189h | | | XXh |
| 018Ah | | | |
| 018Bh | | | |
| 018Ch | DMA0 Control Register | DM0CON | 0000 0X00b |
| 018Dh | | | |
| 018Eh | | | |
| 018Fh | | | |
| 0190h | DMA1 Source Pointer | SAR1 | XXh |
| 0191h | | | XXh |
| 0192h | | | 0Xh |
| 0193h | | | |
| 0194h | DMA1 Destination Pointer | DAR1 | XXh |
| 0195h | | | XXh |
| 0196h | | | 0Xh |
| 0197h | | | |
| 0198h | DMA1 Transfer Counter | TCR1 | XXh |
| 0199h | | | XXh |
| 019Ah | | | |
| 019Bh | | | |
| 019Ch | DMA1 Control Register | DM1CON | 0000 0X00b |
| 019Dh | | | |
| 019Eh | | | |
| 019Fh | | | |
| 01A0h | DMA2 Source Pointer | SAR2 | XXh |
| 01A1h | | | XXh |
| 01A2h | | | 0Xh |
| 01A3h | | | |
| 01A4h | DMA2 Destination Pointer | DAR2 | XXh |
| 01A5h | | | XXh |
| 01A6h | | | 0Xh |
| 01A7h | | | |
| 01A8h | DMA2 Transfer Counter | TCR2 | XXh |
| 01A9h | | | XXh |
| 01AAh | | | |
| 01ABh | | | |
| 01ACh | DMA2 Control Register | DM2CON | 0000 0X00b |
| 01ADh | | | |
| 01AEh | | | |
| 01AFh | | | |

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

**Table 4.9 SFR Information (9)** (1)

| Address | Register | Symbol | Reset Value |
|---|---|---|---|
| 0240h | | | |
| 0241h | | | |
| 0242h | | | |
| 0243h | | | |
| 0244h | UART0 Special Mode Register 4 | U0SMR4 | 00h |
| 0245h | UART0 Special Mode Register 3 | U0SMR3 | 000X 0X0Xb |
| 0246h | UART0 Special Mode Register 2 | U0SMR2 | X000 0000b |
| 0247h | UART0 Special Mode Register | U0SMR | X000 0000b |
| 0248h | UART0 Transmit/Receive Mode Register | U0MR | 00h |
| 0249h | UART0 Bit Rate Register | U0BRG | XXh |
| 024Ah | UART0 Transmit Buffer Register | U0TB | XXh |
| 024Bh | | | XXh |
| 024Ch | UART0 Transmit/Receive Control Register 0 | U0C0 | 0000 1000b |
| 024Dh | UART0 Transmit/Receive Control Register 1 | U0C1 | 00XX 0010b |
| 024Eh | UART0 Receive Buffer Register | U0RB | XXh |
| 024Fh | | | XXh |
| 0250h | UART Transmit/Receive Control Register 2 | UCON | X000 0000b |
| 0251h | | | |
| 0252h | UART Clock Select Register | UCLKSEL0 | X0h |
| 0253h | | | |
| 0254h | UART1 Special Mode Register 4 | U1SMR4 | 00h |
| 0255h | UART1 Special Mode Register 3 | U1SMR3 | 000X 0X0Xb |
| 0256h | UART1 Special Mode Register 2 | U1SMR2 | X000 0000b |
| 0257h | UART1 Special Mode Register | U1SMR | X000 0000b |
| 0258h | UART1 Transmit/Receive Mode Register | U1MR | 00h |
| 0259h | UART1 Bit Rate Register | U1BRG | XXh |
| 025Ah | UART1 Transmit Buffer Register | U1TB | XXh |
| 025Bh | | | XXh |
| 025Ch | UART1 Transmit/Receive Control Register 0 | U1C0 | 0000 1000b |
| 025Dh | UART1 Transmit/Receive Control Register 1 | U1C1 | 00XX 0010b |
| 025Eh | UART1 Receive Buffer Register | U1RB | XXh |
| 025Fh | | | XXh |
| 0260h | | | |
| 0261h | | | |
| 0262h | | | |
| 0263h | | | |
| 0264h | UART2 Special Mode Register 4 | U2SMR4 | 00h |
| 0265h | UART2 Special Mode Register 3 | U2SMR3 | 000X 0X0Xb |
| 0266h | UART2 Special Mode Register 2 | U2SMR2 | X000 0000b |
| 0267h | UART2 Special Mode Register | U2SMR | X000 0000b |
| 0268h | UART2 Transmit/Receive Mode Register | U2MR | 00h |
| 0269h | UART2 Bit Rate Register | U2BRG | XXh |
| 026Ah | UART2 Transmit Buffer Register | U2TB | XXh |
| 026Bh | | | XXh |
| 026Ch | UART2 Transmit/Receive Control Register 0 | U2C0 | 0000 1000b |
| 026Dh | UART2 Transmit/Receive Control Register 1 | U2C1 | 0000 0010b |
| 026Eh | UART2 Receive Buffer Register | U2RB | XXh |
| 026Fh | | | XXh |

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

# 5. Electrical Characteristics

## 5.1 Electrical Characteristics (Common to 3 V and 5 V)

### 5.1.1 Absolute Maximum Rating

**Table 5.1 Absolute Maximum Ratings**

| Symbol | Parameter | | Condition | Rated Value | Unit |
|---|---|---|---|---|---|
| $V_{CC1}$ | Supply voltage | | $V_{CC1} = AV_{CC}$ | –0.3 to 6.5 | V |
| $V_{CC2}$ | Supply voltage | | $V_{CC1} = AV_{CC}$ | –0.3 to $V_{CC1}$ + 0.1 (1) | V |
| $AV_{CC}$ | Analog supply voltage | | $V_{CC1} = AV_{CC}$ | –0.3 to 6.5 | V |
| $V_{REF}$ | Analog reference voltage | | $V_{CC1} = AV_{CC}$ | –0.3 to $V_{CC1}$ + 0.1 (1) | V |
| $V_I$ | Input voltage | $\overline{RESET}$, CNVSS, BYTE,<br>P6_0 to P6_7, P7_2 to P7_7,<br>P8_0 to P8_4, P8_6, P8_7,<br>P9_0 to P9_7, P10_0 to P10_7,<br>P11_0 to P11_7, P14_0, P14_1<br>XIN | | –0.3 to $V_{CC1}$ + 0.3 (1) | V |
| | | P0_0 to P0_7, P1_0 to P1_7,<br>P2_0 to P2_7, P3_0 to P3_7,<br>P4_0 to P4_7, P5_0 to P5_7,<br>P12_0 to P12_7, P13_0 to P13_7 | | –0.3 to $V_{CC2}$ + 0.3 (1) | V |
| | | P7_0, P7_1, P8_5 | | –0.3 to 6.5 | V |
| $V_O$ | Output voltage | P6_0 to P6_7, P7_2 to P7_7,<br>P8_0 to P8_4, P8_6, P8_7,<br>P9_0 to P9_7, P10_0 to P10_7,<br>P11_0 to P11_7, P14_0, P14_1<br>XOUT | | –0.3 to $V_{CC1}$ + 0.3 (1) | V |
| | | P0_0 to P0_7, P1_0 to P1_7,<br>P2_0 to P2_7, P3_0 to P3_7,<br>P4_0 to P4_7, P5_0 to P5_7,<br>P12_0 to P12_7, P13_0 to P13_7 | | –0.3 to $V_{CC2}$ + 0.3 (1) | V |
| | | P7_0, P7_1, P8_5 | | –0.3 to 6.5 | V |
| $P_d$ | Power consumption | | $-40°C < T_{opr} \leq 85°C$ | 300 | mW |
| $T_{opr}$ | Operating temperature | When the MCU is operating | | –20 to 85/–40 to 85 | °C |
| | | Flash program erase | Program area | 0 to 60 | |
| | | | Data area | –20 to 85/–40 to 85 | |
| $T_{stg}$ | Storage temperature | | | –65 to 150 | °C |

Note:
1. Maximum value is 6.5 V.

**Table 5.6 A/D Conversion Characteristics (2/2) (1)**

$V_{CC1}$ = $AV_{CC}$ = 3.0 to 5.5 V ≥ $V_{CC2}$ ≥ $V_{REF}$, $V_{SS}$ = $AV_{SS}$ = 0 V at $T_{opr}$ = -20°C to 85°C/-40°C to 85°C unless otherwise specified.

| Symbol | Parameter | | Measuring Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| ϕAD | A/D operating clock frequency | AN0 to AN7 input, ANEX0 to ANEX1 input | 4.0 V ≤ $V_{CC1}$ ≤ 5.5 V | 2 | | 25 | MHz |
| | | | 3.2 V ≤ $V_{CC1}$ ≤ 4.0 V | 2 | | 16 | MHz |
| | | | 3.0 V ≤ $V_{CC1}$ ≤ 3.2 V | 2 | | 10 | MHz |
| | | AN0_0 to AN0_7 input, AN2_0 to AN2_7 input | 4.0 V ≤ $V_{CC2}$ ≤ 5.5 V | 2 | | 25 | MHz |
| | | | 3.2 V ≤ $V_{CC2}$ ≤ 4.0 V | 2 | | 16 | MHz |
| | | | 3.0 V ≤ $V_{CC2}$ ≤ 3.2 V | 2 | | 10 | MHz |
| - | Tolerance level impedance | | | | 3 | | kΩ |
| $D_{NL}$ | Differential non-linearity error | | (4) | | | ±1 | LSB |
| - | Offset error | | (4) | | | ±3 | LSB |
| - | Gain error | | (4) | | | ±3 | LSB |
| $t_{CONV}$ | 10-bit conversion time | | $V_{CC1}$ = 5 V, ϕAD = 25 MHz | 1.60 | | | µs |
| $t_{SAMP}$ | Sampling time | | | 0.60 | | | µs |
| $V_{REF}$ | Reference voltage | | | 3.0 | | $V_{CC1}$ | V |
| $V_{IA}$ | Analog input voltage (2), (3) | | | 0 | | $V_{REF}$ | V |

Notes:
1. Use when $AV_{CC}$ = $V_{CC1}$.
2. When $V_{CC1}$ ≥ $V_{CC2}$, set as below:
   Analog input voltage (AN0 to AN7, ANEX0, and ANEX1) ≤ $V_{CC1}$
   Analog input voltage (AN0_0 to AN0_7 and AN2_0 to AN2_7) ≤ $V_{CC2}$.
3. When analog input voltage is over reference voltage, the result of A/D conversion is 3FFh.
4. Flash memory rewrite disabled. Except for the analog input pin, set the pins to be measured as input ports and connect them to $V_{SS}$. See Figure 5.2 “A/D Accuracy Measure Circuit”.

## 5.1.4 D/A Conversion Characteristics

**Table 5.7 D/A Conversion Characteristics**

$V_{CC1}$ = $AV_{CC}$ = $V_{REF}$ = 3.0 to 5.5 V, $V_{SS}$ = $AV_{SS}$ = 0 V at $T_{opr}$ = -20°C to 85°C/-40°C to 85°C unless otherwise specified.

| Symbol | Parameter | Measuring Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| - | Resolution | | | | 8 | Bits |
| - | Absolute Accuracy | | | | 2.5 | LSB |
| $t_{SU}$ | Setup Time | | | | 3 | µs |
| $R_O$ | Output Resistance | | 5 | 6 | 8.2 | kΩ |
| $I_{VREF}$ | Reference Power Supply Input Current | See Notes 1 and 2 | | | 1.5 | mA |

Notes:
1. This applies when using one D/A converter, with the D/A register for the unused D/A converter set to 00h.
2. The current consumption of the A/D converter is not included. Also, the $I_{VREF}$ of the D/A converter will flow even if the ADSTBY bit in the ADCON1 register is 0 (A/D operation stopped (standby)).

### Table 5.13 Voltage Detector 2 Electrical Characteristics

The measurement condition is $V_{CC1}$ = 2.7 to 5.5 V, $T_{opr}$ = -20°C to 85°C/-40°C to 85°C, unless otherwise specified.

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{det2}$ | Voltage detection level Vdet2_0 | When $V_{CC1}$ is falling | 3.50 | 4.00 | 4.50 | V |
| - | Hysteresis width at the rising of $V_{CC1}$ in voltage detector 2 | | | 0.15 | | V |
| - | Voltage detector 2 response time (2) | When $V_{CC1}$ falls from 5 V to (Vdet2_0 - 0.1) V | | | 200 | µs |
| - | Voltage detector self power consumption | VC27 = 1, $V_{CC1}$ = 5.0 V | | 1.8 | | µA |
| $t_{d(E-A)}$ | Waiting time until voltage detector operation starts (1) | | | | 100 | µs |

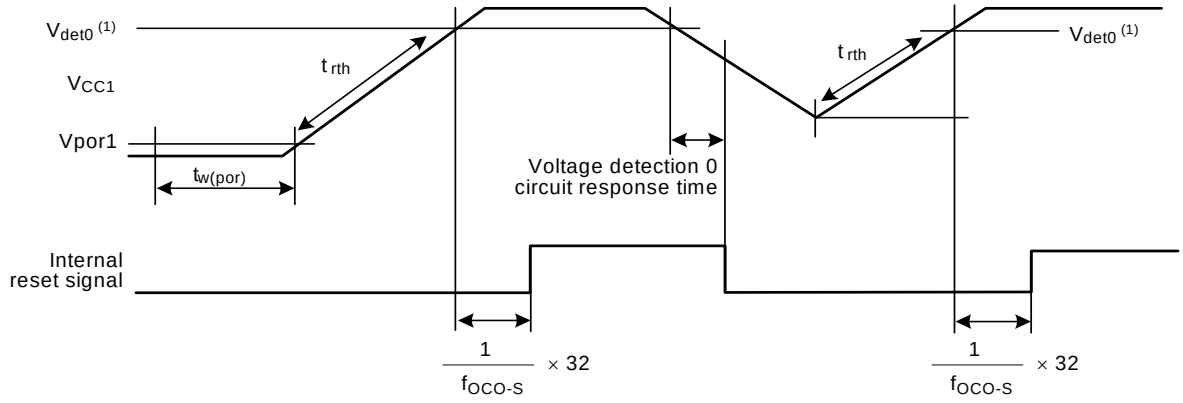
Notes:
1. Necessary time until the voltage detector operates after setting to 1 again after setting the VC27 bit in the VCR2 register to 0.
2. Time from when passing the $V_{det2}$ until when a voltage monitor 2 reset is generated.

### Table 5.14 Power-On Reset Circuit

The measurement condition is $V_{CC1}$ = 2.0 to 5.5 V, $T_{opr}$ = -20°C to 85°C/ -40°C to 85°C, unless otherwise specified.

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{por1}$ | Voltage at which power-on reset enabled (1) | | | | 0.1 | V |
| $t_{rth}$ | External power $V_{CC1}$ rise gradient | | 2.0 | | 50000 | mV/ms |
| $t_{w(por)}$ | Time necessary to enable power-on reset | | 300 | | | ms |

Note:
1. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS1 address to 0. Also, set the VDSEL1 bit to 0 (Vdet0_2).




Note:
1. $V_{det0}$ indicates the voltage detection level of the voltage detection 0 circuit.

**Figure 5.3 Power-On Reset Circuit Electrical Characteristics**

## 5.2 Electrical Characteristics ($V_{CC1}$ = $V_{CC2}$ = 5 V)

### 5.2.1 Electrical Characteristics

$V_{CC1}$ = $V_{CC2}$ = 5 V

**Table 5.19 Electrical Characteristics (1) [1]**

$V_{CC1}$ = $V_{CC2}$ = 4.2 to 5.5 V, $V_{SS}$ = 0 V at $T_{opr}$ = –20°C to 85°C/–40°C to 85°C, $f_{(BCLK)}$ = 32 MHz unless otherwise specified.

| Symbol | Parameter | | | Measuring Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | |
| $V_{OH}$ | High output voltage | P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1 | | $I_{OH}$ = –5 mA | $V_{CC1}$ – 2.0 | | $V_{CC1}$ | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7 | | $I_{OH}$ = –5 mA | $V_{CC2}$ – 2.0 | | $V_{CC2}$ | |
| $V_{OH}$ | High output voltage | P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1 | | $I_{OH}$ = –200 µA | $V_{CC1}$ – 0.3 | | $V_{CC1}$ | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7 | | $I_{OH}$ = –200 µA | $V_{CC2}$ – 0.3 | | $V_{CC2}$ | |
| $V_{OH}$ | High output voltage | XOUT | HIGH POWER | $I_{OH}$ = –1 mA | $V_{CC1}$ – 2.0 | | $V_{CC1}$ | V |
| | | | LOW POWER | $I_{OH}$ = –0.5 mA | $V_{CC1}$ – 2.0 | | $V_{CC1}$ | |
| | High output voltage | XCOUT | HIGH POWER | With no load applied | | 2.6 | | V |
| | | | LOW POWER | With no load applied | | 2.2 | | |
| $V_{OL}$ | Low output voltage | P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1 | | $I_{OL}$ = 5 mA | | | 2.0 | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7 | | $I_{OL}$ = 5 mA | | | 2.0 | |
| $V_{OL}$ | Low output voltage | P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1 | | $I_{OL}$ = 200 µA | | | 0.45 | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7 | | $I_{OL}$ = 200 µA | | | 0.45 | |
| $V_{OL}$ | Low output voltage | XOUT | HIGH POWER | $I_{OL}$ = 1 mA | | | 2.0 | V |
| | | | LOW POWER | $I_{OL}$ = 0.5 mA | | | 2.0 | |
| | Low output voltage | XCOUT | HIGH POWER | With no load applied | | 0 | | V |
| | | | LOW POWER | With no load applied | | 0 | | |

Note:
1. When $V_{CC1} \neq V_{CC2}$, refer to 5 V or 3 V standard depending on the voltage.

$V_{CC1} = V_{CC2} = 5\ V$

**Table 5.21 Electrical Characteristics (3)**

R5F36506NFA, R5F36506NFB, R5F36506DFA, R5F36506DFB, R5F3650ENFA, R5F3650ENFB, R5F3650EDFA, R5F3650EDFB

$V_{CC1} = V_{CC2} = 4.2$ to 5.5 V, $V_{SS} = 0$ V at $T_{opr} = -20°C$ to 85°C/−40°C to 85°C, $f_{(BCLK)} = 32$ MHz unless otherwise specified.

| Symbol | Parameter | Measuring Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $R_{fXCIN}$ | Feedback resistance XCIN | | | | 8 | | MΩ |
| $I_{CC}$ | Power supply current<br><br>In single-chip, mode, the output pin are open and other pins are $V_{SS}$ | High-speed mode | $f_{(BCLK)}$ = 32 MHz<br>XIN = 4 MHz (square wave), PLL multiplied by 8<br>125 kHz on-chip oscillator stopped | | 24.0 | | mA |
| | | | $f_{(BCLK)}$ =32 MHz, A/D conversion<br>XIN = 4 MHz (square wave), PLL multiplied by 8<br>125 kHz on-chip oscillator stopped | | 24.7 | | mA |
| | | | $f_{(BCLK)}$ = 20 MHz<br>XIN = 20 MHz (square wave)<br>125 kHz on-chip oscillator stopped | | 16.0 | | mA |
| | | 40 MHz on-chip oscillator mode | Main clock stopped<br>40 MHz on-chip oscillator on,<br>divide-by-4 ($f_{(BCLK)}$ = 10 MHz)<br>125 kHz on-chip oscillator stopped | | 17.0 | | mA |
| | | 125 kHz on-chip oscillator mode | Main clock stopped<br>40 MHz on-chip oscillator stopped,<br>125 kHz on-chip oscillator on, no division<br>FMR22 = 1 (slow read mode) | | 500.0 | | µA |
| | | Low-power mode | $f_{(BCLK)}$ = 32 kHz<br>In low-power mode<br>FMR22 = FMR23 = 1<br>On flash memory (1) | | 160.0 | | µA |
| | | | $f_{(BCLK)}$ = 32 kHz<br>In low-power mode<br>On RAM (1) | | 45.0 | | µA |
| | | Wait mode | Main clock stopped<br>40 MHz on-chip oscillator stopped<br>125 kHz on-chip oscillator on<br>Peripheral clock operating<br>$T_{opr}$ = 25°C | | 20.0 | | µA |
| | | | $f_{(BCLK)}$ = 32 kHz (oscillation capacity High)<br>40 MHz on-chip oscillator stopped<br>125 kHz on-chip oscillator stopped<br>Peripheral clock operating<br>$T_{opr}$ = 25°C | | 11.0 | | µA |
| | | | $f_{(BCLK)}$ = 32 kHz (oscillation capacity Low)<br>40 MHz on-chip oscillator stopped<br>125 kHz on-chip oscillator stopped<br>Peripheral clock operating<br>$T_{opr}$ = 25°C | | 6.0 | | µA |
| | | Stop mode | Main clock stopped<br>40 MHz on-chip oscillator stopped<br>125 kHz on-chip oscillator stopped<br>Peripheral clock stopped<br>$T_{opr}$ = 25°C | | 1.7 | | µA |
| | | During flash memory program | $f_{(BCLK)}$ = 10 MHz, PM17 = 1 (one wait)<br>$V_{CC1}$ = 5.0 V | | 20.0 | | mA |
| | | During flash memory erase | $f_{(BCLK)}$ = 10 MHz, PM17 = 1 (one wait)<br>$V_{CC1}$ = 5.0 V | | 30.0 | | mA |

Note:
1. This indicates the memory in which the program to be executed exists.

$V_{CC1} = V_{CC2} = 5\ V$

**Timing Requirements**

($V_{CC1} = V_{CC2} = 5$ V, $V_{SS} = 0$ V, at $T_{opr}$ = -20°C to 85°C/-40°C to 85°C unless otherwise specified)

## 5.2.3 Timing Requirements (Memory Expansion Mode and Microprocessor Mode)

**Table 5.37 Memory Expansion Mode and Microprocessor Mode**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{ac1(RD-DB)}$ | Data input access time (for setting with no wait) | | (Note 1) | ns |
| $t_{ac2(RD-DB)}$ | Data input access time (for setting with 1 to 3 waits) | | (Note 2) | ns |
| $t_{ac3(RD-DB)}$ | Data input access time (when accessing multiplex bus area) | | (Note 3) | ns |
| $t_{ac4(RD-DB)}$ | Data input access time (for setting with 2ϕ + 3ϕ or more) | | (Note 4) | ns |
| $t_{su(DB-RD)}$ | Data input setup time | 40 | | ns |
| $t_{su(RDY-BCLK)}$ | $\overline{RDY}$ input setup time | 80 | | ns |
| $t_{h(RD-DB)}$ | Data input hold time | 0 | | ns |
| $t_{h(BCLK-RDY)}$ | $\overline{RDY}$ input hold time | 0 | | ns |

Notes:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f_{(BCLK)}} - 45[ns]$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n + 0.5) \times 10^9}{f_{(BCLK)}} - 45[ns]$$ n is 1 for 1 wait setting, 2 for 2 waits setting and 3 for 3 waits setting.

3. Calculated according to the BCLK frequency as follows:

$$\frac{(n - 0.5) \times 10^9}{f_{(BCLK)}} - 45[ns]$$ n is 2 for 2 waits setting, and 3 for 3 waits setting.

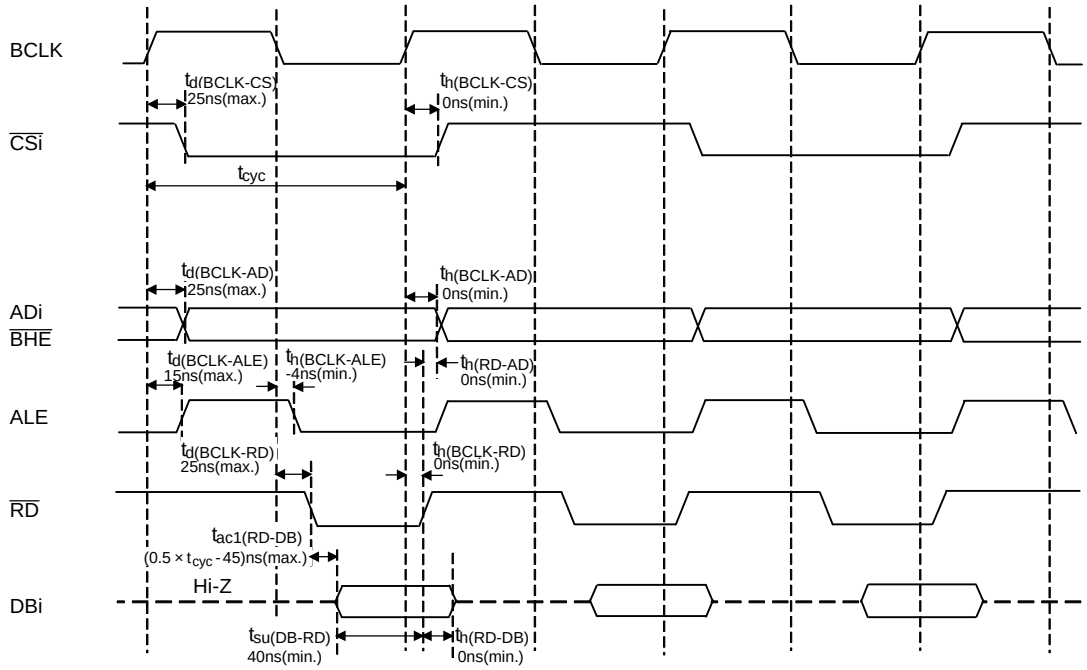
4. Calculated according to the BCLK frequency as follows:

$$\frac{n \times 10^9}{f_{(BCLK)}} - 45[ns]$$ n is 3 for 2ϕ + 3ϕ, 4 for 2ϕ + 4ϕ, 4 for 3ϕ + 4ϕ, and 5 for 4ϕ + 5ϕ.

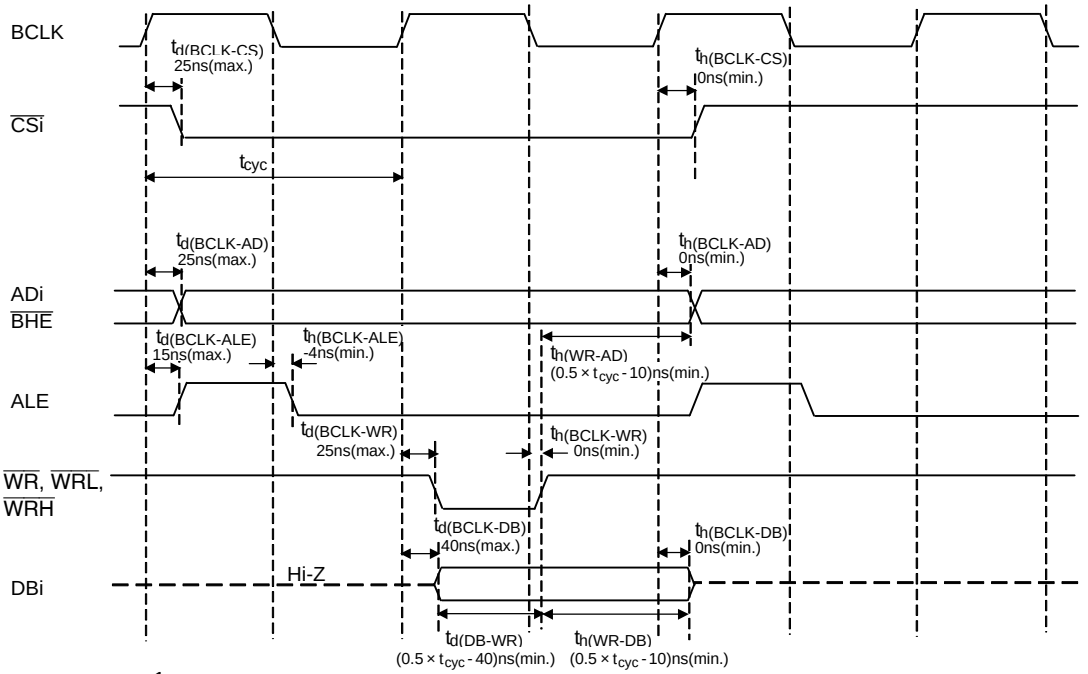
Memory Expansion Mode and Microprocessor Mode
(in no wait state setting)

$V_{CC1} = V_{CC2} = 5V$

Read timing




Write timing




$$t_{cyc} = \frac{1}{f_{(BCLK)}}$$

Measuring conditions

- $V_{CC1} = V_{CC2} = 5V$
- Input timing voltage: $V_{IL} = 0.8$ V, $V_{IH} = 2.0$ V
- Output timing voltage: $V_{OL} = 0.4$ V, $V_{OH} = 2.4$ V

**Figure 5.15 Timing Diagram**

$V_{CC1} = V_{CC2} = 5\ V$

**Switching Characteristics**

($V_{CC1} = V_{CC2} = 5$ V, $V_{SS} = 0$ V, at $T_{opr}$ = -20°C to 85°C/-40°C to 85°C unless otherwise specified)

### 5.2.4.4 In Wait State Setting 2φ + 3φ, 2φ + 4φ, 3φ + 4φ, and 4φ + 5φ, and When Accessing External Area

**Table 5.41 Memory Expansion Mode and Microprocessor Mode (in Wait State Setting 2 φ + 3 φ, 2 φ + 4φ, 3φ + 4φ, and 4φ + 5φ, and When Accessing External Area)**

| Symbol | Parameter | Measuring Condition | Standard | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| $t_{d(BCLK-AD)}$ | Address output delay time | See Figure 5.14 | | 25 | ns |
| $t_{h(BCLK-AD)}$ | Address output hold time (in relation to BCLK) | | 0 | | ns |
| $t_{h(RD-AD)}$ | Address output hold time (in relation to RD) | | 0 | | ns |
| $t_{h(WR-AD)}$ | Address output hold time (in relation to WR) | | (Note 2) | | ns |
| $t_{d(BCLK-CS)}$ | Chip select output delay time | | | 25 | ns |
| $t_{h(BCLK-CS)}$ | Chip select output hold time (in relation to BCLK) | | 0 | | ns |
| $t_{d(BCLK-ALE)}$ | ALE signal output delay time | | | 15 | ns |
| $t_{h(BCLK-ALE)}$ | ALE signal output hold time | | -4 | | ns |
| $t_{d(BCLK-RD)}$ | RD signal output delay time | | | 25 | ns |
| $t_{h(BCLK-RD)}$ | RD signal output hold time | | 0 | | ns |
| $t_{d(BCLK-WR)}$ | WR signal output delay time | | | 25 | ns |
| $t_{h(BCLK-WR)}$ | WR signal output hold time | | 0 | | ns |
| $t_{d(BCLK-DB)}$ | Data output delay time (in relation to BCLK) | | | 40 | ns |
| $t_{h(BCLK-DB)}$ | Data output hold time (in relation to BCLK) (3) | | 0 | | ns |
| $t_{d(DB-WR)}$ | Data output delay time (in relation to WR) | | (Note 1) | | ns |
| $t_{h(WR-DB)}$ | Data output hold time (in relation to WR) (3) | | (Note 2) | | ns |

Notes:

1. Calculated according to the BCLK frequency as follows:

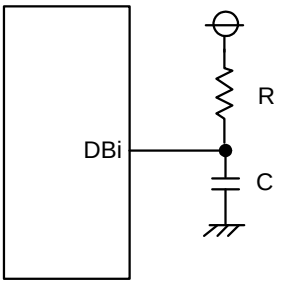
$$\frac{(n-0.5)\times 10^9}{f_{(BCLK)}} - 40[ns]$$

n is 3 for 2φ + 3φ, 4 for 2φ + 4φ, 4 for 3φ + 4φ, and 5 for 4φ + 5φ.

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5\times 10^9}{f_{(BCLK)}} - 10[ns]$$

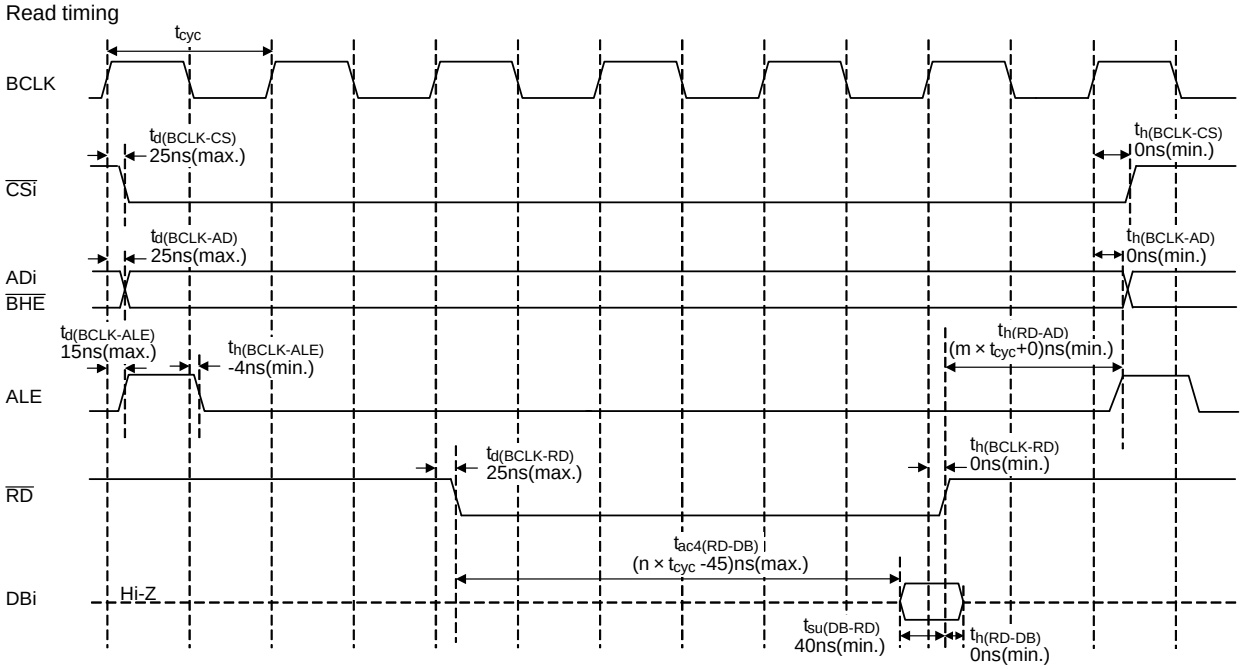
3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
Hold time of data bus is expressed in
$t = -CR \times \ln(1 - V_{OL}/V_{CC2})$
by a circuit of the right figure.
For example, when $V_{OL} = 0.2V_{CC2}$, C = 30 pF, R = 1 kΩ, hold time of output low level is
$t = -30\ pF \times 1\ k\Omega \times \ln(1 - 0.2V_{CC2}/V_{CC2})$
= 6.7 ns.



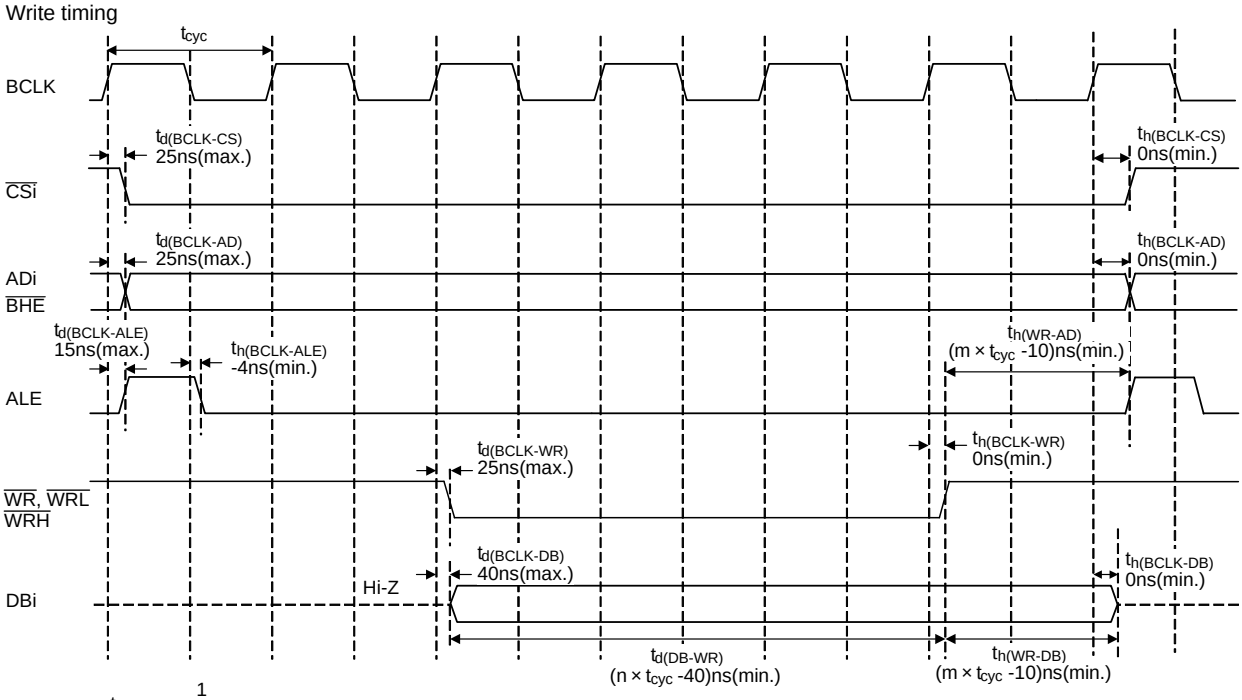
Memory Expansion Mode and Microprocessor Mode
(in wait state setting 2 ϕ + 3 ϕ, 2 ϕ + 4 ϕ, 3ϕ + 4 ϕ, and 4 ϕ + 5 ϕ, and when inserting 1 to 3 recovery cycles and accessing external area)

$V_{CC1} = V_{CC2} = 5V$

Read timing




Write timing




$$t_{cyc} = \frac{1}{f(BCLK)}$$

Measuring conditions

- $V_{CC1} = V_{CC2} = 5V$
- Input timing voltage: $V_{IL} = 0.8$ V, $V_{IH} = 2.0$ V
- Output timing voltage: $V_{OL} = 0.4$ V, $V_{OH} = 2.4$ V

n: 3 (when 2 ϕ + 3 ϕ)
4 (when 2 ϕ + 4 ϕ or 3 ϕ + 4 ϕ)
5 (when 4 ϕ + 5 ϕ)

m: 1 (when 1 recovery cycle inserted )
2 (when 2 recovery cycles inserted)
3 (when 3 recovery cycles inserted)

**Figure 5.19 Timing Diagram**

$V_{CC1} = V_{CC2} = 3\ V$

**Table 5.46 Electrical Characteristics (4)**

R5F3651RNFC, R5F3650RNFA, R5F3650RNFB, R5F3651RDFC, R5F3650RDFA, R5F3650RDFB, R5F3651TNFC, R5F3650TNFA, R5F3650TNFB, R5F3651TDFC, R5F3650TDFA, R5F3650TDFB

$V_{CC1} = V_{CC2} = 2.7$ to $3.3\ V$, $V_{SS} = 0\ V$ at $T_{opr} = -20°C$ to $85°C$/$-40°C$ to $85°C$, $f_{(BCLK)} = 32$ MHz unless otherwise specified.

| Symbol | Parameter | Measuring Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $R_{fXCIN}$ | Feedback resistance XCIN | | | | 25 | | MΩ |
| $I_{CC}$ | Power supply current<br><br>In single-chip, mode, the output pin are open and other pins are $V_{SS}$ | High-speed mode | $f_{(BCLK)}$ = 32 MHz<br>XIN = 4 MHz (square wave),<br>PLL multiplied by 8<br>125 kHz on-chip oscillator stopped | | 32.0 | | mA |
| | | | $f_{(BCLK)}$ = 32 MHz, A/D conversion<br>XIN = 4 MHz (square wave),<br>PLL multiplied by 8<br>125 kHz on-chip oscillator stopped | | 32.7 | | mA |
| | | | $f_{(BCLK)}$ = 20 MHz<br>XIN = 20 MHz (square wave)<br>125 kHz on-chip oscillator stopped | | 21.0 | | mA |
| | | 40 MHz on-chip oscillator mode | Main clock stopped<br>40 MHz on-chip oscillator on,<br>divide-by-4 (f(BCLK) = 10 MHz)<br>125 kHz on-chip oscillator stopped | | 23.0 | | mA |
| | | 125 kHz on-chip oscillator mode | Main clock stopped<br>40 MHz on-chip oscillator stopped<br>125 kHz on-chip oscillator on, no division<br>FMR22 = 1 (slow read mode) | | 750.0 | | µA |
| | | Low-power mode | $f_{(BCLK)}$ = 32 MHz<br>In low-power mode,<br>FMR 22 = FMR23 = 1<br>on flash memory (1) | | 300.0 | | µA |
| | | | $f_{(BCLK)}$ = 32 MHz<br>In low-power mode,<br>on RAM (1) | | 40.0 | | µA |
| | | Wait mode | Main clock stopped<br>40 MHz on-chip oscillator stopped<br>125 kHz on-chip oscillator on<br>Peripheral clock operating<br>$T_{opr}$ = 25°C | | 20.0 | | µA |
| | | | $f_{(BCLK)}$ = 32 MHz (oscillation capacity High)<br>40 MHz on-chip oscillator stopped<br>125 kHz on-chip oscillator stopped<br>Peripheral clock operating<br>$T_{opr}$ = 25°C | | 8.0 | | µA |
| | | | $f_{(BCLK)}$ = 32 kHz (oscillation capacity Low)<br>40 MHz on-chip oscillator stopped<br>125 kHz on-chip oscillator stopped<br>Peripheral clock operating<br>$T_{opr}$ = 25°C | | 4.0 | | µA |
| | | Stop mode | Main clock stopped<br>40 MHz on-chip oscillator stopped<br>125 kHz on-chip oscillator stopped<br>Peripheral clock stopped<br>$T_{opr}$ = 25°C | | 1.6 | | µA |
| | | During flash memory program | $f_{(BCLK)}$ = 10 MHz, PM17 = 1 (one wait)<br>$V_{CC1}$ = 3.0 V | | 20.0 | | mA |
| | | During flash memory erase | $f_{(BCLK)}$ = 10 MHz, PM17 = 1 (one wait)<br>$V_{CC1}$ = 3.0 V | | 30.0 | | mA |

Note:

1. This indicates the memory in which the program to be executed exists.

$V_{CC1} = V_{CC2} = 3\ V$

**Timing Requirements**

($V_{CC1} = V_{CC2} = 3$ V, $V_{SS} = 0$ V, at $T_{opr}$ = -20°C to 85°C/-40°C to 85°C unless otherwise specified)

### 5.3.2.3 Timer A Input

**Table 5.49 Timer A Input (Counter Input in Event Counter Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN input cycle time | 150 | | ns |
| $t_{w(TAH)}$ | TAiIN input high pulse width | 60 | | ns |
| $t_{w(TAL)}$ | TAiIN input low pulse width | 60 | | ns |

**Table 5.50 Timer A Input (Gating Input in Timer Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN input cycle time | 600 | | ns |
| $t_{w(TAH)}$ | TAiIN input high pulse width | 300 | | ns |
| $t_{w(TAL)}$ | TAiIN input low pulse width | 300 | | ns |

**Table 5.51 Timer A Input (External Trigger Input in One-Shot Timer Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN input cycle time | 300 | | ns |
| $t_{w(TAH)}$ | TAiIN input high pulse width | 150 | | ns |
| $t_{w(TAL)}$ | TAiIN input low pulse width | 150 | | ns |

**Table 5.52 Timer A Input (External Trigger Input in Pulse Width Modulation Mode and Programmable Output Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{w(TAH)}$ | TAiIN input high pulse width | 150 | | ns |
| $t_{w(TAL)}$ | TAiIN input low pulse width | 150 | | ns |

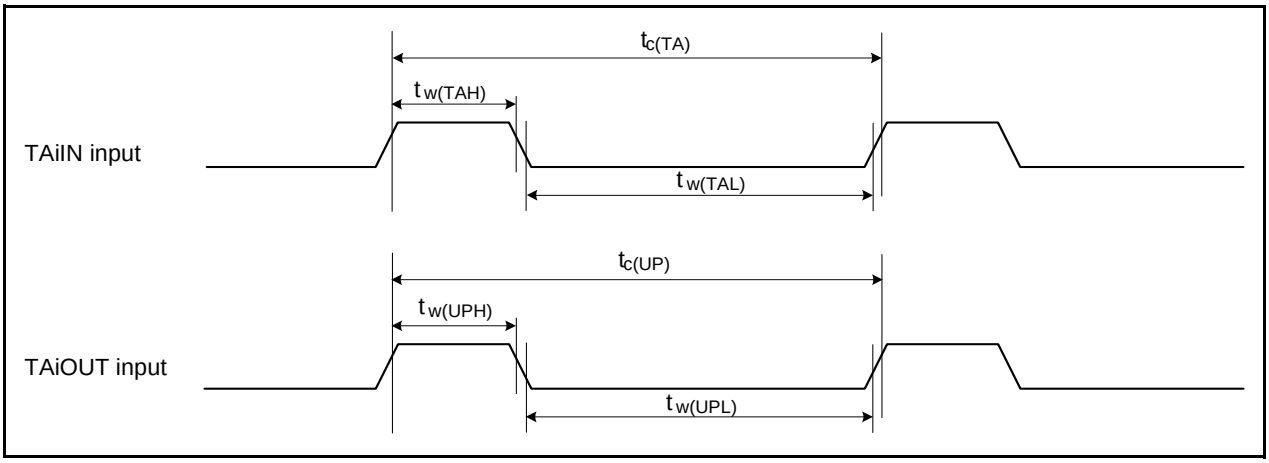



**Figure 5.22 Timer A Input**

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