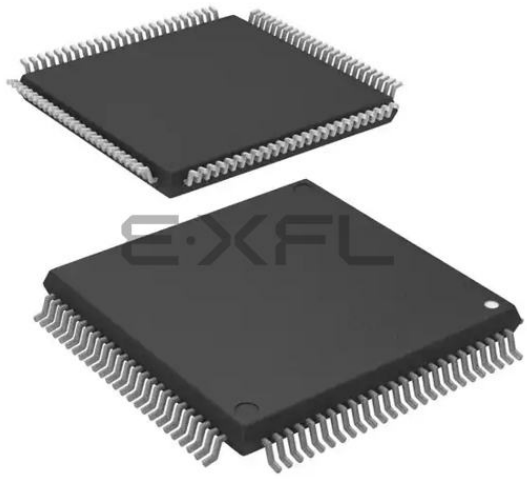
Renesas Electronics America Inc - R5F3650EDFB#30 Datasheet



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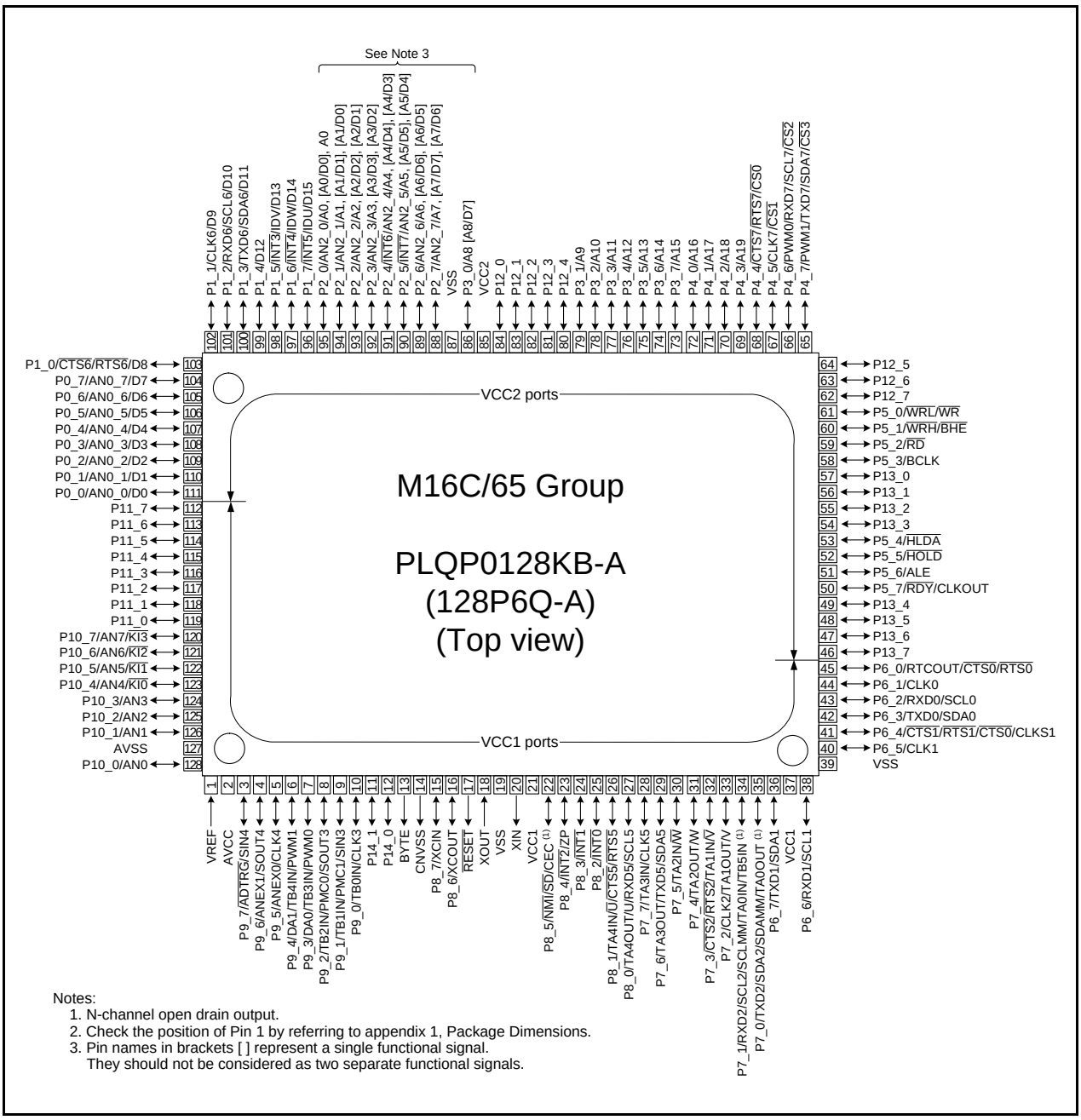
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	M16C/60
Core Size	16-Bit
Speed	32MHz
Connectivity	EBI/EMI, I²C, SIO, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	85
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f3650edfb-30

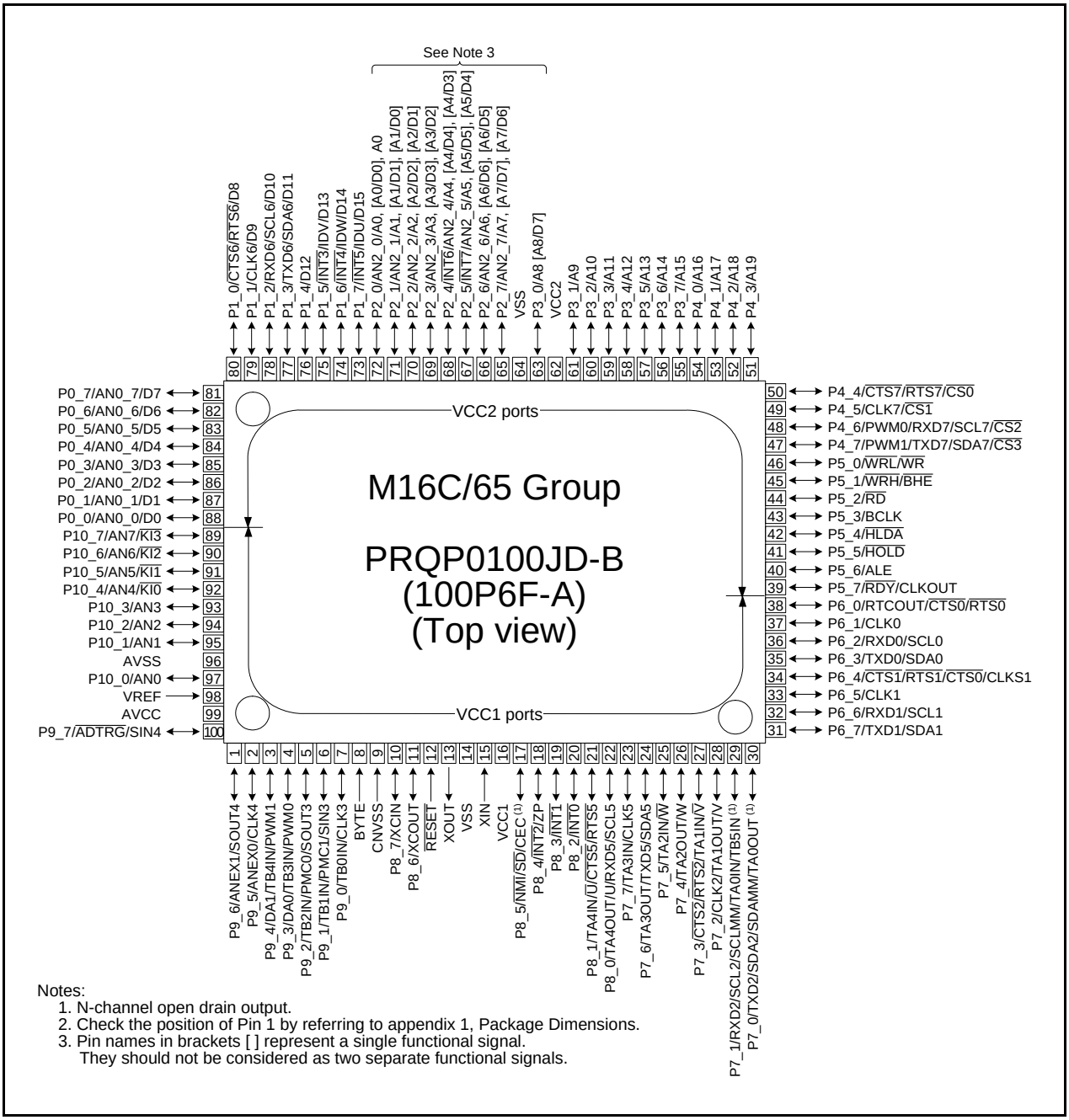
1.5 Pin Assignments

Figure 1.5 to Figure 1.7 show pin assignments. Table 1.7 to Table 1.11 list pin names.



Notes:
1. N-channel open drain output.
2. Check the position of Pin 1 by referring to appendix 1, Package Dimensions.
3. Pin names in brackets [ ] represent a single functional signal.
They should not be considered as two separate functional signals.

Figure 1.5 Pin Assignment for the 128-Pin Package



Notes:
1. N-channel open drain output.
2. Check the position of Pin 1 by referring to appendix 1, Package Dimensions.
3. Pin names in brackets [ ] represent a single functional signal.
They should not be considered as two separate functional signals.

Figure 1.6 Pin Assignment for the 100-Pin Package

Table 4.3 SFR Information (3) (1)

Address	Register	Symbol	Reset Value
0040h			
0041h			
0042h	$\overline{\text{INT7}}$ Interrupt Control Register	INT7IC	XX00 X000b
0043h	$\overline{\text{INT6}}$ Interrupt Control Register	INT6IC	XX00 X000b
0044h	$\overline{\text{INT3}}$ Interrupt Control Register	INT3IC	XX00 X000b
0045h	Timer B5 Interrupt Control Register	TB5IC	XXXX X000b
0046h	Timer B4 Interrupt Control Register UART1 Bus Collision Detection Interrupt Control Register	TB4IC U1BCNIC	XXXX X000b
0047h	Timer B3 Interrupt Control Register UART0 Bus Collision Detection Interrupt Control Register	TB3IC U0BCNIC	XXXX X000b
0048h	SI/O4 Interrupt Control Register $\overline{\text{INT5}}$ Interrupt Control Register	S4IC INT5IC	XX00 X000b
0049h	SI/O3 Interrupt Control Register $\overline{\text{INT4}}$ Interrupt Control Register	S3IC INT4IC	XX00 X000b
004Ah	UART2 Bus Collision Detection Interrupt Control Register	BCNIC	XXXX X000b
004Bh	DMA0 Interrupt Control Register	DM0IC	XXXX X000b
004Ch	DMA1 Interrupt Control Register	DM1IC	XXXX X000b
004Dh	Key Input Interrupt Control Register	KUPIC	XXXX X000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXX X000b
004Fh	UART2 Transmit Interrupt Control Register	S2TIC	XXXX X000b
0050h	UART2 Receive Interrupt Control Register	S2RIC	XXXX X000b
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXX X000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXX X000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXX X000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXX X000b
0055h	Timer A0 Interrupt Control Register	TA0IC	XXXX X000b
0056h	Timer A1 Interrupt Control Register	TA1IC	XXXX X000b
0057h	Timer A2 Interrupt Control Register	TA2IC	XXXX X000b
0058h	Timer A3 Interrupt Control Register	TA3IC	XXXX X000b
0059h	Timer A4 Interrupt Control Register	TA4IC	XXXX X000b
005Ah	Timer B0 Interrupt Control Register	TB0IC	XXXX X000b
005Bh	Timer B1 Interrupt Control Register	TB1IC	XXXX X000b
005Ch	Timer B2 Interrupt Control Register	TB2IC	XXXX X000b
005Dh	$\overline{\text{INT0}}$ Interrupt Control Register	INT0IC	XX00 X000b
005Eh	$\overline{\text{INT1}}$ Interrupt Control Register	INT1IC	XX00 X000b
005Fh	$\overline{\text{INT2}}$ Interrupt Control Register	INT2IC	XX00 X000b

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.10 SFR Information (10) (1)

Address	Register	Symbol	Reset Value
0270h	SI/O3 Transmit/Receive Register	S3TRR	XXh
0271h			
0272h	SI/O3 Control Register	S3C	0100 0000b
0273h	SI/O3 Bit Rate Register	S3BRG	XXh
0274h	SI/O4 Transmit/Receive Register	S4TRR	XXh
0275h			
0276h	SI/O4 Control Register	S4C	0100 0000b
0277h	SI/O4 Bit Rate Register	S4BRG	XXh
0278h	SI/O3, 4 Control Register 2	S34C2	00XX X0X0b
0279h			
027Ah			
027Bh			
027Ch			
027Dh			
027Eh			
027Fh			
0280h			
0281h			
0282h			
0283h			
0284h	UART5 Special Mode Register 4	U5SMR4	00h
0285h	UART5 Special Mode Register 3	U5SMR3	000X 0X0Xb
0286h	UART5 Special Mode Register 2	U5SMR2	X000 0000b
0287h	UART5 Special Mode Register	U5SMR	X000 0000b
0288h	UART5 Transmit/Receive Mode Register	U5MR	00h
0289h	UART5 Bit Rate Register	U5BRG	XXh
028Ah	UART5 Transmit Buffer Register	U5TB	XXh
028Bh			XXh
028Ch	UART5 Transmit/Receive Control Register 0	U5C0	0000 1000b
028Dh	UART5 Transmit/Receive Control Register 1	U5C1	0000 0010b
028Eh	UART5 Receive Buffer Register	U5RB	XXh
028Fh			XXh
0290h			
0291h			
0292h			
0293h			
0294h	UART6 Special Mode Register 4	U6SMR4	00h
0295h	UART6 Special Mode Register 3	U6SMR3	000X 0X0Xb
0296h	UART6 Special Mode Register 2	U6SMR2	X000 0000b
0297h	UART6 Special Mode Register	U6SMR	X000 0000b
0298h	UART6 Transmit/Receive Mode Register	U6MR	00h
0299h	UART6 Bit Rate Register	U6BRG	XXh
029Ah	UART6 Transmit Buffer Register	U6TB	XXh
029Bh			XXh
029Ch	UART6 Transmit/Receive Control Register 0	U6C0	0000 1000b
029Dh	UART6 Transmit/Receive Control Register 1	U6C1	0000 0010b
029Eh	UART6 Receive Buffer Register	U6RB	XXh
029Fh			XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.15 SFR Information (15) (1)

Address	Register	Symbol	Reset Value
0390h	DMA2 Source Select Register	DM2SL	00h
0391h			
0392h	DMA3 Source Select Register	DM3SL	00h
0393h			
0394h			
0395h			
0396h			
0397h			
0398h	DMA0 Source Select Register	DM0SL	00h
0399h			
039Ah	DMA1 Source Select Register	DM1SL	00h
039Bh			
039Ch			
039Dh			
039Eh			
039Fh			
03A0h			
03A1h			
03A2h	Open-Circuit Detection Assist Function Register	AINRST	XX00 XXXXb
03A3h			
03A4h			
03A5h			
03A6h			
03A7h			
03A8h			
03A9h			
03AAh			
03ABh			
03ACh			
03ADh			
03AEh			
03AFh			
03B0h			
03B1h			
03B2h			
03B3h			
03B4h	SFR Snoop Address Register	CRCSAR	XXXX XXXXb
03B5h			00XX XXXXb
03B6h	CRC Mode Register	CRCMR	0XXX XXX0b
03B7h			
03B8h			
03B9h			
03BAh			
03BBh			
03BCh	CRC Data Register	CRCD	XXh
03BDh			XXh
03BEh	CRC Input Register	CRCIN	XXh
03BFh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 5.3 Recommended Operating Conditions (2/3)

V_{CC1} = V_{CC2} = 2.7 to 5.5 V at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified.

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
$I_{OL(sum)}$	Low peak output current	Sum of $I_{OL(peak)}$ at P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0 to P14_1			80.0	mA
		Sum of $I_{OL(peak)}$ at P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_5, P12_0 to P12_7, P13_0 to P13_7			80.0	mA
$I_{OL(peak)}$	Low peak output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			10.0	mA
$I_{OL(avg)}$	Low average output current (1)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			5.0	mA
$f_{(XIN)}$	Main clock input oscillation frequency	V_{CC1} = 2.7 V to 5.5 V	2		20	MHz
$f_{(XCIN)}$	Sub clock oscillation frequency			32.768	50	kHz
$f_{(PLL)}$	PLL clock oscillation frequency	V_{CC1} = 2.7 V to 5.5 V	10		32	MHz
$f_{(BCLK)}$	CPU operation clock		2		32	MHz
$t_{SU(PLL)}$	PLL frequency synthesizer stabilization wait time	V_{CC1} = 5.0 V			2	ms
		V_{CC1} = 3.0 V			3	ms

Note:
1. The average output current is the mean value within 100 ms.

5.1.5 Flash Memory Electrical Characteristics

Table 5.8 CPU Clock When Operating Flash Memory ($f_{(BCLK)}$)

V_{CC1} = 2.7 to 5.5 V, T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified.

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
-	CPU rewrite mode				10 (1)	MHz
f(SLOW_R)	Slow read mode				5 (3)	MHz
-	Low current consumption read mode			fC(32.768)	35	kHz
-	Data flash read	2.7 V ≤ V_{CC1} ≤ 3.0 V			16 (2)	MHz
		3.0 V < V_{CC1} ≤ 5.5 V			20 (2)	MHz

Notes:
1. Set the PM17 bit in the PM1 register to 1 (one wait).
2. When the frequency is over this value, set the FMR17 bit in the FMR1 register to 0 (one wait) or the PM17 bit in the PM1 register to 1 (one wait)
3. Set the PM17 bit in the PM1 register to 1 (one wait). When using 125 kHz on-chip oscillator clock or sub clock as the CPU clock source, a wait is not necessary.

Table 5.9 Flash Memory (Program ROM 1, 2) Electrical Characteristics

V_{CC1} = 2.7 to 5.5 V at T_{opr} = 0°C to 60°C (option: -40°C to 85°C), unless otherwise specified.

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
-	Program and erase cycles (1), (3), (4)	V_{CC1} = 3.3 V, T_{opr} = 25°C	1,000 (2)			times
-	2 word program time	V_{CC1} = 3.3 V, T_{opr} = 25°C		150	4000	µs
-	Lock bit program time	V_{CC1} = 3.3 V, T_{opr} = 25°C		70	3000	µs
-	Block erase time	V_{CC1} = 3.3 V, T_{opr} = 25°C		0.2	3.0	s
-	Program, erase voltage		2.7		5.5	V
-	Read voltage	T_{opr}= -20°C to 85°C/-40°C to 85°C	2.7		5.5	V
-	Program, erase temperature		0		60	°C
t_{PS}	Flash memory circuit stabilization wait time				50	µs
-	Data hold time (6)	Ambient temperature = 55°C	20			year

Notes:
1. Definition of program and erase cycles:
   The program and erase cycles refer to the number of per-block erasures. If the program and erase cycles are n (n = 1,000), each block can be erased n times. For example, if a block is erased after writing 2 word data 16,384 times, each to a different address, this counts as one program and erase cycles. Data cannot be written to the same address more than once without erasing the block (rewrite prohibited).
2. Cycles to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
3. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. It is advisable to retain data on the erasure cycles of each block and limit the number of erase operations to a certain number.
4. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
5. Customers desiring program/erase failure rate information should contact a Renesas Electronics sales office.
6. The data hold time includes time that the power supply is off or the clock is not supplied.

$V_{CC1} = V_{CC2} = 5\ V$

Table 5.23 Electrical Characteristics (5)

R5F3651RNFC, R5F3650RNFA, R5F3650RNFB, R5F3651RDFC, R5F3650RDFA, R5F3650RDFB, R5F3651TNFC, R5F3650TNFA, R5F3650TNFB, R5F3651TDFC, R5F3650TDFA, R5F3650TDFB

$V_{CC1} = V_{CC2} = 4.2$ to 5.5 V, $V_{SS} = 0$ V at $T_{opr} = -20$ to 85°C/−40 to 85°C, $f_{(BCLK)} = 32$ MHz unless otherwise specified.

Symbol	Parameter	Measuring Condition		Standard			Unit
				Min.	Typ.	Max.	
R_{fXCIN}	Feedback resistance XCIN				15		MΩ
I_{CC}	Power supply current In single-chip, mode, the output pin are open and other pins are V_{SS}	High-speed mode	$f_{(BCLK)}$ = 32 MHz XIN = 4 MHz (square wave), PLL multiplied by 8 125 kHz on-chip oscillator stopped		32.0		mA
			$f_{(BCLK)}$ = 32 MHz, A/D conversion XIN = 4 MHz (square wave), PLL multiplied by 8 125 kHz on-chip oscillator stopped		32.7		mA
			$f_{(BCLK)}$ = 20 MHz XIN = 20 MHz (square wave) 125 kHz on-chip oscillator stopped		21.0		mA
		40 MHz on-chip oscillator mode	Main clock stopped 40 MHz on-chip oscillator on, divide-by-4 (f(BCLK) = 10 MHz) 125 kHz on-chip oscillator stopped		23.0		mA
		125 kHz on-chip oscillator mode	Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator on, no division FMR22 = 1 (slow read mode)		750.0		µA
		Low-power mode	$f_{(BCLK)}$ = 32 kHz In low-power mode FMR22 = FMR23 = 1 on flash memory (1)		250.0		µA
			$f_{(BCLK)}$ = 32 kHz In low-power mode on RAM (1)		45.0		µA
		Wait mode	Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator on Peripheral clock operating T_{opr} = 25°C		21.0		µA
			$f_{(BCLK)}$ = 32 kHz (oscillation capacity High) 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator stopped Peripheral clock operating T_{opr} = 25°C		11.0		µA
			$f_{(BCLK)}$ = 32 kHz (oscillation capacity Low) 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator stopped Peripheral clock operating T_{opr} = 25°C		6.0		µA
		Stop mode	Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator stopped Peripheral clock stopped T_{opr} = 25°C		1.7		µA
		During flash memory program	$f_{(BCLK)}$ = 10 MHz, PM17 = 1 (one wait) V_{CC1} = 5.0 V		20.0		mA
		During flash memory erase	$f_{(BCLK)}$ = 10 MHz, PM17 = 1 (one wait) V_{CC1} = 5.0 V		30.0		mA

Note:
1. This indicates the memory in which the program to be executed exists.

$V_{CC1} = V_{CC2} = 5\ V$

5.2.2 Timing Requirements (Peripheral Functions and Others)

($V_{CC1} = V_{CC2} = 5$ V, $V_{SS} = 0$ V, at $T_{opr} = -20°C$ to 85°C/-40°C to 85°C unless otherwise specified)

5.2.2.1 Reset Input ($\overline{\text{RESET}}$ Input)

Table 5.24 Reset Input ($\overline{\text{RESET}}$ Input)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(RSTL)}$	$\overline{\text{RESET}}$ input low pulse width	10		µs

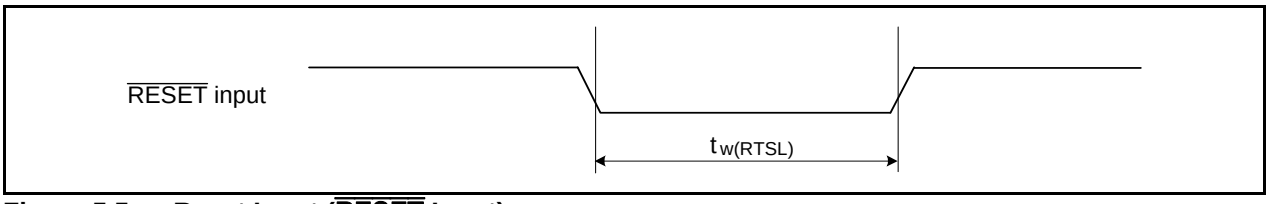


Figure 5.5 Reset Input ($\overline{\text{RESET}}$ Input)

5.2.2.2 External Clock Input

Table 5.25 External Clock Input (XIN Input) (1)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External clock input cycle time	50		ns
$t_{w(H)}$	External clock input high pulse width	20		ns
$t_{w(L)}$	External clock input low pulse width	20		ns
t_r	External clock rise time		9	ns
t_f	External clock fall time		9	ns

Note:
1. The condition is $V_{CC1} = V_{CC2} = 3.0$ to 5.0 V.

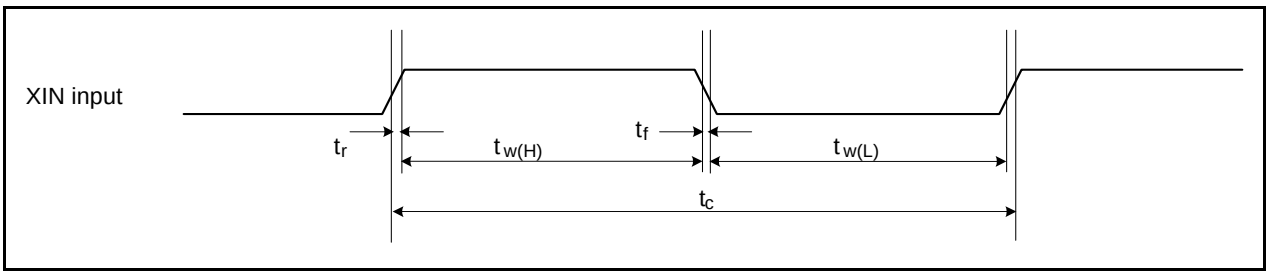


Figure 5.6 External Clock Input (XIN Input)

$V_{CC1} = V_{CC2} = 5\ V$

Timing Requirements

($V_{CC1} = V_{CC2} = 5$ V, $V_{SS} = 0$ V, at $T_{opr} = -20°C$ to 85°C/-40°C to 85°C unless otherwise specified)

5.2.2.4 Timer B Input

Table 5.31 Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBiIN input high pulse width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBiIN input low pulse width (counted on one edge)	40		ns
$t_{c(TB)}$	TBiIN input cycle time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBiIN input high pulse width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBiIN input low pulse width (counted on both edges)	80		ns

Table 5.32 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	400		ns
$t_{w(TBH)}$	TBiIN input high pulse width	200		ns
$t_{w(TBL)}$	TBiIN input low pulse width	200		ns

Table 5.33 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	400		ns
$t_{w(TBH)}$	TBiIN input high pulse width	200		ns
$t_{w(TBL)}$	TBiIN input low pulse width	200		ns

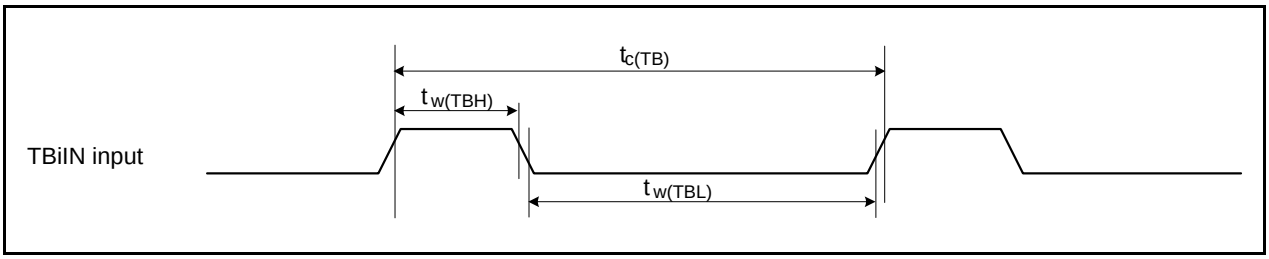


Figure 5.9 Timer B Input

$V_{CC1} = V_{CC2} = 3\ V$

Table 5.44 Electrical Characteristics (2)

R5F36506NFA, R5F36506NFB, R5F36506DFA, R5F36506DFB, R5F3650ENFA, R5F3650ENFB, R5F3650EDFA, R5F3650EDFB

$V_{CC1} = V_{CC2} = 2.7$ to 3.3 V, $V_{SS} = 0$ V at $T_{opr} = -20°C$ to 85°C/–40°C to 85°C, $f_{(BCLK)} = 32$ MHz unless otherwise specified.

Symbol	Parameter	Measuring Condition		Standard			Unit
				Min.	Typ.	Max.	
R_{fXCIN}	Feedback resistance XCIN				16		MΩ
I_{CC}	Power supply current In single-chip, mode, the output pin are open and other pins are V_{SS}	High-speed mode	$f_{(BCLK)}$ = 32 MHz XIN = 4 MHz (square wave), PLL multiplied by 8 125 kHz on-chip oscillator stopped		24.0		mA
			$f_{(BCLK)}$ = 32 MHz, A/D conversion XIN = 4 MHz (square wave), PLL multiplied by 8 125 kHz on-chip oscillator stopped		24.7		mA
			$f_{(BCLK)}$ = 20 MHz XIN = 20 MHz (square wave) 125 kHz on-chip oscillator stopped		16.0		mA
		40 MHz on-chip oscillator mode	Main clock stopped 40 MHz on-chip oscillator on, divide-by-4 ($f_{(BCLK)}$ = 10 MHz) 125 kHz on-chip oscillator stopped		17.0		mA
		125 kHz on-chip oscillator mode	Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator on, no division FMR22 = 1 (slow read mode)		450.0		µA
		Low-power mode	$f_{(BCLK)}$ = 32 MHz In low-power mode FMR 22 = FMR23 = 1 On flash memory (1)		160.0		µA
			$f_{(BCLK)}$ = 32 MHz In low-power mode On RAM (1)		40.0		µA
		Wait mode	Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator on Peripheral clock operating T_{opr} = 25°C		20.0		µA
			$f_{(BCLK)}$ = 32 MHz (oscillation capacity High) 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator stopped Peripheral clock operating T_{opr} = 25°C		8.0		µA
			$f_{(BCLK)}$ = 32 kHz (oscillation capacity Low) 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator stopped Peripheral clock operating T_{opr} = 25°C		4.0		µA
		Stop mode	Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator stopped Peripheral clock stopped T_{opr} = 25°C		1.6		µA
		During flash memory program	$f_{(BCLK)}$ = 10 MHz, PM17 = 1 (one wait) V_{CC1} = 3.0 V		20.0		mA
		During flash memory erase	$f_{(BCLK)}$ = 10 MHz, PM17 = 1 (one wait) V_{CC1} = 3.0 V		30.0		mA

Note:
1. This indicates the memory in which the program to be executed exists.

$V_{CC1} = V_{CC2} = 3\ V$

Timing Requirements

($V_{CC1} = V_{CC2} = 3$ V, $V_{SS} = 0$ V, at $T_{opr} = -20°C$ to 85°C/-40°C to 85°C unless otherwise specified)

5.3.2.4 Timer B Input

Table 5.54 Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (counted on one edge)	150		ns
$t_{w(TBH)}$	TBiIN input high pulse width (counted on one edge)	60		ns
$t_{w(TBL)}$	TBiIN input low pulse width (counted on one edge)	60		ns
$t_{c(TB)}$	TBiIN input cycle time (counted on both edges)	300		ns
$t_{w(TBH)}$	TBiIN input high pulse width (counted on both edges)	120		ns
$t_{w(TBL)}$	TBiIN input low pulse width (counted on both edges)	120		ns

Table 5.55 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	600		ns
$t_{w(TBH)}$	TBiIN input high pulse width	300		ns
$t_{w(TBL)}$	TBiIN input low pulse width	300		ns

Table 5.56 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	600		ns
$t_{w(TBH)}$	TBiIN input high pulse width	300		ns
$t^{w(TBL)}$	TBiIN input low pulse width	300		ns

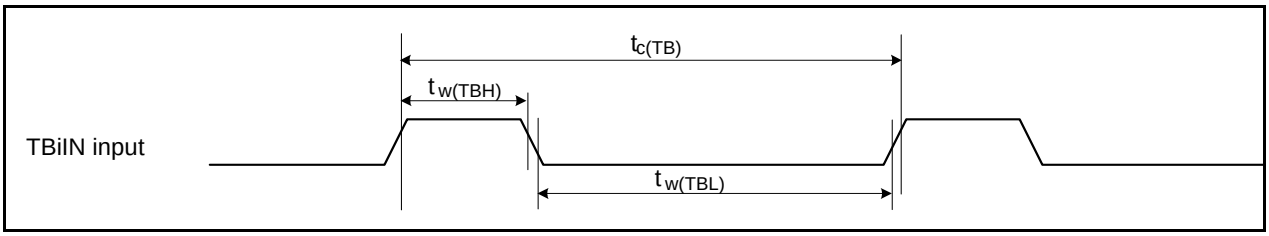


Figure 5.24 Timer B Input

$V_{CC1} = V_{CC2} = 3\ V$

Timing Requirements

($V_{CC1} = V_{CC2} = 3$ V, $V_{SS} = 0$ V, at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified)

5.3.2.5 Serial Interface

Table 5.57 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300		ns
$t_{w(CKH)}$	CLKi input high pulse width	150		ns
$t_{w(CKL)}$	CLKi input low pulse width	150		ns
$t_{d(C-Q)}$	TXDi output delay time		160	ns
$t_{h(C-Q)}$	TXDi hold time	0		ns
$t_{su(D-C)}$	RXDi input setup time	100		ns
$t_{h(C-D)}$	RXDi input hold time	90		ns

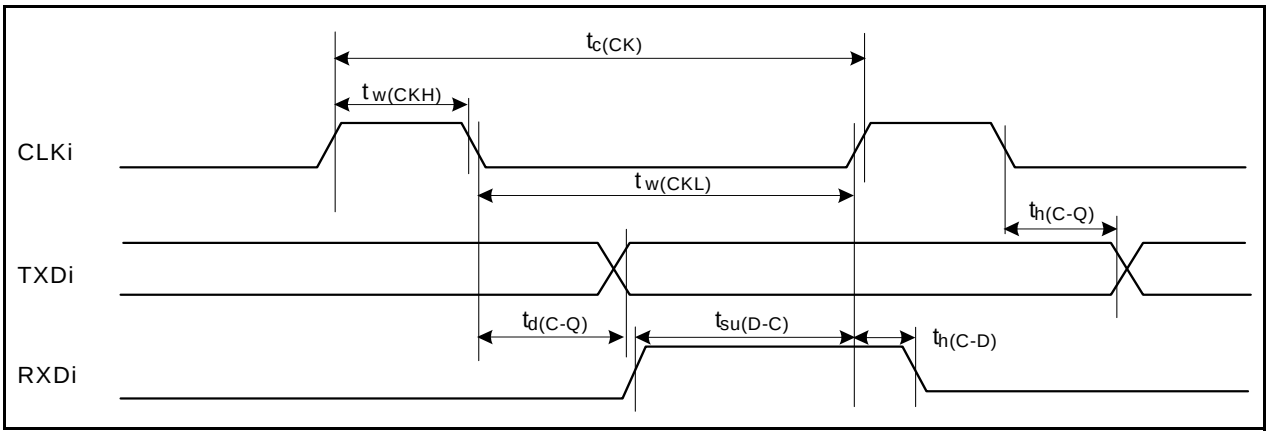


Figure 5.25 Serial Interface

5.3.2.6 External Interrupt $\overline{INTi}$ Input

Table 5.58 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input high pulse width	380		ns
$t_{w(INL)}$	$\overline{INTi}$ input low pulse width	380		ns

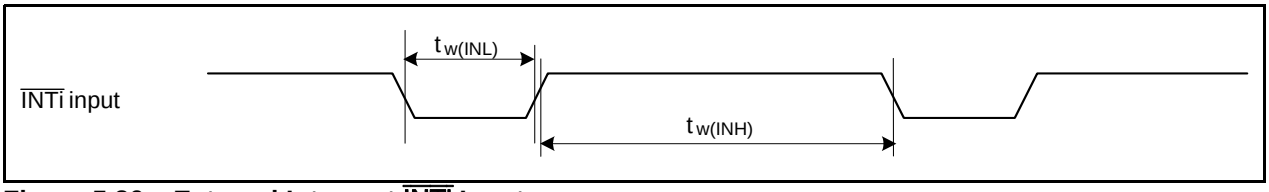


Figure 5.26 External Interrupt $\overline{INTi}$ Input

$V_{CC1} = V_{CC2} = 3\ V$

Timing Requirements

($V_{CC1} = V_{CC2} = 3$ V, $V_{SS} = 0$ V, at $T_{opr} = -20°C$ to 85°C/-40°C to 85°C unless otherwise specified)

5.3.2.7 Multi-master I²C-bus

Table 5.59 Multi-master I²C-bus

Symbol	Parameter	Standard Clock Mode		Fast-mode		Unit
		Min.	Max.	Min.	Max.	
t_{BUF}	Bus free time	4.7		1.3		µs
$t_{HD;STA}$	Hold time in start condition	4.0		0.6		µs
t_{LOW}	Hold time in SCL clock 0 status	4.7		1.3		µs
t_R	SCL, SDA signals' rising time		1000	20 + 0.1 Cb	300	ns
$t_{HD;DAT}$	Data hold time	0		0	0.9	µs
t_{HIGH}	Hold time in SCL clock 1 status	4.0		0.6		µs
f_F	SCL, SDA signals' falling time		300	20 + 0.1 Cb	300	ns
$t_{su;DAT}$	Data setup time	250		100		ns
$t_{su;STA}$	Setup time in restart condition	4.7		0.6		µs
$t_{su;STO}$	Stop condition setup time	4.0		0.6		µs

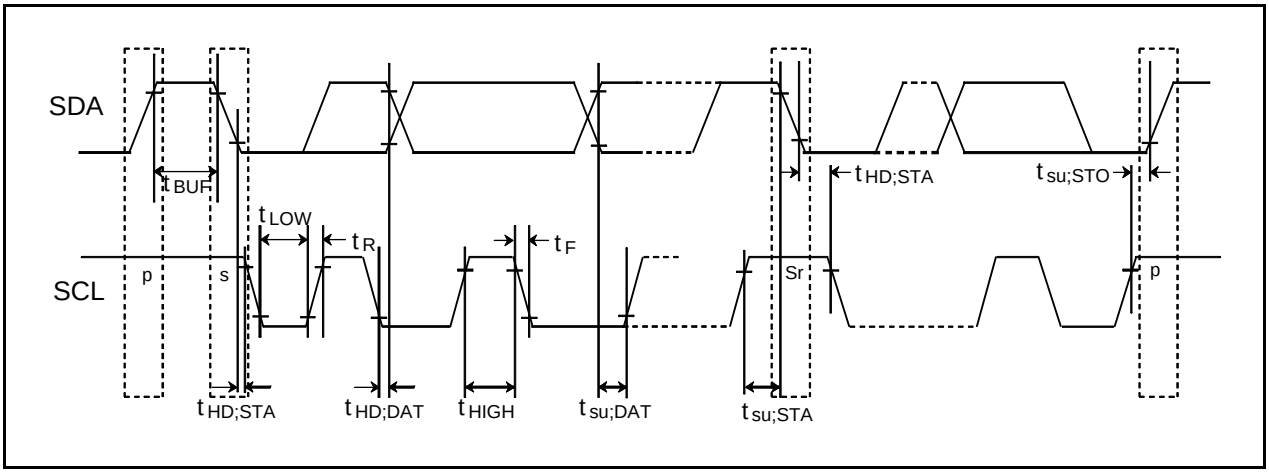


Figure 5.27 Multi-master I²C-bus

$V_{CC1} = V_{CC2} = 3\ V$

5.3.4 Switching Characteristics (Memory Expansion Mode and Microprocessor Mode)

($V_{CC1} = V_{CC2} = 3$ V, $V_{SS} = 0$ V, at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified)

5.3.4.1 In No Wait State Setting

Table 5.61 Memory Expansion and Microprocessor Modes (in No Wait State Setting)

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	See Figure 5.29		30	ns
$t_{h(BCLK-AD)}$	Address output hold time (in relation to BCLK)		0		ns
$t_{h(RD-AD)}$	Address output hold time (in relation to RD)		0		ns
$t_{h(WR-AD)}$	Address output hold time (in relation to WR)		(Note 2)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			30	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (in relation to BCLK)		0		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			25	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		–4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			30	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			30	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (in relation to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data output hold time (in relation to BCLK) (3)		0		ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(Note 1)		ns
$t_{h(WR-DB)}$	Data output hold time (in relation to WR) (3)		(Note 2)		ns

Notes:

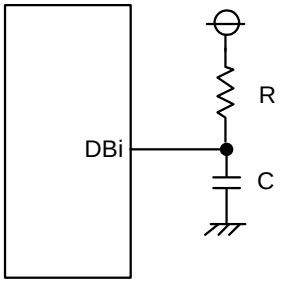
1. Calculated according to the BCLK frequency as follows:

   $\frac{0.5 \times 10^9}{f_{(BCLK)}} - 40[ns]$ $f_{(BCLK)}$ is 12.5 MHz or less.

2. Calculated according to the BCLK frequency as follows:

   $\frac{0.5 \times 10^9}{f_{(BCLK)}} - 10[ns]$

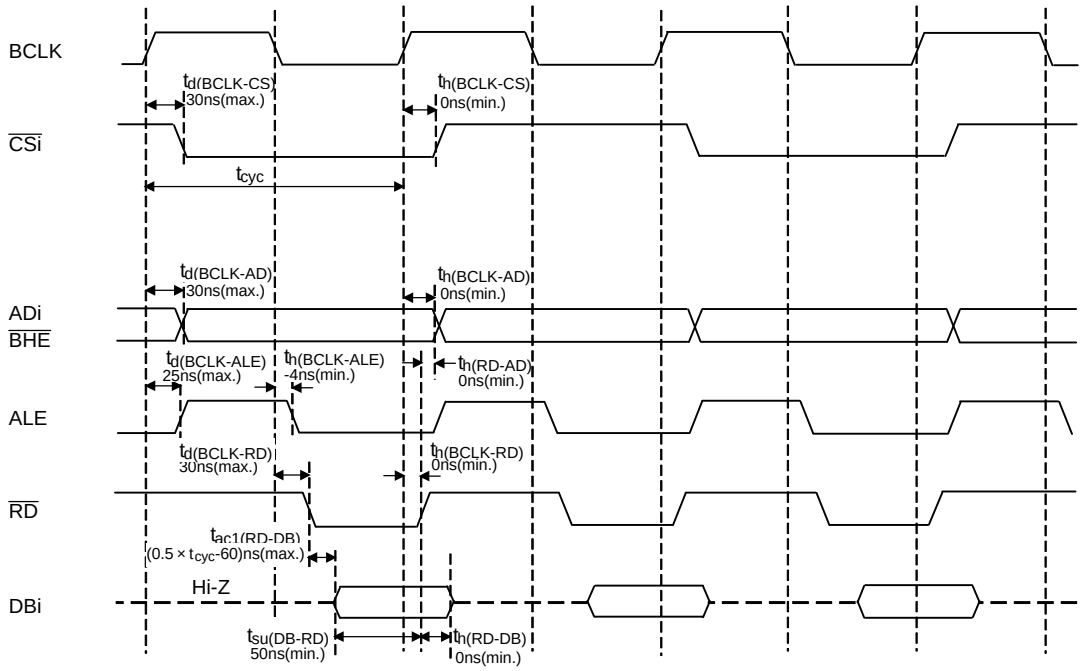
3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
   Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
   Hold time of data bus is expressed in
   $t = -CR \times \ln(1 - V_{OL}/V_{CC2})$
   by a circuit of the right figure.
   For example, when $V_{OL} = 0.2V_{CC2}$, C = 30 pF, R = 1 kΩ,
   hold time of output low level is
   $t = -30\ pF \times 1\ k\Omega \times \ln(1 - 0.2V_{CC2}/V_{CC2})$
   = 6.7 ns.



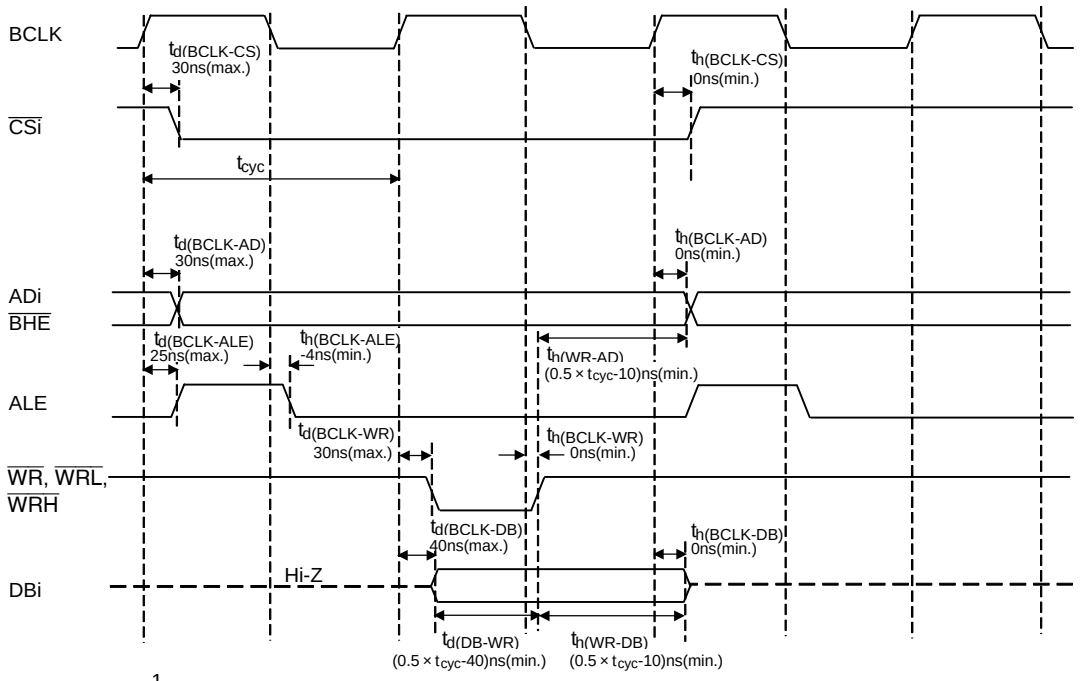
Memory Expansion Mode and Microprocessor Mode
(in no wait state setting)

$V_{CC1} = V_{CC2} = 3V$

Read timing



Write timing



$$t_{cyc} = \frac{1}{f_{(BCLK)}}$$

Measuring conditions

- $V_{CC1} = V_{CC2} = 3V$
- Input timing voltage: $V_{IL} = 0.6$ V, $V_{IH} = 2.4$ V
- Output timing voltage: $V_{OL} = 1.5$ V, $V_{OH} = 1.5$ V

Figure 5.30 Timing Diagram

$V_{CC1} = V_{CC2} = 3\ V$

Switching Characteristics

($V_{CC1} = V_{CC2} = 3$ V, $V_{SS} = 0$ V, at $T_{opr} = -20°C$ to 85°C/-40°C to 85°C unless otherwise specified)

5.3.4.4 In Wait State Setting 2φ + 3φ, 2φ + 4φ, 3φ + 4φ, and 4φ + 5φ, and When Accessing External Area

Table 5.64 Memory Expansion and Microprocessor Modes (in Wait State Setting 2φ + 3φ, 2φ + 4φ, 3φ + 4φ, and 4φ + 5φ, and When Accessing External Area)

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	See Figure 5.29		30	ns
$t_{h(BCLK-AD)}$	Address output hold time (in relation to BCLK)		0		ns
$t_{h(RD-AD)}$	Address output hold time (in relation to RD)		0		ns
$t_{h(WR-AD)}$	Address output hold time (in relation to WR)		(Note 2)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			30	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (in relation to BCLK)		0		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			25	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		-4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			30	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			30	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (in relation to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data output hold time (in relation to BCLK) (3)		0		ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(Note 1)		ns
$t_{h(WR-DB)}$	Data output hold time (in relation to WR) (3)		(Note 2)		ns

Notes:

1. Calculated according to the BCLK frequency as follows:

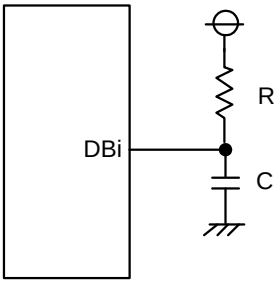
$$\frac{(n-0.5)\times 10^9}{f_{(BCLK)}} - 40[ns]$$

n is 3 for 2φ + 3φ, 4 for 2φ + 4φ, 4 for 3φ + 4φ, and 5 for 4φ + 5φ.

2. Calculated according to the BCLK frequency as follows:

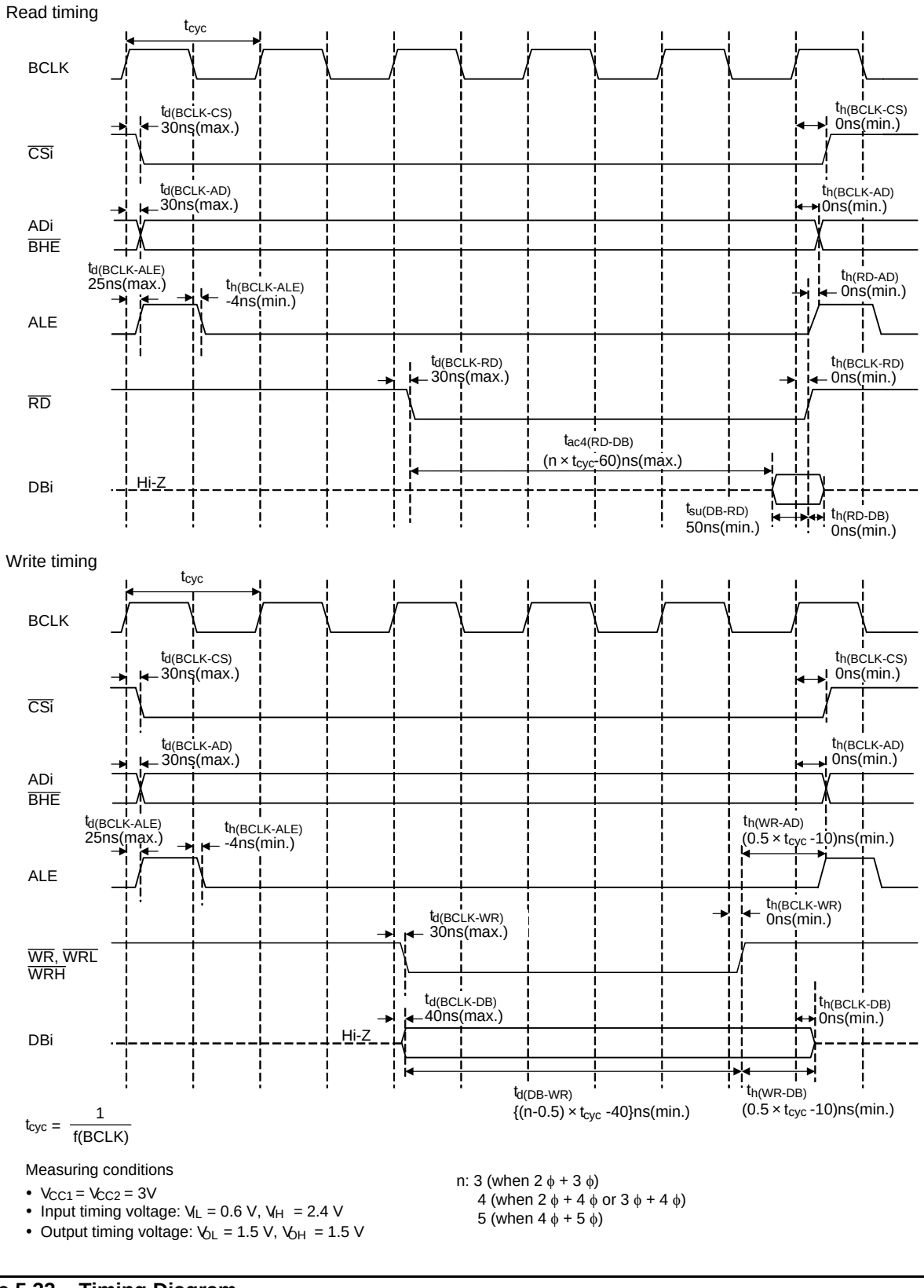
$$\frac{0.5\times 10^9}{f_{(BCLK)}} - 10[ns]$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
Hold time of data bus is expressed in
$t = -CR \times \ln(1 - V_{OL}/V_{CC2})$
by a circuit of the right figure.
For example, when $V_{OL} = 0.2V_{CC2}$, C = 30 pF, R = 1 kΩ, hold time of output low level is
$t = -30\ pF \times 1\ k\Omega \times \ln(1 - 0.2V_{CC2}/V_{CC2})$
= 6.7 ns.



Memory Expansion Mode, Microprocessor Mode
(in wait state setting 2 ϕ + 3 ϕ, 2 ϕ + 4 ϕ, 3ϕ + 4 ϕ, and 4 ϕ + 5 ϕ, and when accessing external area)

$V_{CC1} = V_{CC2} = 3V$



$t_{cyc} = \frac{1}{f(BCLK)}$

Measuring conditions

- $V_{CC1} = V_{CC2} = 3V$
- Input timing voltage: $V_{IL} = 0.6$ V, $V_{IH} = 2.4$ V
- Output timing voltage: $V_{OL} = 1.5$ V, $V_{OH} = 1.5$ V

n: 3 (when 2 ϕ + 3 ϕ)
4 (when 2 ϕ + 4 ϕ or 3 ϕ + 4 ϕ)
5 (when 4 ϕ + 5 ϕ)

Figure 5.33 Timing Diagram

REVISION HISTORY	M16C/65 Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	Feb 02, 2009	-	First Edition issued.
1.10	Sep 24, 2009	3	Table 1.2 Specifications for the 128-Pin Package (2/2) partially modified
		5	Table 1.4 Specifications for the 100-Pin Package (2/2) partially modified
		6	Table 1.5 Product List (1/2) partially modified
		7	Table 1.6 Product List (2/2) partially modified
		8	Figure 1.2 Marking Diagram (Top View) partially modified
		29	Figure 3.2 Memory Map 13800h → 13000h
		32	Table 4.2 “SFR Information (2/16)”notes partially modified
		48	Table 5.1 Absolute Maximum Ratings partially modified
		49	Table 5.2 Recommended Operating Conditions (1/3) partially modified
		50	Table 5.3 Recommended Operating Conditions (2/3) partially modified
		51	Table 5.4 Recommended Operating Conditions (3/3) added
		51	Figure 5.1 Ripple Waveform added
		52	Table 5.5 A/D Conversion Characteristics (1/2) partially modified
		52	Figure 5.2 A/D Accuracy Measure Circuit added
		53	Table 5.6 A/D Conversion Characteristics (2/2) partially modified
		55	Table 5.8 CPU Clock When Operating Flash Memory ($f_{(BCLK)}$) partially modified
		55	Table 5.9 Flash Memory (Program ROM 1, 2) Electrical Characteristics partially modified
		56	Table 5.10 Flash Memory (Data Flash) Electrical Characteristics notes modified
		57	Table 5.11 Voltage Detector 0 Electrical Characteristics partially modified
		57	Table 5.12 Voltage Detector 1 Electrical Characteristics partially modified
		58	Table 5.13 Voltage Detector 2 Electrical Characteristics partially modified
		58	Table 5.14 Power-On Reset Circuit partially modified
		59	Figure 5.3 Power-On Reset Circuit Electrical Characteristics 0.1 V → V_{por1}
		61	Table 5.16 40 MHz On-Chip Oscillator Circuit Electrical Characteristics (1/2) partially modified
		61	Table 5.17 40 MHz On-Chip Oscillator Circuit Electrical Characteristics (2/2) added
		61	Table 5.18 125 kHz On-Chip Oscillator Circuit Electrical Characteristics partially modified
		63	Table 5.20 Electrical Characteristics (2) partially modified
		64	Table 5.21 Electrical Characteristics (3) partially modified
		65	Table 5.22 Electrical Characteristics (4) partially modified
		66	Table 5.23 Electrical Characteristics (5) partially modified
		67	Table 5.24 Reset Input ($\overline{\text{RESET}}$ Input) partially modified
		85	Table 5.42 Electrical Characteristics (1) partially modified
		87	Table 5.44 Electrical Characteristics (3) partially modified
		88	Table 5.45 Electrical Characteristics (4) partially modified
		89	Table 5.46 Electrical Characteristics (5) partially modified
		90	Table 5.47 Reset Input ($\overline{\text{RESET}}$ Input) partially modified
2.00	Dec 10, 2010	Overall	001Ah Voltage Detector Operation Enable Register: Changed reset value from “000X 0000b”.
		Overall	002Ah Voltage Monitor 0 Control Register: Changed reset value from “1100 XX10b”.
		Overall	002Bh Voltage Monitor 1 Control Register: Changed reset value from “1000 1X10b”.
		Overall	0324h Increment/Decrement Flag: Changed name from Up/Down Flag.
		Overall	03DCh D/A Control Register: Changed reset value from “XXXX XX00b”.
		Overall	D08Ah to D08Bh PMC0 Counter Value Register: Deleted.
		Overall	D09Eh to D09Fh PMC1 Counter Value Register: Deleted.
		Overview	
		3, 5	Table 1.2 and Table 1.4 Specifications for the 128/100-Pin Package: Deleted note 1.
		6	Table 1.5 Product List (1/2): Changed the development status.
		19, 22	Table 1.12 and Table 1.15 Pin Functions: Changed the descriptions of the $\overline{\text{HOLD}}$ pin.
		Address Space	
		29	Figure 3.2 Memory Map: Added note 1 and 3 to the reserved areas.

REVISION HISTORY	M16C/65 Group Datasheet

Rev.	Date	Description	
		Page	Summary
2.00	Dec 10, 2010	**Special Function Registers (SFRs)**	
		31	Table 4.1 SFR Information (1): • Deleted “the VCR1 register, the VCR2 register” from note 2. • Deleted notes 5 to 6 and added note 5.
		32	Table 4.2 SFR Information (2): Deleted notes 2 to 7 and added note 2.
		49	4.2.1 Register Settings: Added the description regarding read-modify-write instructions.
		50	Table 4.20 Read-Modify-Write Instructions: Added.
		Electrical Characteristics	
		51	Table 5.1 Absolute Maximum Ratings: Added a row for the data area value to T_{opr} (Flash program erase).
		52	Table 5.2 Recommended Operating Conditions (1/3): Added rows for the CEC value to V_{CC1}, V_{CC2}, V_{IH}, and V_{IL}.
		57	Table 5.9 Flash Memory (Program ROM 1, 2) Electrical Characteristics: Added a condition to the Read voltage row.
		60	Table 5.14 Power-On Reset Circuit: • Added the $t_{w(por)}$ row. • Added the last line in note 1.
		60	Figure 5.3 Power-On Reset Circuit Electrical Characteristics: Deleted note 2.
		64	Table 5.20 Electrical Characteristics (2): Added “ZP, IDU, IDV, IDW” to the V_{T+} - V_{T-} row.
		65	Table 5.21 Electrical Characteristics (3): Moved R5F3651ENFC and R5F3651EDFC to Table 5.22 Electrical Characteristics (4).
		73, 96	5.2.2.7 and 5.3.2.7 Multi-master I^2C-bus: Added.
		74 to 81, 97 to 104	Table 5.37 to Table 5.42 and Table 5.60 to Table 5.65 Memory Expansion Mode and Microprocessor Mode: Deleted the following: • $\overline{HOLD}$ input setup time • $\overline{HOLD}$ input hold time • $\overline{HLDA}$ output delay time
		74	Table 5.37 Memory Expansion Mode and Microprocessor Mode: Changed $\overline{RDY}$ input setup time from 30.
		75, 98	Figure 5.13 and Figure 5.28 Timing Diagram: Deleted lower figure (Common to wait state and no wait state settings).
		86, 109	Figure 5.19 and Figure 5.34 Timing Diagram: Changed the width of th(RD-AD).
		87	Table 5.43 Electrical Characteristics (1): • Added rows for the CEC value to V_{OL}, V_{T+}-V_{T-}, and Leakage current in powered-off state. • Added “ZP, IDU, IDV, IDW” to the V_{T+} - V_{T-} row.
		88	Table 5.44 Electrical Characteristics (2): Moved R5F3651ENFC and R5F3651EDFC to Table 5.45 Electrical Characteristics (3).
		88 to 90	Table 5.44 to Table 5.46 Electrical Characteristics (2) to (4): Changed “VCC1 = 5.0 V” to "VCC1 = 3.0 V" in the During flash memory program and During flash memory erase rows.
		97	Table 5.60 Memory Expansion Mode and Microprocessor Mode: Changed $\overline{RDY}$ input setup time from 40.
2.10	Ju. 31, 2012	**Electrical Characteristics**	
		Vcc = 5 V	
		65, 66, 67	Table 5.21 Electrical Characteristics (3), Table 5.22 Electrical Characteristics (4), and Table 5.23 Electrical Characteristics (5): Changed the Measuring Condition column of 40 MHz on-chip oscillator for the 40 MHz on-chip oscillator mode in the I_{CC}.
		Vcc = 3 V	
		88, 89, 90	Table 5.44 Electrical Characteristics (2), Table 5.45 Electrical Characteristics (3), and Table 5.46 Electrical Characteristics (4): Changed the Measuring Condition column of 40 MHz on-chip oscillator for the 40 MHz on-chip oscillator mode in the I_{CC}.