Renesas Electronics America Inc - R5F3650KDFA#U0 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	M16C/60
Core Size	16-Bit
Speed	32MHz
Connectivity	EBI/EMI, I²C, SIO, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	85
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	31K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f3650kdfa-u0

Table 1.2 Specifications for the 128-Pin Package (2/2)

Item	Function	Description
Timers	Timer A	16-bit timer × 5 Timer mode, event counter mode, one-shot timer mode, pulse width modulation (PWM) mode Event counter two-phase pulse signal processing (two-phase encoder input) × 3 Programmable output mode × 3
	Timer B	16-bit timer × 6 Timer mode, event counter mode, pulse period measurement mode, pulse width measurement mode
	Three-phase motor control timer functions	• Three-phase inverter control (timer A1, timer A2, timer A4, timer B2) • On-chip dead time timer
	Real-time clock	Count: seconds, minutes, hours, days of the week
	PWM function	8 bits × 2
	Remote control signal receiver	• 2 circuits • 4 wave pattern matchings (differentiate wave pattern for headers, data 0, data 1, and special data) • 6-byte receive buffer (1 circuit only) • Operating frequency of 32 kHz
Serial Interface	UART0 to UART2, UART5 to UART7	Clock synchronous/asynchronous × 6 channels I^2C-bus, IEBus, special mode 2 SIM (UART2)
	SI/O3, SI/O4	Clock synchronization only × 2 channels
Multi-master I^2C-bus Interface		1 channel
CEC Functions (2)		CEC transmit/receive, arbitration lost detection, ACK automatic output, operation frequency of 32 kHz
A/D Converter		10-bit resolution × 26 channels, including sample and hold function Conversion time: 1.72 µs
D/A Converter		8-bit resolution × 2 circuits
CRC Calculator		CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$), CRC-16 ($X^{16} + X^{15} + X^2 + 1$) compliant
Flash Memory		• Program and erase power supply voltage: 2.7 to 5.5 V • Program and erase cycles: 1,000 times (program ROM 1, program ROM 2), 10,000 times (data flash) • Program security: ROM code protect, ID code check
Debug Functions		On-chip debug, on-board flash rewrite, address match interrupt × 4
Operation Frequency/Supply Voltage		32 MHz/VCC1 = 2.7 to 5.5 V, VCC2 = 2.7 V to VCC1
Current Consumption		Described in Electrical Characteristics
Operating Temperature		-20°C to 85°C, -40°C to 85°C (1)
Package		128-pin LQFP: PLQP0128KB-A (Previous package code: 128P6Q-A)

Notes:
1. See Table 1.5 “Product List (1/2)” and Table 1.6 “Product List (2/2)” for the operating temperature.
2. The CEC function indicates circuitry which supports the transmission and reception of CEC signals standardized by the High-Definition Multimedia Interface (HDMI). HDMI and High-Definition Multimedia Interface are registered trademarks of HDMI Licensing, LLC.

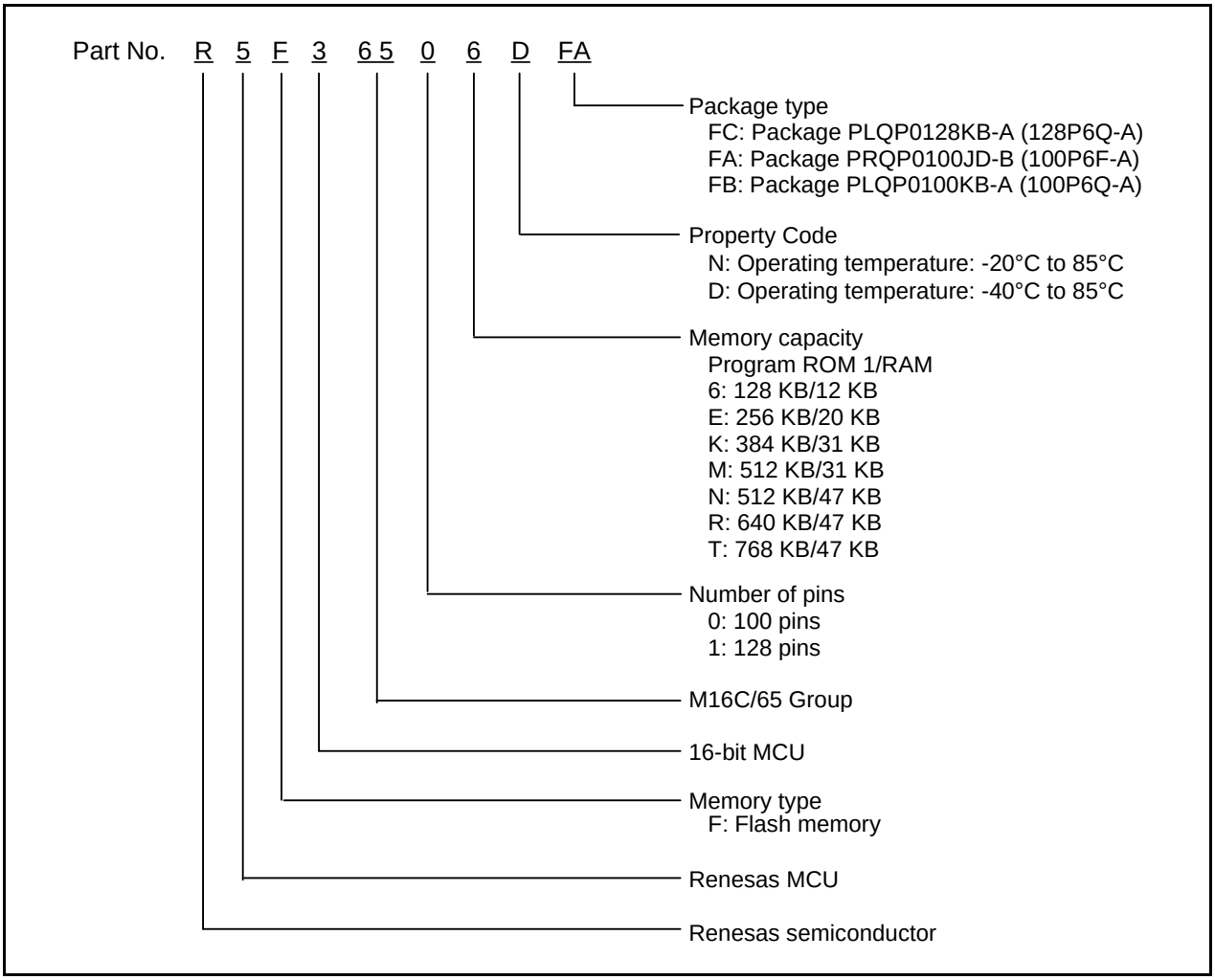


Figure 1.1 Part No., with Memory Size and Package

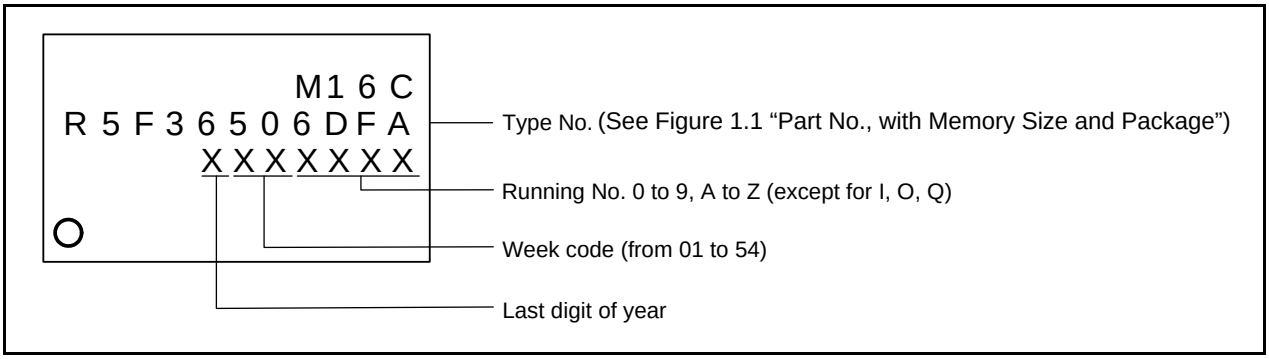


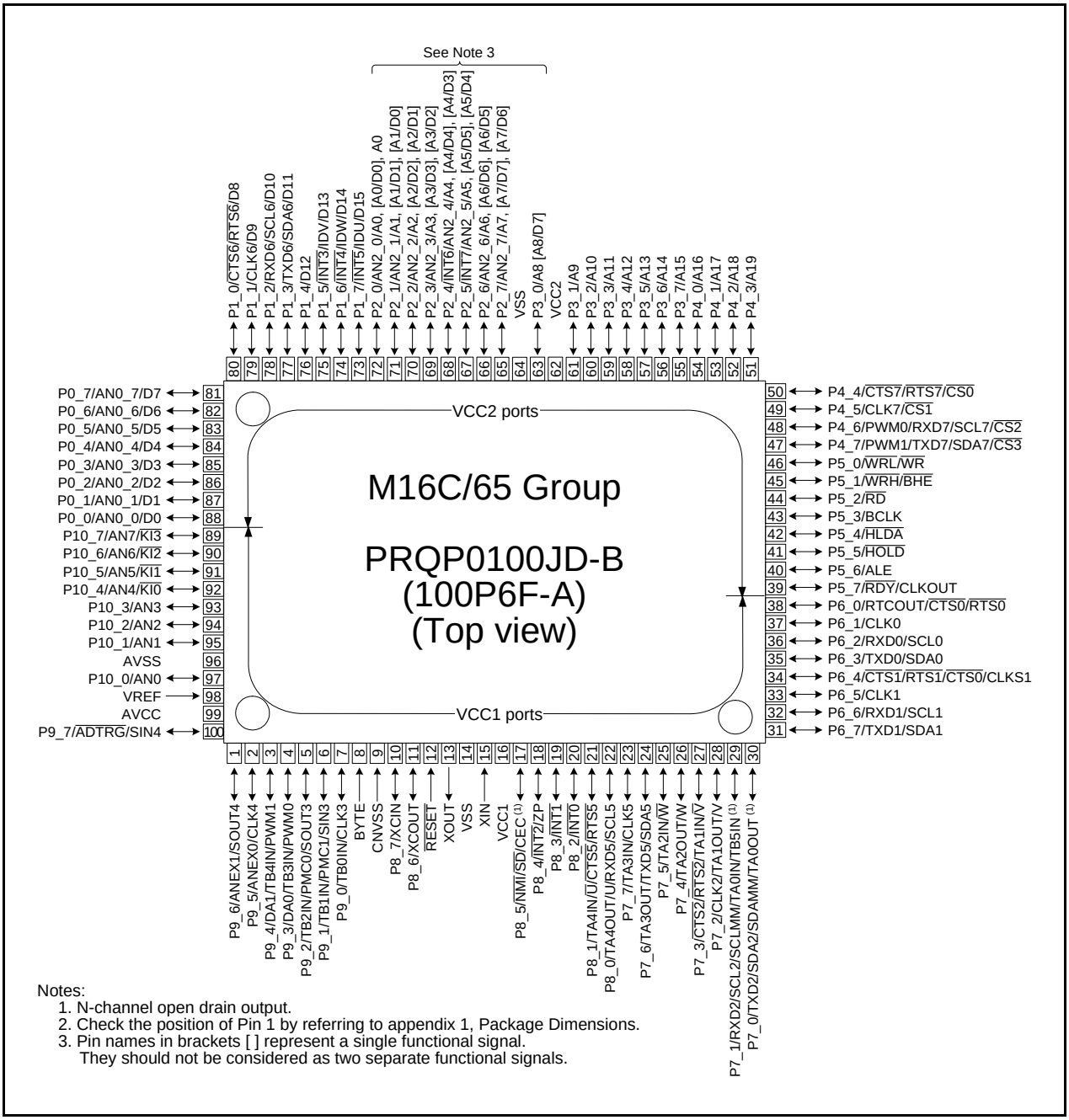
Figure 1.2 Marking Diagram (Top View)

Table 1.7 Pin Names for the 128-Pin Package (1/3)

Pin No.	Control Pin	Port	I/O Pin for Peripheral Function				Bus Control Pin
			Interrupt	Timer	Serial interface	A/D converter, D/A converter	
1	VREF						
2	AVCC						
3		P9_7			SIN4	$\overline{ADTRG}$	
4		P9_6			SOUT4	ANEX1	
5		P9_5			CLK4	ANEX0	
6		P9_4		TB4IN/PWM1		DA1	
7		P9_3		TB3IN/PWM0		DA0	
8		P9_2		TB2IN/PMC0	SOUT3		
9		P9_1		TB1IN/PMC1	SIN3		
10		P9_0		TB0IN	CLK3		
11		P14_1					
12		P14_0					
13	BYTE						
14	CNVSS						
15	XCIN	P8_7					
16	XCOUT	P8_6					
17	$\overline{RESET}$						
18	XOUT						
19	VSS						
20	XIN						
21	VCC1						
22		P8_5	$\overline{NMI}$	$\overline{SD}$	CEC		
23		P8_4	$\overline{INT2}$	ZP			
24		P8_3	$\overline{INT1}$				
25		P8_2	$\overline{INT0}$				
26		P8_1		TA4IN/$\overline{U}$	$\overline{CTS5}$/$\overline{RTS5}$		
27		P8_0		TA4OUT/U	RXD5/SCL5		
28		P7_7		TA3IN	CLK5		
29		P7_6		TA3OUT	TXD5/SDA5		
30		P7_5		TA2IN/$\overline{W}$			
31		P7_4		TA2OUT/W			
32		P7_3		TA1IN/$\overline{V}$	$\overline{CTS2}$/$\overline{RTS2}$		
33		P7_2		TA1OUT/V	CLK2		
34		P7_1		TA0IN/TB5IN	RXD2/SCL2/SCLMM		
35		P7_0		TA0OUT	TXD2/SDA2/SDAMM		
36		P6_7			TXD1/SDA1		
37	VCC1						
38		P6_6			RXD1/SCL1		
39	VSS						
40		P6_5			CLK1		
41		P6_4			$\overline{CTS1}$/$\overline{RTS1}$/$\overline{CTS0}$/CLKS1		
42		P6_3			TXD0/SDA0		
43		P6_2			RXD0/SCL0		
44		P6_1			CLK0		
45		P6_0		RTCOUT	$\overline{CTS0}$/$\overline{RTS0}$		
46		P13_7					
47		P13_6					
48		P13_5					
49		P13_4					
50	CLKOUT	P5_7					$\overline{RDY}$

Table 1.8 Pin Names for the 128-Pin Package (2/3)

Pin No.	Control Pin	Port	I/O Pin for Peripheral Function				Bus Control Pin
			Interrupt	Timer	Serial interface	A/D converter, D/A converter	
51		P5_6					ALE
52		P5_5					$\overline{\text{HOLD}}$
53		P5_4					$\overline{\text{HLDA}}$
54		P13_3					
55		P13_2					
56		P13_1					
57		P13_0					
58		P5_3					BCLK
59		P5_2					$\overline{\text{RD}}$
60		P5_1					$\overline{\text{WRH/BHE}}$
61		P5_0					$\overline{\text{WRL/WR}}$
62		P12_7					
63		P12_6					
64		P12_5					
65		P4_7		PWM1	TXD7/SDA7		$\overline{\text{CS3}}$
66		P4_6		PWM0	RXD7/SCL7		$\overline{\text{CS2}}$
67		P4_5			CLK7		$\overline{\text{CS1}}$
68		P4_4			$\overline{\text{CTS7/RTS7}}$		$\overline{\text{CS0}}$
69		P4_3					A19
70		P4_2					A18
71		P4_1					A17
72		P4_0					A16
73		P3_7					A15
74		P3_6					A14
75		P3_5					A13
76		P3_4					A12
77		P3_3					A11
78		P3_2					A10
79		P3_1					A9
80		P12_4					
81		P12_3					
82		P12_2					
83		P12_1					
84		P12_0					
85	VCC2						
86		P3_0					A8, [A8/D7]
87	VSS						
88		P2_7				AN2_7	A7, [A7/D7], [A7/D6]
89		P2_6				AN2_6	A6, [A6/D6], [A6/D5]
90		P2_5	$\overline{\text{INT7}}$			AN2_5	A5, [A5/D5], [A5/D4]
91		P2_4	$\overline{\text{INT6}}$			AN2_4	A4[A4/D4], [A4/D3]
92		P2_3				AN2_3	A3, [A3/D3], [A3/D2]
93		P2_2				AN2_2	A2, [A2/D2], [A2/D1]
94		P2_1				AN2_1	A1, [A1/D1], [A1/D0]
95		P2_0				AN2_0	A0, [A0/D0], A0
96		P1_7	$\overline{\text{INT5}}$	IDU			D15
97		P1_6	$\overline{\text{INT4}}$	IDW			D14
98		P1_5	$\overline{\text{INT3}}$	IDV			D13
99		P1_4					D12
100		P1_3			TXD6/SDA6		D11



Notes:
1. N-channel open drain output.
2. Check the position of Pin 1 by referring to appendix 1, Package Dimensions.
3. Pin names in brackets [ ] represent a single functional signal.
They should not be considered as two separate functional signals.

Figure 1.6 Pin Assignment for the 100-Pin Package

Table 1.10 Pin Names for the 100-Pin Package (1/2)

Pin No.		Control Pin	Port	I/O Pin for Peripheral Function				Bus Control Pin
FA	FB			Interrupt	Timer	Serial interface	A/D converter, D/A converter	
1	99		P9_6			SOUT4	ANEX1	
2	100		P9_5			CLK4	ANEX0	
3	1		P9_4		TB4IN/PWM1		DA1	
4	2		P9_3		TB3IN/PWM0		DA0	
5	3		P9_2		TB2IN/PMC0	SOUT3		
6	4		P9_1		TB1IN/PMC1	SIN3		
7	5		P9_0		TB0IN	CLK3		
8	6	BYTE						
9	7	CNVSS						
10	8	XCIN	P8_7					
11	9	XCOUT	P8_6					
12	10	$\overline{\text{RESET}}$						
13	11	XOUT						
14	12	VSS						
15	13	XIN						
16	14	VCC1						
17	15		P8_5	$\overline{\text{NMI}}$	$\overline{\text{SD}}$	CEC		
18	16		P8_4	$\overline{\text{INT2}}$	ZP			
19	17		P8_3	$\overline{\text{INT1}}$				
20	18		P8_2	$\overline{\text{INT0}}$				
21	19		P8_1		TA4IN/$\overline{\text{U}}$	$\overline{\text{CTS5/RTS5}}$		
22	20		P8_0		TA4OUT/U	RXD5/SCL5		
23	21		P7_7		TA3IN	CLK5		
24	22		P7_6		TA3OUT	TXD5/SDA5		
25	23		P7_5		TA2IN/$\overline{\text{W}}$			
26	24		P7_4		TA2OUT/W			
27	25		P7_3		TA1IN/$\overline{\text{V}}$	$\overline{\text{CTS2/RTS2}}$		
28	26		P7_2		TA1OUT/V	CLK2		
29	27		P7_1		TA0IN/TB5IN	RXD2/SCL2/SCLMM		
30	28		P7_0		TA0OUT	TXD2/SDA2/SDAMM		
31	29		P6_7			TXD1/SDA1		
32	30		P6_6			RXD1/SCL1		
33	31		P6_5			CLK1		
34	32		P6_4			$\overline{\text{CTS1}}$/RTS1/$\overline{\text{CTS0}}$/ CLKS1		
35	33		P6_3			TXD0/SDA0		
36	34		P6_2			RXD0/SCL0		
37	35		P6_1			CLK0		
38	36		P6_0		RTCOUT	$\overline{\text{CTS0/RTS0}}$		
39	37	CLKOUT	P5_7					$\overline{\text{RDY}}$
40	38		P5_6					ALE
41	39		P5_5					$\overline{\text{HOLD}}$
42	40		P5_4					$\overline{\text{HLDA}}$
43	41		P5_3					BCLK
44	42		P5_2					$\overline{\text{RD}}$
45	43		P5_1					$\overline{\text{WRH/BHE}}$
46	44		P5_0					$\overline{\text{WRL/WR}}$
47	45		P4_7		PWM1	TXD7/SDA7		$\overline{\text{CS3}}$
48	46		P4_6		PWM0	RXD7/SCL7		$\overline{\text{CS2}}$
49	47		P4_5			CLK7		$\overline{\text{CS1}}$
50	48		P4_4			$\overline{\text{CTS7/RTS7}}$		$\overline{\text{CS0}}$

1.6 Pin Functions

Table 1.12 Pin Functions for the 128-Pin Package (1/3)

Signal Name	Pin Name	I/O	Power Supply	Description
Power supply input	VCC1, VCC2, VSS	I	-	Apply 2.7 to 5.5 V to pins VCC1 and VCC2 (VCC1 ≥ VCC2), and 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	I	VCC1	This is the power supply for the A/D and D/A converters. Connect the AVCC pin to VCC1, and connect the AVSS pin to VSS.
Reset input	$\overline{\text{RESET}}$	I	VCC1	Driving this pin low resets the MCU.
CNVSS	CNVSS	I	VCC1	Input pin to switch processor modes. After a reset, to start operating in single-chip mode, connect the CNVSS pin to VSS via a resistor. To start operating in microprocessor mode, connect the pin to VCC1.
External data bus width select input	BYTE	I	VCC1	Input pin to select the data bus of the external area. The data bus is 16 bits when it is low and 8 bits when it is high. This pin must be fixed either high or low. Connect the BYTE pin to VSS in single-chip mode.
Bus control pins	D0 to D7	I/O	VCC2	Inputs or outputs data (D0 to D7) while accessing an external area with a separate bus.
	D8 to D15	I/O	VCC2	Inputs or outputs data (D8 to D15) while accessing an external area with a 16-bit separate bus.
	A0 to A19	O	VCC2	Outputs address bits A0 to A19.
	A0/D0 to A7/D7	I/O	VCC2	Inputs or outputs data (D0 to D7) and outputs address bits (A0 to A7) by timesharing, while accessing an external area with an 8-bit multiplexed bus.
	A1/D0 to A8/D7	I/O	VCC2	Inputs or outputs data (D0 to D7) and outputs address bits (A1 to A8) by timesharing, while accessing an external area with a 16-bit multiplexed bus.
	$\overline{\text{CS0}}$ to $\overline{\text{CS3}}$	O	VCC2	Outputs chip-select signals $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$ to specify an external area.
	$\overline{\text{WRL}}$/$\overline{\text{WR}}$ $\overline{\text{WRH}}$/$\overline{\text{BHE}}$ $\overline{\text{RD}}$	O	VCC2	Outputs $\overline{\text{WRL}}$, $\overline{\text{WRH}}$, ($\overline{\text{WR}}$, $\overline{\text{BHE}}$), and $\overline{\text{RD}}$ signals. $\overline{\text{WRL}}$ and $\overline{\text{WRH}}$ can be switched with $\overline{\text{BHE}}$ and $\overline{\text{WR}}$. • $\overline{\text{WRL}}$, $\overline{\text{WRH}}$, and $\overline{\text{RD}}$ selected If the external data bus is 16 bits, data is written to an even address in an external area when $\overline{\text{WRL}}$ is driven low. Data is written to an odd address when $\overline{\text{WRH}}$ is driven low. Data is read when $\overline{\text{RD}}$ is driven low. • $\overline{\text{WR}}$, $\overline{\text{BHE}}$, and $\overline{\text{RD}}$ selected Data is written to an external area when $\overline{\text{WR}}$ is driven low. Data in an external area is read when $\overline{\text{RD}}$ is driven low. An odd address is accessed when $\overline{\text{BHE}}$ is driven low. Select $\overline{\text{WR}}$, $\overline{\text{BHE}}$, and $\overline{\text{RD}}$ when using an 8-bit external data bus.
	ALE	O	VCC2	Outputs an ALE signal to latch the address.
	$\overline{\text{HOLD}}$	I	VCC2	$\overline{\text{HOLD}}$ input is unavailable. Connect the $\overline{\text{HOLD}}$ pin to VCC2 via a resistor (pull-up).
	$\overline{\text{HLDA}}$	O	VCC2	In a hold state, $\overline{\text{HLDA}}$ outputs a low-level signal.
	$\overline{\text{RDY}}$	I	VCC2	The MCU bus is placed in wait state while the $\overline{\text{RDY}}$ pin is driven low.

Power supply: VCC2 is used to supply power to the external bus associated pins. The dual power supply configuration allows VCC2 to interface at a different voltage than VCC1.

Table 1.17 Pin Functions for the 100-Pin Package (3/3)

Signal Name	Pin Name	I/O	Power Supply	Description
UART0 to UART2, UART5 to UART7 I^2C mode	SDA0 to SDA2, SDA5	I/O	VCC1	Serial data I/O.
	SDA6, SDA7	I/O	VCC2	
	SCL0 to SCL2, SCL5	I/O	VCC1	Transmit/receive clock I/O.
	SCL6, SCL7	I/O	VCC2	
Serial interface SI/O3, SI/O4	CLK3, CLK4	I/O	VCC1	Transmit/receive clock I/O.
	SIN3, SIN4	I	VCC1	Serial data input.
	SOUT3, SOUT4	O	VCC1	Serial data output.
Multi-master I^2C-bus interface	SDAMM	I/O	VCC1	Serial data I/O (N-channel open drain output).
	SCLMM	I/O	VCC1	Transmit/receive clock I/O (N-channel open drain output).
CEC I/O	CEC	I/O	VCC1	CEC I/O (N-channel open drain output).
Reference voltage input	VREF	I	VCC1	Reference voltage input for the A/D and D/A converters.
A/D converter	AN0 to AN7	I	VCC1	Analog input.
	AN0_0 to AN0_7 AN2_0 to AN2_7	I	VCC2	
	$\overline{\text{ADTRG}}$	I	VCC1	External trigger input.
	ANEX0, ANEX1	I	VCC1	Extended analog input.
D/A converter	DA0, DA1	O	VCC1	Output for the D/A converter.
I/O ports	P0_0 to P0_7 P1_0 to P1_7 P2_0 to P2_7 P3_0 to P3_7 P4_0 to P4_7 P5_0 to P5_7	I/O	VCC2	8-bit CMOS I/O ports. A direction register determines whether each pin is used as an input port or an output port. A pull-up resistor may be enabled or disabled for input ports in 4-bit units.
	P6_0 to P6_7 P7_0 to P7_7 P8_0 to P8_7 P9_0 to P9_7 P10_0 to P10_7	I/O	VCC1	8-bit I/O ports having equivalent functions to P0. However, P7_0, P7_1, and P8_5 are N-channel open drain output ports. No pull-up resistor is provided. P8_5 is an input port for verifying the $\overline{\text{NMI}}$ pin level and shares a pin with $\overline{\text{NMI}}$.

4. Special Function Registers (SFRs)

4.1 SFRs

An SFR is a control register for a peripheral function.

Table 4.1 SFR Information (1) (1)

Address	Register	Symbol	Reset Value
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	0000 0000b (CNVSS pin is low) 0000 0011b (CNVSS pin is high) (2)
0005h	Processor Mode Register 1	PM1	0000 1000b
0006h	System Clock Control Register 0	CM0	0100 1000b
0007h	System Clock Control Register 1	CM1	0010 0000b
0008h	Chip Select Control Register	CSR	01h
0009h	External Area Recovery Cycle Control Register	EWR	XXXX XX00b
000Ah	Protect Register	PRCR	00h
000Bh	Data Bank Register	DBR	00h
000Ch	Oscillation Stop Detection Register	CM2	0X00 0010b (3)
000Dh			
000Eh			
000Fh			
0010h	Program 2 Area Control Register	PRG2C	XXXX XX00b
0011h	External Area Wait Control Expansion Register	EWC	00h
0012h	Peripheral Clock Select Register	PCLKR	0000 0011b
0013h			
0014h			
0015h	Clock Prescaler Reset Flag	CPSRF	0XXX XXXXb
0016h			
0017h			
0018h	Reset Source Determine Register	RSTFR	XX00 001Xb (hardware reset) (4)
0019h	Voltage Detector 2 Flag Register	VCR1	0000 1000b (5)
001Ah	Voltage Detector Operation Enable Register	VCR2	00h (5)
001Bh	Chip Select Expansion Control Register	CSE	00h
001Ch	PLL Control Register 0	PLC0	0X01 X010b
001Dh			
001Eh	Processor Mode Register 2	PM2	XX00 0X01b
001Fh			

X: Undefined

Notes:
1. The blank areas are reserved. No access is allowed.
2. Software reset, watchdog timer reset, oscillator stop detect reset, voltage monitor 1 reset, and voltage monitor 2 reset do not affect the following bits: bits PM01 and PM00 in the PM0 register.
3. Oscillator stop detect reset does not affect bits CM20, CM21, and CM27.
4. The state of bits in the RSTFR register depends on the reset type.
5. This is the reset value after hardware reset. Refer to the explanation of each register for details.

Table 4.6 SFR Information (6) (1)

Address	Register	Symbol	Reset Value
01B0h	DMA3 Source Pointer	SAR3	XXh
01B1h			XXh
01B2h			0Xh
01B3h			
01B4h	DMA3 Destination Pointer	DAR3	XXh
01B5h			XXh
01B6h			0Xh
01B7h			
01B8h	DMA3 Transfer Counter	TCR3	XXh
01B9h			XXh
01BAh			
01BBh			
01BCh	DMA3 Control Register	DM3CON	0000 0X00b
01BDh			
01BEh			
01BFh			
01C0h	Timer B0-1 Register	TB01	XXh
01C1h			XXh
01C2h	Timer B1-1 Register	TB11	XXh
01C3h			XXh
01C4h	Timer B2-1 Register	TB21	XXh
01C5h			XXh
01C6h	Pulse Period/Pulse Width Measurement Mode Function Select Register 1	PPWFS1	XXXX X000b
01C7h			
01C8h	Timer B Count Source Select Register 0	TBCS0	00h
01C9h	Timer B Count Source Select Register 1	TBCS1	X0h
01CAh			
01CBh	Timer AB Division Control Register 0	TCKDIVC0	0000 X000b
01CCh			
01CDh			
01CEh			
01CFh			
01D0h	Timer A Count Source Select Register 0	TACS0	00h
01D1h	Timer A Count Source Select Register 1	TACS1	00h
01D2h	Timer A Count Source Select Register 2	TACS2	X0h
01D3h			
01D4h	16-bit Pulse Width Modulation Mode Function Select Register	PWMFS	0XX0 X00Xb
01D5h	Timer A Waveform Output Function Select Register	TAPOFS	XXX0 0000b
01D6h			
01D7h			
01D8h	Timer A Output Waveform Change Enable Register	TAOW	XXX0 X00Xb
01D9h			
01DAh	Three-Phase Protect Control Register	TPRC	00h
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.8 SFR Information (8) (1)

Address	Register	Symbol	Reset Value
0210h	Address Match Interrupt Register 0	RMAD0	00h
0211h			00h
0212h			X0h
0213h			
0214h	Address Match Interrupt Register 1	RMAD1	00h
0215h			00h
0216h			X0h
0217h			
0218h	Address Match Interrupt Register 2	RMAD2	00h
0219h			00h
021Ah			X0h
021Bh			
021Ch	Address Match Interrupt Register 3	RMAD3	00h
021Dh			00h
021Eh			X0h
021Fh			
0220h	Flash Memory Control Register 0	FMR0	0000 0001b (Other than user boot mode) 0010 0001b (User boot mode)
0221h	Flash Memory Control Register 1	FMR1	00X0 XX0Xb
0222h	Flash Memory Control Register 2	FMR2	XXXX 0000b
0223h			
0224h			
0225h			
0226h			
0227h			
0228h			
0229h			
022Ah			
022Bh			
022Ch			
022Dh			
022Eh			
022Fh			
0230h	Flash Memory Control Register 6	FMR6	XX0X XX00b
0231h			
0232h			
0233h			
0234h			
0235h			
0236h			
0237h			
0238h			
0239h			
023Ah			
023Bh			
023Ch			
023Dh			
023Eh			
023Fh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.10 SFR Information (10) (1)

Address	Register	Symbol	Reset Value
0270h	SI/O3 Transmit/Receive Register	S3TRR	XXh
0271h			
0272h	SI/O3 Control Register	S3C	0100 0000b
0273h	SI/O3 Bit Rate Register	S3BRG	XXh
0274h	SI/O4 Transmit/Receive Register	S4TRR	XXh
0275h			
0276h	SI/O4 Control Register	S4C	0100 0000b
0277h	SI/O4 Bit Rate Register	S4BRG	XXh
0278h	SI/O3, 4 Control Register 2	S34C2	00XX X0X0b
0279h			
027Ah			
027Bh			
027Ch			
027Dh			
027Eh			
027Fh			
0280h			
0281h			
0282h			
0283h			
0284h	UART5 Special Mode Register 4	U5SMR4	00h
0285h	UART5 Special Mode Register 3	U5SMR3	000X 0X0Xb
0286h	UART5 Special Mode Register 2	U5SMR2	X000 0000b
0287h	UART5 Special Mode Register	U5SMR	X000 0000b
0288h	UART5 Transmit/Receive Mode Register	U5MR	00h
0289h	UART5 Bit Rate Register	U5BRG	XXh
028Ah	UART5 Transmit Buffer Register	U5TB	XXh
028Bh			XXh
028Ch	UART5 Transmit/Receive Control Register 0	U5C0	0000 1000b
028Dh	UART5 Transmit/Receive Control Register 1	U5C1	0000 0010b
028Eh	UART5 Receive Buffer Register	U5RB	XXh
028Fh			XXh
0290h			
0291h			
0292h			
0293h			
0294h	UART6 Special Mode Register 4	U6SMR4	00h
0295h	UART6 Special Mode Register 3	U6SMR3	000X 0X0Xb
0296h	UART6 Special Mode Register 2	U6SMR2	X000 0000b
0297h	UART6 Special Mode Register	U6SMR	X000 0000b
0298h	UART6 Transmit/Receive Mode Register	U6MR	00h
0299h	UART6 Bit Rate Register	U6BRG	XXh
029Ah	UART6 Transmit Buffer Register	U6TB	XXh
029Bh			XXh
029Ch	UART6 Transmit/Receive Control Register 0	U6C0	0000 1000b
029Dh	UART6 Transmit/Receive Control Register 1	U6C1	0000 0010b
029Eh	UART6 Receive Buffer Register	U6RB	XXh
029Fh			XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.14 SFR Information (14) (1)

Address	Register	Symbol	Reset Value
0360h	Pull-Up Control Register 0	PUR0	00h
0361h	Pull-Up Control Register 1	PUR1	0000 0000b (2) 0000 0010b
0362h	Pull-Up Control Register 2	PUR2	00h
0363h	Pull-Up Control Register 3	PUR3	00h
0364h			
0365h			
0366h	Port Control Register	PCR	0000 0XX0b
0367h			
0368h			
0369h	NMI/SD Digital Filter Register	NMIDF	XXXX X000b
036Ah			
036Bh			
036Ch			
036Dh			
036Eh			
036Fh			
0370h	PWM Control Register 0	PWMCON0	00h
0371h			
0372h	PWM0 Prescaler	PWMPRE0	00h
0373h	PWM0 Register	PWMREG0	00h
0374h	PWM1 Prescaler	PWMPRE1	00h
0375h	PWM1 Register	PWMREG1	00h
0376h	PWM Control Register 1	PWMCON1	00h
0377h			
0378h			
0379h			
037Ah			
037Bh			
037Ch	Count Source Protection Mode Register	CSPR	00h (3)
037Dh	Watchdog Timer Refresh Register	WDTR	XXh
037Eh	Watchdog Timer Start Register	WDTS	XXh
037Fh	Watchdog Timer Control Register	WDC	00XX XXXXb
0380h to 038Fh			

X: Undefined

Notes:
1. The blank areas are reserved. No access is allowed.
2. Values after hardware reset, power-on reset, or voltage monitor 0 reset are as follows:
 - 00000000b when a low-level signal is input to the CNVSS pin
 - 00000010b when a high-level signal is input to the CNVSS pin
 Values after voltage monitor 1 reset, voltage monitor 2 reset, software reset, watchdog timer reset, or oscillation stop detect reset are as follows:
 - 00000000b when bits PM01 and PM00 in the PM0 register are 00b (single-chip mode).
 - 00000010b when bits PM01 and PM00 in the PM0 register are 01b (memory expansion mode) or 11b (microprocessor mode).
3. When the CSPROINI bit in the OFS1 address is 0, the reset value is 1000 0000b.

$V_{CC1} = V_{CC2} = 5\ V$

Table 5.21 Electrical Characteristics (3)

R5F36506NFA, R5F36506NFB, R5F36506DFA, R5F36506DFB, R5F3650ENFA, R5F3650ENFB, R5F3650EDFA, R5F3650EDFB

$V_{CC1} = V_{CC2} = 4.2$ to 5.5 V, $V_{SS} = 0$ V at $T_{opr} = -20°C$ to 85°C/−40°C to 85°C, $f_{(BCLK)} = 32$ MHz unless otherwise specified.

Symbol	Parameter	Measuring Condition		Standard			Unit
				Min.	Typ.	Max.	
R_{fXCIN}	Feedback resistance XCIN				8		MΩ
I_{CC}	Power supply current In single-chip, mode, the output pin are open and other pins are V_{SS}	High-speed mode	$f_{(BCLK)}$ = 32 MHz XIN = 4 MHz (square wave), PLL multiplied by 8 125 kHz on-chip oscillator stopped		24.0		mA
			$f_{(BCLK)}$ =32 MHz, A/D conversion XIN = 4 MHz (square wave), PLL multiplied by 8 125 kHz on-chip oscillator stopped		24.7		mA
			$f_{(BCLK)}$ = 20 MHz XIN = 20 MHz (square wave) 125 kHz on-chip oscillator stopped		16.0		mA
		40 MHz on-chip oscillator mode	Main clock stopped 40 MHz on-chip oscillator on, divide-by-4 ($f_{(BCLK)}$ = 10 MHz) 125 kHz on-chip oscillator stopped		17.0		mA
		125 kHz on-chip oscillator mode	Main clock stopped 40 MHz on-chip oscillator stopped, 125 kHz on-chip oscillator on, no division FMR22 = 1 (slow read mode)		500.0		µA
		Low-power mode	$f_{(BCLK)}$ = 32 kHz In low-power mode FMR22 = FMR23 = 1 On flash memory (1)		160.0		µA
			$f_{(BCLK)}$ = 32 kHz In low-power mode On RAM (1)		45.0		µA
		Wait mode	Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator on Peripheral clock operating T_{opr} = 25°C		20.0		µA
			$f_{(BCLK)}$ = 32 kHz (oscillation capacity High) 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator stopped Peripheral clock operating T_{opr} = 25°C		11.0		µA
			$f_{(BCLK)}$ = 32 kHz (oscillation capacity Low) 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator stopped Peripheral clock operating T_{opr} = 25°C		6.0		µA
		Stop mode	Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator stopped Peripheral clock stopped T_{opr} = 25°C		1.7		µA
		During flash memory program	$f_{(BCLK)}$ = 10 MHz, PM17 = 1 (one wait) V_{CC1} = 5.0 V		20.0		mA
		During flash memory erase	$f_{(BCLK)}$ = 10 MHz, PM17 = 1 (one wait) V_{CC1} = 5.0 V		30.0		mA

Note:
1. This indicates the memory in which the program to be executed exists.

$V_{CC1} = V_{CC2} = 5\ V$

Switching Characteristics

($V_{CC1} = V_{CC2} = 5$ V, $V_{SS} = 0$ V, at $T_{opr} = -20°C$ to 85°C/-40°C to 85°C unless otherwise specified)

5.2.4.3 In 2 or 3 Waits Setting, and When Accessing External Area and Using Multiplexed Bus

Table 5.40 Memory Expansion Mode and Microprocessor Mode (in 2 or 3 Waits Setting, and When Accessing External Area and Using Multiplexed Bus) (5)

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	See Figure 5.14		25	ns
$t_{h(BCLK-AD)}$	Address output hold time (in relation to BCLK)		0		ns
$t_{h(RD-AD)}$	Address output hold time (in relation to RD)		(Note 1)		ns
$t_{h(WR-AD)}$	Address output hold time (in relation to WR)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			25	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (in relation to BCLK)		0		ns
$t_{h(RD-CS)}$	Chip select output hold time (in relation to RD)		(Note 1)		ns
$t_{h(WR-CS)}$	Chip select output hold time (in relation to WR)		(Note 1)		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			25	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			25	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (in relation to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data output hold time (in relation to BCLK)		0		ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(Note 2)		ns
$t_{h(WR-DB)}$	Data output hold time (in relation to WR)		(Note 1)		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time (in relation to BCLK)			15	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time (in relation to BCLK)		–4		ns
$t_{d(AD-ALE)}$	ALE signal output delay time (in relation to Address)		(Note 3)		ns
$t_{h(AD-ALE)}$	ALE signal output hold time (in relation to Address)		(Note 4)		ns
$t_{d(AD-RD)}$	RD signal output delay from the end of address		0		ns
$t_{d(AD-WR)}$	WR signal output delay from the end of address		0		ns
$t_{dz(RD-AD)}$	Address output floating start time			8	ns

Notes:

1. Calculated according to the BCLK frequency as follows:
$$\frac{0.5 \times 10^9}{f_{(BCLK)}} - 10[ns]$$
2. Calculated according to the BCLK frequency as follows:
$$\frac{(n - 0.5) \times 10^9}{f_{(BCLK)}} - 40[ns]$$
n is 2 for 2-wait setting, 3 for 3-wait setting.
3. Calculated according to the BCLK frequency as follows:
$$\frac{0.5 \times 10^9}{f_{(BCLK)}} - 25[ns]$$
4. Calculated according to the BCLK frequency as follows:
$$\frac{0.5 \times 10^9}{f_{(BCLK)}} - 15[ns]$$
5. When using multiplex bus, set $f_{(BCLK)}$ 12.5 MHz or less.

$V_{CC1} = V_{CC2} = 5\ V$

Switching Characteristics

($V_{CC1} = V_{CC2} = 5$ V, $V_{SS} = 0$ V, at $T_{opr} = -20°C$ to 85°C/-40°C to 85°C unless otherwise specified)

5.2.4.5 In Wait State Setting 2φ + 3φ, 2φ + 4φ, 3φ + 4φ, and 4φ + 5φ, and When Inserting 1 to 3 Recovery Cycles and Accessing External Area

Table 5.42 Memory Expansion and Microprocessor Modes (in Wait State Setting 2φ + 3φ, 2φ + 4φ, 3φ + 4φ, and 4φ + 5φ, and When Inserting 1 to 3 Recovery Cycles and Accessing External Area)

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	See Figure 5.14		25	ns
$t_{h(BCLK-AD)}$	Address output hold time (in relation to BCLK)		0		ns
$t_{h(RD-AD)}$	Address output hold time (in relation to RD)		(Note 4)		ns
$t_{h(WR-AD)}$	Address output hold time (in relation to WR)		(Note 2)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			25	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (in relation to BCLK)		0		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			15	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		-4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			25	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			25	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (in relation to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data output hold time (in relation to BCLK) (3)		0		ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(Note 1)		ns
$t_{h(WR-DB)}$	Data output hold time (in relation to WR) (3)		(Note 2)		ns

Notes:

1. Calculated according to the BCLK frequency as follows:

$$\frac{n \times 10^9}{f_{(BCLK)}} - 40[ns]$$

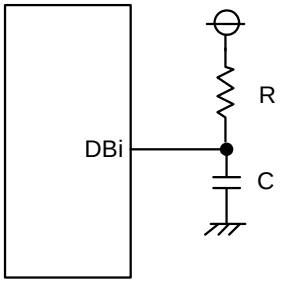
n is 3 for 2φ + 3φ, 4 for 2φ + 4φ, 4 for 3φ + 4φ, and 5 for 4φ + 5φ.

2. Calculated according to the BCLK frequency as follows:

$$\frac{m \times 10^9}{f_{(BCLK)}} - 10[ns]$$

m is 1 when 1 recovery cycle is inserted, 2 when 2 recovery cycles are inserted, and 3 when 3 recovery cycles are inserted.

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
Hold time of data bus is expressed in
$t = -CR \times \ln(1 - V_{OL}/V_{CC2})$
by a circuit of the right figure.
For example, when $V_{OL} = 0.2V_{CC2}$, C = 30 pF, R = 1 kΩ, hold time of output low level is
$t = -30\ pF \times 1\ k\Omega \times \ln(1 - 0.2V_{CC2}/V_{CC2})$
$= 6.7$ ns.



4. Calculated according to the BCLK frequency as follows:

$$\frac{m \times 10^9}{f_{(BCLK)}} + 0[ns]$$

m is 1 when 1 recovery cycle is inserted, 2 when 2 recovery cycles are inserted, and 3 when 3 recovery cycles are inserted.

$V_{CC1} = V_{CC2} = 3\ V$

5.3.2 Timing Requirements (Peripheral Functions and Others)

($V_{CC1} = V_{CC2} = 3$ V, $V_{SS} = 0$ V, at $T_{opr} = -20°C$ to 85°C/-40°C to 85°C unless otherwise specified)

5.3.2.1 Reset Input ($\overline{\text{RESET}}$ Input)

Table 5.47 Reset Input ($\overline{\text{RESET}}$ Input)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(RSTL)}$	$\overline{\text{RESET}}$ input low pulse width	10		µs

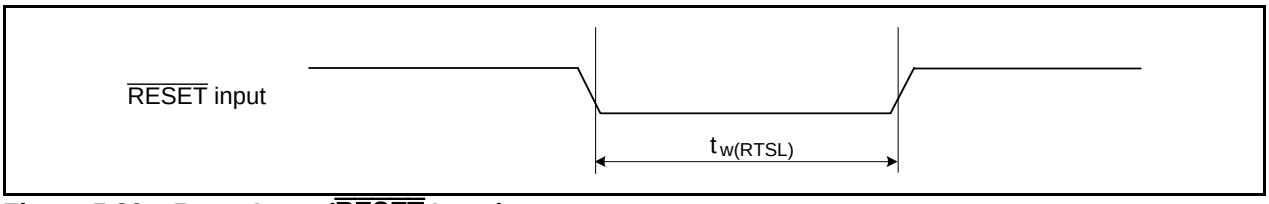


Figure 5.20 Reset Input ($\overline{\text{RESET}}$ Input)

5.3.2.2 External Clock Input

Table 5.48 External Clock Input (XIN Input) (1)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External clock input cycle time	50		ns
$t_{w(H)}$	External clock input high pulse width	20		ns
$t_{w(L)}$	External clock input low pulse width	20		ns
t_r	External clock rise time		9	ns
t_f	External clock fall time		9	ns

Note:
1. The condition is $V_{CC1} = V_{CC2} = 2.7$ to 3.0 V.

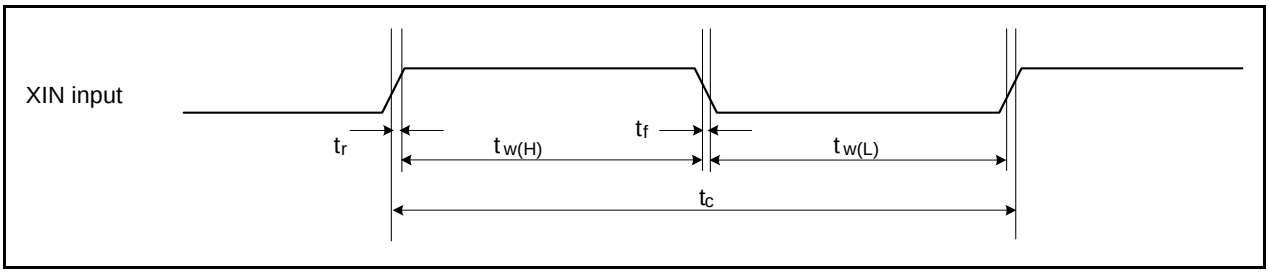


Figure 5.21 External Clock Input (XIN Input)

$V_{CC1} = V_{CC2} = 3\ V$

Timing Requirements

($V_{CC1} = V_{CC2} = 3$ V, $V_{SS} = 0$ V, at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified)

5.3.2.5 Serial Interface

Table 5.57 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300		ns
$t_{w(CKH)}$	CLKi input high pulse width	150		ns
$t_{w(CKL)}$	CLKi input low pulse width	150		ns
$t_{d(C-Q)}$	TXDi output delay time		160	ns
$t_{h(C-Q)}$	TXDi hold time	0		ns
$t_{su(D-C)}$	RXDi input setup time	100		ns
$t_{h(C-D)}$	RXDi input hold time	90		ns

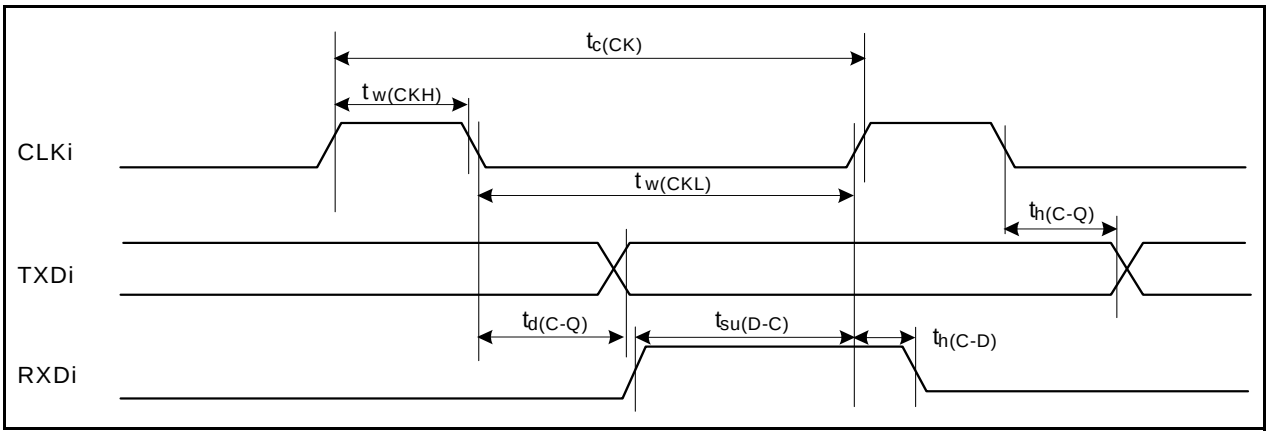


Figure 5.25 Serial Interface

5.3.2.6 External Interrupt $\overline{INTi}$ Input

Table 5.58 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input high pulse width	380		ns
$t_{w(INL)}$	$\overline{INTi}$ input low pulse width	380		ns

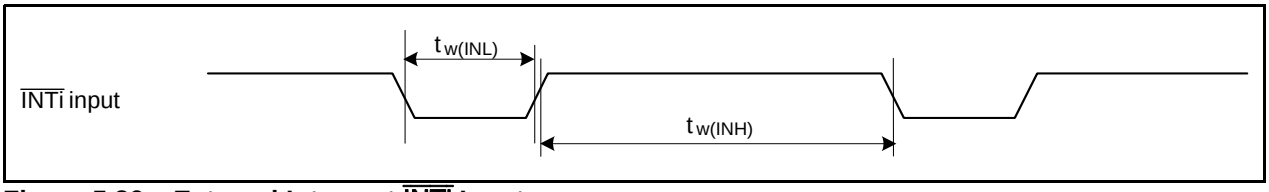


Figure 5.26 External Interrupt $\overline{INTi}$ Input

$V_{CC1} = V_{CC2} = 3\ V$

Switching Characteristics

($V_{CC1} = V_{CC2} = 3$ V, $V_{SS} = 0$ V, at $T_{opr} = -20°C$ to 85°C/-40°C to 85°C unless otherwise specified)

5.3.4.5 In Wait State Setting 2φ + 3φ, 2φ + 4φ, 3φ + 4φ, and 4φ + 5φ, and Inserting 1 to 3 Recovery Cycles and Accessing External Area

Table 5.65 Memory Expansion Mode and Microprocessor Mode (in Wait State Setting 2φ + 3φ, 2φ + 4φ, 3φ + 4φ, and 4φ + 5φ, and Inserting 1 to 3 Recovery Cycles and Accessing External Area)

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	See Figure 5.29		30	ns
$t_{h(BCLK-AD)}$	Address output hold time (in relation to BCLK)		0		ns
$t_{h(RD-AD)}$	Address output hold time (in relation to RD)		(Note 4)		ns
$t_{h(WR-AD)}$	Address output hold time (in relation to WR)		(Note 2)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			30	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (in relation to BCLK)		0		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			25	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		-4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			30	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			30	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (in relation to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data output hold time (in relation to BCLK) (3)		0		ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(Note 1)		ns
$t_{h(WR-DB)}$	Data output hold time (in relation to WR) (3)		(Note 2)		ns

Notes:

1. Calculated according to the BCLK frequency as follows:

$$\frac{n \times 10^9}{f_{(BCLK)}} - 40[ns]$$

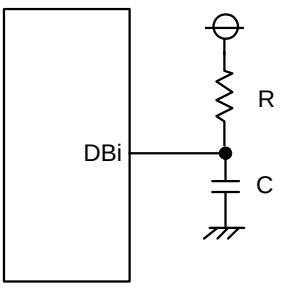
n is 3 for 2φ + 3φ, 4 for 2φ + 4φ, 4 for 3φ + 4φ, and 5 for 4φ + 5φ.

2. Calculated according to the BCLK frequency as follows:

$$\frac{m \times 10^9}{f_{(BCLK)}} - 10[ns]$$

m is 1 when 1 recovery cycle is inserted, 2 when 2 recovery cycles are inserted, and 3 when 3 recovery cycles are inserted.

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
Hold time of data bus is expressed in
$t = -CR \times \ln(1 - V_{OL}/V_{CC2})$
by a circuit of the right figure.
For example, when $V_{OL} = 0.2V_{CC2}$, C = 30 pF, R = 1 kΩ, hold time of output low level is
$t = -30\ pF \times 1\ k\Omega \times \ln(1 - 0.2V_{CC2}/V_{CC2})$
= 6.7 ns.



4. Calculated according to the BCLK frequency as follows:

$$\frac{m \times 10^9}{f_{(BCLK)}} + 0[ns]$$

m is 1 when 1 recovery cycle is inserted, 2 when 2 recovery cycles are inserted, and 3 when 3 recovery cycles are inserted.

REVISION HISTORY	M16C/65 Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	Feb 02, 2009	-	First Edition issued.
1.10	Sep 24, 2009	3	Table 1.2 Specifications for the 128-Pin Package (2/2) partially modified
		5	Table 1.4 Specifications for the 100-Pin Package (2/2) partially modified
		6	Table 1.5 Product List (1/2) partially modified
		7	Table 1.6 Product List (2/2) partially modified
		8	Figure 1.2 Marking Diagram (Top View) partially modified
		29	Figure 3.2 Memory Map 13800h → 13000h
		32	Table 4.2 “SFR Information (2/16)”notes partially modified
		48	Table 5.1 Absolute Maximum Ratings partially modified
		49	Table 5.2 Recommended Operating Conditions (1/3) partially modified
		50	Table 5.3 Recommended Operating Conditions (2/3) partially modified
		51	Table 5.4 Recommended Operating Conditions (3/3) added
		51	Figure 5.1 Ripple Waveform added
		52	Table 5.5 A/D Conversion Characteristics (1/2) partially modified
		52	Figure 5.2 A/D Accuracy Measure Circuit added
		53	Table 5.6 A/D Conversion Characteristics (2/2) partially modified
		55	Table 5.8 CPU Clock When Operating Flash Memory ($f_{(BCLK)}$) partially modified
		55	Table 5.9 Flash Memory (Program ROM 1, 2) Electrical Characteristics partially modified
		56	Table 5.10 Flash Memory (Data Flash) Electrical Characteristics notes modified
		57	Table 5.11 Voltage Detector 0 Electrical Characteristics partially modified
		57	Table 5.12 Voltage Detector 1 Electrical Characteristics partially modified
		58	Table 5.13 Voltage Detector 2 Electrical Characteristics partially modified
		58	Table 5.14 Power-On Reset Circuit partially modified
		59	Figure 5.3 Power-On Reset Circuit Electrical Characteristics 0.1 V → V_{por1}
		61	Table 5.16 40 MHz On-Chip Oscillator Circuit Electrical Characteristics (1/2) partially modified
		61	Table 5.17 40 MHz On-Chip Oscillator Circuit Electrical Characteristics (2/2) added
		61	Table 5.18 125 kHz On-Chip Oscillator Circuit Electrical Characteristics partially modified
		63	Table 5.20 Electrical Characteristics (2) partially modified
		64	Table 5.21 Electrical Characteristics (3) partially modified
		65	Table 5.22 Electrical Characteristics (4) partially modified
		66	Table 5.23 Electrical Characteristics (5) partially modified
		67	Table 5.24 Reset Input ($\overline{\text{RESET}}$ Input) partially modified
		85	Table 5.42 Electrical Characteristics (1) partially modified
		87	Table 5.44 Electrical Characteristics (3) partially modified
		88	Table 5.45 Electrical Characteristics (4) partially modified
		89	Table 5.46 Electrical Characteristics (5) partially modified
		90	Table 5.47 Reset Input ($\overline{\text{RESET}}$ Input) partially modified
2.00	Dec 10, 2010	Overall	001Ah Voltage Detector Operation Enable Register: Changed reset value from “000X 0000b”.
		Overall	002Ah Voltage Monitor 0 Control Register: Changed reset value from “1100 XX10b”.
		Overall	002Bh Voltage Monitor 1 Control Register: Changed reset value from “1000 1X10b”.
		Overall	0324h Increment/Decrement Flag: Changed name from Up/Down Flag.
		Overall	03DCh D/A Control Register: Changed reset value from “XXXX XX00b”.
		Overall	D08Ah to D08Bh PMC0 Counter Value Register: Deleted.
		Overall	D09Eh to D09Fh PMC1 Counter Value Register: Deleted.
		Overview	
		3, 5	Table 1.2 and Table 1.4 Specifications for the 128/100-Pin Package: Deleted note 1.
		6	Table 1.5 Product List (1/2): Changed the development status.
		19, 22	Table 1.12 and Table 1.15 Pin Functions: Changed the descriptions of the $\overline{\text{HOLD}}$ pin.
		Address Space	
		29	Figure 3.2 Memory Map: Added note 1 and 3 to the reserved areas.