Renesas Electronics America Inc - R5F3650TDFA#U0 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	M16C/60
Core Size	16-Bit
Speed	32MHz
Connectivity	EBI/EMI, I²C, SIO, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	85
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	47K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f3650tdfa-u0

1.6 Pin Functions

Table 1.12 Pin Functions for the 128-Pin Package (1/3)

Signal Name	Pin Name	I/O	Power Supply	Description
Power supply input	VCC1, VCC2, VSS	I	-	Apply 2.7 to 5.5 V to pins VCC1 and VCC2 (VCC1 ≥ VCC2), and 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	I	VCC1	This is the power supply for the A/D and D/A converters. Connect the AVCC pin to VCC1, and connect the AVSS pin to VSS.
Reset input	$\overline{\text{RESET}}$	I	VCC1	Driving this pin low resets the MCU.
CNVSS	CNVSS	I	VCC1	Input pin to switch processor modes. After a reset, to start operating in single-chip mode, connect the CNVSS pin to VSS via a resistor. To start operating in microprocessor mode, connect the pin to VCC1.
External data bus width select input	BYTE	I	VCC1	Input pin to select the data bus of the external area. The data bus is 16 bits when it is low and 8 bits when it is high. This pin must be fixed either high or low. Connect the BYTE pin to VSS in single-chip mode.
Bus control pins	D0 to D7	I/O	VCC2	Inputs or outputs data (D0 to D7) while accessing an external area with a separate bus.
	D8 to D15	I/O	VCC2	Inputs or outputs data (D8 to D15) while accessing an external area with a 16-bit separate bus.
	A0 to A19	O	VCC2	Outputs address bits A0 to A19.
	A0/D0 to A7/D7	I/O	VCC2	Inputs or outputs data (D0 to D7) and outputs address bits (A0 to A7) by timesharing, while accessing an external area with an 8-bit multiplexed bus.
	A1/D0 to A8/D7	I/O	VCC2	Inputs or outputs data (D0 to D7) and outputs address bits (A1 to A8) by timesharing, while accessing an external area with a 16-bit multiplexed bus.
	$\overline{\text{CS0}}$ to $\overline{\text{CS3}}$	O	VCC2	Outputs chip-select signals $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$ to specify an external area.
	$\overline{\text{WRL}}$/$\overline{\text{WR}}$ $\overline{\text{WRH}}$/$\overline{\text{BHE}}$ $\overline{\text{RD}}$	O	VCC2	Outputs $\overline{\text{WRL}}$, $\overline{\text{WRH}}$, ($\overline{\text{WR}}$, $\overline{\text{BHE}}$), and $\overline{\text{RD}}$ signals. $\overline{\text{WRL}}$ and $\overline{\text{WRH}}$ can be switched with $\overline{\text{BHE}}$ and $\overline{\text{WR}}$. • $\overline{\text{WRL}}$, $\overline{\text{WRH}}$, and $\overline{\text{RD}}$ selected If the external data bus is 16 bits, data is written to an even address in an external area when $\overline{\text{WRL}}$ is driven low. Data is written to an odd address when $\overline{\text{WRH}}$ is driven low. Data is read when $\overline{\text{RD}}$ is driven low. • $\overline{\text{WR}}$, $\overline{\text{BHE}}$, and $\overline{\text{RD}}$ selected Data is written to an external area when $\overline{\text{WR}}$ is driven low. Data in an external area is read when $\overline{\text{RD}}$ is driven low. An odd address is accessed when $\overline{\text{BHE}}$ is driven low. Select $\overline{\text{WR}}$, $\overline{\text{BHE}}$, and $\overline{\text{RD}}$ when using an 8-bit external data bus.
	ALE	O	VCC2	Outputs an ALE signal to latch the address.
	$\overline{\text{HOLD}}$	I	VCC2	$\overline{\text{HOLD}}$ input is unavailable. Connect the $\overline{\text{HOLD}}$ pin to VCC2 via a resistor (pull-up).
	$\overline{\text{HLDA}}$	O	VCC2	In a hold state, $\overline{\text{HLDA}}$ outputs a low-level signal.
	$\overline{\text{RDY}}$	I	VCC2	The MCU bus is placed in wait state while the $\overline{\text{RDY}}$ pin is driven low.

Power supply: VCC2 is used to supply power to the external bus associated pins. The dual power supply configuration allows VCC2 to interface at a different voltage than VCC1.

Table 1.15 Pin Functions for the 100-Pin Package (1/3)

Signal Name	Pin Name	I/O	Power Supply	Description
Power supply input	VCC1, VCC2, VSS	I	-	Apply 2.7 to 5.5 V to pins VCC1 and VCC2 (VCC1 ≥ VCC2) and 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	I	VCC1	This is the power supply for the A/D and D/A converters. Connect the AVCC pin to VCC1, and connect the AVSS pin to VSS.
Reset input	$\overline{\text{RESET}}$	I	VCC1	Driving this pin low resets the MCU.
CNVSS	CNVSS	I	VCC1	Input pin to switch processor modes. After a reset, to start operating in single-chip mode, connect the CNVSS pin to VSS via a resistor. To start operating in microprocessor mode, connect the pin to VCC1.
External data bus width select input	BYTE	I	VCC1	Input pin to select the data bus of the external area. The data bus is 16 bits when it is low, and 8 bits when it is high. This pin must be fixed either high or low. Connect the BYTE pin to VSS in single-chip mode.
Bus control pins	D0 to D7	I/O	VCC2	Inputs or outputs data (D0 to D7) while accessing an external area with a separate bus.
	D8 to D15	I/O	VCC2	Inputs or outputs data (D8 to D15) while accessing an external area with a 16-bit separate bus.
	A0 to A19	O	VCC2	Outputs address bits A0 to A19.
	A0/D0 to A7/D7	I/O	VCC2	Inputs or outputs data (D0 to D7) and outputs address bits (A0 to A7) by timesharing, while accessing an external area with an 8-bit multiplexed bus.
	A1/D0 to A8/D7	I/O	VCC2	Inputs or outputs data (D0 to D7) and outputs address bits (A1 to A8) by timesharing, while accessing an external area with a 16-bit multiplexed bus.
	$\overline{\text{CS0}}$ to $\overline{\text{CS3}}$	O	VCC2	Outputs chip-select signals $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$ to specify an external area.
	$\overline{\text{WRL}}$/$\overline{\text{WR}}$ $\overline{\text{WRH}}$/$\overline{\text{BHE}}$ $\overline{\text{RD}}$	O	VCC2	Outputs $\overline{\text{WRL}}$, $\overline{\text{WRH}}$, ($\overline{\text{WR}}$, $\overline{\text{BHE}}$), and $\overline{\text{RD}}$ signals. $\overline{\text{WRL}}$ and $\overline{\text{WRH}}$ can be switched with $\overline{\text{BHE}}$ and $\overline{\text{WR}}$. • $\overline{\text{WRL}}$, $\overline{\text{WRH}}$, and $\overline{\text{RD}}$ selected If the external data bus is 16 bits, data is written to an even address in an external area when $\overline{\text{WRL}}$ is driven low. Data is written to an odd address when $\overline{\text{WRH}}$ is driven low. Data is read when $\overline{\text{RD}}$ is driven low. • $\overline{\text{WR}}$, $\overline{\text{BHE}}$, and $\overline{\text{RD}}$ selected Data is written to an external area when $\overline{\text{WR}}$ is driven low. Data in an external area is read when $\overline{\text{RD}}$ is driven low. An odd address is accessed when $\overline{\text{BHE}}$ is driven low. Select $\overline{\text{WR}}$, $\overline{\text{BHE}}$, and $\overline{\text{RD}}$ when using an 8-bit external data bus.
	ALE	O	VCC2	Outputs an ALE signal to latch the address.
	$\overline{\text{HOLD}}$	I	VCC2	$\overline{\text{HOLD}}$ input is unavailable. Connect the $\overline{\text{HOLD}}$ pin to VCC2 via a resistor (pull-up).
	$\overline{\text{HLDA}}$	O	VCC2	In a hold state, $\overline{\text{HLDA}}$ outputs a low-level signal.
	$\overline{\text{RDY}}$	I	VCC2	The MCU bus is placed in a wait state while the $\overline{\text{RDY}}$ pin is driven low.

Power supply: VCC2 is used to supply power to the external bus associated pins. The dual power supply configuration allows VCC2 to interface at a different voltage than VCC1.

Table 4.7 SFR Information (7) (1)

Address	Register	Symbol	Reset Value
01E0h	Timer B3-1 Register	TB31	XXh
01E1h			XXh
01E2h	Timer B4-1 Register	TB41	XXh
01E3h			XXh
01E4h	Timer B5-1 Register	TB51	XXh
01E5h			XXh
01E6h	Pulse Period/Pulse Width Measurement Mode Function Select Register 2	PPWFS2	XXXX X000b
01E7h			
01E8h	Timer B Count Source Select Register 2	TBCS2	00h
01E9h	Timer B Count Source Select Register 3	TBCS3	X0h
01EAh			
01EBh			
01ECh			
01EDh			
01EEh			
01EFh			
01F0h	PMC0 Function Select Register 0	PMC0CON0	00h
01F1h	PMC0 Function Select Register 1	PMC0CON1	00XX 0000b
01F2h	PMC0 Function Select Register 2	PMC0CON2	0000 00X0b
01F3h	PMC0 Function Select Register 3	PMC0CON3	00h
01F4h	PMC0 Status Register	PMC0STS	00h
01F5h	PMC0 Interrupt Source Select Register	PMC0INT	00h
01F6h	PMC0 Compare Control Register	PMC0CPC	XXX0 X000b
01F7h	PMC0 Compare Data Register	PMC0CPD	00h
01F8h	PMC1 Function Select Register 0	PMC1CON0	XXX0 X000b
01F9h	PMC1 Function Select Register 1	PMC1CON1	XXXX 0X00b
01FAh	PMC1 Function Select Register 2	PMC1CON2	0000 00X0b
01FBh	PMC1 Function Select Register 3	PMC1CON3	00h
01FCh	PMC1 Status Register	PMC1STS	X000 X00Xb
01FDh	PMC1 Interrupt Source Select Register	PMC1INT	X000 X00Xb
01FEh			
01FFh			
0200h			
0201h			
0202h			
0203h			
0204h			
0205h	Interrupt Source Select Register 3	IFSR3A	00h
0206h	Interrupt Source Select Register 2	IFSR2A	00h
0207h	Interrupt Source Select Register	IFSR	00h
0208h			
0209h			
020Ah			
020Bh			
020Ch			
020Dh			
020Eh	Address Match Interrupt Enable Register	AIER	XXXX XX00b
020Fh	Address Match Interrupt Enable Register 2	AIER2	XXXX XX00b

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.15 SFR Information (15) (1)

Address	Register	Symbol	Reset Value
0390h	DMA2 Source Select Register	DM2SL	00h
0391h			
0392h	DMA3 Source Select Register	DM3SL	00h
0393h			
0394h			
0395h			
0396h			
0397h			
0398h	DMA0 Source Select Register	DM0SL	00h
0399h			
039Ah	DMA1 Source Select Register	DM1SL	00h
039Bh			
039Ch			
039Dh			
039Eh			
039Fh			
03A0h			
03A1h			
03A2h	Open-Circuit Detection Assist Function Register	AINRST	XX00 XXXXb
03A3h			
03A4h			
03A5h			
03A6h			
03A7h			
03A8h			
03A9h			
03AAh			
03ABh			
03ACh			
03ADh			
03AEh			
03AFh			
03B0h			
03B1h			
03B2h			
03B3h			
03B4h	SFR Snoop Address Register	CRCSAR	XXXX XXXXb
03B5h			00XX XXXXb
03B6h	CRC Mode Register	CRCMR	0XXX XXX0b
03B7h			
03B8h			
03B9h			
03BAh			
03BBh			
03BCh	CRC Data Register	CRCD	XXh
03BDh			XXh
03BEh	CRC Input Register	CRCIN	XXh
03BFh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.17 SFR Information (17) (1)

Address	Register	Symbol	Reset Value
03F0h	Port P8 Register	P8	XXh
03F1h	Port P9 Register	P9	XXh
03F2h	Port P8 Direction Register	PD8	00h
03F3h	Port P9 Direction Register	PD9	00h
03F4h	Port P10 Register	P10	XXh
03F5h	Port P11 Register	P11	XXh
03F6h	Port P10 Direction Register	PD10	00h
03F7h	Port P11 Direction Register	PD11	00h
03F8h	Port P12 Register	P12	XXh
03F9h	Port P13 Register	P13	XXh
03FAh	Port P12 Direction Register	PD12	00h
03FBh	Port P13 Direction Register	PD13	00h
03FCh	Port P14 Register	P14	XXh
03FDh			
03FEh	Port P14 Direction Register	PD14	XXXX XX00b
03FFh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

4.2 Notes on SFRs

4.2.1 Register Settings

Table 4.19 lists Registers with Write-Only Bits and registers whose function differs between reading and writing. Set these registers with immediate values. Do not use read-modify-write instructions. When establishing the next value by altering the existing value, write the existing value to the RAM as well as to the register. Transfer the next value to the register after making changes in the RAM.
Read-modify-write instructions can be used when writing to the no register bits.

Table 4.19 Registers with Write-Only Bits

Address	Register	Symbol
0249h	UART0 Bit Rate Register	U0BRG
024Bh to 024Ah	UART0 Transmit Buffer Register	U0TB
0259h	UART1 Bit Rate Register	U1BRG
025Bh to 025Ah	UART1 Transmit Buffer Register	U1TB
0269h	UART2 Bit Rate Register	U2BRG
026Bh to 026Ah	UART2 Transmit Buffer Register	U2TB
0273h	SI/O3 Bit Rate Register	S3BRG
0277h	SI/O4 Bit Rate Register	S4BRG
0289h	UART5 Bit Rate Register	U5BRG
028Bh to 028Ah	UART5 Transmit Buffer Register	U5TB
0299h	UART6 Bit Rate Register	U6BRG
029Bh to 029Ah	UART6 Transmit Buffer Register	U6TB
02A9h	UART7 Bit Rate Register	U7BRG
02ABh to 02AAh	UART7 Transmit Buffer Register	U7TB
02B6h	I2C0 Control Register 1	S3D0
02B8h	I2C0 Status Register 0	S10
0303h to 0302h	Timer A1-1 Register	TA11
0305h to 0304h	Timer A2-1 Register	TA21
0307h to 0306h	Timer A4-1 Register	TA41
030Ah	Three-Phase Output Buffer Register 0	IDB0
030Bh	Three-Phase Output Buffer Register 1	IDB1
030Ch	Dead Time Timer	DTT
030Dh	Timer B2 Interrupt Generation Frequency Set Counter	ICTB2
0327h to 0326h	Timer A0 Register	TA0
0329h to 0328h	Timer A1 Register	TA1
032Bh to 032Ah	Timer A2 Register	TA2
032Dh to 032Ch	Timer A3 Register	TA3
032Fh to 032Eh	Timer A4 Register	TA4
037Dh	Watchdog Timer Refresh Register	WDTR
037Eh	Watchdog Timer Start Register	WDTS

5. Electrical Characteristics

5.1 Electrical Characteristics (Common to 3 V and 5 V)

5.1.1 Absolute Maximum Rating

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter		Condition	Rated Value	Unit
V_{CC1}	Supply voltage		$V_{CC1} = AV_{CC}$	–0.3 to 6.5	V
V_{CC2}	Supply voltage		$V_{CC1} = AV_{CC}$	–0.3 to V_{CC1} + 0.1 (1)	V
AV_{CC}	Analog supply voltage		$V_{CC1} = AV_{CC}$	–0.3 to 6.5	V
V_{REF}	Analog reference voltage		$V_{CC1} = AV_{CC}$	–0.3 to V_{CC1} + 0.1 (1)	V
V_I	Input voltage	$\overline{RESET}$, CNVSS, BYTE, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1 XIN		–0.3 to V_{CC1} + 0.3 (1)	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7		–0.3 to V_{CC2} + 0.3 (1)	V
		P7_0, P7_1, P8_5		–0.3 to 6.5	V
V_O	Output voltage	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1 XOUT		–0.3 to V_{CC1} + 0.3 (1)	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7		–0.3 to V_{CC2} + 0.3 (1)	V
		P7_0, P7_1, P8_5		–0.3 to 6.5	V
P_d	Power consumption		$-40°C < T_{opr} \leq 85°C$	300	mW
T_{opr}	Operating temperature	When the MCU is operating		–20 to 85/–40 to 85	°C
		Flash program erase	Program area	0 to 60	
			Data area	–20 to 85/–40 to 85	
T_{stg}	Storage temperature			–65 to 150	°C

Note:
1. Maximum value is 6.5 V.

5.1.2 Recommended Operating Conditions

Table 5.2 Recommended Operating Conditions (1/3)

V_{CC1} = V_{CC2} = 2.7 to 5.5 V at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified.

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
V_{CC1}, V_{CC2}	Supply voltage ($V_{CC1} \geq V_{CC2}$)	CEC function is not used	2.7	5.0	5.5	V
		CEC function is used	2.7		3.63	V
AV_{CC}	Analog supply voltage			V_{CC1}		V
V_{SS}	Supply voltage			0		V
AV_{SS}	Analog supply voltage			0		V
V_{IH}	High input voltage	P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	$0.8V_{CC2}$		V_{CC2}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (in single-chip mode)	$0.8V_{CC2}$		V_{CC2}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (data input in memory expansion and microprocessor modes)	$0.5V_{CC2}$		V_{CC2}	V
		P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1 XIN, $\overline{\text{RESET}}$, CNVSS, BYTE	$0.8V_{CC1}$		V_{CC1}	V
		P7_0, P7_1, P8_5	$0.8V_{CC1}$		6.5	V
		CEC	$0.7V_{CC1}$			V
V_{IL}	Low input voltage	P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	0		$0.2V_{CC2}$	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (in single-chip mode)	0		$0.2V_{CC2}$	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (data input in memory expansion and microprocessor mode)	0		$0.16V_{CC2}$	V
		P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7,P11_0 to P11_7, P14_0, P14_1 XIN, $\overline{\text{RESET}}$, CNVSS, BYTE	0		$0.2V_{CC1}$	V
		CEC			$0.26V_{CC1}$	V
$I_{OH(sum)}$	High peak output current	Sum of $I_{OH(peak)}$ at P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7			-40.0	mA
		Sum of $I_{OH(peak)}$ at P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, and P13_0 to P13_7			-40.0	mA
		Sum of $I_{OH(peak)}$ at P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4			-40.0	mA
		Sum of $I_{OH(peak)}$ at P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0 to P14_1			-40.0	mA
$I_{OH(peak)}$	High peak output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			–10.0	mA
$I_{OH(avg)}$	High average output current (1)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			–5.0	mA

Note:
1. The average output current is the mean value within 100 ms.

5.1.3 A/D Conversion Characteristics

Table 5.5 A/D Conversion Characteristics (1/2) (1)

V_{CC1} = AV_{CC} = 3.0 to 5.5 V ≥ V_{CC2} ≥ V_{REF}, V_{SS} = AV_{SS} = 0 V at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified.

Symbol	Parameter		Measuring Condition		Standard			Unit
					Min.	Typ.	Max.	
-	Resolution		AV_{CC} = V_{CC1} ≥ V_{CC2} ≥ V_{REF}				10	Bits
I_{NL}	Integral non-linearity error	10 bits	V_{CC1} = 5.0 V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input (Note 2)			±3	LSB
			V_{CC1} = 3.3 V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input (Note 2)			±3	LSB
			V_{CC1} = 3.0 V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input (Note 2)			±3	LSB
-	Absolute accuracy	10 bits	V_{CC1} = 5.0 V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input (Note 2)			±3	LSB
			V_{CC1} = 3.3 V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input (Note 2)			±3	LSB
			V_{CC1} = 3.0 V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input (Note 2)			±3	LSB

Notes:
1. Use when AV_{CC} = V_{CC1}.
2. Flash memory rewrite disabled. Except for the analog input pin, set the pins to be measured as input ports and connect them to V_{SS}. See Figure 5.2 “A/D Accuracy Measure Circuit”.

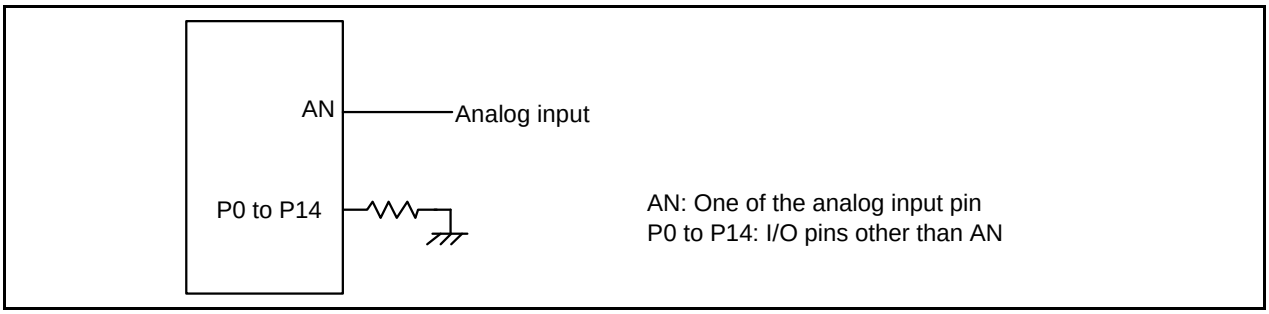


Figure 5.2 A/D Accuracy Measure Circuit

Table 5.6 A/D Conversion Characteristics (2/2) (1)

V_{CC1} = AV_{CC} = 3.0 to 5.5 V ≥ V_{CC2} ≥ V_{REF}, V_{SS} = AV_{SS} = 0 V at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified.

Symbol	Parameter		Measuring Condition	Standard			Unit
				Min.	Typ.	Max.	
ϕAD	A/D operating clock frequency	AN0 to AN7 input, ANEX0 to ANEX1 input	4.0 V ≤ V_{CC1} ≤ 5.5 V	2		25	MHz
			3.2 V ≤ V_{CC1} ≤ 4.0 V	2		16	MHz
			3.0 V ≤ V_{CC1} ≤ 3.2 V	2		10	MHz
		AN0_0 to AN0_7 input, AN2_0 to AN2_7 input	4.0 V ≤ V_{CC2} ≤ 5.5 V	2		25	MHz
			3.2 V ≤ V_{CC2} ≤ 4.0 V	2		16	MHz
			3.0 V ≤ V_{CC2} ≤ 3.2 V	2		10	MHz
-	Tolerance level impedance				3		kΩ
D_{NL}	Differential non-linearity error		(4)			±1	LSB
-	Offset error		(4)			±3	LSB
-	Gain error		(4)			±3	LSB
t_{CONV}	10-bit conversion time		V_{CC1} = 5 V, ϕAD = 25 MHz	1.60			µs
t_{SAMP}	Sampling time			0.60			µs
V_{REF}	Reference voltage			3.0		V_{CC1}	V
V_{IA}	Analog input voltage (2), (3)			0		V_{REF}	V

Notes:
1. Use when AV_{CC} = V_{CC1}.
2. When V_{CC1} ≥ V_{CC2}, set as below:
   Analog input voltage (AN0 to AN7, ANEX0, and ANEX1) ≤ V_{CC1}
   Analog input voltage (AN0_0 to AN0_7 and AN2_0 to AN2_7) ≤ V_{CC2}.
3. When analog input voltage is over reference voltage, the result of A/D conversion is 3FFh.
4. Flash memory rewrite disabled. Except for the analog input pin, set the pins to be measured as input ports and connect them to V_{SS}. See Figure 5.2 “A/D Accuracy Measure Circuit”.

5.1.4 D/A Conversion Characteristics

Table 5.7 D/A Conversion Characteristics

V_{CC1} = AV_{CC} = V_{REF} = 3.0 to 5.5 V, V_{SS} = AV_{SS} = 0 V at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified.

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
-	Resolution				8	Bits
-	Absolute Accuracy				2.5	LSB
t_{SU}	Setup Time				3	µs
R_O	Output Resistance		5	6	8.2	kΩ
I_{VREF}	Reference Power Supply Input Current	See Notes 1 and 2			1.5	mA

Notes:
1. This applies when using one D/A converter, with the D/A register for the unused D/A converter set to 00h.
2. The current consumption of the A/D converter is not included. Also, the I_{VREF} of the D/A converter will flow even if the ADSTBY bit in the ADCON1 register is 0 (A/D operation stopped (standby)).

$V_{CC1} = V_{CC2} = 5\ V$

Table 5.21 Electrical Characteristics (3)

R5F36506NFA, R5F36506NFB, R5F36506DFA, R5F36506DFB, R5F3650ENFA, R5F3650ENFB, R5F3650EDFA, R5F3650EDFB

$V_{CC1} = V_{CC2} = 4.2$ to 5.5 V, $V_{SS} = 0$ V at $T_{opr} = -20°C$ to 85°C/−40°C to 85°C, $f_{(BCLK)} = 32$ MHz unless otherwise specified.

Symbol	Parameter	Measuring Condition		Standard			Unit
				Min.	Typ.	Max.	
R_{fXCIN}	Feedback resistance XCIN				8		MΩ
I_{CC}	Power supply current In single-chip, mode, the output pin are open and other pins are V_{SS}	High-speed mode	$f_{(BCLK)}$ = 32 MHz XIN = 4 MHz (square wave), PLL multiplied by 8 125 kHz on-chip oscillator stopped		24.0		mA
			$f_{(BCLK)}$ =32 MHz, A/D conversion XIN = 4 MHz (square wave), PLL multiplied by 8 125 kHz on-chip oscillator stopped		24.7		mA
			$f_{(BCLK)}$ = 20 MHz XIN = 20 MHz (square wave) 125 kHz on-chip oscillator stopped		16.0		mA
		40 MHz on-chip oscillator mode	Main clock stopped 40 MHz on-chip oscillator on, divide-by-4 ($f_{(BCLK)}$ = 10 MHz) 125 kHz on-chip oscillator stopped		17.0		mA
		125 kHz on-chip oscillator mode	Main clock stopped 40 MHz on-chip oscillator stopped, 125 kHz on-chip oscillator on, no division FMR22 = 1 (slow read mode)		500.0		µA
		Low-power mode	$f_{(BCLK)}$ = 32 kHz In low-power mode FMR22 = FMR23 = 1 On flash memory (1)		160.0		µA
			$f_{(BCLK)}$ = 32 kHz In low-power mode On RAM (1)		45.0		µA
		Wait mode	Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator on Peripheral clock operating T_{opr} = 25°C		20.0		µA
			$f_{(BCLK)}$ = 32 kHz (oscillation capacity High) 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator stopped Peripheral clock operating T_{opr} = 25°C		11.0		µA
			$f_{(BCLK)}$ = 32 kHz (oscillation capacity Low) 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator stopped Peripheral clock operating T_{opr} = 25°C		6.0		µA
		Stop mode	Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator stopped Peripheral clock stopped T_{opr} = 25°C		1.7		µA
		During flash memory program	$f_{(BCLK)}$ = 10 MHz, PM17 = 1 (one wait) V_{CC1} = 5.0 V		20.0		mA
		During flash memory erase	$f_{(BCLK)}$ = 10 MHz, PM17 = 1 (one wait) V_{CC1} = 5.0 V		30.0		mA

Note:
1. This indicates the memory in which the program to be executed exists.

$V_{CC1} = V_{CC2} = 5\ V$

Table 5.23 Electrical Characteristics (5)

R5F3651RNFC, R5F3650RNFA, R5F3650RNFB, R5F3651RDFC, R5F3650RDFA, R5F3650RDFB, R5F3651TNFC, R5F3650TNFA, R5F3650TNFB, R5F3651TDFC, R5F3650TDFA, R5F3650TDFB

$V_{CC1} = V_{CC2} = 4.2$ to 5.5 V, $V_{SS} = 0$ V at $T_{opr} = -20$ to 85°C/−40 to 85°C, $f_{(BCLK)} = 32$ MHz unless otherwise specified.

Symbol	Parameter	Measuring Condition		Standard			Unit
				Min.	Typ.	Max.	
R_{fXCIN}	Feedback resistance XCIN				15		MΩ
I_{CC}	Power supply current In single-chip, mode, the output pin are open and other pins are V_{SS}	High-speed mode	$f_{(BCLK)}$ = 32 MHz XIN = 4 MHz (square wave), PLL multiplied by 8 125 kHz on-chip oscillator stopped		32.0		mA
			$f_{(BCLK)}$ = 32 MHz, A/D conversion XIN = 4 MHz (square wave), PLL multiplied by 8 125 kHz on-chip oscillator stopped		32.7		mA
			$f_{(BCLK)}$ = 20 MHz XIN = 20 MHz (square wave) 125 kHz on-chip oscillator stopped		21.0		mA
		40 MHz on-chip oscillator mode	Main clock stopped 40 MHz on-chip oscillator on, divide-by-4 (f(BCLK) = 10 MHz) 125 kHz on-chip oscillator stopped		23.0		mA
		125 kHz on-chip oscillator mode	Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator on, no division FMR22 = 1 (slow read mode)		750.0		µA
		Low-power mode	$f_{(BCLK)}$ = 32 kHz In low-power mode FMR22 = FMR23 = 1 on flash memory (1)		250.0		µA
			$f_{(BCLK)}$ = 32 kHz In low-power mode on RAM (1)		45.0		µA
		Wait mode	Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator on Peripheral clock operating T_{opr} = 25°C		21.0		µA
			$f_{(BCLK)}$ = 32 kHz (oscillation capacity High) 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator stopped Peripheral clock operating T_{opr} = 25°C		11.0		µA
			$f_{(BCLK)}$ = 32 kHz (oscillation capacity Low) 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator stopped Peripheral clock operating T_{opr} = 25°C		6.0		µA
		Stop mode	Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator stopped Peripheral clock stopped T_{opr} = 25°C		1.7		µA
		During flash memory program	$f_{(BCLK)}$ = 10 MHz, PM17 = 1 (one wait) V_{CC1} = 5.0 V		20.0		mA
		During flash memory erase	$f_{(BCLK)}$ = 10 MHz, PM17 = 1 (one wait) V_{CC1} = 5.0 V		30.0		mA

Note:
1. This indicates the memory in which the program to be executed exists.

$V_{CC1} = V_{CC2} = 5\ V$

5.2.2 Timing Requirements (Peripheral Functions and Others)

($V_{CC1} = V_{CC2} = 5$ V, $V_{SS} = 0$ V, at $T_{opr} = -20°C$ to 85°C/-40°C to 85°C unless otherwise specified)

5.2.2.1 Reset Input ($\overline{\text{RESET}}$ Input)

Table 5.24 Reset Input ($\overline{\text{RESET}}$ Input)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(RSTL)}$	$\overline{\text{RESET}}$ input low pulse width	10		µs

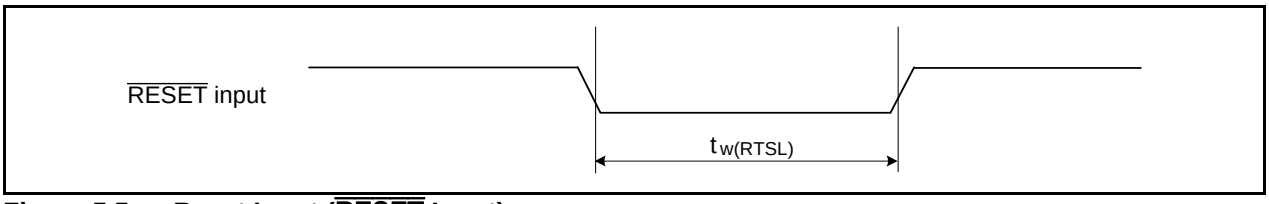


Figure 5.5 Reset Input ($\overline{\text{RESET}}$ Input)

5.2.2.2 External Clock Input

Table 5.25 External Clock Input (XIN Input) (1)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External clock input cycle time	50		ns
$t_{w(H)}$	External clock input high pulse width	20		ns
$t_{w(L)}$	External clock input low pulse width	20		ns
t_r	External clock rise time		9	ns
t_f	External clock fall time		9	ns

Note:
1. The condition is $V_{CC1} = V_{CC2} = 3.0$ to 5.0 V.

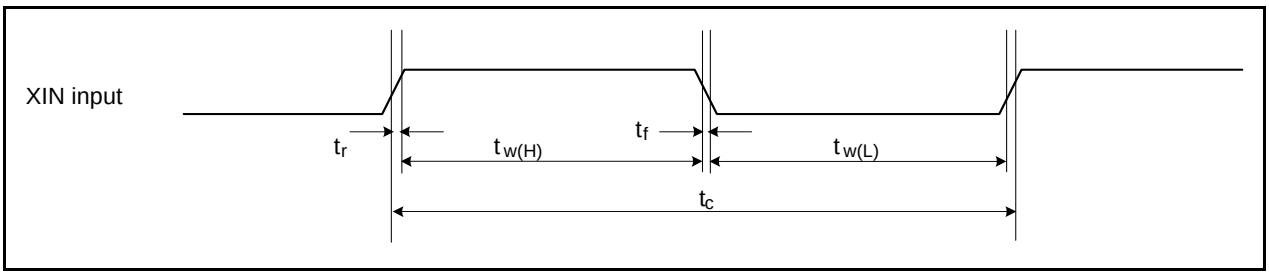


Figure 5.6 External Clock Input (XIN Input)

5.3 Electrical Characteristics (V_{CC1} = V_{CC2} = 3 V)

5.3.1 Electrical Characteristics

VCC1 = VCC2 = 3 V

Table 5.43 Electrical Characteristics (1) [1]

V_{CC1} = V_{CC2} = 2.7 to 3.3 V, V_{SS} = 0 V at T_{opr} = -20°C to 85°C/-40°C to 85°C, $f_{(BCLK)}$ = 32 MHz unless otherwise specified.

Symbol	Parameter			Measuring Condition	Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	High output voltage	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1		I_{OH} = –1 mA	V_{CC1} – 0.5		V_{CC1}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7		I_{OH} = –1 mA	V_{CC2} – 0.5		V_{CC2}	
V_{OH}	High output voltage XOUT		HIGH POWER	I_{OH} = –0.1 mA	V_{CC1} – 0.5		V_{CC1}	V
			LOW POWER	I_{OH} = –50 µA	V_{CC1} – 0.5		V_{CC1}	
	High output voltage XCOUT		HIGH POWER	With no load applied		2.6		V
			LOW POWER	With no load applied		2.2		
V_{OL}	Low output voltage	P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1		I_{OL} = 1 mA			0.5	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7		I_{OL} = 1 mA			0.5	
		CEC		I_{OL} = 1 mA		0	0.5	V
V_{OL}	Low output voltage XOUT		HIGH POWER	I_{OL} = 0.1 mA			0.5	V
			LOW POWER	I_{OL} = 50 µA			0.5	
	Low output voltage XCOUT		HIGH POWER	With no load applied		0		V
			LOW POWER	With no load applied		0		
V_{T+}-V_{T-}	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, TA0IN to TA4IN, TB0IN to TB5IN, $\overline{INT0}$ to $\overline{INT7}$, $\overline{NMI}$, $\overline{ADTRG}$, $\overline{CTS0}$ to $\overline{CTS2}$, $\overline{CTS5}$ to $\overline{CTS7}$, SCL0 to SCL2, SCL5 to SCL7, SDA0 to SDA2, SDA5 to SDA7, CLK0 to CLK7, TA0OUT to TA4OUT, $\overline{KI0}$ to $\overline{KI3}$, RXD0 to RXD2, RXD5 to RXD7, SIN3, SIN4, $\overline{SD}$, PMC0, PMC1, SCLMM, SDAMM, ZP, IDU, IDV, IDW			0.2		1.0	V
		CEC			0.2	0.5	1.0	V
		$\overline{RESET}$			0.2		1.8	V
I_{IH}	High input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1 XIN, $\overline{RESET}$, CNVSS, BYTE		V_I = 3 V			4.0	µA
–	Leakage current in powered-off state		CEC	V_{CC1} = 0 V			1.8	µA
I_{IL}	Low input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1 XIN, $\overline{RESET}$, CNVSS, BYTE		V_I = 0 V			–4.0	µA
R_{PULLUP}	Pull-up resistance	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1		V_I = 0 V	50	80	150	kΩ
R_{fXIN}	Feedback resistance XIN					3.0		MΩ
V_{RAM}	RAM retention voltage			In stop mode	1.8			V

Note:
1. When $V_{CC1} \neq V_{CC2}$, refer to 5 V or 3 V standard depending on the voltage.

$V_{CC1} = V_{CC2} = 3\ V$

5.3.2 Timing Requirements (Peripheral Functions and Others)

($V_{CC1} = V_{CC2} = 3$ V, $V_{SS} = 0$ V, at $T_{opr} = -20°C$ to 85°C/-40°C to 85°C unless otherwise specified)

5.3.2.1 Reset Input ($\overline{\text{RESET}}$ Input)

Table 5.47 Reset Input ($\overline{\text{RESET}}$ Input)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(RSTL)}$	$\overline{\text{RESET}}$ input low pulse width	10		µs

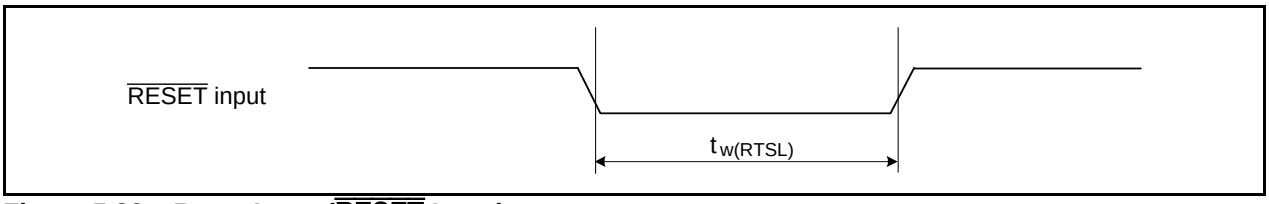


Figure 5.20 Reset Input ($\overline{\text{RESET}}$ Input)

5.3.2.2 External Clock Input

Table 5.48 External Clock Input (XIN Input) (1)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External clock input cycle time	50		ns
$t_{w(H)}$	External clock input high pulse width	20		ns
$t_{w(L)}$	External clock input low pulse width	20		ns
t_r	External clock rise time		9	ns
t_f	External clock fall time		9	ns

Note:
1. The condition is $V_{CC1} = V_{CC2} = 2.7$ to 3.0 V.

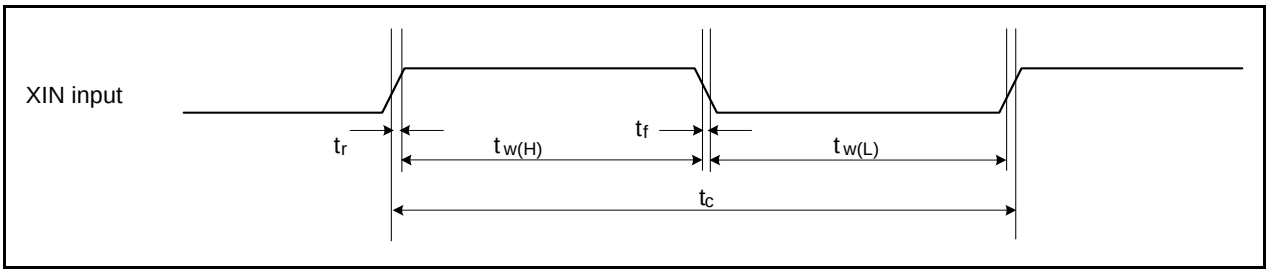


Figure 5.21 External Clock Input (XIN Input)

$V_{CC1} = V_{CC2} = 3\ V$

5.3.4 Switching Characteristics (Memory Expansion Mode and Microprocessor Mode)

($V_{CC1} = V_{CC2} = 3$ V, $V_{SS} = 0$ V, at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified)

5.3.4.1 In No Wait State Setting

Table 5.61 Memory Expansion and Microprocessor Modes (in No Wait State Setting)

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	See Figure 5.29		30	ns
$t_{h(BCLK-AD)}$	Address output hold time (in relation to BCLK)		0		ns
$t_{h(RD-AD)}$	Address output hold time (in relation to RD)		0		ns
$t_{h(WR-AD)}$	Address output hold time (in relation to WR)		(Note 2)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			30	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (in relation to BCLK)		0		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			25	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		–4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			30	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			30	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (in relation to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data output hold time (in relation to BCLK) (3)		0		ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(Note 1)		ns
$t_{h(WR-DB)}$	Data output hold time (in relation to WR) (3)		(Note 2)		ns

Notes:

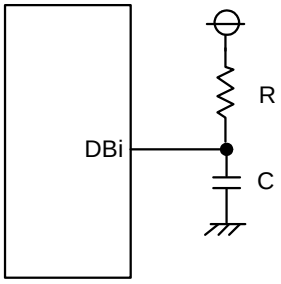
1. Calculated according to the BCLK frequency as follows:

   $\frac{0.5 \times 10^9}{f_{(BCLK)}} - 40[ns]$ $f_{(BCLK)}$ is 12.5 MHz or less.

2. Calculated according to the BCLK frequency as follows:

   $\frac{0.5 \times 10^9}{f_{(BCLK)}} - 10[ns]$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
   Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
   Hold time of data bus is expressed in
   $t = -CR \times \ln(1 - V_{OL}/V_{CC2})$
   by a circuit of the right figure.
   For example, when $V_{OL} = 0.2V_{CC2}$, C = 30 pF, R = 1 kΩ,
   hold time of output low level is
   $t = -30\ pF \times 1\ k\Omega \times \ln(1 - 0.2V_{CC2}/V_{CC2})$
   = 6.7 ns.



$V_{CC1} = V_{CC2} = 3\ V$

Switching Characteristics

($V_{CC1} = V_{CC2} = 3$ V, $V_{SS} = 0$ V, at $T_{opr} = -20°C$ to 85°C/-40°C to 85°C unless otherwise specified)

5.3.4.2 In 1 to 3 Waits Setting and When Accessing External Area

Table 5.62 Memory Expansion Mode and Microprocessor Mode (in 1 to 3 Waits Setting and When Accessing External Area)

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	See Figure 5.29		30	ns
$t_{h(BCLK-AD)}$	Address output hold time (in relation to BCLK)		0		ns
$t_{h(RD-AD)}$	Address output hold time (in relation to RD)		0		ns
$t_{h(WR-AD)}$	Address output hold time (in relation to WR)		(Note 2)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			30	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (in relation to BCLK)		0		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			25	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		-4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			30	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			30	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (in relation to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data output hold time (in relation to BCLK) (3)		0		ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(Note 1)		ns
$t_{h(WR-DB)}$	Data output hold time (in relation to WR) (3)		(Note 2)		ns

Notes:

1. Calculated according to the BCLK frequency as follows:

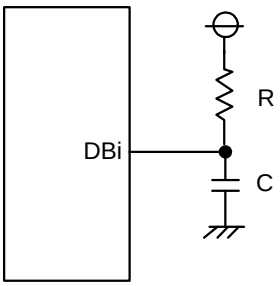
$$\frac{(n-0.5)\times 10^9}{f_{(BCLK)}} - 40[ns]$$

n is 1 for 1 wait setting, 2 for 2 waits setting and 3 for 3 waits setting.
When n = 1, $f_{(BCLK)}$ is 12.5 MHz or less.

2. Calculated according to the BCLK frequency as follows:

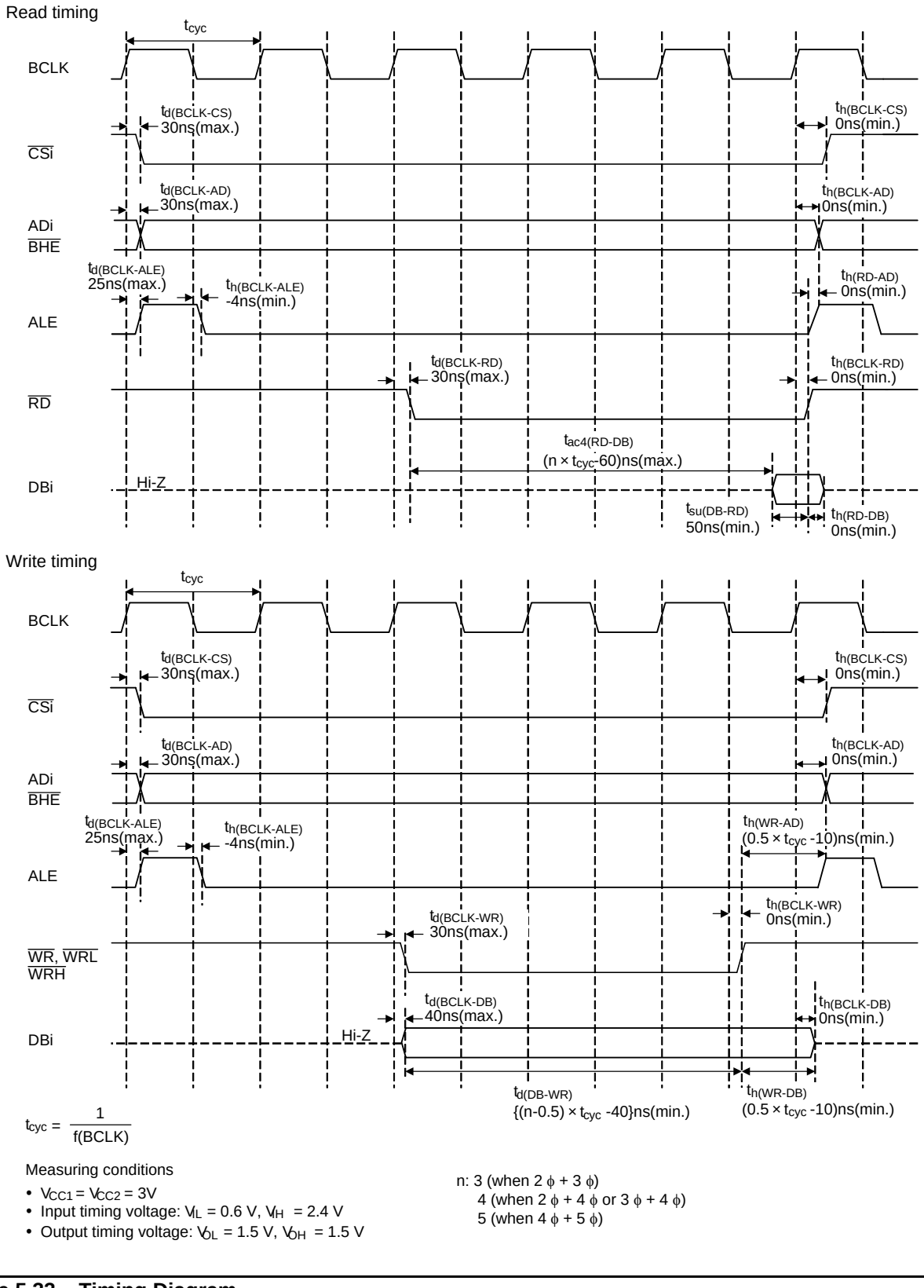
$$\frac{0.5\times 10^9}{f_{(BCLK)}} - 10[ns]$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
Hold time of data bus is expressed in
$t = -CR \times \ln(1 - V_{OL}/V_{CC2})$
by a circuit of the right figure.
For example, when $V_{OL} = 0.2V_{CC2}$, C = 30 pF, R = 1 kΩ, hold time of output low level is
$t = -30\ pF \times 1\ k\Omega \times \ln(1 - 0.2V_{CC2}/V_{CC2})$
= 6.7 ns.



Memory Expansion Mode, Microprocessor Mode
(in wait state setting 2 ϕ + 3 ϕ, 2 ϕ + 4 ϕ, 3ϕ + 4 ϕ, and 4 ϕ + 5 ϕ, and when accessing external area)

$V_{CC1} = V_{CC2} = 3V$



$t_{cyc} = \frac{1}{f(BCLK)}$

Measuring conditions

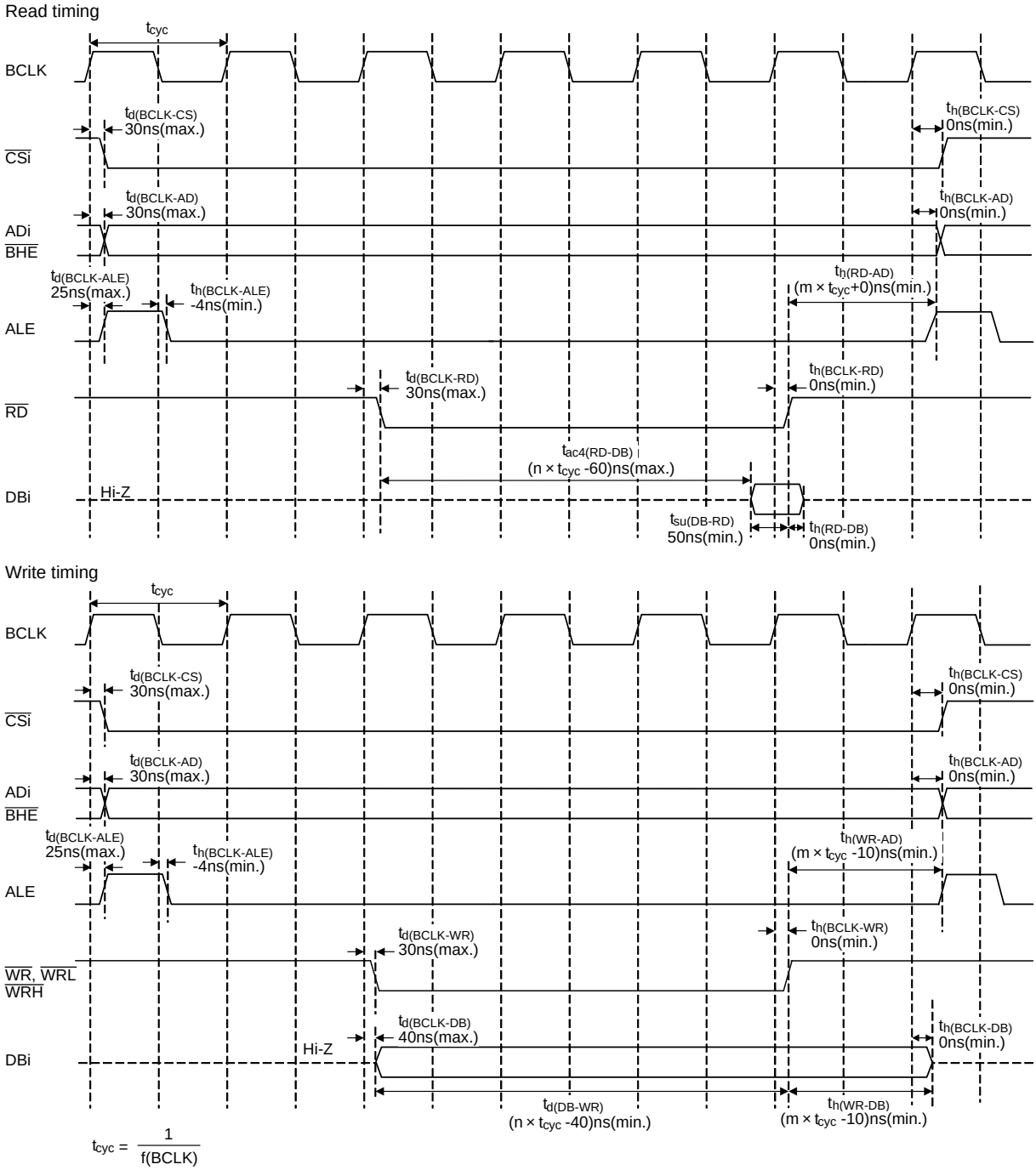
- $V_{CC1} = V_{CC2} = 3V$
- Input timing voltage: $V_{IL} = 0.6$ V, $V_{IH} = 2.4$ V
- Output timing voltage: $V_{OL} = 1.5$ V, $V_{OH} = 1.5$ V

n: 3 (when 2 ϕ + 3 ϕ)
4 (when 2 ϕ + 4 ϕ or 3 ϕ + 4 ϕ)
5 (when 4 ϕ + 5 ϕ)

Figure 5.33 Timing Diagram

Memory Expansion Mode and Microprocessor Mode
(in wait state setting 2 ϕ + 3 ϕ, 2 ϕ + 4 ϕ, 3ϕ + 4 ϕ, and 4 ϕ + 5 ϕ, and
when inserting 1 to 3 recovery cycles inserted and accessing external area)

$V_{CC1} = V_{CC2} = 3V$



$$t_{cyc} = \frac{1}{f(BCLK)}$$

Measuring conditions

- $V_{CC1} = V_{CC2} = 3V$
- Input timing voltage: $V_{IL} = 0.6$ V, $V_{IH} = 2.4$ V
- Output timing voltage: $V_{OL} = 1.5$ V, $V_{OH} = 1.5$ V

n: 3 (when 2 ϕ + 3 ϕ)
4 (when 2 ϕ + 4 ϕ or 3 ϕ + 4 ϕ)
5 (when 4 ϕ + 5 ϕ)

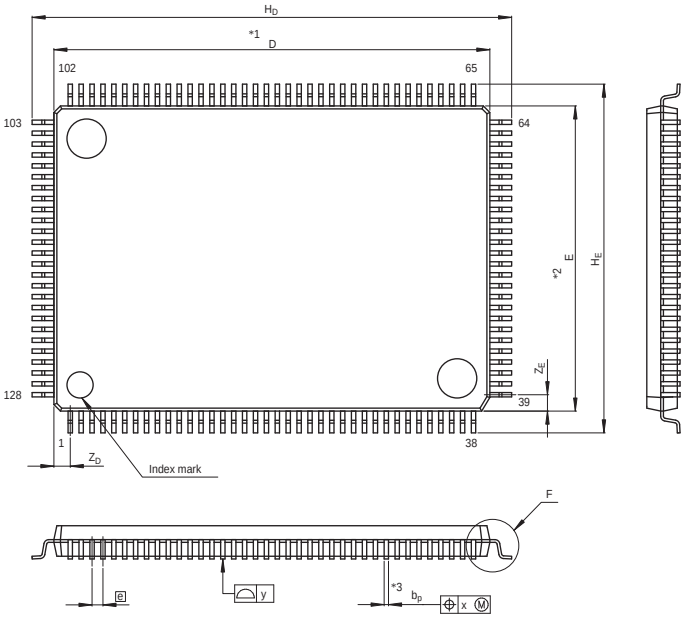
m: 1 (when 1 recovery cycle inserted)
2 (when 2 recovery cycles inserted)
3 (when 3 recovery cycles inserted)

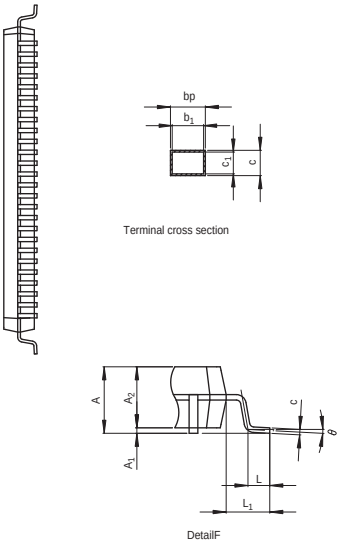
Figure 5.34 Timing Diagram

Appendix 1. Package Dimensions

The information on the latest package dimensions or packaging may be obtained from “Packages“ on the Renesas Electronics website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP128-14x20-0.50	PLQP0128KB-A	128P6Q-A	0.9g

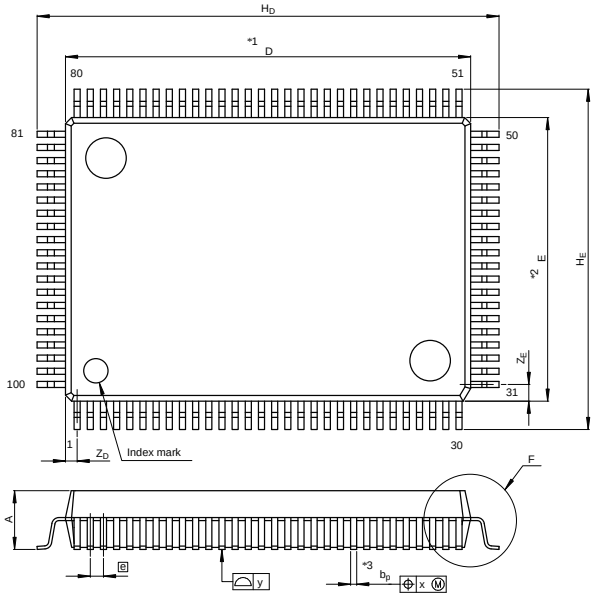


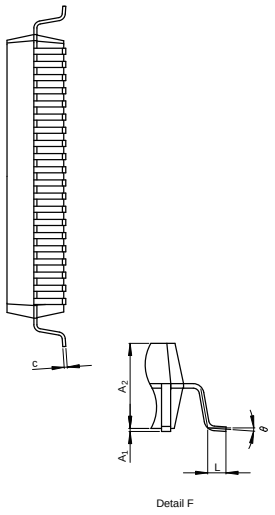


NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.9	20.0	20.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	21.8	22.0	22.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.125	0.2
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.10
y	—	—	0.10
Z_D	—	0.75	—
Z_E	—	0.75	—
L	0.35	0.5	0.65
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-QFP100-14x20-0.65	PRQP0100JD-B	100P6F-A	1.8g





NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.8	20.0	20.2
E	13.8	14.0	14.2
A_2	—	2.8	—
H_D	22.5	22.8	23.1
H_E	16.5	16.8	17.1
A	—	—	3.05
A_1	0	0.1	0.2
b_p	0.25	0.3	0.4
c	0.13	0.15	0.2
θ	0°	—	10°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	0.575	—
Z_E	—	0.825	—
L	0.4	0.6	0.8