# Renesas Electronics America Inc - R5F3651EDFC#U0 Datasheet

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | M16C/60 |
| Core Size | 16-Bit |
| Speed | 32MHz |
| Connectivity | EBI/EMI, I²C, SIO, UART/USART |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 111 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 20K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | A/D 26x10b; D/A 2x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 128-LQFP |
| Supplier Device Package | 128-LFQFP (14x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f3651edfc-u0 |

**Table 1.3 Specifications for the 100-Pin Package (1/2)**

| Item | Function | Description |
|---|---|---|
| CPU | Central processing unit | M16C/60 Series core<br>(multiplier: 16 bit × 16 bit → 32 bit,<br>multiply and accumulate instruction: 16 bit × 16 bit + 32 bit → 32 bit)<br>• Number of basic instructions: 91<br>• Minimum instruction execution time:<br>31.25 ns (f(BCLK) = 32 MHz, VCC1 = VCC2 = 2.7 to 5.5 V)<br>• Operating modes: Single-chip, memory expansion, and microprocessor |
| Memory | ROM, RAM, data flash | See Table 1.5 “Product List (1/2)” and Table 1.6 “Product List (2/2)”. |
| Voltage Detection | Voltage detector | • Power-on reset<br>• 3 voltage detection points (detection level of voltage detection 0 and 1 selectable) |
| Clock | Clock generator | • 5 circuits: Main clock, sub clock, low-speed on-chip oscillator (125 kHz), high-speed on-chip oscillator (40 MHz ±10%), PLL frequency synthesizer<br>• Oscillation stop detection: Main clock oscillation stop/restart detection function<br>• Frequency divider circuit: Divide ratio selectable from 1, 2, 4, 8, and 16<br>• Power saving features: Wait mode, stop mode<br>• Real-time clock |
| External Bus Expansion | Bus memory expansion | • Address space: 1 MB<br>• External bus interface: 0 to 8 waits inserted, 4 chip select outputs, memory area expansion function (expandable to 4 MB), 3 V and 5 V interfaces<br>• Bus format: Separate bus or multiplexed bus selectable, data bus width selectable (8 or 16 bits), number of address buses selectable (12, 16, or 20) |
| I/O Ports | Programmable I/O ports | • CMOS I/O ports: 85 (selectable pull-up resistors)<br>• N-channel open drain ports: 3 |
| Interrupts | | • Interrupt vectors: 70<br>• External interrupt inputs: 13 ($\overline{\text{NMI}}$, $\overline{\text{INT}}$ × 8, key input × 4)<br>• Interrupt priority levels: 7 |
| Watchdog Timer | | 15-bit timer × 1 (with prescaler)<br>Automatic reset start function selectable |
| DMA | DMAC | • 4 channels, cycle steal mode<br>• Trigger sources: 43<br>• Transfer modes: 2 (single transfer, repeat transfer) |

**Table 1.6 Product List (2/2)** As of July 2012

| Part No. | ROM Capacity | | | RAM Capacity | Package Code | Remarks |
|---|---|---|---|---|---|---|
| | Program ROM 1 | Program ROM 2 | Data flash | | | |
| R5F3651TNFC | 768 KB | 16 KB | 4 KB × 2 blocks | 47 KB | PLQP0128KB-A | Operating temperature -20°C to 85°C |
| R5F3650TNFA | | | | | PRQP0100JD-B | |
| R5F3650TNFB | | | | | PLQP0100KB-A | |
| R5F3651TDFC | | | | | PLQP0128KB-A | Operating temperature -40°C to 85°C |
| R5F3650TDFA | | | | | PRQP0100JD-B | |
| R5F3650TDFB | | | | | PLQP0100KB-A | |

(D): Under development
(P): Planning

Previous package codes are as follows:
PLQP0128KB-A: 128P6Q-A
PRQP0100JD-B: 100P6F-A
PLQP0100KB-A: 100P6Q-A

**Table 1.9 Pin Names for the 128-Pin Package (3/3)**

| Pin No. | Control Pin | Port | I/O Pin for Peripheral Function | | | | Bus Control Pin |
|---|---|---|---|---|---|---|---|
| | | | Interrupt | Timer | Serial interface | A/D converter, D/A converter | |
| 101 | | P1_2 | | | RXD6/SCL6 | | D10 |
| 102 | | P1_1 | | | CLK6 | | D9 |
| 103 | | P1_0 | | | $\overline{\text{CTS6/RTS6}}$ | | D8 |
| 104 | | P0_7 | | | | AN0_7 | D7 |
| 105 | | P0_6 | | | | AN0_6 | D6 |
| 106 | | P0_5 | | | | AN0_5 | D5 |
| 107 | | P0_4 | | | | AN0_4 | D4 |
| 108 | | P0_3 | | | | AN0_3 | D3 |
| 109 | | P0_2 | | | | AN0_2 | D2 |
| 110 | | P0_1 | | | | AN0_1 | D1 |
| 111 | | P0_0 | | | | AN0_0 | D0 |
| 112 | | P11_7 | | | | | |
| 113 | | P11_6 | | | | | |
| 114 | | P11_5 | | | | | |
| 115 | | P11_4 | | | | | |
| 116 | | P11_3 | | | | | |
| 117 | | P11_2 | | | | | |
| 118 | | P11_1 | | | | | |
| 119 | | P11_0 | | | | | |
| 120 | | P10_7 | $\overline{\text{KI3}}$ | | | AN7 | |
| 121 | | P10_6 | $\overline{\text{KI2}}$ | | | AN6 | |
| 122 | | P10_5 | $\overline{\text{KI1}}$ | | | AN5 | |
| 123 | | P10_4 | $\overline{\text{KI0}}$ | | | AN4 | |
| 124 | | P10_3 | | | | AN3 | |
| 125 | | P10_2 | | | | AN2 | |
| 126 | | P10_1 | | | | AN1 | |
| 127 | AVSS | | | | | | |
| 128 | | P10_0 | | | | AN0 | |

**Table 1.10 Pin Names for the 100-Pin Package (1/2)**

| Pin No. | | Control Pin | Port | I/O Pin for Peripheral Function | | | | Bus Control Pin |
|---|---|---|---|---|---|---|---|---|
| FA | FB | | | Interrupt | Timer | Serial interface | A/D converter, D/A converter | |
| 1 | 99 | | P9_6 | | | SOUT4 | ANEX1 | |
| 2 | 100 | | P9_5 | | | CLK4 | ANEX0 | |
| 3 | 1 | | P9_4 | | TB4IN/PWM1 | | DA1 | |
| 4 | 2 | | P9_3 | | TB3IN/PWM0 | | DA0 | |
| 5 | 3 | | P9_2 | | TB2IN/PMC0 | SOUT3 | | |
| 6 | 4 | | P9_1 | | TB1IN/PMC1 | SIN3 | | |
| 7 | 5 | | P9_0 | | TB0IN | CLK3 | | |
| 8 | 6 | BYTE | | | | | | |
| 9 | 7 | CNVSS | | | | | | |
| 10 | 8 | XCIN | P8_7 | | | | | |
| 11 | 9 | XCOUT | P8_6 | | | | | |
| 12 | 10 | $\overline{\text{RESET}}$ | | | | | | |
| 13 | 11 | XOUT | | | | | | |
| 14 | 12 | VSS | | | | | | |
| 15 | 13 | XIN | | | | | | |
| 16 | 14 | VCC1 | | | | | | |
| 17 | 15 | | P8_5 | $\overline{\text{NMI}}$ | $\overline{\text{SD}}$ | CEC | | |
| 18 | 16 | | P8_4 | $\overline{\text{INT2}}$ | ZP | | | |
| 19 | 17 | | P8_3 | $\overline{\text{INT1}}$ | | | | |
| 20 | 18 | | P8_2 | $\overline{\text{INT0}}$ | | | | |
| 21 | 19 | | P8_1 | | TA4IN/$\overline{\text{U}}$ | $\overline{\text{CTS5/RTS5}}$ | | |
| 22 | 20 | | P8_0 | | TA4OUT/U | RXD5/SCL5 | | |
| 23 | 21 | | P7_7 | | TA3IN | CLK5 | | |
| 24 | 22 | | P7_6 | | TA3OUT | TXD5/SDA5 | | |
| 25 | 23 | | P7_5 | | TA2IN/$\overline{\text{W}}$ | | | |
| 26 | 24 | | P7_4 | | TA2OUT/W | | | |
| 27 | 25 | | P7_3 | | TA1IN/$\overline{\text{V}}$ | $\overline{\text{CTS2/RTS2}}$ | | |
| 28 | 26 | | P7_2 | | TA1OUT/V | CLK2 | | |
| 29 | 27 | | P7_1 | | TA0IN/TB5IN | RXD2/SCL2/SCLMM | | |
| 30 | 28 | | P7_0 | | TA0OUT | TXD2/SDA2/SDAMM | | |
| 31 | 29 | | P6_7 | | | TXD1/SDA1 | | |
| 32 | 30 | | P6_6 | | | RXD1/SCL1 | | |
| 33 | 31 | | P6_5 | | | CLK1 | | |
| 34 | 32 | | P6_4 | | | $\overline{\text{CTS1}}$/RTS1/$\overline{\text{CTS0}}$/ CLKS1 | | |
| 35 | 33 | | P6_3 | | | TXD0/SDA0 | | |
| 36 | 34 | | P6_2 | | | RXD0/SCL0 | | |
| 37 | 35 | | P6_1 | | | CLK0 | | |
| 38 | 36 | | P6_0 | | RTCOUT | $\overline{\text{CTS0/RTS0}}$ | | |
| 39 | 37 | CLKOUT | P5_7 | | | | | $\overline{\text{RDY}}$ |
| 40 | 38 | | P5_6 | | | | | ALE |
| 41 | 39 | | P5_5 | | | | | $\overline{\text{HOLD}}$ |
| 42 | 40 | | P5_4 | | | | | $\overline{\text{HLDA}}$ |
| 43 | 41 | | P5_3 | | | | | BCLK |
| 44 | 42 | | P5_2 | | | | | $\overline{\text{RD}}$ |
| 45 | 43 | | P5_1 | | | | | $\overline{\text{WRH/BHE}}$ |
| 46 | 44 | | P5_0 | | | | | $\overline{\text{WRL/WR}}$ |
| 47 | 45 | | P4_7 | | PWM1 | TXD7/SDA7 | | $\overline{\text{CS3}}$ |
| 48 | 46 | | P4_6 | | PWM0 | RXD7/SCL7 | | $\overline{\text{CS2}}$ |
| 49 | 47 | | P4_5 | | | CLK7 | | $\overline{\text{CS1}}$ |
| 50 | 48 | | P4_4 | | | $\overline{\text{CTS7/RTS7}}$ | | $\overline{\text{CS0}}$ |

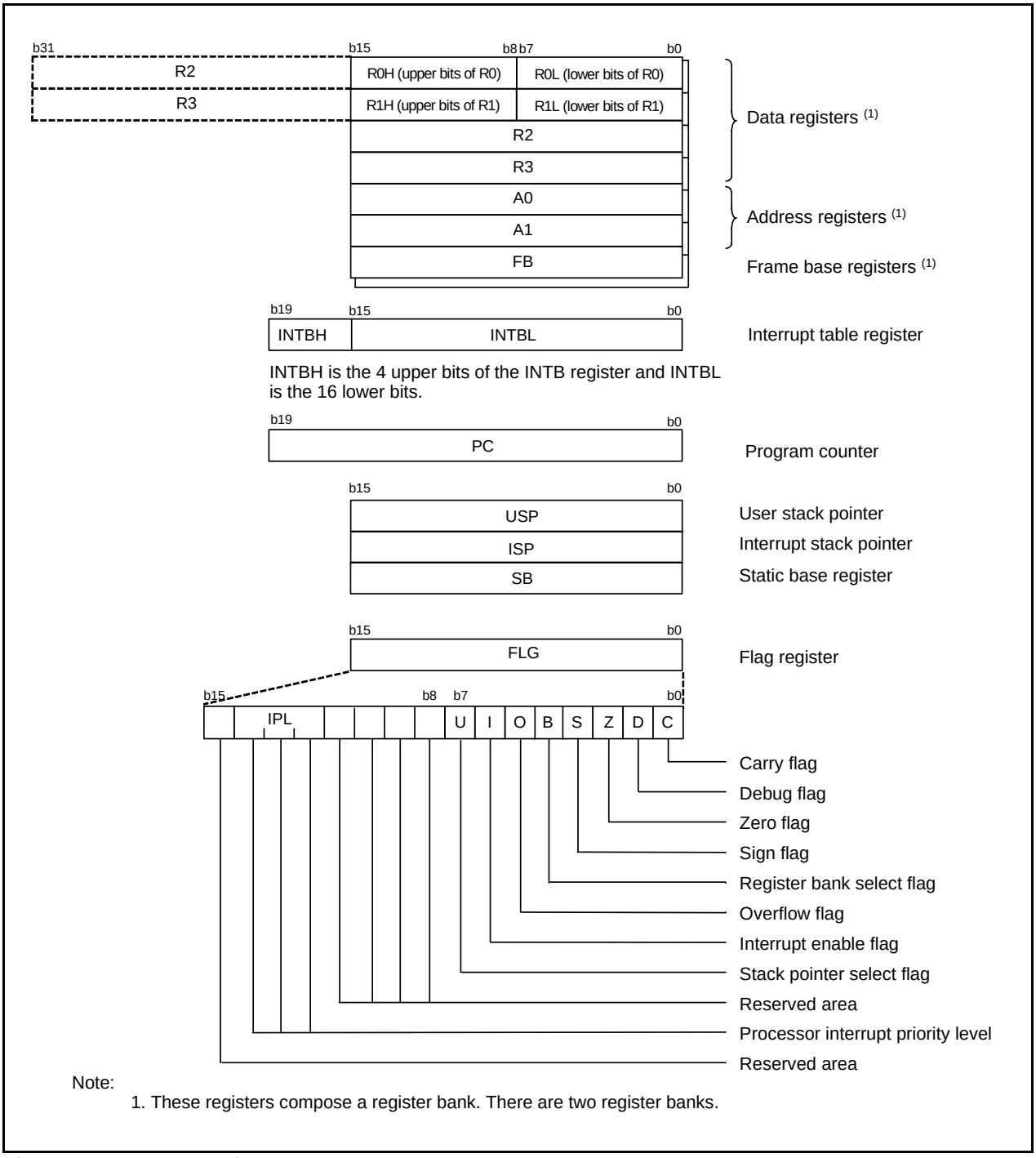
**Table 1.16 Pin Functions for the 100-Pin Package (2/3)**

| Signal Name | Pin Name | I/O | Power Supply | Description |
|---|---|---|---|---|
| Main clock input | XIN | I | VCC1 | I/O for the main clock oscillator. Connect a ceramic resonator or crystal between pins XIN and XOUT. (1) Input an external clock to XIN pin and leave XOUT pin open. |
| Main clock output | XOUT | O | VCC1 | |
| Sub clock input | XCIN | I | VCC1 | I/O for a sub clock oscillator. Connect a crystal between XCIN pin and XCOUT pin. (1) Input an external clock to XCIN pin and leave XCOUT pin open. |
| Sub clock output | XCOUT | O | VCC1 | |
| BCLK output | BCLK | O | VCC2 | Outputs the BCLK signal. |
| Clock output | CLKOUT | O | VCC2 | Outputs a clock with the same frequency as fC, f1, f8, or f32. |
| $\overline{INT}$ interrupt input | $\overline{INT0}$ to $\overline{INT2}$ | I | VCC1 | Input for the $\overline{INT}$ interrupt. |
| | $\overline{INT3}$ to $\overline{INT7}$ | I | VCC2 | |
| $\overline{NMI}$ interrupt input | $\overline{NMI}$ | I | VCC1 | Input for the $\overline{NMI}$ interrupt. |
| Key input interrupt input | $\overline{KI0}$ to $\overline{KI3}$ | I | VCC1 | Input for the key input interrupt. |
| Timer A | TA0OUT to TA4OUT | I/O | VCC1 | I/O for timers A0 to A4 (TA0OUT is N-channel open drain output). |
| | TA0IN to TA4IN | I | VCC1 | Input for timers A0 to A4. |
| | ZP | I | VCC1 | Input for Z-phase. |
| Timer B | TB0IN to TB5IN | I | VCC1 | Input for timers B0 to B5. |
| Three-phase motor control timer | U, $\overline{U}$, V, $\overline{V}$, W, $\overline{W}$ | O | VCC1 | Output for the three-phase motor control timer. |
| | $\overline{SD}$ | I | VCC1 | Forced cutoff input. |
| | IDU, IDV, IDW | I | VCC2 | Input for the position data. |
| Real-time clock output | RTCOUT | O | VCC1 | Output for the real-time clock. |
| PWM output | PWM0, PWM1 | O | VCC1, VCC2 | PWM output. |
| Remote control signal receiver input | PMC0, PMC1 | I | VCC1 | Input for the remote control signal receiver. |
| Serial interface UART0 to UART2, UART5 to UART7 | $\overline{CTS0}$ to $\overline{CTS2}$, $\overline{CTS5}$ | I | VCC1 | Input pins to control data transmission. |
| | $\overline{CTS6}$, $\overline{CTS7}$ | I | VCC2 | |
| | $\overline{RTS0}$ to $\overline{RTS2}$, $\overline{RTS5}$ | O | VCC1 | Output pins to control data reception. |
| | $\overline{RTS6}$, $\overline{RTS7}$ | O | VCC2 | |
| | CLK0 to CLK2, CLK5 | I/O | VCC1 | Transmit/receive clock I/O. |
| | CLK6, CLK7 | I/O | VCC2 | |
| | RXD0 to RXD2, RXD5 | I | VCC1 | Serial data input. |
| | RXD6, RXD7 | I | VCC2 | |
| | TXD0 to TXD2, TXD5 | O | VCC1 | Serial data output. (2) |
| | TXD6, TXD7 | O | VCC2 | |
| | CLKS1 | O | VCC1 | Output for the transmit/receive clock multiple-pin output function. |

Notes:
1. Contact the manufacturer of crystal/ceramic resonator regarding the oscillation characteristics.
2. TXD2, SDA2, and SCL2 are N-channel open drain output pins. TXDi (i = 0, 1, 5 to 7), SDAi, and SCLi can be selected as CMOS output pins or N-channel open drain output pins.

# 2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. Seven registers (R0, R1, R2, R3, A0, A1, and FB) out of 13 compose a register bank, and there are two register banks.




Note:
1. These registers compose a register bank. There are two register banks.

**Figure 2.1 CPU Registers**

### 2.8.7 Interrupt Enable Flag (I Flag)

The I flag enables maskable interrupts.
Maskable interrupts are disabled when the I flag is 0, and enabled when it is 1. The I flag becomes 0 when an interrupt request is accepted.

### 2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is 0. USP is selected when the U flag is 1.
The U flag becomes 0 when a hardware interrupt request is accepted, or the INT instruction of software interrupt number 0 to 31 is executed.

### 2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from 0 to 7.
If a requested interrupt has higher priority than IPL, the interrupt request is enabled.

### 2.8.10 Reserved Areas

Only set these bits to 0. The read value is undefined.

**Table 4.7 SFR Information (7)** (1)

| Address | Register | Symbol | Reset Value |
|---|---|---|---|
| 01E0h | Timer B3-1 Register | TB31 | XXh |
| 01E1h | | | XXh |
| 01E2h | Timer B4-1 Register | TB41 | XXh |
| 01E3h | | | XXh |
| 01E4h | Timer B5-1 Register | TB51 | XXh |
| 01E5h | | | XXh |
| 01E6h | Pulse Period/Pulse Width Measurement Mode Function Select Register 2 | PPWFS2 | XXXX X000b |
| 01E7h | | | |
| 01E8h | Timer B Count Source Select Register 2 | TBCS2 | 00h |
| 01E9h | Timer B Count Source Select Register 3 | TBCS3 | X0h |
| 01EAh | | | |
| 01EBh | | | |
| 01ECh | | | |
| 01EDh | | | |
| 01EEh | | | |
| 01EFh | | | |
| 01F0h | PMC0 Function Select Register 0 | PMC0CON0 | 00h |
| 01F1h | PMC0 Function Select Register 1 | PMC0CON1 | 00XX 0000b |
| 01F2h | PMC0 Function Select Register 2 | PMC0CON2 | 0000 00X0b |
| 01F3h | PMC0 Function Select Register 3 | PMC0CON3 | 00h |
| 01F4h | PMC0 Status Register | PMC0STS | 00h |
| 01F5h | PMC0 Interrupt Source Select Register | PMC0INT | 00h |
| 01F6h | PMC0 Compare Control Register | PMC0CPC | XXX0 X000b |
| 01F7h | PMC0 Compare Data Register | PMC0CPD | 00h |
| 01F8h | PMC1 Function Select Register 0 | PMC1CON0 | XXX0 X000b |
| 01F9h | PMC1 Function Select Register 1 | PMC1CON1 | XXXX 0X00b |
| 01FAh | PMC1 Function Select Register 2 | PMC1CON2 | 0000 00X0b |
| 01FBh | PMC1 Function Select Register 3 | PMC1CON3 | 00h |
| 01FCh | PMC1 Status Register | PMC1STS | X000 X00Xb |
| 01FDh | PMC1 Interrupt Source Select Register | PMC1INT | X000 X00Xb |
| 01FEh | | | |
| 01FFh | | | |
| 0200h | | | |
| 0201h | | | |
| 0202h | | | |
| 0203h | | | |
| 0204h | | | |
| 0205h | Interrupt Source Select Register 3 | IFSR3A | 00h |
| 0206h | Interrupt Source Select Register 2 | IFSR2A | 00h |
| 0207h | Interrupt Source Select Register | IFSR | 00h |
| 0208h | | | |
| 0209h | | | |
| 020Ah | | | |
| 020Bh | | | |
| 020Ch | | | |
| 020Dh | | | |
| 020Eh | Address Match Interrupt Enable Register | AIER | XXXX XX00b |
| 020Fh | Address Match Interrupt Enable Register 2 | AIER2 | XXXX XX00b |

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

**Table 4.8 SFR Information (8)** (1)

| Address | Register | Symbol | Reset Value |
|---|---|---|---|
| 0210h | Address Match Interrupt Register 0 | RMAD0 | 00h |
| 0211h | | | 00h |
| 0212h | | | X0h |
| 0213h | | | |
| 0214h | Address Match Interrupt Register 1 | RMAD1 | 00h |
| 0215h | | | 00h |
| 0216h | | | X0h |
| 0217h | | | |
| 0218h | Address Match Interrupt Register 2 | RMAD2 | 00h |
| 0219h | | | 00h |
| 021Ah | | | X0h |
| 021Bh | | | |
| 021Ch | Address Match Interrupt Register 3 | RMAD3 | 00h |
| 021Dh | | | 00h |
| 021Eh | | | X0h |
| 021Fh | | | |
| 0220h | Flash Memory Control Register 0 | FMR0 | 0000 0001b (Other than user boot mode)<br>0010 0001b (User boot mode) |
| 0221h | Flash Memory Control Register 1 | FMR1 | 00X0 XX0Xb |
| 0222h | Flash Memory Control Register 2 | FMR2 | XXXX 0000b |
| 0223h | | | |
| 0224h | | | |
| 0225h | | | |
| 0226h | | | |
| 0227h | | | |
| 0228h | | | |
| 0229h | | | |
| 022Ah | | | |
| 022Bh | | | |
| 022Ch | | | |
| 022Dh | | | |
| 022Eh | | | |
| 022Fh | | | |
| 0230h | Flash Memory Control Register 6 | FMR6 | XX0X XX00b |
| 0231h | | | |
| 0232h | | | |
| 0233h | | | |
| 0234h | | | |
| 0235h | | | |
| 0236h | | | |
| 0237h | | | |
| 0238h | | | |
| 0239h | | | |
| 023Ah | | | |
| 023Bh | | | |
| 023Ch | | | |
| 023Dh | | | |
| 023Eh | | | |
| 023Fh | | | |

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

**Table 4.9 SFR Information (9)** (1)

| Address | Register | Symbol | Reset Value |
|---|---|---|---|
| 0240h | | | |
| 0241h | | | |
| 0242h | | | |
| 0243h | | | |
| 0244h | UART0 Special Mode Register 4 | U0SMR4 | 00h |
| 0245h | UART0 Special Mode Register 3 | U0SMR3 | 000X 0X0Xb |
| 0246h | UART0 Special Mode Register 2 | U0SMR2 | X000 0000b |
| 0247h | UART0 Special Mode Register | U0SMR | X000 0000b |
| 0248h | UART0 Transmit/Receive Mode Register | U0MR | 00h |
| 0249h | UART0 Bit Rate Register | U0BRG | XXh |
| 024Ah | UART0 Transmit Buffer Register | U0TB | XXh |
| 024Bh | | | XXh |
| 024Ch | UART0 Transmit/Receive Control Register 0 | U0C0 | 0000 1000b |
| 024Dh | UART0 Transmit/Receive Control Register 1 | U0C1 | 00XX 0010b |
| 024Eh | UART0 Receive Buffer Register | U0RB | XXh |
| 024Fh | | | XXh |
| 0250h | UART Transmit/Receive Control Register 2 | UCON | X000 0000b |
| 0251h | | | |
| 0252h | UART Clock Select Register | UCLKSEL0 | X0h |
| 0253h | | | |
| 0254h | UART1 Special Mode Register 4 | U1SMR4 | 00h |
| 0255h | UART1 Special Mode Register 3 | U1SMR3 | 000X 0X0Xb |
| 0256h | UART1 Special Mode Register 2 | U1SMR2 | X000 0000b |
| 0257h | UART1 Special Mode Register | U1SMR | X000 0000b |
| 0258h | UART1 Transmit/Receive Mode Register | U1MR | 00h |
| 0259h | UART1 Bit Rate Register | U1BRG | XXh |
| 025Ah | UART1 Transmit Buffer Register | U1TB | XXh |
| 025Bh | | | XXh |
| 025Ch | UART1 Transmit/Receive Control Register 0 | U1C0 | 0000 1000b |
| 025Dh | UART1 Transmit/Receive Control Register 1 | U1C1 | 00XX 0010b |
| 025Eh | UART1 Receive Buffer Register | U1RB | XXh |
| 025Fh | | | XXh |
| 0260h | | | |
| 0261h | | | |
| 0262h | | | |
| 0263h | | | |
| 0264h | UART2 Special Mode Register 4 | U2SMR4 | 00h |
| 0265h | UART2 Special Mode Register 3 | U2SMR3 | 000X 0X0Xb |
| 0266h | UART2 Special Mode Register 2 | U2SMR2 | X000 0000b |
| 0267h | UART2 Special Mode Register | U2SMR | X000 0000b |
| 0268h | UART2 Transmit/Receive Mode Register | U2MR | 00h |
| 0269h | UART2 Bit Rate Register | U2BRG | XXh |
| 026Ah | UART2 Transmit Buffer Register | U2TB | XXh |
| 026Bh | | | XXh |
| 026Ch | UART2 Transmit/Receive Control Register 0 | U2C0 | 0000 1000b |
| 026Dh | UART2 Transmit/Receive Control Register 1 | U2C1 | 0000 0010b |
| 026Eh | UART2 Receive Buffer Register | U2RB | XXh |
| 026Fh | | | XXh |

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

**Table 4.11 SFR Information (11)** (1)

| Address | Register | Symbol | Reset Value |
|---|---|---|---|
| 02A0h | | | |
| 02A1h | | | |
| 02A2h | | | |
| 02A3h | | | |
| 02A4h | UART7 Special Mode Register 4 | U7SMR4 | 00h |
| 02A5h | UART7 Special Mode Register 3 | U7SMR3 | 000X 0X0Xb |
| 02A6h | UART7 Special Mode Register 2 | U7SMR2 | X000 0000b |
| 02A7h | UART7 Special Mode Register | U7SMR | X000 0000b |
| 02A8h | UART7 Transmit/Receive Mode Register | U7MR | 00h |
| 02A9h | UART7 Bit Rate Register | U7BRG | XXh |
| 02AAh | UART7 Transmit Buffer Register | U7TB | XXh |
| 02ABh | | | XXh |
| 02ACh | UART7 Transmit/Receive Control Register 0 | U7C0 | 0000 1000b |
| 02ADh | UART7 Transmit/Receive Control Register 1 | U7C1 | 0000 0010b |
| 02AEh | UART7 Receive Buffer Register | U7RB | XXh |
| 02AFh | | | XXh |
| 02B0h | I2C0 Data Shift Register | S00 | XXh |
| 02B1h | | | |
| 02B2h | I2C0 Address Register 0 | S0D0 | 0000 000Xb |
| 02B3h | I2C0 Control Register 0 | S1D0 | 00h |
| 02B4h | I2C0 Clock Control Register | S20 | 00h |
| 02B5h | I2C0 Start/Stop Condition Control Register | S2D0 | 0001 1010b |
| 02B6h | I2C0 Control Register 1 | S3D0 | 0011 0000b |
| 02B7h | I2C0 Control Register 2 | S4D0 | 00h |
| 02B8h | I2C0 Status Register 0 | S10 | 0001 000Xb |
| 02B9h | I2C0 Status Register 1 | S11 | XXXX X000b |
| 02BAh | I2C0 Address Register 1 | S0D1 | 0000 000Xb |
| 02BBh | I2C0 Address Register 2 | S0D2 | 0000 000Xb |
| 02BCh | | | |
| 02BDh | | | |
| 02BEh | | | |
| 02BFh | | | |
| 02C0h to 02FFh | | | |

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

## 4.2 Notes on SFRs

### 4.2.1 Register Settings

Table 4.19 lists Registers with Write-Only Bits and registers whose function differs between reading and writing. Set these registers with immediate values. Do not use read-modify-write instructions. When establishing the next value by altering the existing value, write the existing value to the RAM as well as to the register. Transfer the next value to the register after making changes in the RAM.
Read-modify-write instructions can be used when writing to the no register bits.

**Table 4.19 Registers with Write-Only Bits**

| Address | Register | Symbol |
|---|---|---|
| 0249h | UART0 Bit Rate Register | U0BRG |
| 024Bh to 024Ah | UART0 Transmit Buffer Register | U0TB |
| 0259h | UART1 Bit Rate Register | U1BRG |
| 025Bh to 025Ah | UART1 Transmit Buffer Register | U1TB |
| 0269h | UART2 Bit Rate Register | U2BRG |
| 026Bh to 026Ah | UART2 Transmit Buffer Register | U2TB |
| 0273h | SI/O3 Bit Rate Register | S3BRG |
| 0277h | SI/O4 Bit Rate Register | S4BRG |
| 0289h | UART5 Bit Rate Register | U5BRG |
| 028Bh to 028Ah | UART5 Transmit Buffer Register | U5TB |
| 0299h | UART6 Bit Rate Register | U6BRG |
| 029Bh to 029Ah | UART6 Transmit Buffer Register | U6TB |
| 02A9h | UART7 Bit Rate Register | U7BRG |
| 02ABh to 02AAh | UART7 Transmit Buffer Register | U7TB |
| 02B6h | I2C0 Control Register 1 | S3D0 |
| 02B8h | I2C0 Status Register 0 | S10 |
| 0303h to 0302h | Timer A1-1 Register | TA11 |
| 0305h to 0304h | Timer A2-1 Register | TA21 |
| 0307h to 0306h | Timer A4-1 Register | TA41 |
| 030Ah | Three-Phase Output Buffer Register 0 | IDB0 |
| 030Bh | Three-Phase Output Buffer Register 1 | IDB1 |
| 030Ch | Dead Time Timer | DTT |
| 030Dh | Timer B2 Interrupt Generation Frequency Set Counter | ICTB2 |
| 0327h to 0326h | Timer A0 Register | TA0 |
| 0329h to 0328h | Timer A1 Register | TA1 |
| 032Bh to 032Ah | Timer A2 Register | TA2 |
| 032Dh to 032Ch | Timer A3 Register | TA3 |
| 032Fh to 032Eh | Timer A4 Register | TA4 |
| 037Dh | Watchdog Timer Refresh Register | WDTR |
| 037Eh | Watchdog Timer Start Register | WDTS |

# 5. Electrical Characteristics

## 5.1 Electrical Characteristics (Common to 3 V and 5 V)

### 5.1.1 Absolute Maximum Rating

**Table 5.1 Absolute Maximum Ratings**

| Symbol | Parameter | | Condition | Rated Value | Unit |
|---|---|---|---|---|---|
| $V_{CC1}$ | Supply voltage | | $V_{CC1} = AV_{CC}$ | –0.3 to 6.5 | V |
| $V_{CC2}$ | Supply voltage | | $V_{CC1} = AV_{CC}$ | –0.3 to $V_{CC1}$ + 0.1 (1) | V |
| $AV_{CC}$ | Analog supply voltage | | $V_{CC1} = AV_{CC}$ | –0.3 to 6.5 | V |
| $V_{REF}$ | Analog reference voltage | | $V_{CC1} = AV_{CC}$ | –0.3 to $V_{CC1}$ + 0.1 (1) | V |
| $V_I$ | Input voltage | $\overline{RESET}$, CNVSS, BYTE,<br>P6_0 to P6_7, P7_2 to P7_7,<br>P8_0 to P8_4, P8_6, P8_7,<br>P9_0 to P9_7, P10_0 to P10_7,<br>P11_0 to P11_7, P14_0, P14_1<br>XIN | | –0.3 to $V_{CC1}$ + 0.3 (1) | V |
| | | P0_0 to P0_7, P1_0 to P1_7,<br>P2_0 to P2_7, P3_0 to P3_7,<br>P4_0 to P4_7, P5_0 to P5_7,<br>P12_0 to P12_7, P13_0 to P13_7 | | –0.3 to $V_{CC2}$ + 0.3 (1) | V |
| | | P7_0, P7_1, P8_5 | | –0.3 to 6.5 | V |
| $V_O$ | Output voltage | P6_0 to P6_7, P7_2 to P7_7,<br>P8_0 to P8_4, P8_6, P8_7,<br>P9_0 to P9_7, P10_0 to P10_7,<br>P11_0 to P11_7, P14_0, P14_1<br>XOUT | | –0.3 to $V_{CC1}$ + 0.3 (1) | V |
| | | P0_0 to P0_7, P1_0 to P1_7,<br>P2_0 to P2_7, P3_0 to P3_7,<br>P4_0 to P4_7, P5_0 to P5_7,<br>P12_0 to P12_7, P13_0 to P13_7 | | –0.3 to $V_{CC2}$ + 0.3 (1) | V |
| | | P7_0, P7_1, P8_5 | | –0.3 to 6.5 | V |
| $P_d$ | Power consumption | | $-40°C < T_{opr} \leq 85°C$ | 300 | mW |
| $T_{opr}$ | Operating temperature | When the MCU is operating | | –20 to 85/–40 to 85 | °C |
| | | Flash program erase | Program area | 0 to 60 | |
| | | | Data area | –20 to 85/–40 to 85 | |
| $T_{stg}$ | Storage temperature | | | –65 to 150 | °C |

Note:
1. Maximum value is 6.5 V.

## 5.1.2 Recommended Operating Conditions

**Table 5.2 Recommended Operating Conditions (1/3)**

$V_{CC1}$ = $V_{CC2}$ = 2.7 to 5.5 V at $T_{opr}$ = -20°C to 85°C/-40°C to 85°C unless otherwise specified.

| Symbol | Parameter | | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{CC1}$, $V_{CC2}$ | Supply voltage ($V_{CC1} \geq V_{CC2}$) | CEC function is not used | 2.7 | 5.0 | 5.5 | V |
| | | CEC function is used | 2.7 | | 3.63 | V |
| $AV_{CC}$ | Analog supply voltage | | | $V_{CC1}$ | | V |
| $V_{SS}$ | Supply voltage | | | 0 | | V |
| $AV_{SS}$ | Analog supply voltage | | | 0 | | V |
| $V_{IH}$ | High input voltage | P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7 | $0.8V_{CC2}$ | | $V_{CC2}$ | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (in single-chip mode) | $0.8V_{CC2}$ | | $V_{CC2}$ | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (data input in memory expansion and microprocessor modes) | $0.5V_{CC2}$ | | $V_{CC2}$ | V |
| | | P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1 XIN, $\overline{\text{RESET}}$, CNVSS, BYTE | $0.8V_{CC1}$ | | $V_{CC1}$ | V |
| | | P7_0, P7_1, P8_5 | $0.8V_{CC1}$ | | 6.5 | V |
| | | CEC | $0.7V_{CC1}$ | | | V |
| $V_{IL}$ | Low input voltage | P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7 | 0 | | $0.2V_{CC2}$ | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (in single-chip mode) | 0 | | $0.2V_{CC2}$ | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (data input in memory expansion and microprocessor mode) | 0 | | $0.16V_{CC2}$ | V |
| | | P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7,P11_0 to P11_7, P14_0, P14_1 XIN, $\overline{\text{RESET}}$, CNVSS, BYTE | 0 | | $0.2V_{CC1}$ | V |
| | | CEC | | | $0.26V_{CC1}$ | V |
| $I_{OH(sum)}$ | High peak output current | Sum of $I_{OH(peak)}$ at P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7 | | | -40.0 | mA |
| | | Sum of $I_{OH(peak)}$ at P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, and P13_0 to P13_7 | | | -40.0 | mA |
| | | Sum of $I_{OH(peak)}$ at P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4 | | | -40.0 | mA |
| | | Sum of $I_{OH(peak)}$ at P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0 to P14_1 | | | -40.0 | mA |
| $I_{OH(peak)}$ | High peak output current | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1 | | | –10.0 | mA |
| $I_{OH(avg)}$ | High average output current (1) | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1 | | | –5.0 | mA |

Note:
1. The average output current is the mean value within 100 ms.

### 5.1.6 Voltage Detector and Power Supply Circuit Electrical Characteristics

**Table 5.11 Voltage Detector 0 Electrical Characteristics**

The measurement condition is $V_{CC1}$ = 2.7 to 5.5 V, $T_{opr}$ = -20°C to 85°C/-40°C to 85°C, unless otherwise specified.

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{det0}$ | Voltage detection level Vdet0_0 (1) | When $V_{CC1}$ is falling. | 1.60 | 1.90 | 2.20 | V |
| | Voltage detection level Vdet0_2 (1) | When $V_{CC1}$ is falling. | 2.55 | 2.85 | 3.15 | V |
| - | Voltage detector 0 response time (3) | When $V_{CC1}$ falls from 5 V to (Vdet0_0 - 0.1) V | | | 200 | µs |
| - | Voltage detector self power consumption | VC25 = 1, $V_{CC1}$ = 5.0 V | | 1.8 | | µA |
| $t_{d(E-A)}$ | Waiting time until voltage detector operation starts (2) | | | | 100 | µs |

Notes:
1. Select the voltage detection level with the VDSEL1 bit in the OFS1 address.
2. Necessary time until the voltage detector operates when setting to 1 again after setting the VC25 bit in the VCR2 register to 0.
3. Time from when passing the $V_{det0}$ until when a voltage monitor 0 reset is generated.

**Table 5.12 Voltage Detector 1 Electrical Characteristics**

The measurement condition is $V_{CC1}$ = 2.7 to 5.5 V, $T_{opr}$ = -20°C to 85°C/-40°C to 85°C, unless otherwise specified.

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{det1}$ | Voltage detection level Vdet1_6 (1) | When $V_{CC1}$ is falling. | 2.79 | 3.09 | 3.39 | V |
| | Voltage detection level Vdet1_B (1) | When $V_{CC1}$ is falling. | 3.54 | 3.84 | 4.14 | V |
| | Voltage detection level Vdet1_F (1) | When $V_{CC1}$ is falling. | 3.94 | 4.44 | 4.94 | V |
| - | Hysteresis width when $V_{CC1}$ of voltage detector 1 is rising | | | 0.15 | | V |
| - | Voltage detector 1 response time (3) | When $V_{CC1}$ falls from 5 V to (Vdet1_0 - 0.1) V | | | 200 | µs |
| - | Voltage detector self power consumption | VC26 = 1, $V_{CC1}$ = 5.0 V | | 1.8 | | µA |
| $t_{d(E-A)}$ | Waiting time until voltage detector operation starts (2) | | | | 100 | µs |

Notes:
1. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
2. Necessary time until the voltage detector operates when setting to 1 again after setting the VC26 bit in the VCR2 register to 0.
3. Time from when passing the $V_{det1}$ until when a voltage monitor 1 reset is generated.

$V_{CC1} = V_{CC2} = 5\ V$

## 5.2.2 Timing Requirements (Peripheral Functions and Others)

($V_{CC1} = V_{CC2} = 5$ V, $V_{SS} = 0$ V, at $T_{opr} = -20°C$ to 85°C/-40°C to 85°C unless otherwise specified)

### 5.2.2.1 Reset Input ($\overline{\text{RESET}}$ Input)

**Table 5.24 Reset Input ($\overline{\text{RESET}}$ Input)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{w(RSTL)}$ | $\overline{\text{RESET}}$ input low pulse width | 10 | | µs |

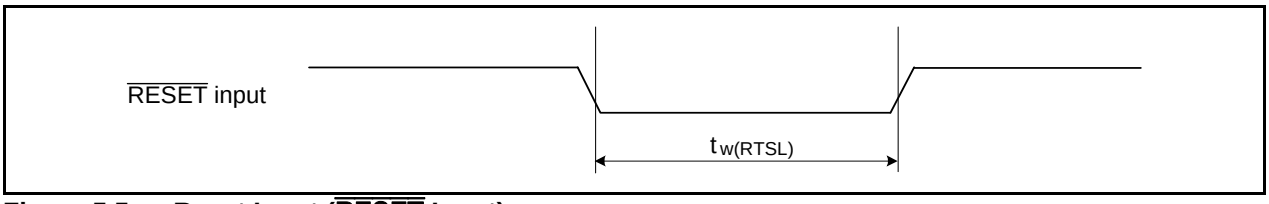



**Figure 5.5 Reset Input ($\overline{\text{RESET}}$ Input)**

### 5.2.2.2 External Clock Input

**Table 5.25 External Clock Input (XIN Input) (1)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_c$ | External clock input cycle time | 50 | | ns |
| $t_{w(H)}$ | External clock input high pulse width | 20 | | ns |
| $t_{w(L)}$ | External clock input low pulse width | 20 | | ns |
| $t_r$ | External clock rise time | | 9 | ns |
| $t_f$ | External clock fall time | | 9 | ns |

Note:
1. The condition is $V_{CC1} = V_{CC2} = 3.0$ to 5.0 V.

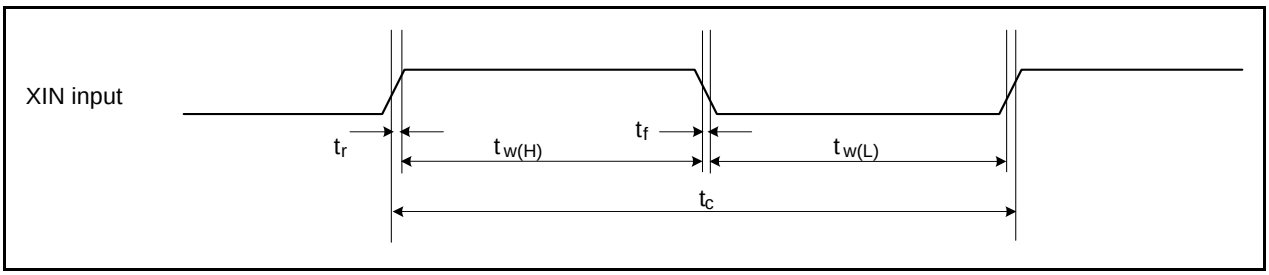
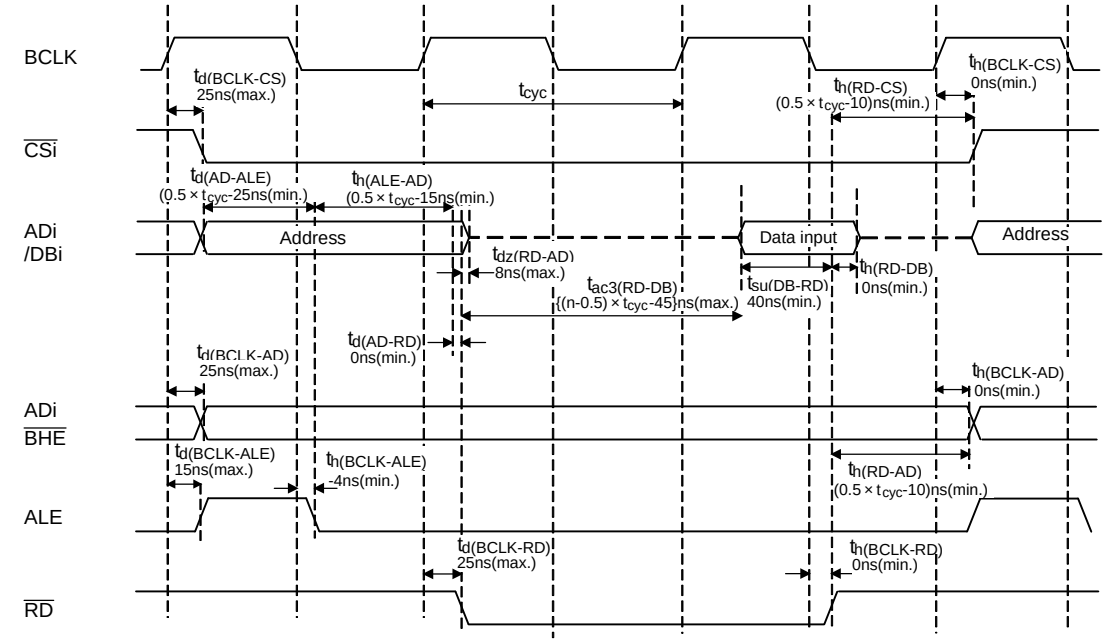



**Figure 5.6 External Clock Input (XIN Input)**

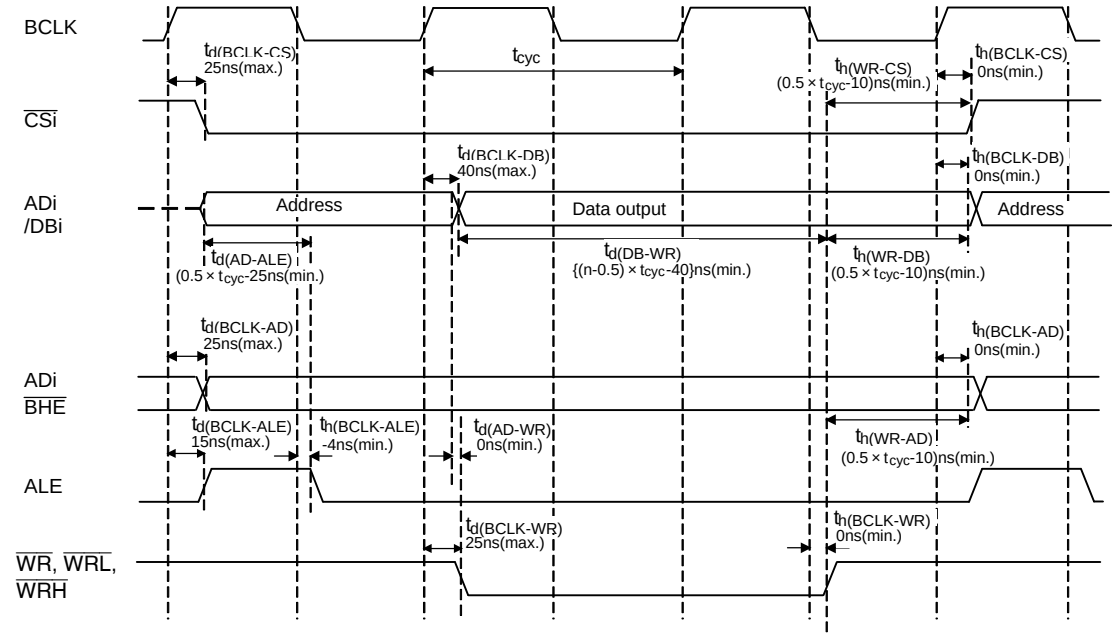
Memory Expansion Mode and Microprocessor Mode
(in 2 or 3 waits setting, and when accessing external area and using multiplexed bus)

$V_{CC1} = V_{CC2} = 5V$

Read timing




Write timing




n: 2 (when 2 waits)
3 (when 3 waits)

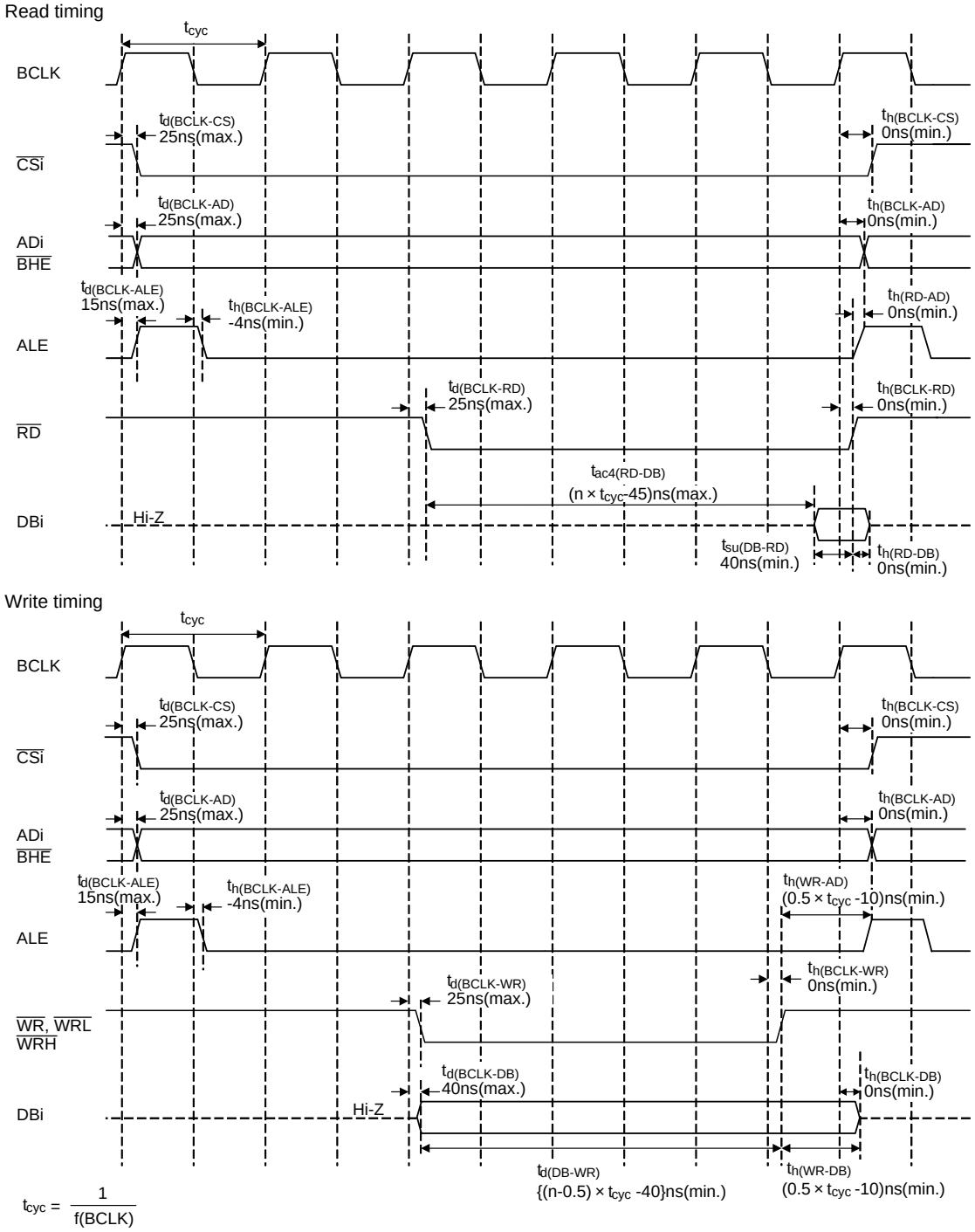
Measuring conditions

- $V_{CC1} = V_{CC2} = 5V$
- Input timing voltage: $V_{IL} = 0.8$ V, $V_{IH} = 2.0$ V
- Output timing voltage: $V_{OL} = 0.4$ V, $V_{OH} = 2.4$ V

**Figure 5.17 Timing Diagram**

Memory Expansion Mode and Microprocessor Mode
(in wait state setting 2 ϕ + 3 ϕ, 2 ϕ + 4 ϕ, 3ϕ + 4 ϕ, and 4 ϕ + 5 ϕ, and when accessing external area)

$V_{CC1} = V_{CC2} = 5V$




$t_{cyc} = \frac{1}{f(BCLK)}$

Measuring conditions

- $V_{CC1} = V_{CC2} = 5V$
- Input timing voltage: $V_{IL}$ = 0.8 V, $V_{IH}$ = 2.0 V
- Output timing voltage: $V_{OL}$ = 0.4 V, $V_{OH}$ = 2.4 V

n: 3 (when 2 ϕ + 3 ϕ)
4 (when 2 ϕ + 4 ϕ or 3 ϕ + 4 ϕ)
5 (when 4 ϕ + 5 ϕ)

**Figure 5.18 Timing Diagram**

$V_{CC1} = V_{CC2} = 3\ V$

**Timing Requirements**

($V_{CC1} = V_{CC2} = 3$ V, $V_{SS} = 0$ V, at $T_{opr}$ = -20°C to 85°C/-40°C to 85°C unless otherwise specified)

### 5.3.3 Timing Requirements (Memory Expansion Mode and Microprocessor Mode)

**Table 5.60 Memory Expansion Mode and Microprocessor Mode**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{ac1(RD-DB)}$ | Data input access time (for setting with no wait) | | (Note 1) | ns |
| $t_{ac2(RD-DB)}$ | Data input access time (for setting with wait) | | (Note 2) | ns |
| $t_{ac3(RD-DB)}$ | Data input access time (when accessing multiplex bus area) | | (Note 3) | ns |
| $t_{ac4(RD-DB)}$ | Data input access time (for setting with 2 ϕ + 3 ϕ or more) | | (Note 4) | ns |
| $t_{su(DB-RD)}$ | Data input setup time | 50 | | ns |
| $t_{su(RDY-BCLK)}$ | $\overline{RDY}$ input setup time | 85 | | ns |
| $t_{h(RD-DB)}$ | Data input hold time | 0 | | ns |
| $t_{h(BCLK-RDY)}$ | $\overline{RDY}$ input hold time | 0 | | ns |

Notes:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f_{(BCLK)}} - 60[ns]$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n + 0.5) \times 10^9}{f_{(BCLK)}} - 60[ns]$$ n is 1 for 1 wait setting, 2 for 2 waits setting and 3 for 3 waits setting.

3. Calculated according to the BCLK frequency as follows:

$$\frac{(n - 0.5) \times 10^9}{f_{(BCLK)}} - 60[ns]$$ n is 2 for 2 waits setting, 3 for 3 waits setting.

4. Calculated according to the BCLK frequency as follows:

$$\frac{n \times 10^9}{f_{(BCLK)}} - 60[ns]$$ n is 3 for 2 ϕ + 3 ϕ, 4 for 2 ϕ + 4 ϕ, 4 for 3 ϕ + 4 ϕ, 5 for 4 ϕ + 5 ϕ,.

$V_{CC1} = V_{CC2} = 3\ V$

**Switching Characteristics**

($V_{CC1} = V_{CC2} = 3$ V, $V_{SS} = 0$ V, at $T_{opr} = -20°C$ to 85°C/-40°C to 85°C unless otherwise specified)

### 5.3.4.4 In Wait State Setting 2φ + 3φ, 2φ + 4φ, 3φ + 4φ, and 4φ + 5φ, and When Accessing External Area

**Table 5.64 Memory Expansion and Microprocessor Modes (in Wait State Setting 2φ + 3φ, 2φ + 4φ, 3φ + 4φ, and 4φ + 5φ, and When Accessing External Area)**

| Symbol | Parameter | Measuring Condition | Standard | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| $t_{d(BCLK-AD)}$ | Address output delay time | See Figure 5.29 | | 30 | ns |
| $t_{h(BCLK-AD)}$ | Address output hold time (in relation to BCLK) | | 0 | | ns |
| $t_{h(RD-AD)}$ | Address output hold time (in relation to RD) | | 0 | | ns |
| $t_{h(WR-AD)}$ | Address output hold time (in relation to WR) | | (Note 2) | | ns |
| $t_{d(BCLK-CS)}$ | Chip select output delay time | | | 30 | ns |
| $t_{h(BCLK-CS)}$ | Chip select output hold time (in relation to BCLK) | | 0 | | ns |
| $t_{d(BCLK-ALE)}$ | ALE signal output delay time | | | 25 | ns |
| $t_{h(BCLK-ALE)}$ | ALE signal output hold time | | -4 | | ns |
| $t_{d(BCLK-RD)}$ | RD signal output delay time | | | 30 | ns |
| $t_{h(BCLK-RD)}$ | RD signal output hold time | | 0 | | ns |
| $t_{d(BCLK-WR)}$ | WR signal output delay time | | | 30 | ns |
| $t_{h(BCLK-WR)}$ | WR signal output hold time | | 0 | | ns |
| $t_{d(BCLK-DB)}$ | Data output delay time (in relation to BCLK) | | | 40 | ns |
| $t_{h(BCLK-DB)}$ | Data output hold time (in relation to BCLK) (3) | | 0 | | ns |
| $t_{d(DB-WR)}$ | Data output delay time (in relation to WR) | | (Note 1) | | ns |
| $t_{h(WR-DB)}$ | Data output hold time (in relation to WR) (3) | | (Note 2) | | ns |

Notes:

1. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5)\times 10^9}{f_{(BCLK)}} - 40[ns]$$

n is 3 for 2φ + 3φ, 4 for 2φ + 4φ, 4 for 3φ + 4φ, and 5 for 4φ + 5φ.

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5\times 10^9}{f_{(BCLK)}} - 10[ns]$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
Hold time of data bus is expressed in
$t = -CR \times \ln(1 - V_{OL}/V_{CC2})$
by a circuit of the right figure.
For example, when $V_{OL} = 0.2V_{CC2}$, C = 30 pF, R = 1 kΩ, hold time of output low level is
$t = -30\ pF \times 1\ k\Omega \times \ln(1 - 0.2V_{CC2}/V_{CC2})$
= 6.7 ns.