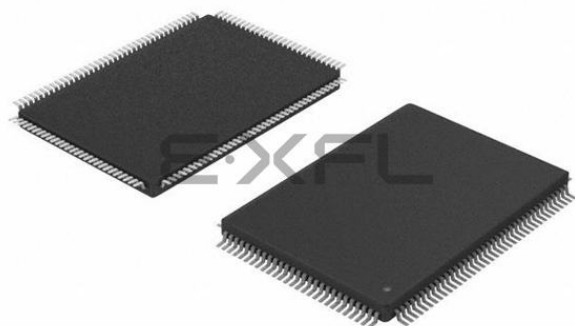




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Details

Product Status	Not For New Designs
Core Processor	M16C/60
Core Size	16-Bit
Speed	32MHz
Connectivity	EBI/EMI, I ² C, SIO, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	111
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	47K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	128-LFQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f3651tdfc-u0

Table 1.7 Pin Names for the 128-Pin Package (1/3)

Pin No.	Control Pin	Port	I/O Pin for Peripheral Function				Bus Control Pin
			Interrupt	Timer	Serial interface	A/D converter, D/A converter	
1	VREF						
2	AVCC						
3		P9_7			SIN4	ADTRG	
4		P9_6			SOUT4	ANEX1	
5		P9_5			CLK4	ANEX0	
6		P9_4		TB4IN/PWM1		DA1	
7		P9_3		TB3IN/PWM0		DA0	
8		P9_2		TB2IN/PMC0	SOUT3		
9		P9_1		TB1IN/PMC1	SIN3		
10		P9_0		TB0IN	CLK3		
11		P14_1					
12		P14_0					
13	BYTE						
14	CNVSS						
15	XCIN	P8_7					
16	XCOUT	P8_6					
17	RESET						
18	XOUT						
19	VSS						
20	XIN						
21	VCC1						
22		P8_5	NMI	SD	CEC		
23		P8_4	INT2	ZP			
24		P8_3	INT1				
25		P8_2	INT0				
26		P8_1		TA4IN/U	CTS5/RTS5		
27		P8_0		TA4OUT/U	RXD5/SCL5		
28		P7_7		TA3IN	CLK5		
29		P7_6		TA3OUT	TXD5/SDA5		
30		P7_5		TA2IN/W			
31		P7_4		TA2OUT/W			
32		P7_3		TA1IN/V	CTS2/RTS2		
33		P7_2		TA1OUT/V	CLK2		
34		P7_1		TA0IN/TB5IN	RXD2/SCL2/SCLMM		
35		P7_0		TA0OUT	TXD2/SDA2/SDAMM		
36		P6_7			TXD1/SDA1		
37	VCC1						
38		P6_6			RXD1/SCL1		
39	VSS						
40		P6_5			CLK1		
41		P6_4			CTS1/RTS1/CTS0/CLKS1		
42		P6_3			TXD0/SDA0		
43		P6_2			RXD0/SCL0		
44		P6_1			CLK0		
45		P6_0		RTCOU	CTS0/RTS0		
46		P13_7					
47		P13_6					
48		P13_5					
49		P13_4					
50	CLKOUT	P5_7					RDY

Table 1.9 Pin Names for the 128-Pin Package (3/3)

Pin No.	Control Pin	Port	I/O Pin for Peripheral Function				Bus Control Pin
			Interrupt	Timer	Serial interface	A/D converter, D/A converter	
101		P1_2			RXD6/SCL6		D10
102		P1_1			CLK6		D9
103		P1_0			CTS6/RTS6		D8
104		P0_7				AN0_7	D7
105		P0_6				AN0_6	D6
106		P0_5				AN0_5	D5
107		P0_4				AN0_4	D4
108		P0_3				AN0_3	D3
109		P0_2				AN0_2	D2
110		P0_1				AN0_1	D1
111		P0_0				AN0_0	D0
112		P11_7					
113		P11_6					
114		P11_5					
115		P11_4					
116		P11_3					
117		P11_2					
118		P11_1					
119		P11_0					
120		P10_7	KI3			AN7	
121		P10_6	KI2			AN6	
122		P10_5	KI1			AN5	
123		P10_4	KI0			AN4	
124		P10_3				AN3	
125		P10_2				AN2	
126		P10_1				AN1	
127	AVSS						
128		P10_0				AN0	

Table 4.4 SFR Information (4) ⁽¹⁾

Address	Register	Symbol	Reset Value
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h	DMA2 Interrupt Control Register	DM2IC	XXXX X000b
006Ah	DMA3 Interrupt Control Register	DM3IC	XXXX X000b
006Bh	UART5 Bus Collision Detection Interrupt Control Register CEC1 Interrupt Control Register	U5BCNIC CEC1IC	XXXX X000b
006Ch	UART5 Transmit Interrupt Control Register CEC2 Interrupt Control Register	S5TIC CEC2IC	XXXX X000b
006Dh	UART5 Receive Interrupt Control Register	S5RIC	XXXX X000b
006Eh	UART6 Bus Collision Detection Interrupt Control Register Real-Time Clock Periodic Interrupt Control Register	U6BCNIC RTCTIC	XXXX X000b
006Fh	UART6 Transmit Interrupt Control Register Real-Time Clock Compare Interrupt Control Register	S6TIC RTCCIC	XXXX X000b
0070h	UART6 Receive Interrupt Control Register	S6RIC	XXXX X000b
0071h	UART7 Bus Collision Detection Interrupt Control Register Remote Control Signal Receiver 0 Interrupt Control Register	U7BCNIC PMC0IC	XXXX X000b
0072h	UART7 Transmit Interrupt Control Register Remote Control Signal Receiver 1 Interrupt Control Register	S7TIC PMC1IC	XXXX X000b
0073h	UART7 Receive Interrupt Control Register	S7RIC	XXXX X000b
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh	I2C-bus Interface Interrupt Control Register	IICIC	XXXX X000b
007Ch	SCL/SDA Interrupt Control Register	SCLDAIC	XXXX X000b
007Dh			
007Eh			
007Fh			
0080h to 017Fh			

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 4.8 SFR Information (8) ⁽¹⁾

Address	Register	Symbol	Reset Value
0210h	Address Match Interrupt Register 0	RMAD0	00h
0211h			00h
0212h			X0h
0213h			
0214h	Address Match Interrupt Register 1	RMAD1	00h
0215h			00h
0216h			X0h
0217h			
0218h	Address Match Interrupt Register 2	RMAD2	00h
0219h			00h
021Ah			X0h
021Bh			
021Ch	Address Match Interrupt Register 3	RMAD3	00h
021Dh			00h
021Eh			X0h
021Fh			
0220h	Flash Memory Control Register 0	FMR0	0000 0001b (Other than user boot mode) 0010 0001b (User boot mode)
0221h	Flash Memory Control Register 1	FMR1	00X0 XX0Xb
0222h	Flash Memory Control Register 2	FMR2	XXXX 0000b
0223h			
0224h			
0225h			
0226h			
0227h			
0228h			
0229h			
022Ah			
022Bh			
022Ch			
022Dh			
022Eh			
022Fh			
0230h	Flash Memory Control Register 6	FMR6	XX0X XX00b
0231h			
0232h			
0233h			
0234h			
0235h			
0236h			
0237h			
0238h			
0239h			
023Ah			
023Bh			
023Ch			
023Dh			
023Eh			
023Fh			

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 4.11 SFR Information (11) ⁽¹⁾

Address	Register	Symbol	Reset Value
02A0h			
02A1h			
02A2h			
02A3h			
02A4h	UART7 Special Mode Register 4	U7SMR4	00h
02A5h	UART7 Special Mode Register 3	U7SMR3	000X 0X0Xb
02A6h	UART7 Special Mode Register 2	U7SMR2	X000 0000b
02A7h	UART7 Special Mode Register	U7SMR	X000 0000b
02A8h	UART7 Transmit/Receive Mode Register	U7MR	00h
02A9h	UART7 Bit Rate Register	U7BRG	XXh
02AAh	UART7 Transmit Buffer Register	U7TB	XXh
02ABh			XXh
02ACh	UART7 Transmit/Receive Control Register 0	U7C0	0000 1000b
02ADh	UART7 Transmit/Receive Control Register 1	U7C1	0000 0010b
02AEh	UART7 Receive Buffer Register	U7RB	XXh
02AFh			XXh
02B0h	I2C0 Data Shift Register	S00	XXh
02B1h			
02B2h	I2C0 Address Register 0	S0D0	0000 000Xb
02B3h	I2C0 Control Register 0	S1D0	00h
02B4h	I2C0 Clock Control Register	S20	00h
02B5h	I2C0 Start/Stop Condition Control Register	S2D0	0001 1010b
02B6h	I2C0 Control Register 1	S3D0	0011 0000b
02B7h	I2C0 Control Register 2	S4D0	00h
02B8h	I2C0 Status Register 0	S10	0001 000Xb
02B9h	I2C0 Status Register 1	S11	XXXX X000b
02BAh	I2C0 Address Register 1	S0D1	0000 000Xb
02BBh	I2C0 Address Register 2	S0D2	0000 000Xb
02BCh			
02BDh			
02BEh			
02BFh			
02C0h to 02FFh			

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

4.2 Notes on SFRs

4.2.1 Register Settings

Table 4.19 lists Registers with Write-Only Bits and registers whose function differs between reading and writing. Set these registers with immediate values. Do not use read-modify-write instructions. When establishing the next value by altering the existing value, write the existing value to the RAM as well as to the register. Transfer the next value to the register after making changes in the RAM. Read-modify-write instructions can be used when writing to the no register bits.

Table 4.19 Registers with Write-Only Bits

Address	Register	Symbol
0249h	UART0 Bit Rate Register	U0BRG
024Bh to 024Ah	UART0 Transmit Buffer Register	U0TB
0259h	UART1 Bit Rate Register	U1BRG
025Bh to 025Ah	UART1 Transmit Buffer Register	U1TB
0269h	UART2 Bit Rate Register	U2BRG
026Bh to 026Ah	UART2 Transmit Buffer Register	U2TB
0273h	SI/O3 Bit Rate Register	S3BRG
0277h	SI/O4 Bit Rate Register	S4BRG
0289h	UART5 Bit Rate Register	U5BRG
028Bh to 028Ah	UART5 Transmit Buffer Register	U5TB
0299h	UART6 Bit Rate Register	U6BRG
029Bh to 029Ah	UART6 Transmit Buffer Register	U6TB
02A9h	UART7 Bit Rate Register	U7BRG
02ABh to 02AAh	UART7 Transmit Buffer Register	U7TB
02B6h	I2C0 Control Register 1	S3D0
02B8h	I2C0 Status Register 0	S10
0303h to 0302h	Timer A1-1 Register	TA11
0305h to 0304h	Timer A2-1 Register	TA21
0307h to 0306h	Timer A4-1 Register	TA41
030Ah	Three-Phase Output Buffer Register 0	IDB0
030Bh	Three-Phase Output Buffer Register 1	IDB1
030Ch	Dead Time Timer	DTT
030Dh	Timer B2 Interrupt Generation Frequency Set Counter	ICTB2
0327h to 0326h	Timer A0 Register	TA0
0329h to 0328h	Timer A1 Register	TA1
032Bh to 032Ah	Timer A2 Register	TA2
032Dh to 032Ch	Timer A3 Register	TA3
032Fh to 032Eh	Timer A4 Register	TA4
037Dh	Watchdog Timer Refresh Register	WDTR
037Eh	Watchdog Timer Start Register	WDTS

5.1.5 Flash Memory Electrical Characteristics

Table 5.8 CPU Clock When Operating Flash Memory (f_{BCLK})

$V_{\text{CC1}} = 2.7$ to 5.5 V, $T_{\text{opr}} = -20^{\circ}\text{C}$ to $85^{\circ}\text{C}/-40^{\circ}\text{C}$ to 85°C unless otherwise specified.

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
-	CPU rewrite mode				10 (1)	MHz
$f(\text{SLOW_R})$	Slow read mode				5 (3)	MHz
-	Low current consumption read mode			$f\text{C}(32.768)$	35	kHz
-	Data flash read	$2.7\text{ V} \leq V_{\text{CC1}} \leq 3.0\text{ V}$			16 (2)	MHz
		$3.0\text{ V} < V_{\text{CC1}} \leq 5.5\text{ V}$			20 (2)	MHz

Notes:

1. Set the PM17 bit in the PM1 register to 1 (one wait).
2. When the frequency is over this value, set the FMR17 bit in the FMR1 register to 0 (one wait) or the PM17 bit in the PM1 register to 1 (one wait).
3. Set the PM17 bit in the PM1 register to 1 (one wait). When using 125 kHz on-chip oscillator clock or sub clock as the CPU clock source, a wait is not necessary.

Table 5.9 Flash Memory (Program ROM 1, 2) Electrical Characteristics

$V_{\text{CC1}} = 2.7$ to 5.5 V at $T_{\text{opr}} = 0^{\circ}\text{C}$ to 60°C (option: -40°C to 85°C), unless otherwise specified.

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
-	Program and erase cycles (1), (3), (4)	$V_{\text{CC1}} = 3.3\text{ V}$, $T_{\text{opr}} = 25^{\circ}\text{C}$	1,000 (2)			times
-	2 word program time	$V_{\text{CC1}} = 3.3\text{ V}$, $T_{\text{opr}} = 25^{\circ}\text{C}$		150	4000	μs
-	Lock bit program time	$V_{\text{CC1}} = 3.3\text{ V}$, $T_{\text{opr}} = 25^{\circ}\text{C}$		70	3000	μs
-	Block erase time	$V_{\text{CC1}} = 3.3\text{ V}$, $T_{\text{opr}} = 25^{\circ}\text{C}$		0.2	3.0	s
-	Program, erase voltage		2.7		5.5	V
-	Read voltage	$T_{\text{opr}} = -20^{\circ}\text{C}$ to $85^{\circ}\text{C}/-40^{\circ}\text{C}$ to 85°C	2.7		5.5	V
-	Program, erase temperature		0		60	$^{\circ}\text{C}$
t_{PS}	Flash memory circuit stabilization wait time				50	μs
-	Data hold time (6)	Ambient temperature = 55°C	20			year

Notes:

1. Definition of program and erase cycles:
The program and erase cycles refer to the number of per-block erasures. If the program and erase cycles are n ($n = 1,000$), each block can be erased n times. For example, if a block is erased after writing 2 word data 16,384 times, each to a different address, this counts as one program and erase cycles. Data cannot be written to the same address more than once without erasing the block (rewrite prohibited).
2. Cycles to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
3. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. It is advisable to retain data on the erasure cycles of each block and limit the number of erase operations to a certain number.
4. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
5. Customers desiring program/erase failure rate information should contact a Renesas Electronics sales office.
6. The data hold time includes time that the power supply is off or the clock is not supplied.

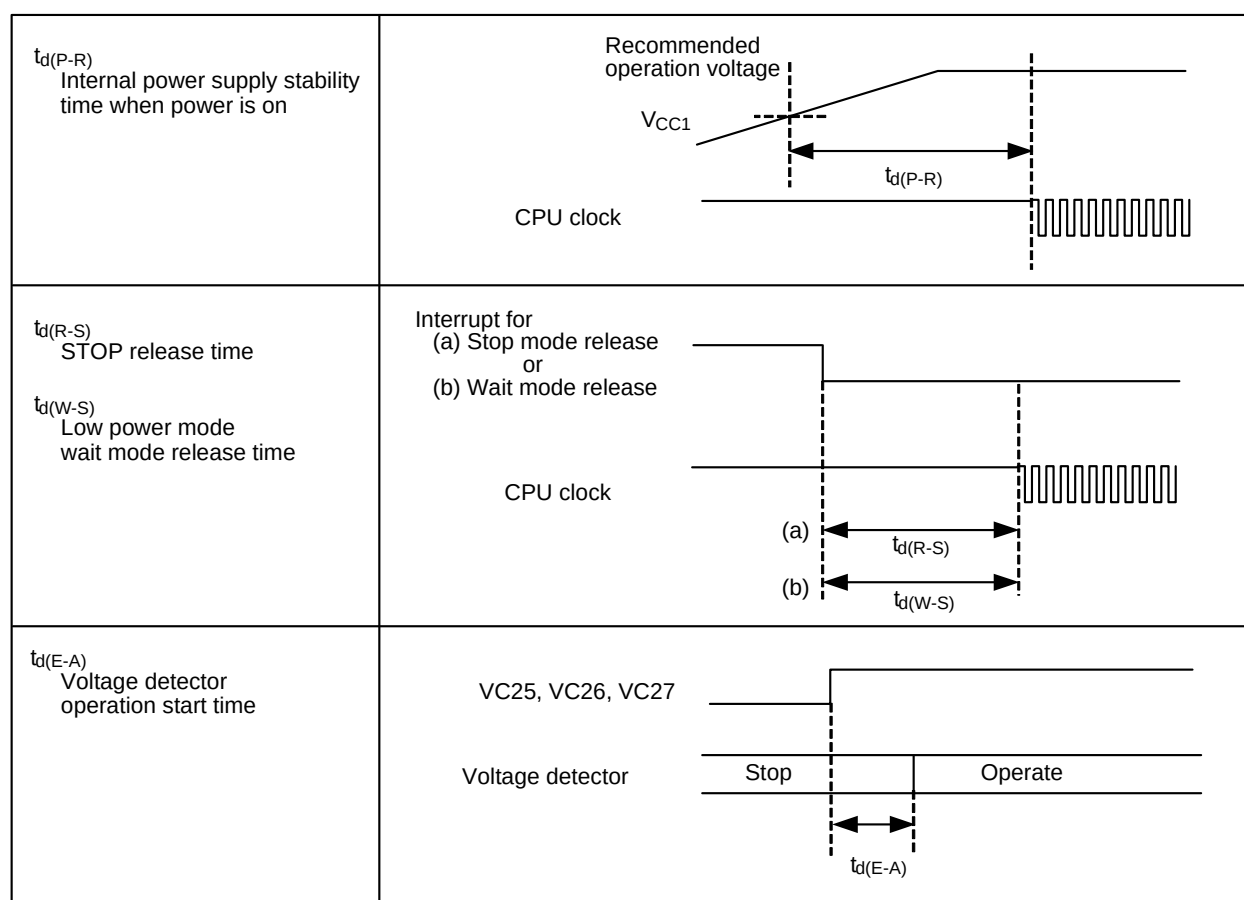
Table 5.15 Power Supply Circuit Timing Characteristics

The measurement condition is $V_{CC1} = 2.7$ to 5.5 V and $T_{opr} = 25^{\circ}\text{C}$, unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Internal power supply stability time when power is on ⁽¹⁾				5	ms
$t_{d(R-S)}$	STOP release time				150	μs
$t_{d(W-S)}$	Low power mode wait mode release time				150	μs

Note:

- Waiting time until the internal power supply generator stabilizes when power is on.

**Figure 5.4 Power Supply Circuit Timing Diagram**

$$V_{CC1} = V_{CC2} = 5 \text{ V}$$

5.2.2 Timing Requirements (Peripheral Functions and Others)

($V_{CC1} = V_{CC2} = 5 \text{ V}$, $V_{SS} = 0 \text{ V}$, at $T_{opr} = -20^{\circ}\text{C}$ to 85°C / -40°C to 85°C unless otherwise specified)

5.2.2.1 Reset Input ($\overline{\text{RESET}}$ Input)

Table 5.24 Reset Input ($\overline{\text{RESET}}$ Input)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(RSTL)}$	$\overline{\text{RESET}}$ input low pulse width	10		μs

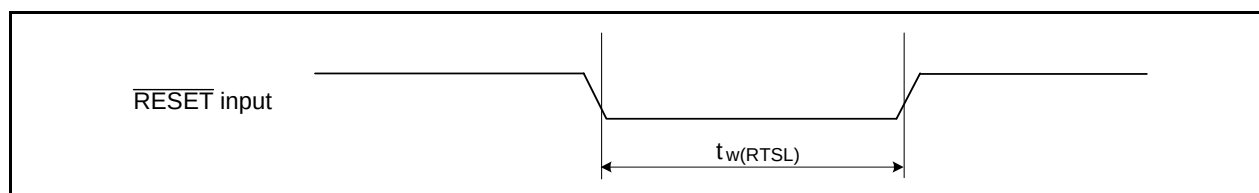


Figure 5.5 Reset Input ($\overline{\text{RESET}}$ Input)

5.2.2.2 External Clock Input

Table 5.25 External Clock Input (XIN Input) (1)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External clock input cycle time	50		ns
$t_{w(H)}$	External clock input high pulse width	20		ns
$t_{w(L)}$	External clock input low pulse width	20		ns
t_r	External clock rise time		9	ns
t_f	External clock fall time		9	ns

Note:

- The condition is $V_{CC1} = V_{CC2} = 3.0$ to 5.0 V .

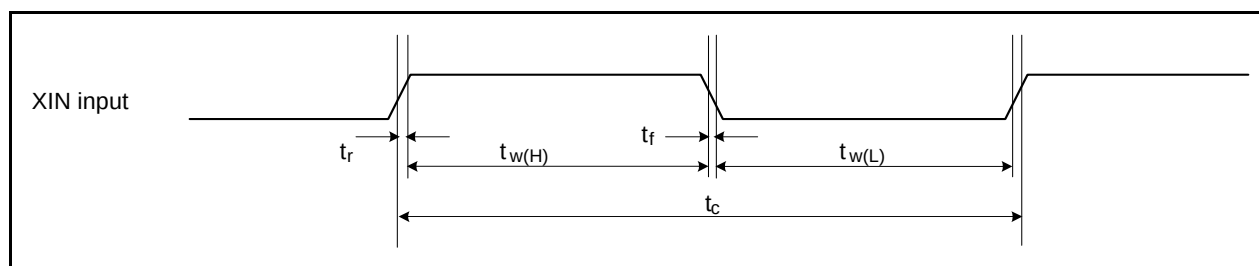


Figure 5.6 External Clock Input (XIN Input)

$$V_{CC1} = V_{CC2} = 5\text{ V}$$

Timing Requirements

($V_{CC1} = V_{CC2} = 5\text{ V}$, $V_{SS} = 0\text{ V}$, at $T_{opr} = -20^{\circ}\text{C}$ to 85°C / -40°C to 85°C unless otherwise specified)

5.2.2.3 Timer A Input**Table 5.26 Timer A Input (Counter Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	100		ns
$t_{w(TAH)}$	TAiIN input high pulse width	40		ns
$t_{w(TAL)}$	TAiIN input low pulse width	40		ns

Table 5.27 Timer A Input (Gating Input in Timer Mode)

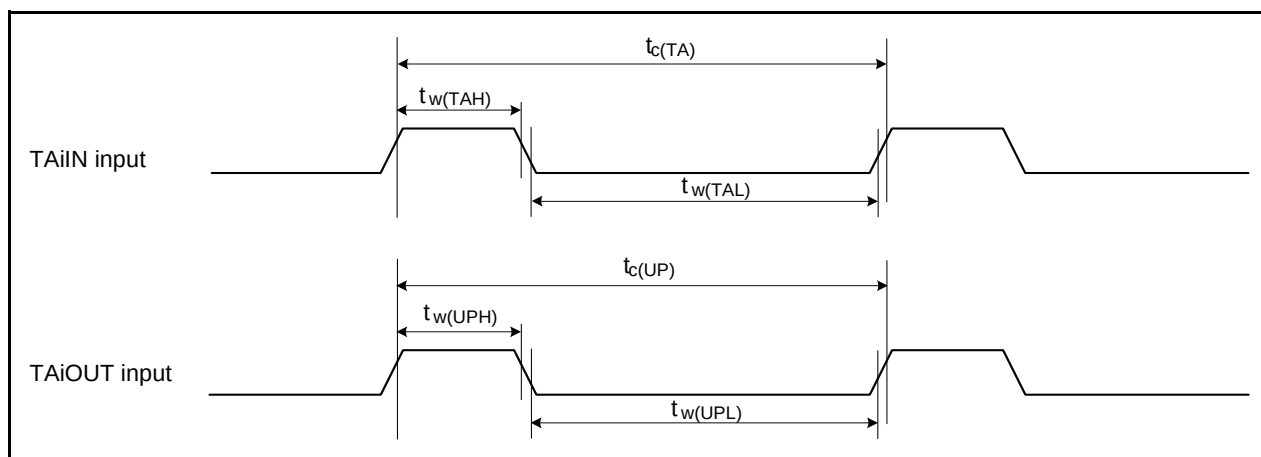
Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	400		ns
$t_{w(TAH)}$	TAiIN input high pulse width	200		ns
$t_{w(TAL)}$	TAiIN input low pulse width	200		ns

Table 5.28 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	200		ns
$t_{w(TAH)}$	TAiIN input high pulse width	100		ns
$t_{w(TAL)}$	TAiIN input low pulse width	100		ns

Table 5.29 Timer A Input (External Trigger Input in Pulse Width Modulation Mode and Programmable Output Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN input high pulse width	100		ns
$t_{w(TAL)}$	TAiIN input low pulse width	100		ns

**Figure 5.7 Timer A Input**

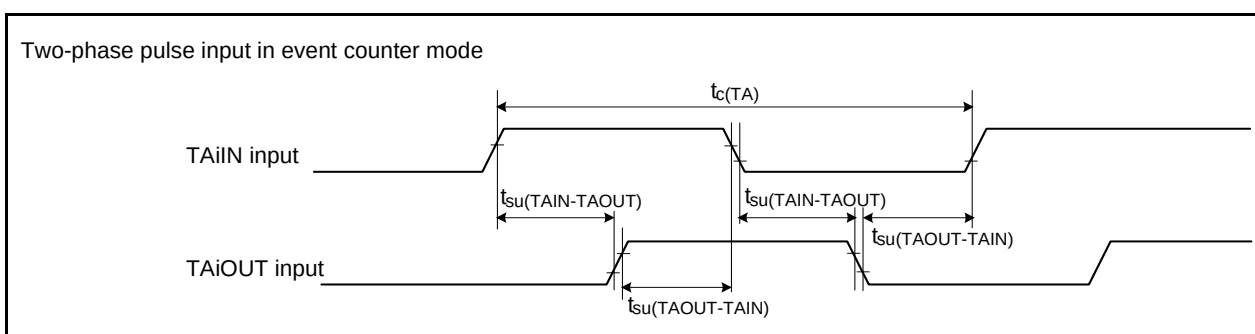
$$V_{CC1} = V_{CC2} = 5\text{ V}$$

Timing Requirements

($V_{CC1} = V_{CC2} = 5\text{ V}$, $V_{SS} = 0\text{ V}$, at $T_{opr} = -20^{\circ}\text{C}$ to $85^{\circ}\text{C}/-40^{\circ}\text{C}$ to 85°C unless otherwise specified)

Table 5.30 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	800		ns
$t_{su(TAIN-TAOUT)}$	TAiOUT input setup time	200		ns
$t_{su(TAOUT-TAIN)}$	TAiIN input setup time	200		ns

**Figure 5.8 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)**

$$V_{CC1} = V_{CC2} = 5\text{ V}$$

Timing Requirements

($V_{CC1} = V_{CC2} = 5\text{ V}$, $V_{SS} = 0\text{ V}$, at $T_{opr} = -20^{\circ}\text{C}$ to $85^{\circ}\text{C}/-40^{\circ}\text{C}$ to 85°C unless otherwise specified)

5.2.2.4 Timer B Input

Table 5.31 Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBiIN input high pulse width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBiIN input low pulse width (counted on one edge)	40		ns
$t_{c(TB)}$	TBiIN input cycle time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBiIN input high pulse width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBiIN input low pulse width (counted on both edges)	80		ns

Table 5.32 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	400		ns
$t_{w(TBH)}$	TBiIN input high pulse width	200		ns
$t_{w(TBL)}$	TBiIN input low pulse width	200		ns

Table 5.33 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	400		ns
$t_{w(TBH)}$	TBiIN input high pulse width	200		ns
$t_{w(TBL)}$	TBiIN input low pulse width	200		ns

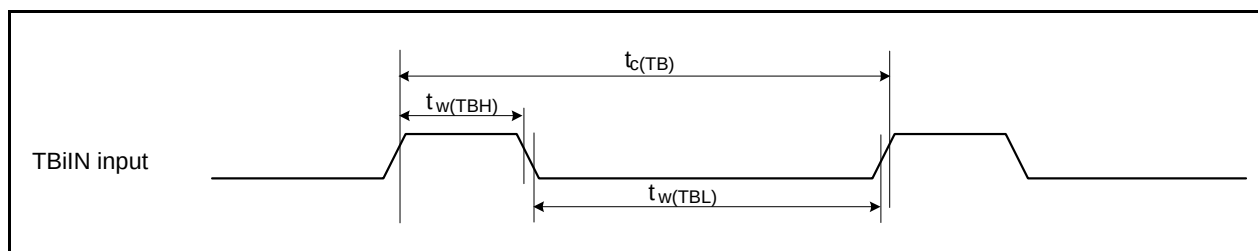


Figure 5.9 Timer B Input

$$V_{CC1} = V_{CC2} = 5\text{ V}$$

Timing Requirements

($V_{CC1} = V_{CC2} = 5\text{ V}$, $V_{SS} = 0\text{ V}$, at $T_{opr} = -20^{\circ}\text{C}$ to 85°C / -40°C to 85°C unless otherwise specified)

5.2.3 Timing Requirements (Memory Expansion Mode and Microprocessor Mode)

Table 5.37 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{ac1}(\text{RD-DB})$	Data input access time (for setting with no wait)		(Note 1)	ns
$t_{ac2}(\text{RD-DB})$	Data input access time (for setting with 1 to 3 waits)		(Note 2)	ns
$t_{ac3}(\text{RD-DB})$	Data input access time (when accessing multiplex bus area)		(Note 3)	ns
$t_{ac4}(\text{RD-DB})$	Data input access time (for setting with $2\phi + 3\phi$ or more)		(Note 4)	ns
$t_{su}(\text{DB-RD})$	Data input setup time	40		ns
$t_{su}(\text{RDY-BCLK})$	RDY input setup time	80		ns
$t_h(\text{RD-DB})$	Data input hold time	0		ns
$t_h(\text{BCLK-RDY})$	RDY input hold time	0		ns

Notes:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f_{(BCLK)}} - 45[\text{ns}]$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n + 0.5) \times 10^9}{f_{(BCLK)}} - 45[\text{ns}] \quad n \text{ is 1 for 1 wait setting, 2 for 2 waits setting and 3 for 3 waits setting.}$$

3. Calculated according to the BCLK frequency as follows:

$$\frac{(n - 0.5) \times 10^9}{f_{(BCLK)}} - 45[\text{ns}] \quad n \text{ is 2 for 2 waits setting, and 3 for 3 waits setting.}$$

4. Calculated according to the BCLK frequency as follows:

$$\frac{n \times 10^9}{f_{(BCLK)}} - 45[\text{ns}] \quad n \text{ is 3 for } 2\phi + 3\phi, 4 \text{ for } 2\phi + 4\phi, 4 \text{ for } 3\phi + 4\phi, \text{ and } 5 \text{ for } 4\phi + 5\phi.$$

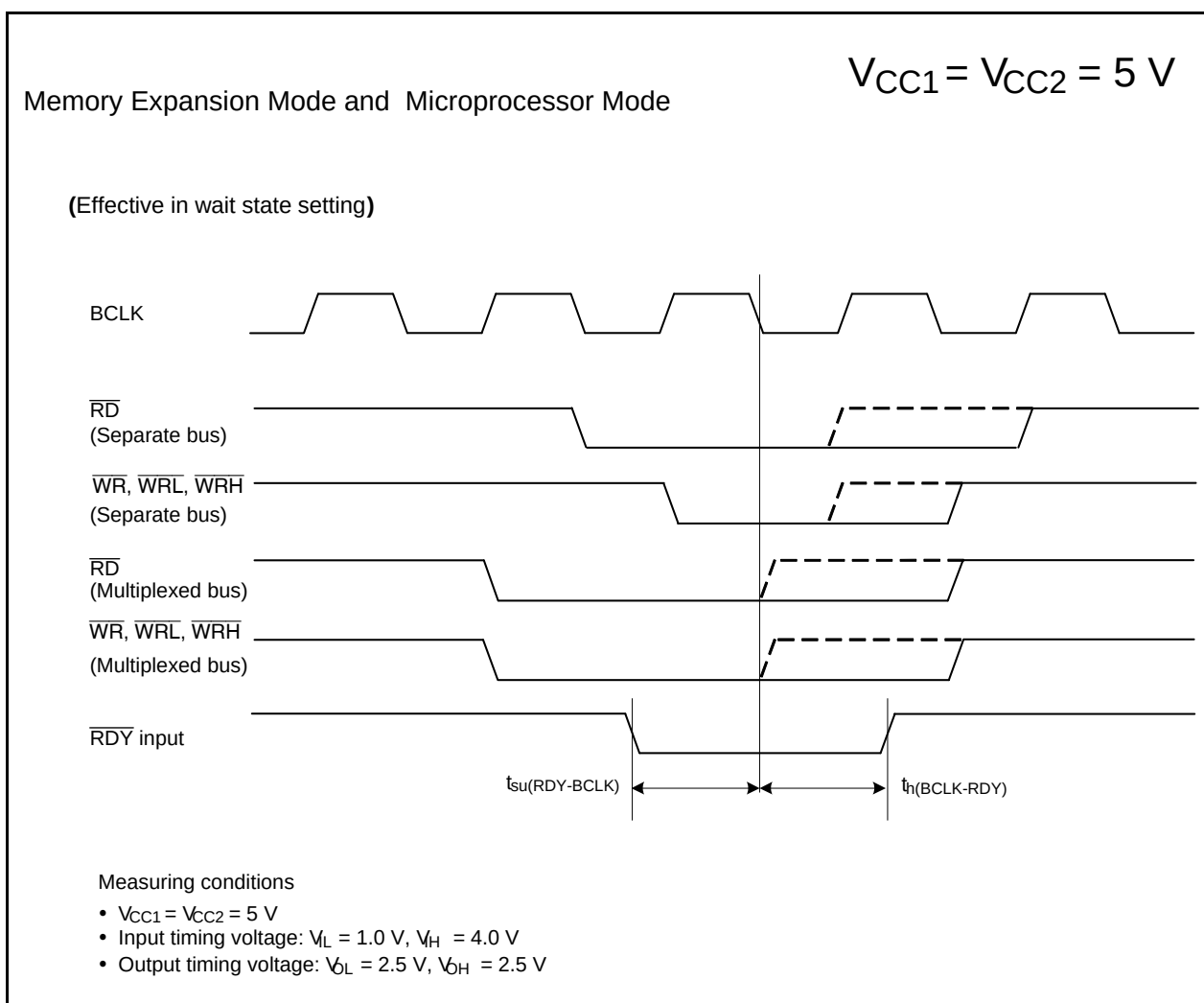


Figure 5.13 Timing Diagram

$$V_{CC1} = V_{CC2} = 5 \text{ V}$$

Switching Characteristics

($V_{CC1} = V_{CC2} = 5 \text{ V}$, $V_{SS} = 0 \text{ V}$, at $T_{opr} = -20^{\circ}\text{C}$ to $85^{\circ}\text{C}/-40^{\circ}\text{C}$ to 85°C unless otherwise specified)

5.2.4.4 In Wait State Setting $2\phi + 3\phi$, $2\phi + 4\phi$, $3\phi + 4\phi$, and $4\phi + 5\phi$, and When Accessing External Area

Table 5.41 Memory Expansion Mode and Microprocessor Mode (in Wait State Setting $2\phi + 3\phi$, $2\phi + 4\phi$, $3\phi + 4\phi$, and $4\phi + 5\phi$, and When Accessing External Area)

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	See Figure 5.14		25	ns
$t_{h(BCLK-AD)}$	Address output hold time (in relation to BCLK)		0		ns
$t_{h(RD-AD)}$	Address output hold time (in relation to RD)		0		ns
$t_{h(WR-AD)}$	Address output hold time (in relation to WR)		(Note 2)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			25	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (in relation to BCLK)		0		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			15	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		-4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			25	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			25	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (in relation to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data output hold time (in relation to BCLK) ⁽³⁾		0		ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(Note 1)		ns
$t_{h(WR-DB)}$	Data output hold time (in relation to WR) ⁽³⁾		(Note 2)		ns

Notes:

1. Calculated according to the BCLK frequency as follows:

$$\frac{(n - 0.5) \times 10^9}{f_{(BCLK)}} - 40 [ns] \quad n \text{ is 3 for } 2\phi + 3\phi, 4 \text{ for } 2\phi + 4\phi, 4 \text{ for } 3\phi + 4\phi, \text{ and } 5 \text{ for } 4\phi + 5\phi.$$

2. Calculated according to the BCLK frequency as follows:

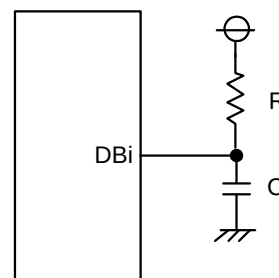
$$\frac{0.5 \times 10^9}{f_{(BCLK)}} - 10 [ns]$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
Hold time of data bus is expressed in

$$t = -CR \times \ln(1 - V_{OL}/V_{CC2})$$
 by a circuit of the right figure.
 For example, when $V_{OL} = 0.2V_{CC2}$, $C = 30 \text{ pF}$, $R = 1 \text{ k}\Omega$, hold time of output low level is

$$t = -30 \text{ pF} \times 1 \text{ k}\Omega \times \ln(1 - 0.2V_{CC2}/V_{CC2})$$

$$= 6.7 \text{ ns}.$$



5.3 Electrical Characteristics ($V_{CC1} = V_{CC2} = 3\text{ V}$)

5.3.1 Electrical Characteristics

 $V_{CC1} = V_{CC2} = 3\text{ V}$
Table 5.43 Electrical Characteristics (1) (1)
 $V_{CC1} = V_{CC2} = 2.7\text{ to }3.3\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{opr} = -20^{\circ}\text{C to }85^{\circ}\text{C}/-40^{\circ}\text{C to }85^{\circ}\text{C}$, $f_{(BCLK)} = 32\text{ MHz}$ unless otherwise specified.

Symbol	Parameter		Measuring Condition	Standard			Unit
				Min.	Typ.	Max.	
V_{OH}	High output voltage	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1	$I_{OH} = -1\text{ mA}$	$V_{CC1} - 0.5$		V_{CC1}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	$I_{OH} = -1\text{ mA}$	$V_{CC2} - 0.5$		V_{CC2}	
V_{OH}	High output voltage XOUT	HIGH POWER	$I_{OH} = -0.1\text{ mA}$	$V_{CC1} - 0.5$		V_{CC1}	V
		LOW POWER	$I_{OH} = -50\text{ }\mu\text{A}$	$V_{CC1} - 0.5$		V_{CC1}	
	High output voltage XCOUT	HIGH POWER	With no load applied		2.6		V
		LOW POWER	With no load applied		2.2		
V_{OL}	Low output voltage	P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1	$I_{OL} = 1\text{ mA}$			0.5	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	$I_{OL} = 1\text{ mA}$			0.5	
	CEC		$I_{OL} = 1\text{ mA}$		0	0.5	V
V_{OL}	Low output voltage XOUT	HIGH POWER	$I_{OL} = 0.1\text{ mA}$			0.5	V
		LOW POWER	$I_{OL} = 50\text{ }\mu\text{A}$			0.5	
	Low output voltage XCOUT	HIGH POWER	With no load applied		0		V
		LOW POWER	With no load applied		0		
$V_{T+}-V_{T-}$	Hysteresis	HOLD, RDY, TA0IN to TA4IN, TB0IN to TB5IN, INT0 to INT7, NMI, ADTRG, CTS0 to CTS2, CTS5 to CTS7, SCL0 to SCL2, SCL5 to SCL7, SDA0 to SDA2, SDA5 to SDA7, CLK0 to CLK7, TA0OUT to TA4OUT, K10 to K13, RXD0 to RXD2, RXD5 to RXD7, SIN3, SIN4, $\overline{\text{SD}}$, PMC0, PMC1, SCLMM, SDAMM, ZP, IDU, IDV, IDW		0.2		1.0	V
		CEC		0.2	0.5	1.0	V
		RESET		0.2		1.8	V
I_{IH}	High input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1 XIN, RESET, CNVSS, BYTE	$V_I = 3\text{ V}$			4.0	μA
—	Leakage current in powered-off state		CEC	$V_{CC1} = 0\text{ V}$		1.8	μA
I_{IL}	Low input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1 XIN, RESET, CNVSS, BYTE	$V_I = 0\text{ V}$			-4.0	μA
R_{PULLUP}	Pull-up resistance	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1	$V_I = 0\text{ V}$	50	80	150	$\text{k}\Omega$
R_{FXIN}	Feedback resistance XIN				3.0		$\text{M}\Omega$
V_{RAM}	RAM retention voltage		In stop mode	1.8			V

Note:

- When $V_{CC1} \neq V_{CC2}$, refer to 5 V or 3 V standard depending on the voltage.

$$V_{CC1} = V_{CC2} = 3\text{ V}$$

Timing Requirements

($V_{CC1} = V_{CC2} = 3\text{ V}$, $V_{SS} = 0\text{ V}$, at $T_{opr} = -20^{\circ}\text{C}$ to 85°C / -40°C to 85°C unless otherwise specified)

5.3.2.3 Timer A Input

Table 5.49 Timer A Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	150		ns
$t_{w(TAH)}$	TAiIN input high pulse width	60		ns
$t_{w(TAL)}$	TAiIN input low pulse width	60		ns

Table 5.50 Timer A Input (Gating Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	600		ns
$t_{w(TAH)}$	TAiIN input high pulse width	300		ns
$t_{w(TAL)}$	TAiIN input low pulse width	300		ns

Table 5.51 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	300		ns
$t_{w(TAH)}$	TAiIN input high pulse width	150		ns
$t_{w(TAL)}$	TAiIN input low pulse width	150		ns

Table 5.52 Timer A Input (External Trigger Input in Pulse Width Modulation Mode and Programmable Output Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN input high pulse width	150		ns
$t_{w(TAL)}$	TAiIN input low pulse width	150		ns

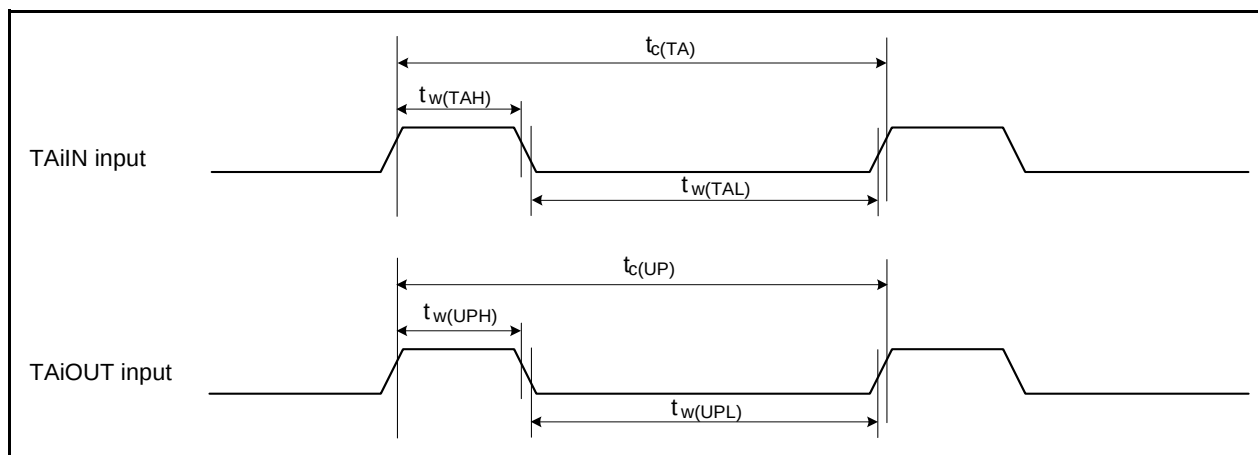


Figure 5.22 Timer A Input

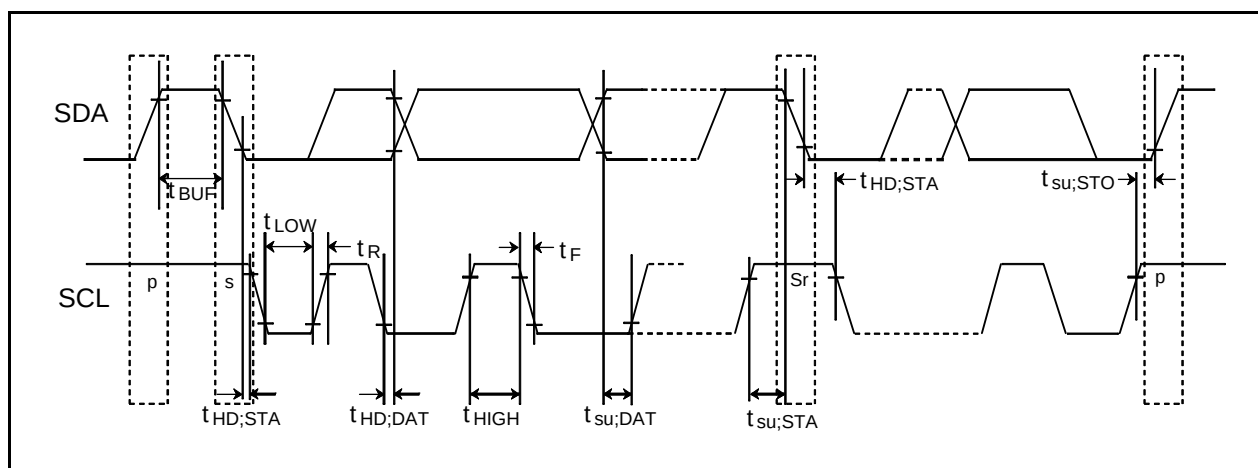
$$V_{CC1} = V_{CC2} = 3\text{ V}$$

Timing Requirements

($V_{CC1} = V_{CC2} = 3\text{ V}$, $V_{SS} = 0\text{ V}$, at $T_{opr} = -20^{\circ}\text{C}$ to $85^{\circ}\text{C}/-40^{\circ}\text{C}$ to 85°C unless otherwise specified)

5.3.2.7 Multi-master I²C-bus**Table 5.59 Multi-master I²C-bus**

Symbol	Parameter	Standard Clock Mode		Fast-mode		Unit
		Min.	Max.	Min.	Max.	
t_{BUF}	Bus free time	4.7		1.3		μs
$t_{HD;STA}$	Hold time in start condition	4.0		0.6		μs
t_{LOW}	Hold time in SCL clock 0 status	4.7		1.3		μs
t_R	SCL, SDA signals' rising time		1000	$20 + 0.1 C_b$	300	ns
$t_{HD;DAT}$	Data hold time	0		0	0.9	μs
t_{HIGH}	Hold time in SCL clock 1 status	4.0		0.6		μs
t_F	SCL, SDA signals' falling time		300	$20 + 0.1 C_b$	300	ns
$t_{su;DAT}$	Data setup time	250		100		ns
$t_{su;STA}$	Setup time in restart condition	4.7		0.6		μs
$t_{su;STO}$	Stop condition setup time	4.0		0.6		μs

**Figure 5.27 Multi-master I²C-bus**

$$V_{CC1} = V_{CC2} = 3 \text{ V}$$

Timing Requirements

($V_{CC1} = V_{CC2} = 3 \text{ V}$, $V_{SS} = 0 \text{ V}$, at $T_{opr} = -20^{\circ}\text{C}$ to 85°C / -40°C to 85°C unless otherwise specified)

5.3.3 Timing Requirements (Memory Expansion Mode and Microprocessor Mode)

Table 5.60 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{ac1(RD-DB)}$	Data input access time (for setting with no wait)		(Note 1)	ns
$t_{ac2(RD-DB)}$	Data input access time (for setting with wait)		(Note 2)	ns
$t_{ac3(RD-DB)}$	Data input access time (when accessing multiplex bus area)		(Note 3)	ns
$t_{ac4(RD-DB)}$	Data input access time (for setting with 2 ϕ + 3 ϕ or more)		(Note 4)	ns
$t_{su(DB-RD)}$	Data input setup time	50		ns
$t_{su(RDY-BCLK)}$	$\overline{RDY}$ input setup time	85		ns
$t_h(RD-DB)$	Data input hold time	0		ns
$t_h(BCLK-RDY)$	$\overline{RDY}$ input hold time	0		ns

Notes:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f_{(BCLK)}} - 60[ns]$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n + 0.5) \times 10^9}{f_{(BCLK)}} - 60[ns] \quad n \text{ is 1 for 1 wait setting, 2 for 2 waits setting and 3 for 3 waits setting.}$$

3. Calculated according to the BCLK frequency as follows:

$$\frac{(n - 0.5) \times 10^9}{f_{(BCLK)}} - 60[ns] \quad n \text{ is 2 for 2 waits setting, 3 for 3 waits setting.}$$

4. Calculated according to the BCLK frequency as follows:

$$\frac{n \times 10^9}{f_{(BCLK)}} - 60[ns] \quad n \text{ is 3 for 2 } \phi + 3 \phi, 4 \text{ for 2 } \phi + 4 \phi, 4 \text{ for 3 } \phi + 4 \phi, 5 \text{ for 4 } \phi + 5 \phi, \dots$$

