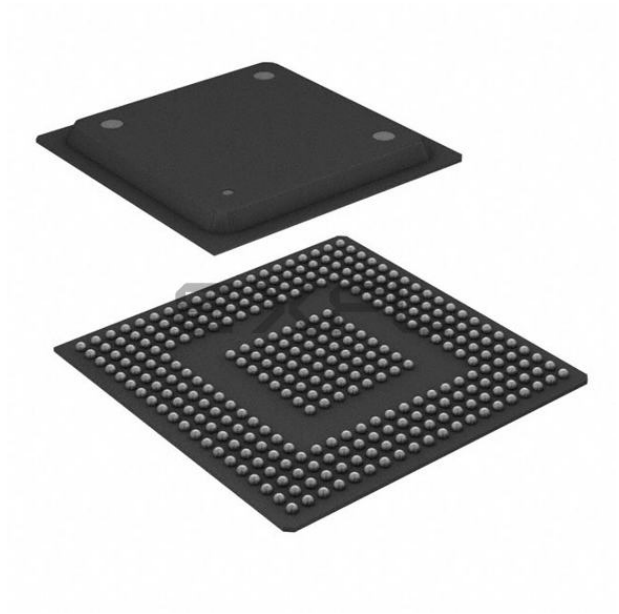
Infineon Technologies - MB91F469QAHPB-GSK6E1 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	FR60 RISC
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	205
Program Memory Size	2.0625MB (2.0625M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	112K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 40x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	320-BBGA
Supplier Device Package	320-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f469qahpb-gsk6e1

(Continued)

- Low-power consumption modes : Sleep/stop mode function
- Supply Supervisor: Low voltage detection circuit for external $V_{DD}5$ and internal 1.8V core voltage
- Clock supervisor
  Monitors the sub-clock (32 kHz) and the main clock (4 MHz) , and switches to a recovery clock (CR oscillator, etc.) when the oscillations stop.
- Clock modulator
- Clock monitor
- Sub-clock calibration
  Corrects the real-time clock timer when operating with the 32 kHz or CR oscillator
- Main oscillator stabilization timer
  Generates an interrupt in sub-clock mode after the stabilization wait time has elapsed on the 23-bit stabilization wait time counter
- Sub-oscillator stabilization timer
  Generates an interrupt in main clock mode after the stabilization wait time has elapsed on the 15-bit stabilization wait time counter

3. Package and technology

- Package : 320-pin plastic BGA (BGA-320)
- CMOS 0.18 µm technology
- Power supply range 3 V to 5 V (1.8 V internal logic provided by a step-down voltage converter)
- Operating temperature range: between − 40 °C and + 105 °C / +125 °C *1

1. For maximum ambient temperature $T_{A(max)}$, please refer to ORDERING INFORMATION on page 152.

■ PIN ASSIGNMENT

1. MB91F469QA

(TOP VIEW)

▲	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	1	76	75	74	73	72	71	70	69	68	67	66	65	64	63	62	61	60	59	58	A
B	2	77	144	143	142	141	140	139	138	137	136	135	134	133	132	131	130	129	128	57	B
C	3	78	145	204	203	202	201	200	199	198	197	196	195	194	193	192	191	190	127	56	C
D	4	79	146	205	256	255	254	253	252	251	250	249	248	247	246	245	244	189	126	55	D
E	5	80	147	206													243	188	125	54	E
F	6	81	148	207													242	187	124	53	F
G	7	82	149	208			257	284	283	282	281	280	279	278			241	186	123	52	G
H	8	83	150	209			258	285	304	303	302	301	300	277			240	185	122	51	H
J	9	84	151	210			259	286	305	316	315	314	299	276			239	184	121	50	J
K	10	85	152	211			260	287	306	317	320	313	298	275			238	183	120	49	K
L	11	86	153	212			261	288	307	318	319	312	297	274			237	182	119	48	L
M	12	87	154	213			262	289	308	309	310	311	296	273			236	181	118	47	M
N	13	88	155	214			263	290	291	292	293	294	295	272			235	180	117	46	N
P	14	89	156	215			264	265	266	267	268	269	270	271			234	179	116	45	P
R	15	90	157	216													233	178	115	44	R
T	16	91	158	217													232	177	114	43	T
U	17	92	159	218	219	220	221	222	223	224	225	226	227	228	229	230	231	176	113	42	U
V	18	93	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	112	41	V
W	19	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	40	W
Y	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

BGA-320P-M06

JEDEC	Pin no.	Pin name	I/O	I/O circuit type [1]	Description
V1	18	P05_6	I/O	A	General-purpose input/output port
		A22			Signal pin of external address bus (bit22)
W1	19	P04_1	I/O	A	General-purpose input/output port
		A25			Signal pin of external address bus (bit25)
Y2	21	P04_3	I/O	A	General-purpose input/output port
		A27			Signal pin of external address bus (bit27)
Y3	22	P03_1	I/O	A	General-purpose input/output port
		D1			Signal pin of external data bus (bit1)
Y4	23	P03_4	I/O	A	General-purpose input/output port
		D4			Signal pin of external data bus (bit4)
Y5	24	P02_0	I/O	A	General-purpose input/output port
		D8			Signal pin of external data bus (bit8)
Y6	25	P02_3	I/O	A	General-purpose input/output port
		D11			Signal pin of external data bus (bit11)
Y7	26	P02_7	I/O	A	General-purpose input/output port
		D15			Signal pin of external data bus (bit15)
Y8	27	P01_2	I/O	A	General-purpose input/output port
		D18			Signal pin of external data bus (bit18)
Y9	28	P01_6	I/O	A	General-purpose input/output port
		D22			Signal pin of external data bus (bit22)
Y10	29	P00_1	I/O	A	General-purpose input/output port
		D25			Signal pin of external data bus (bit25)
Y11	30	P00_5	I/O	A	General-purpose input/output port
		D29			Signal pin of external data bus (bit29)
Y12	31	P00_6	I/O	A	General-purpose input/output port
		D30			Signal pin of external data bus (bit30)
Y13	32	P00_7	I/O	A	General-purpose input/output port
		D31			Signal pin of external data bus (bit31)
Y14	33	P10_4	I/O	A	General-purpose input/output port
		MCLKO			Clock output pin for memory
Y16	35	MONCLK	O	M	Clock monitor pin
W20	40	P21_0	I/O	A	General-purpose input/output port
		SIN0			Data input pin of USART0
V20	41	P21_4	I/O	A	General-purpose input/output port
		SIN1			Data input pin of USART1

JEDEC	Pin no.	Pin name	I/O	I/O circuit type [1]	Description
C10	198	P14_0	I/O	A	General-purpose input/output port
		ICU0			Input capture input pin
		TIN0			External trigger input pin of reload timer
		TTG8/0			External trigger input pin of PPG timer
C9	199	P14_4	I/O	A	General-purpose input/output port
		ICU4			Input capture input pin
		TIN4			External trigger input pin of reload timer
		TTG12/4			External trigger input pin of PPG timer
C8	200	P16_0	I/O	A	General-purpose input/output port
		PPG8			Output pin of PPG timer
C7	201	P16_3	I/O	A	General-purpose input/output port
		PPG11			Output pin of PPG timer
C6	202	P16_7	I/O	A	General-purpose input/output port
		PPG15			Output pin of PPG timer
		ATGX			A/D converter external trigger input pin
C5	203	P15_2	I/O	A	General-purpose input/output port
		OCU2			Output compare output pin
		TOT2			Reload timer output pin
C4	204	P15_6	I/O	A	General-purpose input/output port
		OCU6			Output compare output pin
		TOT6			Reload timer output pin
E4	206	P24_7	I/O	C	General-purpose input/output port
		INT7			External interrupt input pin
		SCL3			I^2C bus clock input/output pin (open drain)
G4	208	P09_2	I/O	A	General-purpose input/output port
		CSX2			Chip select output pin
J4	210	P08_1	I/O	A	General-purpose input/output port
		WRX1			External write strobe output pin
L4	212	P07_0	I/O	A	General-purpose input/output port
		A0			Signal pin of external address bus (bit0)
M4	213	P07_4	I/O	A	General-purpose input/output port
		A4			Signal pin of external address bus (bit4)
P4	215	P06_3	I/O	A	General-purpose input/output port
		A11			Signal pin of external address bus (bit11)
T4	217	P05_2	I/O	A	General-purpose input/output port
		A18			Signal pin of external address bus (bit18)

[Power supply/Ground pins]

Pin no. (JEDEC)	Pin name	Description
1 (A1),20(Y1),34(Y15),39 (Y20), 58 (A20),205 (D4),209 (H4), 214 (N4),218 (U4),222 (U8), 227 (U13),231 (U17),235 (N17), 240 (H17),244 (D17),248 (D13), 253 (D8) 257 to 320 (G7..G14....P7..P14)	VSS	GND pins
233 (R17),237 (L17),242 (F17), 246 (D15),250 (D11),255 (D6)	VDD5	Power supply pins
207 (F4), 211 (K4),216 (R4), 220 (U6),224 (U10),229 (U15)	VDD35	Power supply pins for external bus
36 (Y17),37(Y18)	VDD5R	Power supply pin for internal regulator
60 (A18)	AVSS	Analog GND pin for A/D converter
63 (A15)	AVCC5	Power supply pin for A/D converter
62 (A16)	AVRH5	Reference power supply pin for A/D converter
38(Y19)	VCC18C	Capacitor connection pin for internal regulator

■ NOTES ON DEBUGGER

1. Execution of the RETI Command

If single-step execution is used in an environment where an interrupt occurs frequently, the corresponding interrupt handling routine will be executed repeatedly to the exclusion of other processing. This will prevent the main routine and the handlers for low priority level interrupts from being executed (For example, if the time-base timer interrupt is enabled, stepping over the RETI instruction will always break on the first line of the time-base timer interrupt handler).

Disable the corresponding interrupts when the corresponding interrupt handling routine no longer needs debugging.

2. Break function

If the range of addresses that cause a hardware break (including event breaks) is set to the address of the current system stack pointer or to an area that contains the stack pointer, execution will break after each instruction regardless of whether the user program actually contains data access instructions.

To prevent this, do not set (word) access to the area containing the address of the system stack pointer as the target of the hardware break (including an event breaks).

3. Operand break

It may cause malfunctions if a stack pointer exists in the area which is set as the DSU operand break. Do not set the access to the areas containing the address of system stack pointer as a target of data event break.

■ EMBEDDED PROGRAM/DATA MEMORY (FLASH)

1. Flash features

- MB91F469QA: 2112 Kbytes (32 × 64 Kbytes + 8 × 8 Kbytes = 16.5 Mbits)
- Programmable wait state for read/write access
- Flash and Boot security with security vector at 0x0024:8000 - 0x0024:800F
- Boot security
- Basic specification: Same as MBM29LV400TC (except size and part of sector configuration)

2. Operation modes

(1) 64-bit CPU mode:

- CPU reads and executes programs in word (32-bit) length units.
- Flash writing is not possible.
- Actual Flash Memory access is performed in d-word (64-bit) length units.

(2) 32-bit CPU mode :

- CPU reads and executes programs in word (32-bit) length units.
- Actual Flash Memory access is performed in word (32-bit) length units.

(3) 16-bit CPU mode :

- CPU reads and writes in half-word (16-bit) length units.
- Program execution from the Flash is not possible.
- Actual Flash Memory access is performed in half-word (16-bit) length units.

Note: The operation mode of the flash memory can be selected using a Boot-ROM function. The function start address is 0xBF60. The parameter description is given in the Hardware Manual in chapter 54.6 "Flash Access Mode Switching".

3. Flash access in CPU mode

3.1. Flash configuration

3.1.1. Flash memory map MB91F469QA

Address									
0024:FFFFh 0024:C000h	SA6 (8KB)				SA7 (8KB)				ROMS10
0024:BFFFh 0024:8000h	SA4 (8KB)				SA5 (8KB)				
0024:7FFFh 0024:4000h	SA2 (8KB)				SA3 (8KB)				
0024:3FFFh 0024:0000h	SA0 (8KB)				SA1 (8KB)				
0023:FFFFh 0022:0000h	SA38 (64KB)				SA39 (64KB)				
0021:FFFFh 0020:0000h	SA36 (64KB)				SA37 (64KB)				
001F:FFFFh 001E:0000h	SA34 (64KB)				SA35 (64KB)				ROMS9
001D:FFFFh 001C:0000h	SA32 (64KB)				SA33 (64KB)				
001B:FFFFh 001A:0000h	SA30 (64KB)				SA31 (64KB)				ROMS8
0019:FFFFh 0018:0000h	SA28 (64KB)				SA29 (64KB)				
0017:FFFFh 0016:0000h	SA26 (64KB)				SA27 (64KB)				ROMS7
0015:FFFFh 0014:0000h	SA24 (64KB)				SA25 (64KB)				
0013:FFFFh 0012:0000h	SA22 (64KB)				SA23 (64KB)				ROMS6
0011:FFFFh 0010:0000h	SA20 (64KB)				SA21 (64KB)				
000F:FFFFh 000E:0000h	SA18 (64KB)				SA19 (64KB)				ROMS5
000D:FFFFh 000C:0000h	SA16 (64KB)				SA17 (64KB)				ROMS4
000B:FFFFh 000A:0000h	SA14 (64KB)				SA15 (64KB)				ROMS3
0009:FFFFh 0008:0000h	SA12 (64KB)				SA13 (64KB)				ROMS2
0007:FFFFh 0006:0000h	SA10 (64KB)				SA11 (64KB)				ROMS1
0005:FFFFh 0004:0000h	SA8 (64KB)				SA9 (64KB)				ROMS0
	addr+0	addr+1	addr+2	addr+3	addr+4	addr+5	addr+6	addr+7	
16bit write mode	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
32bit write mode	dat[31:0]				dat[31:0]				

4. Parallel Flash programming mode

4.1. Flash configuration in parallel Flash programming mode

Parallel Flash programming mode (MD[2:0] = 111):

MB91F469QA

FA[21:0]	
003F:FFFFh 003F:0000h	SA39 (64KB)
003E:FFFFh 003E:0000h	SA38 (64KB)
003D:FFFFh 003D:0000h	SA37 (64KB)
003C:FFFFh 003C:0000h	SA36 (64KB)
003B:FFFFh 003B:0000h	SA35 (64KB)
003A:FFFFh 003A:0000h	SA34 (64KB)
0039:FFFFh 0039:0000h	SA33 (64KB)
0038:FFFFh 0038:0000h	SA32 (64KB)
0037:FFFFh 0037:0000h	SA31 (64KB)
0036:FFFFh 0036:0000h	SA30 (64KB)
0035:FFFFh 0035:0000h	SA29 (64KB)
0034:FFFFh 0034:0000h	SA28 (64KB)
0033:FFFFh 0033:0000h	SA27 (64KB)
0032:FFFFh 0032:0000h	SA26 (64KB)
0031:FFFFh 0031:0000h	SA25 (64KB)
0030:FFFFh 0030:0000h	SA24 (64KB)
002F:FFFFh 002F:0000h	SA23 (64KB)
002E:FFFFh 002E:0000h	SA22 (64KB)
002D:FFFFh 002D:0000h	SA21 (64KB)
002C:FFFFh 002C:0000h	SA20 (64KB)
002B:FFFFh 002B:0000h	SA19 (64KB)
002A:FFFFh 002A:0000h	SA18 (64KB)
0029:FFFFh 0029:0000h	SA17 (64KB)
0028:FFFFh 0028:0000h	SA16 (64KB)
0027:FFFFh 0027:0000h	SA15 (64KB)
0026:FFFFh 0026:0000h	SA14 (64KB)
0025:FFFFh 0025:0000h	SA13 (64KB)
0024:FFFFh 0024:0000h	SA12 (64KB)
0023:FFFFh 0023:0000h	SA11 (64KB)
0022:FFFFh 0022:0000h	SA10 (64KB)
0021:FFFFh 0021:0000h	SA9 (64KB)
0020:FFFFh 0020:0000h	SA8 (64KB)
001F:FFFFh 001F:E000h	SA7 (8KB)
001F:DFFFh 001F:C000h	SA6 (8KB)
001F:BFFFh 001F:A000h	SA5 (8KB)
001F:9FFFh 001F:8000h	SA4 (8KB)
001F:7FFFh 001F:6000h	SA3 (8KB)
001F:5FFFh 001F:4000h	SA2 (8KB)
001F:3FFFh 001F:2000h	SA1 (8KB)
001F:1FFFh 001F:0000h	SA0 (8KB)

	FA[1:0]=00	FA[1:0]=10
l6bit write mod	DQ[15:0]	DQ[15:0]

Remark: Always keep FA[0] = 0 and FA[22] = 1

	Register				
Address	**+0**	**+1**	**+2**	**+3**	**Block**
000138H	PTMR05 [R] 11111111 11111111		PCSR05 [W] XXXXXXXX XXXXXXXX		PPG 5
00013CH	PDUT05 [W] XXXXXXXX XXXXXXXX		PCNH05 [R/W] 0000000 -	PCNL05 [R/W] 000000 - 0	
000140H	PTMR06 [R] 11111111 11111111		PCSR06 [W] XXXXXXXX XXXXXXXX		PPG 6
000144H	PDUT06 [W] XXXXXXXX XXXXXXXX		PCNH06 [R/W] 0000000 -	PCNL06 [R/W] 000000 - 0	
000148H	PTMR07 [R] 11111111 11111111		PCSR07 [W] XXXXXXXX XXXXXXXX		PPG 7
00014CH	PDUT07 [W] XXXXXXXX XXXXXXXX		PCNH07 [R/W] 0000000 -	PCNL07 [R/W] 000000 - 0	
000150H	PTMR08 [R] 11111111 11111111		PCSR08 [W] XXXXXXXX XXXXXXXX		PPG 8
000154H	PDUT08 [W] XXXXXXXX XXXXXXXX		PCNH08 [R/W] 0000000 -	PCNL08 [R/W] 000000 - 0	
000158H	PTMR09 [R] 11111111 11111111		PCSR09 [W] XXXXXXXX XXXXXXXX		PPG 9
00015CH	PDUT09 [W] XXXXXXXX XXXXXXXX		PCNH09 [R/W] 0000000 -	PCNL09 [R/W] 000000 - 0	
000160H	PTMR10 [R] 11111111 11111111		PCSR10 [W] XXXXXXXX XXXXXXXX		PPG 10
000164H	PDUT10 [W] XXXXXXXX XXXXXXXX		PCNH10 [R/W] 0000000 -	PCNL10 [R/W] 000000 - 0	
000168H	PTMR11 [R] 11111111 11111111		PCSR11 [W] XXXXXXXX XXXXXXXX		PPG 11
00016CH	PDUT11 [W] XXXXXXXX XXXXXXXX		PCNH11 [R/W] 0000000 -	PCNL11 [R/W] 000000 - 0	
000170H	P0TMCSRH [R/W] - 0 - 000 - 0	P0TMCSRL [R/W] - - - 00000	P1TMCSRH [R/W] - 0 - 000 - 0	P1TMCSRL [R/W] - - - 00000	Pulse Frequency Modulator
000174H	P0TMRLR [W] XXXXXXXX XXXXXXXX		P0TMR [R] XXXXXXXX XXXXXXXX		
000178H	P1TMRLR [W] XXXXXXXX XXXXXXXX		P1TMR [R] XXXXXXXX XXXXXXXX		
00017CH	reserved				reserved
000180H	reserved	ICS01 [R/W] 00000000	reserved	ICS23 [R/W] 00000000	Input Capture 0-3
000184H	IPCP0 [R] XXXXXXXX XXXXXXXX		IPCP1 [R] XXXXXXXX XXXXXXXX		
000188H	IPCP2 [R] XXXXXXXX XXXXXXXX		IPCP3 [R] XXXXXXXX XXXXXXXX		

	Register				
Address	**+0**	**+1**	**+2**	**+3**	**Block**
0005E0H	AD1ERH [R/W] 00000000 00000000		AD1ERL [R/W] 00000000 00000000		A/D Converter 1
0005E4H	AD1CS1 [R/W] 00000000	AD1CS0 [R/W] 00000000	AD1CR1 [R] 000000XX	AD1CR0 [R] XXXXXXXX	
0005E8H	AD1CT1 [R/W] 00010000	AD1CT0 [R/W] 00101100	AD1SCH [R/W] - - - 00000	AD1ECH [R/W] - - - 00000	
0005ECH	reserved				
0005F0H	reserved	ICS89 [R/W] 00000000	reserved	reserved	Input Capture 8-9
0005F4H	IPCP8 [R] XXXXXXXX XXXXXXXX		IPCP9 [R] XXXXXXXX XXXXXXXX		
0005F8H	reserved		rederved		
0005FCH - 000604H	reserved				reserved
000608H	TCDT8 [R/W] 00000000 00000000		reserved	TCCS8 [R/W] 00000000	Free Running Timer 8 (ICU 8-9)
00060CH - 00063CH	reserved				reserved

	Register				
Address	**+0**	**+1**	**+2**	**+3**	**Block**
000DA4H - 000DC4H	reserved				reserved
000DC8H	reserved		EPFR10 [R/W] - - 00 - - - 0	reserved	Extended Port Function register
000DCCH	reserved	EPFR13 [R/W] - 0 - - - 0 - -	EPFR14 [R/W] 00000000	EPFR15 [R/W] 00000000	
000DD0H	EPFR16 [R/W] 0000 - - - -	reserved	EPFR18 [R/W] - 000 - 000	EPFR19 [R/W] - 0 - - - 0 - -	
000DD4H	EPFR20 [R/W] - 000 - 000	EPFR21 [R/W] - 0 - - - 0 - -	reserved		
000DD8H	reserved		EPFR26 [R/W] 00000000	EPFR27 [R/W] 00000000	
000DDCH	reserved				
000DE0H	reserved		EPFR34 [R/W] - - 00 - - 00	EPFR35 [R/W] - - 00 - - 00	
000DE4H - 000DFCH	reserved				reserved
000E00H	PODR00 [R/W] 00000000	PODR01 [R/W] 00000000	PODR02 [R/W] 00000000	PODR03 [R/W] 00000000	Port Output Drive Strength control
000E04H	PODR04 [R/W] - - - - 0000	PODR05 [R/W] 00000000	PODR06 [R/W] 00000000	PODR07 [R/W] 00000000	
000E08H	PODR08 [R/W] 00000000	PODR09 [R/W] 00000000	PODR10 [R/W] - 0000000	PODR11 [R/W] - - - - - - 00	
000E0CH	reserved	PODR13 [R/W] 00000000	PODR14 [R/W] 00000000	PODR15 [R/W] 00000000	
000E10H	PODR16 [R/W] 00000000	PODR17 [R/W] 00000000	PODR18 [R/W] - 000 - 000	PODR19 [R/W] - 000 - 000	
000E14H	PODR20 [R/W] - 000 - 000	PODR21 [R/W] - 000 - 000	PODR22 [R/W] 00 - - 00 - -	PODR23 [R/W] - - - - 0000	
000E18H	PODR24 [R/W] 00000000	reserved	PODR26 [R/W] 00000000	PODR27 [R/W] 00000000	
000E1CH	PODR28 [R/W] 00000000	PODR29 [R/W] 00000000	reserved		
000E20H	reserved	reserved	PODR34 [R/W] - - 00 - - 00	PODR35 [R/W] - - 00 - - 00	
000E24H - 000E3CH	reserved				reserved

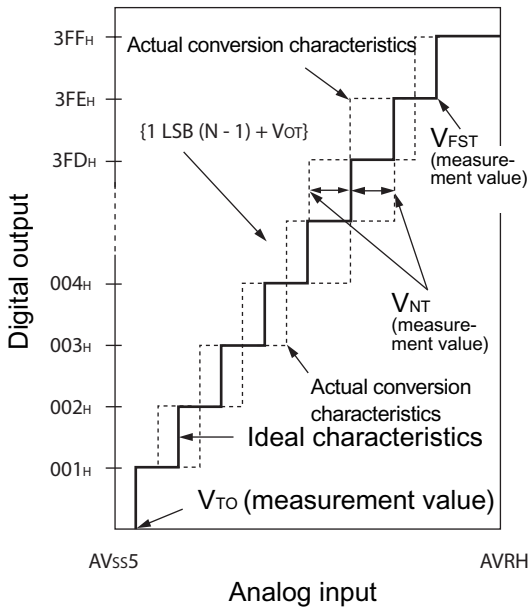
Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Permitted operating frequency MB91F469QA, MB91F469QAH	$f_{max, CLKB}$	—	100	MHz	$T_A \leq 105$ °C, main regulator set to 1.9V
	$f_{max, CLKP}$	—	50		
	$f_{max, CLKT}$	—	50		
	$f_{max, CLKCAN}$	—	50		
Permitted operating frequency MB91F469QAH	$f_{max, CLKB}$	—	96	MHz	$T_A \leq 125$ °C, main regulator set to 1.9V
	$f_{max, CLKP}$	—	48		
	$f_{max, CLKT}$	—	48		
	$f_{max, CLKCAN}$	—	48		
Permitted operating frequency MB91F469QA, MB91F469QAH	$f_{max, CLKB}$	—	88	MHz	$T_A \leq 105$ °C, main regulator set to 1.8V
	$f_{max, CLKP}$	—	44		
	$f_{max, CLKT}$	—	44		
	$f_{max, CLKCAN}$	—	44		
Permitted operating frequency MB91F469QAH	$f_{max, CLKB}$	—	84	MHz	$T_A \leq 125$ °C, main regulator set to 1.8V
	$f_{max, CLKP}$	—	42		
	$f_{max, CLKT}$	—	42		
	$f_{max, CLKCAN}$	—	42		
Permitted power consumption *7	P_D	—	2000 *8	mW	$T_A \leq 85$ °C
		—	1300 *8		$T_A \leq 105$ °C
		—	800 *8		$T_A \leq 115$ °C
		—	2000 *8		$T_A \leq 105$ °C, no Flash program/erase *9 *10
		—	1800 *8		$T_A \leq 115$ °C, no Flash program/erase *9 *10
		—	1300 *8		$T_A \leq 125$ °C, no Flash program/erase *9 *10
Operating temperature	T_A	− 40	$T_{A(max)}$	°C	For $T_{A(max)}$, refer to the ordering information
Storage temperature	Tstg	− 55	+ 150	°C	

*1 : The parameter is based on $V_{SS}5 = AV_{SS}5 = 0.0$ V.

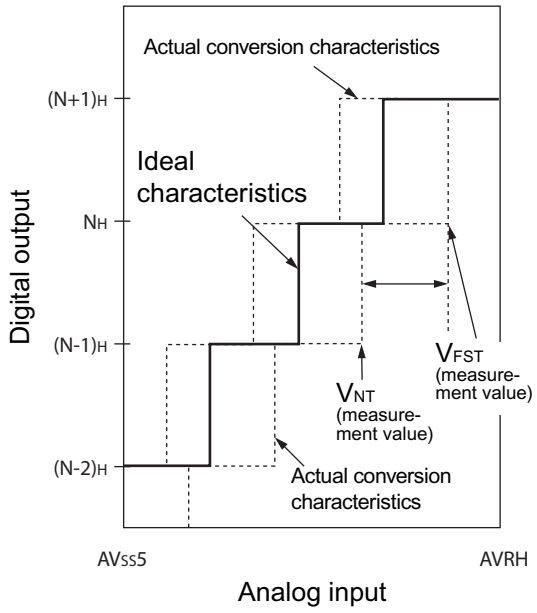
*2 : $AV_{CC}5$ and AVRH5 must not exceed $V_{DD}5 + 0.3$ V.

*3 :
- Use within recommended operating conditions.
- Use with DC voltage (current).
- +B signals are input signals that exceed the $V_{DD}5$ voltage. +B signals should always be applied by connecting a limiting resistor between the +B signal and the microcontroller.
- The value of the limiting resistor should be set so that the current input to the microcontroller pin does not exceed the rated value at any time , either instantaneously or for an extended period, when the +B signal is input.
- Note that when the microcontroller drive current is low, such as in the low power consumption modes, the +B input potential can increase the potential at the power supply pin via a protective diode, possibly affecting other devices.

Nonlinearity error



Differential nonlinearity error



$$\text{Nonlinearity error of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{OT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential nonlinearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{OT}}{1022} \text{ [V]}$$

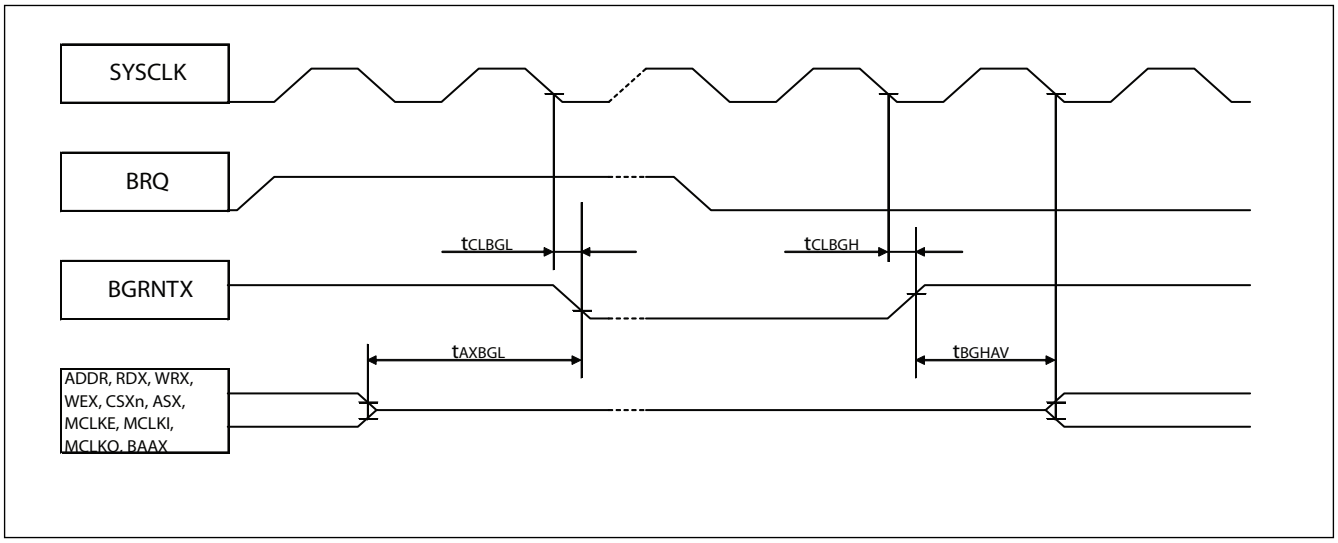
N : A/D converter digital output value
V_{OT} : Voltage at which the digital output changes from 000_H to 001_H.
V_{FST} : Voltage at which the digital output changes from $3FE_H$ to $3FF_H$.

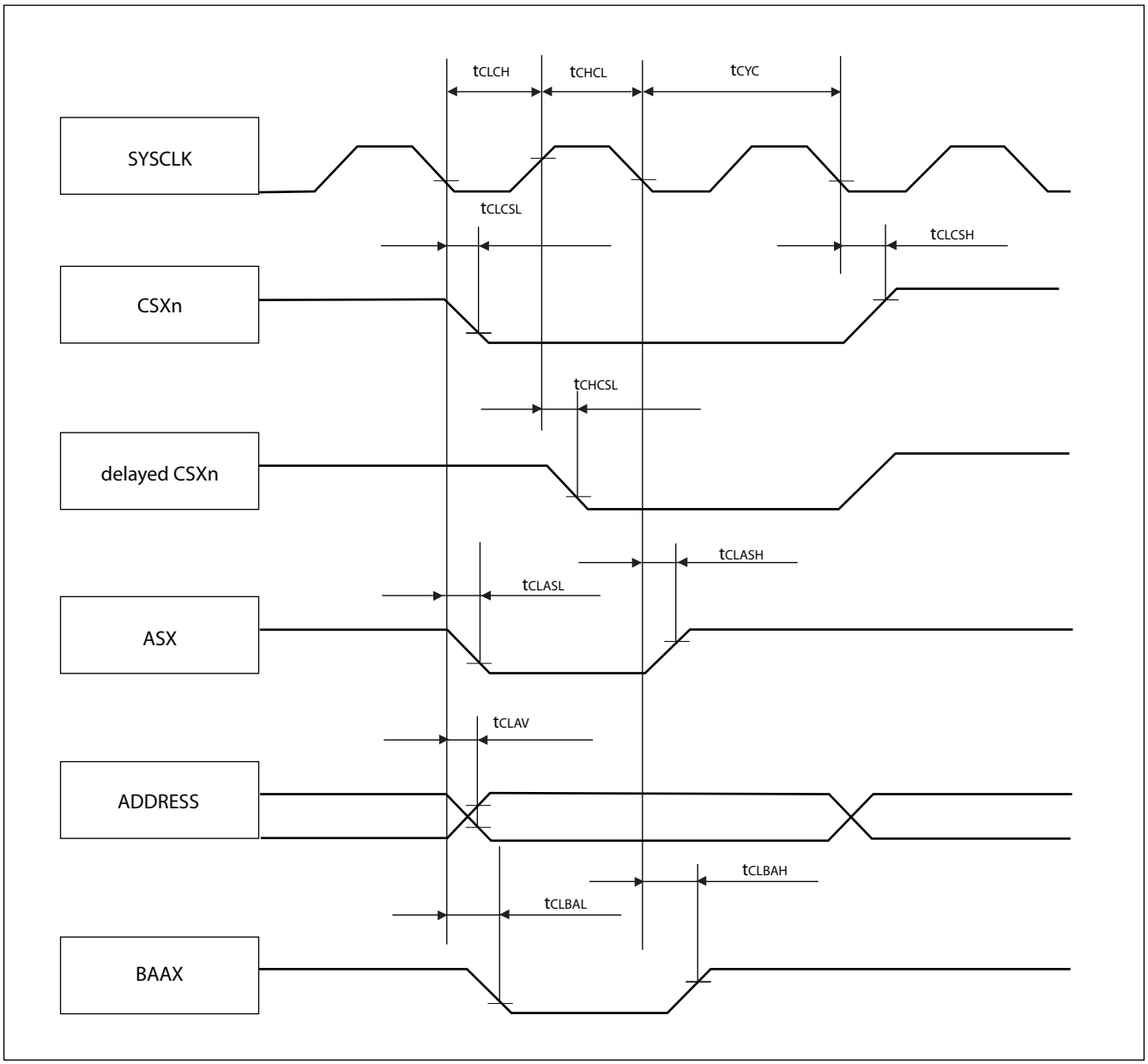
7.7.9. Bus hold timing

($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to $T_{A(max)}$)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
SYSCLK ↓ to BGRNTX delay time	t_{CLBGL}	SYSCLK BGRNTX	—	5	ns
	t_{CLBGH}		—	5	ns
Bus HIZ to BGRNTX ↓	t_{AXBGL}	BGRNTX MCLK* A0 to An RDX, ASX WRXn,WEX CSXn,BAAX	t_{CLKT} + 2	—	ns
BGRNTX ↑ to Bus drive	t_{BGHAV}		t_{CLKT} + 1	—	ns

Note : BRQ must be kept High until the bus is granted (this is acknowledged by the falling edge of BGRNTX).
It must be kept High as long as the bus shall be hold.
After releasing the bus (BRQ set to Low) this is acknowledged by the rising edge of BGRNTX.

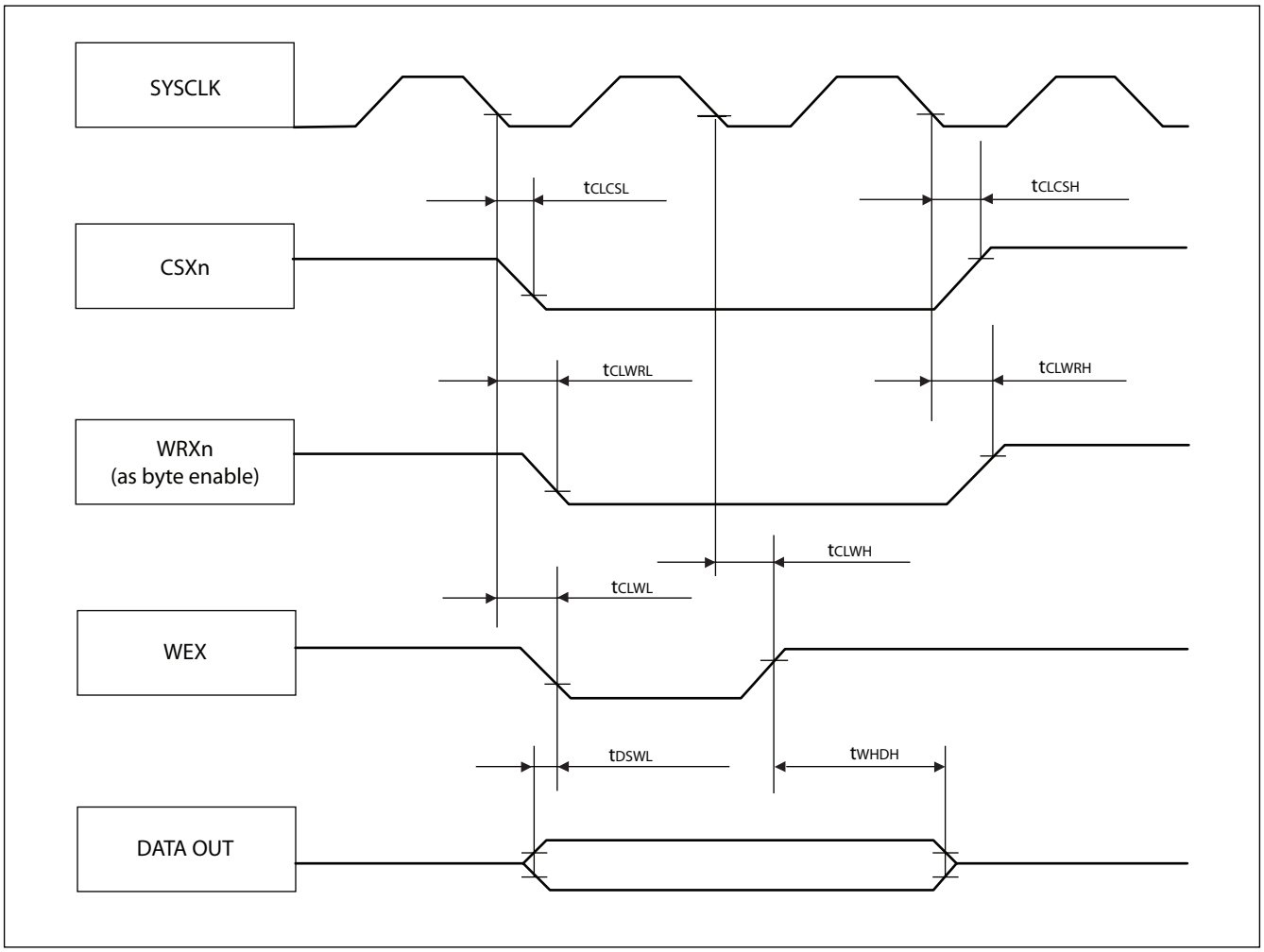



tCLCH
tCHCL
tCYC
SYSCLK
tCLCSL
tCLCSH
CSXn
tCHCSL
delayed CSXn
tCLASH
tCLASL
ASX
tCLAV
ADDRESS
tCLBAH
tCLBAL
BAAX

7.8.4. Synchronous write access - byte control type

($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to $T_{A(max)}$)

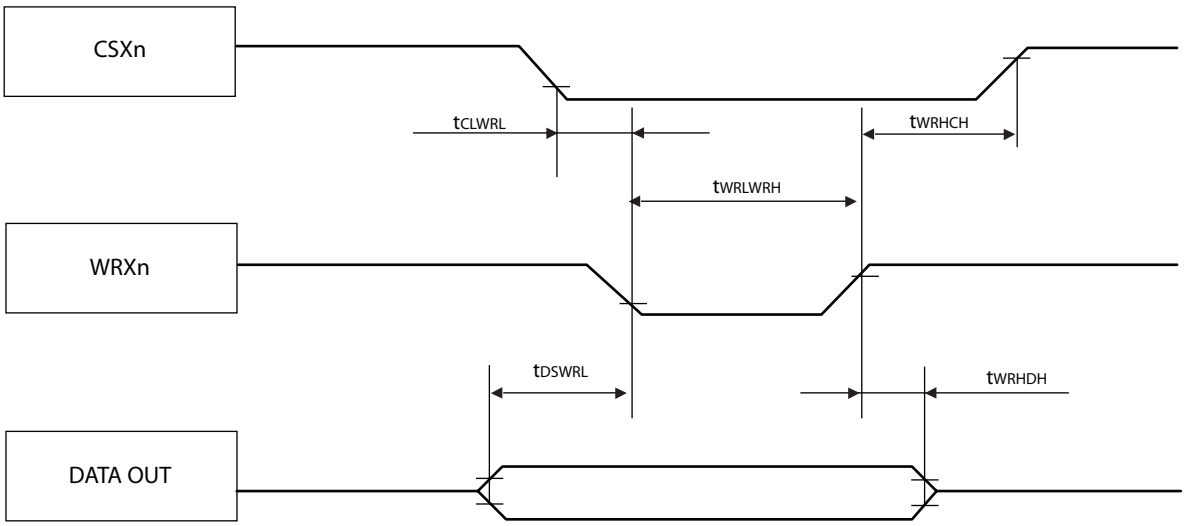
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
SYSCLK ↓ to WEX delay time	t_{CLWL}	SYSCLK WEX	—	5	ns
	t_{CLWH}		- 1	—	ns
Data valid to WEX ↓ setup time	t_{DSWL}	WEX D31 to D0	– 11	—	ns
WEX ↑ to Data valid hold time	t_{WHDH}	WEX D31 to D0	t_{CLKT} – 13	—	ns
SYSCLK ↓ to WRXn (as byte enable) delay time	t_{CLWRL}	SYSCLK WRXn	—	5	ns
	t_{CLWRH}		- 1	—	ns
SYSCLK ↓ to CSXn delay time	t_{CLCSL}	SYSCLK CSXn	—	5	ns
	t_{CLCSH}		—	6	ns



7.8.7. Asynchronous write access - no byte control type

($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to $T_{A(max)}$)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
WRXn ↓ to WRXn ↑ pulse width	t_{WRLWRH}	WRXn	t_{CLKT} – 3	—	ns
Data valid to WRXn ↓ setup time	t_{DSWRL}	WRXn D31 to D0	1/2 × t_{CLKT} – 12	—	ns
WRXn ↑ to Data valid hold time	t_{WRHDH}	WRXn D31 to D0	1/2 × t_{CLKT} – 11	—	ns
WRXn to CSXn delay time	t_{CLWRL}	WRXn CSXn	—	1/2 × t_{CLKT} – 1	ns
	t_{WRHCH}		1/2 × t_{CLKT} + 1	—	ns



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