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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	1.1V, 1.3V
Operating Temperature	-40°C ~ 110°C (TJ)
Security Features	-
Package / Case	360-BCBGA
Supplier Device Package	360-HiTCE-CBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pcx7447avgh1000nb

  - Address translation for 4-Kbyte pages, variable-sized blocks, and 256-Mbyte segments
  - Memory programmable as write-back/write-through, caching-inhibited/caching-allowed, and memory coherency enforced/memory coherency not enforced on a page or block basis
  - Separate IBATs and DBATs (eight each) also defined as SPRs
  - Separate instruction and data translation look aside buffers (TLBs)

    Both TLBs are 128-entry, two-way set-associative, and use a LRU replacement algorithm

    TLBs are hardware- or software-reloadable (that is, a page table search is performed in hardware or by system software on a TLB miss).
- Efficient data flow
  - Although the VR/LSU interface is 128 bits, the L1/L2 bus interface allows up to 256 bits
  - The L1 data cache is fully pipelined to provide 128 bits/cycle to or from the VRs
  - L2 cache is fully pipelined to provide 256 bits per processor clock cycle to the L1 cache
  - As many as eight outstanding, out-of-order, cache misses are allowed between the L1 data cache and the L2 bus
  - As many as 16 out-of-order transactions can be present on the MPX bus
  - Store merging for multiple store misses to the same line. Only coherency action taken (address-only) for store misses merged to all 32 bytes of a cache block (no data tenure needed)
  - Three-entry finished store queue and five-entry completed store queue between the LSU and the L1 data cache
  - Separate additional queues for efficient buffering of outbound data (such as castouts and write-through stores) from the L1 data cache and L2 cache
- Multiprocessing support features include the following:
  - Hardware-enforced, MESI cache coherency protocols for data cache
  - Load/store with reservation instruction pair for atomic memory references, semaphores, and other multiprocessor operations
- Power and thermal management
  - A new dynamic frequency switching (DFS) feature allows the processor core frequency to be halved through software to reduce power consumption
  - The following three power-saving modes are available to the system:

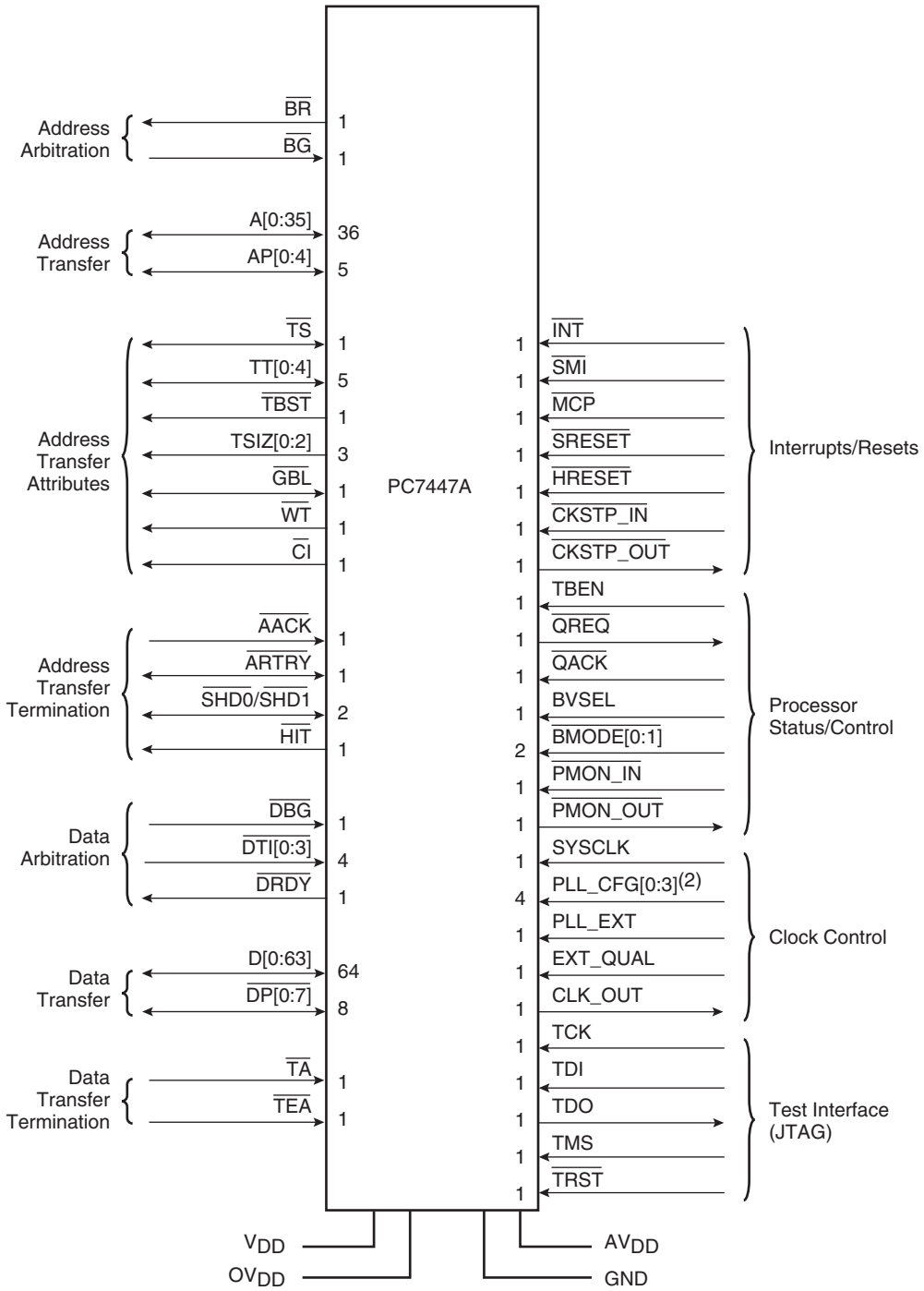
    Nap: Instruction fetching is halted. Only the clocks for the time base, decrementer, and JTAG logic remain running. The part goes into the doze state to snoop memory operations on the bus and then back to nap using a QREQ/QACK processor-system handshake protocol.

    Sleep: Power consumption is further reduced by disabling bus snooping, leaving only the PLL in a locked and running state. All internal functional units are disabled.

    Deep sleep: When the part is in the deep Sleep state, the system can disable the PLL. The system can then disable the SYSCLK source for greater system power savings. Power-on reset procedures for restarting and relocking the PLL must be followed upon exiting the deep sleep state.

4. Signal Description

Figure 4-1. PC7447A Microprocessor Signal Groups



Note: For the PC7447A, there are 5 PLL_CFG signals, (PLL_CFG[0:4]

5. Detailed Specification

This specification describes the specific requirements for the microprocessor PC7447A in compliance with e2v standard screening.

6. Applicable Documents

1. MIL-STD-883: Test methods and procedures for electronics
2. MIL-PRF-38535: Appendix A: General specifications for microcircuits

The microcircuits are in accordance with the applicable documents and as specified herein.

6.1 Design and Construction

6.1.1 Terminal Connections

Depending on the package, the terminal connections are as shown in Table 8-1, Table 6-2 and Figure 4-1.

6.2 Absolute Maximum Ratings

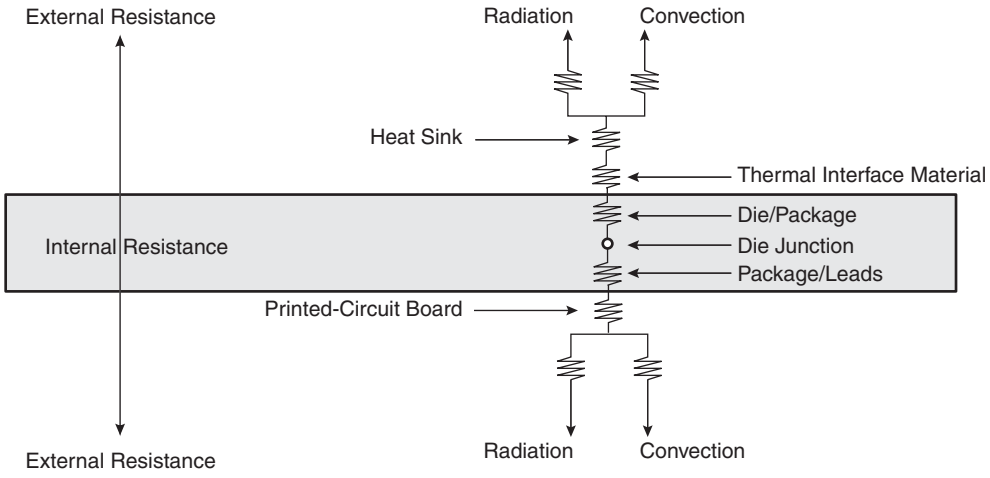
The tables in this section describe the PC7447A DC electrical characteristics. Table 6-1 provides the absolute maximum ratings.

Table 6-1. Absolute Maximum Ratings(1)

Symbol	Characteristic		Maximum Value	Unit
V_{DD}(2)	Core supply voltage		-0.3 to 1.60	V
AV_{DD}(2)	PLL supply voltage		-0.3 to 1.60	V
OV_{DD}(3)(4)	Processor bus supply voltage	BVSEL = 0	-0.3 to 1.95	V
OV_{DD}(3)(5)		BVSEL = $\overline{\text{HRESET}}$ or OV_{DD}	-0.3 to 2.7	V
V_{IN}(6)(7)	Input voltage	Processor bus	-0.3 to OV_{DD} + 0.3	V
V_{IN}		JTAG signals	-0.3 to OV_{DD} + 0.3	V
T_{STG}	Storage temperature range		-55 to 150	°C

Notes:
1. Functional and tested operating conditions are given in Table 6-2 on page 10. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. Caution: V_{DD}/AV_{DD} must not exceed OV_{DD} by more than 1V during normal operation; this limit may be exceeded for a maximum of 20 ms during the power-on reset and power-down sequences.
3. Caution: OV_{DD} must not exceed V_{DD}/AV_{DD} by more than 2V during normal operation; this limit may be exceeded for a maximum of 20 ms during the power-on reset and power-down sequences.
4. BVSEL must be set to 0, such that the bus is in 1.8V mode.
5. BVSEL must be set to HRESET or 1, such that the bus is in 2.5V mode.
6. Caution: V_{IN} must not exceed OV_{DD} by more than 0.3V at any time including during power-on reset.
7. V_{IN} may overshoot/undershoot to a voltage and for a maximum duration shown in Figure 6-1 on page 10.

Figure 6-2. C4 Package with Heat Sink Mounted to a Printed-Circuit Board



Note the internal versus external package resistance.

Heat generated on the active side of the chip is conducted through the silicon, through the heat sink attach material (or thermal interface material), and finally to the heat sink where it is removed by forced-air convection.

Because the silicon thermal resistance is quite small, the temperature drop in the silicon may be neglected for a first-order analysis. Thus, the thermal interface material and the heat sink conduction/convective thermal resistances are the dominant terms.

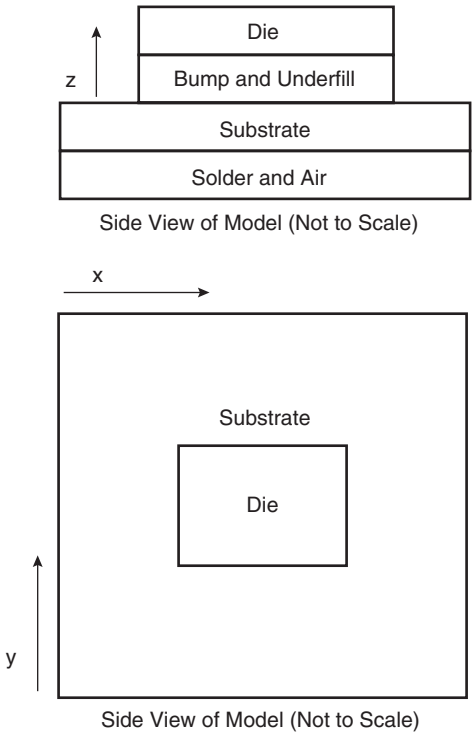
6.4.3 Thermal Management Information

This section provides thermal management information for the high coefficient of the thermal expansion ceramic ball grid array (HITCE) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design – the heat sink, airflow, and thermal interface material. The PC7447A implements several features designed to assist with thermal management, including DFS and the temperature diode. DFS reduces the power consumption of the device by reducing the core frequency; see Table 6-6 on page 19 for specific information regarding power reduction and DFS. The temperature diode allows an external device to monitor the die temperature in order to detect excessive temperature conditions and alert the system; see section “Temperature Diode” on page 16 for more information.

To reduce the die-junction temperature, heat sinks may be attached to the package by several methods – spring clips to holes in the printed-circuit board or package, and mounting clips and screw assembly (see Figure 6-3); however, due to the potentially large mass of the heat sink, attachment through the printed-circuit board is suggested. If a spring clip is used, the spring force should not exceed ten pounds.

Figure 6-5. Recommended Thermal Model of PC7447A

Conductivity	Value	Unit
Bump and Underfill (7.3 x 9.3 x 0.070 mm)		
k_x	0.6	W/(m x K)
k_y	0.6	
k_z	1.9	
Substrate (25 x 25 x 1.2 mm)		
k_x	8.1	
k_y	8.1	
k_z	4.0	
Solder Ball and Air (25 x 25 x 0.6 mm)		
k_x	0.034	
k_y	0.034	
k_z	3.8	



6.4.4.2 Temperature Diode

The PC7447A has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices. These devices use the negative temperature coefficient of a diode operated at a constant current to determine the temperature of the microprocessor and its environment. For proper operation, the monitoring device used should auto-calibrate the device by canceling out the V_{BE} variation of each PC7447A's internal diode.

The following are the specifications of the PC7447A on-board temperature diode:

$V_f > 0.40V$

$V_f < 0.90V$

Operating range 2 - 300 µA

Diode leakage < 10 nA at 125°C

Ideality factor over 5 µA – 150 µA at 60°C: 1 <= n <= TBD

Ideality factor is defined as the deviation from the ideal diode equation:

$$I_{fW} = I_s\left[e^{\frac{qV_f}{nKT}} - 1\right]$$

Another useful equation is:

$$V_H - V_L = n\frac{KT}{q}\left[In\frac{I_H}{I_L}\right]$$

6.4.4.5 *Bus-to-Core Multiplier Constraints with DFS*

DFS is not available for all bus-to-core multipliers as configured by PLL_CFG[0:4] during hard reset. Specifically, because the PC7447A does not support quarter clock ratios or the 1x multiplier, the DFS feature is limited to integer PLL multipliers of 4x and higher. The complete listing is shown in Table 6-5 on page 18.

Table 6-5. Valid Divide Ratio Configurations

Bus-to-Core Multiplier Configured by PLL_CFG[0:4] (see Table 12-1 on page 39)	Bus-to-Core Multiplier with HID1[DFS1] = 1 (÷2)
2x	N/A
3x	N/A
4x	2x
5x	2.5x
5.5x	2x
6x	3x
6.5x	N/A
7x	3.5x
7.5x	N/A
8x	4x
8.5x	N/A
9x	4.5x
9.5x	N/A
10x	5x
10.5x	N/A
11x	5.5x
11.5x	N/A
12x	6x
12.5x	N/A
13x	6.5x
13.5x	N/A
14x	7x
15x	7.5x
16x	8x
17x	8.5x
18x	9x
20x	10x
21x	10.5x
24x	12x
28x	14x

Table 8-1. Pinout Listing for the PC7447A, 360 HITCE Package (Continued)

Signal Name	Pin Number	Active	I/O	I/F Select[1]
GND	B5, C3, D6, D13, E17, F3, G17, H4, H7, H9, H11, H13, J6, J8, J10, J12, K7, K3, K9, K11, K13, L6, L8, L10, L12, M4, M7, M9, M11, M13, N7, P3, P9, P12, R5, R14, R17, T7, T10, U3, U13, U17, V5, V8, V11, V15	–	–	N/A
GND[15]	A17, A19, B13, B16, B18, E12, E19, F13, F16, F18, G19, H18, J14, L14, M15, M17, M19, N14, N16, P15, P19	–	–	N/A
GND_SENSE[19]	G12, N13	–	–	N/A
$\overline{\text{HIT}}$[7]	B2	Low	Output	BVSEL
$\overline{\text{HRESET}}$	D8	Low	Input	BVSEL
$\overline{\text{INT}}$	D4	Low	Input	BVSEL
L1_TSTCLK[9]	G8	High	Input	BVSEL
L2_TSTCLK[10]	B3	High	Input	BVSEL
No Connect[11]	A6, A14, A15, B14, B15, C14, C15, C16, C17, C18, C19, D14, D15, D16, D17, D18, D19, E14, E15, F14, F15, G14, G15, H15, H16, J15, J16, J17, J18, J19, K15, K16, K17, K18, K19, L15, L16, L17, L18, L19	–	–	–
$\overline{\text{LSSD\_MODE}}$[6][12]	E8	Low	Input	BVSEL
$\overline{\text{MCP}}$	C9	Low	Input	BVSEL
OV_{DD}	B4, C2, C12, D5, F2, H3, J5, K2, L5, M3, N6, P2, P8, P11, R4, R13, R16, T6, T9, U2, U12, U16, V4, V7, V10, V14	–	–	N/A
OV_{DD}_SENSE[16]	E18, G18	–	–	N/A
PLL_CFG[0:4]	B8, C8, C7, D7, A7	High	Input	BVSEL
$\overline{\text{PMON\_IN}}$[13]	D9	Low	Input	BVSEL
$\overline{\text{PMON\_OUT}}$	A9	Low	Output	BVSEL
$\overline{\text{QACK}}$	G5	Low	Input	BVSEL
$\overline{\text{QREQ}}$	P4	Low	Output	BVSEL
$\overline{\text{SHD}}$[0:1][3]	E4, H5	Low	I/O	BVSEL
$\overline{\text{SMI}}$	F9	Low	Input	BVSEL
$\overline{\text{SRESET}}$	A2	Low	Input	BVSEL
SYSCLK	A10	–	Input	BVSEL
$\overline{\text{TA}}$	K6	Low	Input	BVSEL
TBEN	E1	High	Input	BVSEL
$\overline{\text{TBST}}$	F11	Low	Output	BVSEL
TCK	C6	High	Input	BVSEL
TDI[6]	B9	High	Input	BVSEL
TDO	A4	High	Output	BVSEL
$\overline{\text{TEA}}$	L1	Low	Input	BVSEL
TEMP_ANODE[17]	N18			
TEMP_CATHODE[17]	N19			

18. These pins are internally connected to V_{DD} and are intended to allow an external device to detect the processor core voltage level present inside the device package. If unused, they must be connected directly to V_{DD} or left unconnected.
19. These pins are internally connected to GND and are intended to allow an external device to detect the processor ground voltage level present inside the device package. If unused, they must be connected directly to GND or left unconnected.

Note: Caution must be exercised when performing boundary scan test operations on a board designed for a PC7447A but populated with an PC7447. This is because in the PC7447 it is possible to drive the latches associated with the former 'No Connect' pins in the PC7447, potentially causing contention on those pins. To prevent this, ensure that these pins are not connected on the board or, if they are connected, ensure that the states of internal PC7447 latches do not cause these pins to be driven during board testing.

9. Electrical Characteristics

9.1 Static Characteristics

Table 9-1 provides the DC electrical characteristics for the PC7447A.

Table 9-1. DC Electrical Specifications (see Table 6-2 on page 10 for Recommended Operating Conditions)

Symbol	Characteristic	Nominal Bus Voltage(1)	Min	Max	Unit	Notes
V_{IH}	Input high voltage (all inputs)	1.8	$OV_{DD} \times 0.65$	$OV_{DD} + 0.3$	V	(2)
		2.5	1.7	$OV_{DD} + 0.3$		
V_{IL}	Input low voltage (all inputs)	1.8	-0.3	$OV_{DD} \times 0.35$	V	(2)(6)
		2.5	-0.3	0.7		
I_{IN}	Input leakage current, $V_{IN} = GV_{DD}/O_{DD}$ V_{IN} = GND	–	–	30 -30	µA	(2)(3)
I_{TSI}	High-impedance (off-state) leakage current, $V_{IN} = GV_{DD}/O_{DD}$ V_{IN} = GND	–	–	30 -30	µA	(2)(3)(4)
V_{OH}	Output high voltage at I_{OH} = -5 mA	1.8	OV_{DD} - 0.45	–	V	
		2.5	1.8	–		
V_{OL}	Output low voltage at I_{OL} = 5 mA	1.8	–	0.45	V	
		2.5	–	0.6		
C_{IN}	Capacitance, V_{IN} = 0V f = 1 MHz — All other inputs		–	8	pF	(5)
V_{IH}	Input high voltage (all inputs)	1.8	$OV_{DD} \times 0.65$	$OV_{DD} + 0.3$	V	(2)
		2.5	1.7	$OV_{DD} + 0.3$		
V_{IL}	Input low voltage (all inputs)	1.8	-0.3	$OV_{DD} \times 0.35$	V	(2)(6)
		2.5	-0.3	0.7		
I_{IN}	Input leakge current, $V_{IN} = GV_{DD}/OV_{DD}$ V_{IN} = GND	–	–	30 -30	µA	(2)(3)

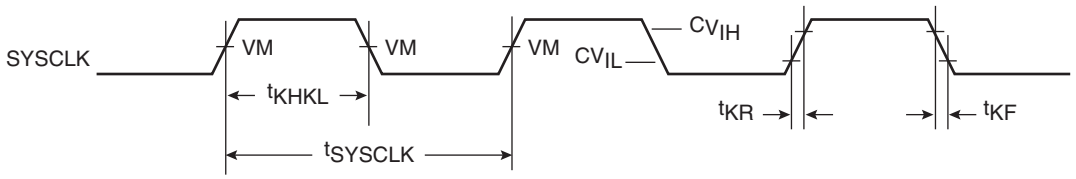
Notes: 1. Nominal voltages; see Table 6-2 on page 10 for recommended operating conditions.
2. For processor bus signals, the reference is OV_{DD} while GV_{DD} is the reference for the L3 bus signals.

Symbol	Characteristic	Maximum Processor Core Frequency				Unit	Notes
		1000 MHz		1167 MHz			
		V_{DD} = 1.1V		V_{DD} = 1.1V			
		Min	Max	Min	Max		
f_{CORE}	Processor core frequency	500	1000	500	1167	MHz	(1)(8)(9)
f_{VCO}	VCO frequency	1000	2000	1000	2233	MHz	(1)(9)
f_{SYSCLK}	SYSCLK frequency	33	167	33	167	MHz	(1)(2)(8)
t_{SYSCLK}	SYSCLK cycle time	6	30	6	30	ns	(2)
t_{KR}, t_{KF}	SYSCLK rise and fall time	–	1	–	1	ns	(3)
t_{KHKL}/t_{SYSCLK}	SYSCLK duty cycle measured at $OV_{DD}/2$	40	60	40	60	%	(4)
	SYSCLK jitter(5)(6)	–	150	–	150	ps	(5)(6)
	Internal PLL relock time(7)	–	100	–	100	µs	(7)

Notes:
1. Caution: The SYSCLK frequency and PLL_CFG[0:4] settings must be chosen such that the resulting SYSCLK (bus) frequency, processor core frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0:4] signal description in Section "PLL Configuration" on page 38 for valid PLL_CFG[0:4] settings.
2. Assumes a lightly-loaded, single-processor system.
3. Rise and fall times for the SYSCLK input measured from 0.4V to 1.4V.
4. Timing is guaranteed by design and characterization.
5. Guaranteed by design.
6. The SYSCLK driver's closed loop jitter bandwidth should be less than 1.5 MHz at -3 dB.
7. Relock timing is guaranteed by design and characterization. PLL relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL relock time during the power-on reset sequence.
8. Caution: If DFS is enabled, the SYSCLK frequency and PLL_CFG[0:4] settings must be chosen such that the resulting processor frequency is greater than or equal to the minimum core frequency.
9. Caution: These values specify the maximum processor core and VCO frequencies when the device is operated at the nominal core voltage. If operating the device at the derated core voltage, the processor core and VCO frequencies must be reduced.

Figure 9-1 provides the SYSCLK input timing diagram.

Figure 9-1. SYSCLK Input Timing Diagram

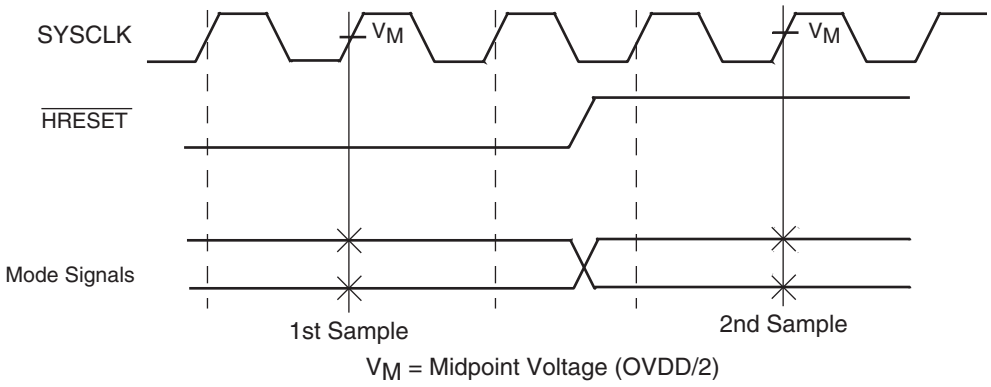


V_M = Midpoint Voltage ($OV_{DD}/2$)

2. The symbology used for timing specifications herein follows the pattern of $t_{(signal)(state)(reference)(state)}$ for inputs and $t_{(reference)(state)(signal)(state)}$ for outputs. For example, t_{IVKH} symbolizes the time input signals (I) reach the valid state (V) relative to the SYSCLK reference (K) going to the high (H) state or input setup time. And t_{KHOV} symbolizes the time from SYSCLK (K) going high (H) until outputs (O) are valid (V) or output valid time. Input hold time can be read as the time that the input signal (I) went invalid (X) with respect to the rising clock edge (KH) (note the position of the reference and its state for inputs) and output hold time can be read as the time from the rising edge (KH) until the output went invalid (OX).
3. t_{SYSCLK} is the period of the external clock (SYSCLK) in ns. The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
4. According to the bus protocol, $\overline{TS}$ is driven only by the currently active bus master. It is asserted low and precharged high before returning to high impedance, as shown in Figure 9-3 on page 29. The nominal precharge width for $\overline{TS}$ is $0.5 \times t_{SYSCLK}$, that is, less than the minimum t_{SYSCLK} period, to ensure that another master asserting $\overline{TS}$ on the following clock will not contend with the precharge. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge.The high-impedance behavior is guaranteed by design.
5. Guaranteed by design and not tested.
6. According to the bus protocol, $\overline{ARTRY}$ can be driven by multiple bus masters through the clock period immediately following $\overline{AACK}$. Bus contention is not an issue because any master asserting $\overline{ARTRY}$ will be driving it low. Any master asserting it low in the first clock following $\overline{AACK}$ will then go to high impedance for 1 clock before precharging it high during the second cycle after the assertion of $\overline{AACK}$. The nominal precharge width for $\overline{ARTRY}$ is 1.0 t_{SYSCLK}; that is, it should be high impedance as shown in Figure 9-3 on page 29 before the first opportunity for another master to assert $\overline{ARTRY}$. Output valid and output hold timing is tested for the signal asserted.The high-impedance behavior is guaranteed by design.
7. According to the MPX bus protocol, $\overline{SHD0}$ and $\overline{SHD1}$ can be driven by multiple bus masters beginning the cycle of $\overline{TS}$. Timing is the same as $\overline{ARTRY}$, that is, the signal is high impedance for a fraction of a cycle, then negated for up to an entire cycle (crossing a bus cycle boundary) before being three-stated again. The nominal precharge width for $\overline{SHD0}$ and $\overline{SHD1}$ is 1.0 t_{SYSCLK}. The edges of the precharge vary depending on the programmed ratio of core to bus (PLL configurations).
8. $\overline{BMODE}$[0:1] and BVSEL are mode select inputs and are sampled before and after $\overline{HRESET}$ negation. These parameters represent the input setup and hold times for each sample. These values are guaranteed by design and not tested. These inputs must remain stable after the second sample. See Figure 9-2 on page 28 for sample timing.

Figure 9-2 provides the mode select input timing diagram for the PC7447A. The mode select inputs are sampled twice, once before and once after $\overline{HRESET}$ negation.

Figure 9-2. Mode Input Sample Timing Diagram



9.2.3 IEEE 1149.1 AC Timing Specifications

Table 9-4 provides the IEEE 1149.1 (JTAG) AC timing specifications as defined in Figure 9-5 through Figure 9-8 on page 32.

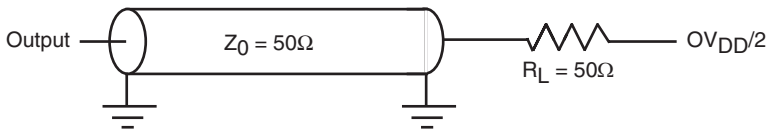
Table 9-4. JTAG AC Timing Specifications (Independent of SYSCLK)(1) at Recommended Operating Conditions (see Table 6-2 on page 10)

Symbol	Parameter	Min	Max	Unit
f_{TCLK}	TCK frequency of operation	0	33.3	MHz
t_{TCLK}	TCK cycle time	30	–	ns
t_{JHJL}	TCK clock pulse width measured at 1.4V	15	–	ns
t_{JR} and t_{JF}	TCK rise and fall times	–	2	ns
t_{TRST}(2)	$\overline{TRST}$ assert time	25	–	ns
t_{DVJH}(3) t_{IVJH}	Input Setup Times: Boundary-scan data TMS, TDI	 4 0	 – –	ns
t_{DXJH}(3) t_{IXJH}	Input Hold Times: Boundary-scan data TMS, TDI	 20 25	 – –	ns
t_{JLDV}(4) t_{JLOV}	Valid Times: Boundary-scan data TDO	 4 4	 20 25	ns
t_{JLDX}(4) t_{JLOX}	Output hold times: Boundary-scan data TDO	 30 30	 – –	
t_{JLDZ}(4)(5) t_{JLOZ}	TCK to output high impedance: Boundary-scan data TDO	 3 3	 19 9	ns

Notes:
1. All outputs are measured from the midpoint voltage of the falling/rising edge of TCLK to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50Ω load (see Figure 9-4). Time-of-flight delays must be added for trace lengths, vias and connectors in the system.
2. $\overline{TRST}$ is an asynchronous level sensitive signal. The time is for test purposes only.
3. Non-JTAG signal input timing with respect to TCK.
4. Non-JTAG signal output timing with respect to TCK.
5. Guaranteed by design and characterization.

Figure 9-4 provides the AC test load for TDO and the boundary-scan outputs of the PC7457.

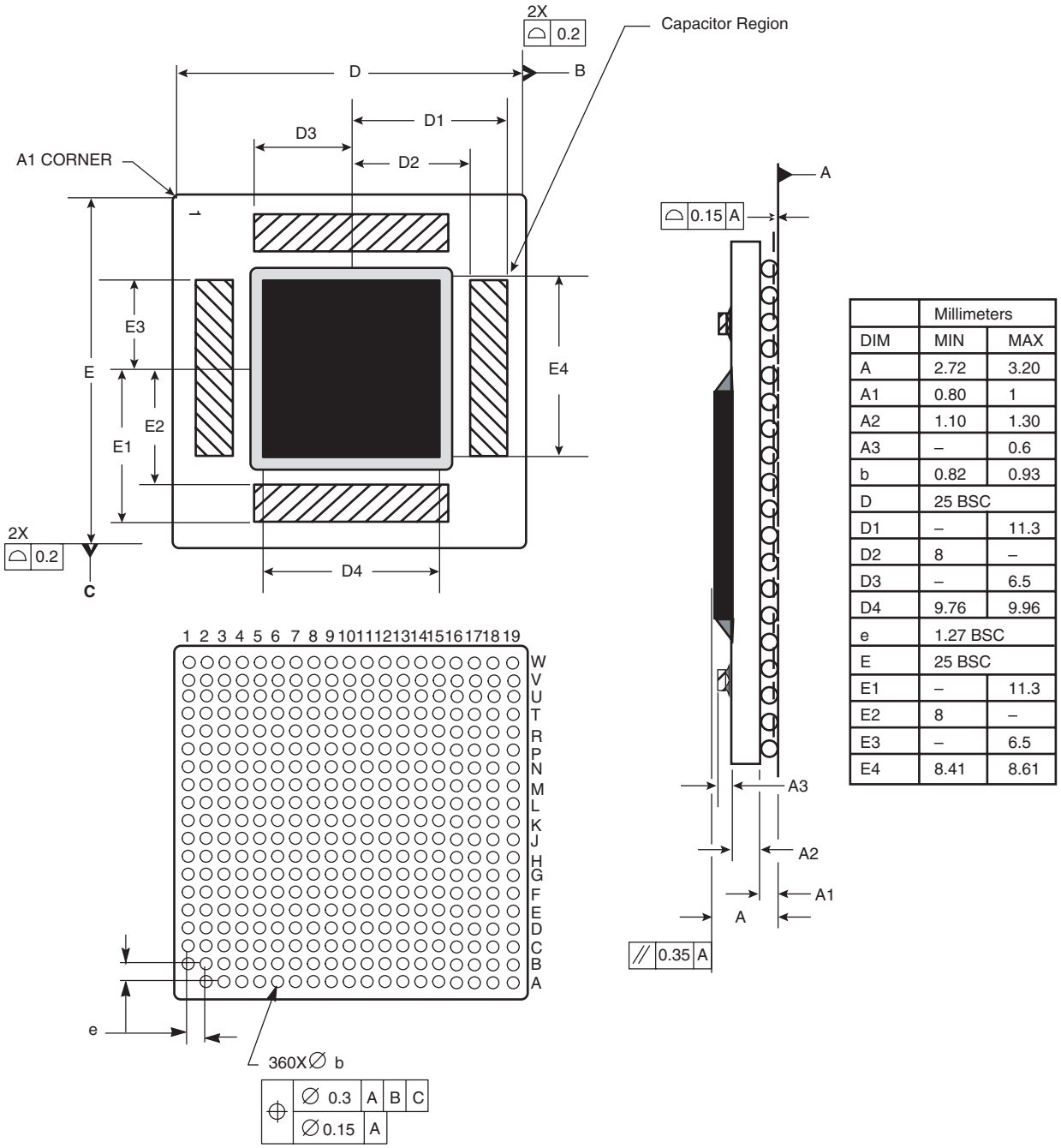
Figure 9-4. Alternate AC Test Load for the JTAG Interface



11.2 Mechanical Dimensions for the PC7447A, 360 HITCE

Figure 11-1 provides the mechanical dimensions and bottom surface nomenclature for the PC7447A, 360 HITCE package.

Figure 11-1. Mechanical Dimensions and Bottom Surface Nomenclature for the PC7447A, 360 CBGA Package



	Millimeters	
DIM	MIN	MAX
A	2.72	3.20
A1	0.80	1
A2	1.10	1.30
A3	–	0.6
b	0.82	0.93
D	25 BSC	
D1	–	11.3
D2	8	–
D3	–	6.5
D4	9.76	9.96
e	1.27 BSC	
E	25 BSC	
E1	–	11.3
E2	8	–
E3	–	6.5
E4	8.41	8.61

Notes:
1. Dimensioning and tolerance per ASME Y14.5M, 1994
2. Dimensions in millimeters
3. Top side A1 corner index is a metallized feature with various shapes. Bottom side A1 corner is designated with a ball missing from the array

11.3 Package Parameters for the PC7447A, 360 HITCE RoHS-Compliant BGA

The package parameters are as provided in the following list. The package type is 25 × 25 mm, 360 lead-free high coefficient of thermal expansion ceramic ball grid array (HITCE).

Package outline	25 mm × 25 mm
Interconnects	360 (19 × 19 ball array - 1)
Pitch	1.27 mm (50 mil)
Minimum module height	2.32 mm
Maximum module height	2.80 mm
Ball diameter	0.89 mm (35 mil)
Coefficient of thermal expansion	12.3 ppm/°C

11.5 Package Parameters for the PC7447A, 360 HCTE LGA

The package parameters are as provided in the following list. The package type is 25 × 25 mm, 360 high coefficient of thermal expansion ceramic land grid array (HCTE).

Package outline	25 mm × 25 mm
Interconnects	360 (19 × 19 ball array - 1)
Pitch	1.27 mm (50 mil)
Minimum module height	1.92 mm
Maximum module height	2.20 mm
Coefficient of thermal expansion	12.3 ppm/°C

Table 12-1. PC7447A Microprocessor PLL Configuration Example for 1420-MHz Parts (Continued)

PLL_CFG[0:4]	Example Bus-to-Core Frequency in MHz (VCO Frequency in MHz)									
	Bus-to-Core Multiplier	Core-to-VCO Multiplier	Bus (SYSCLK) Frequency							
			33.33 MHz	50 MHz	66.66 MHz	75 MHz	83 MHz	100 MHz	133.33 MHz	166.66 MHz
11111	12.5x	2x		600 (1200)	833 (1666)	938 (1876)	1038 (2076)	1250 (2500)		
01011	13x	2x		650 (1300)	865 (1730)	975 (1950)	1079 (2158)	1300 (2600)		
11100	13.5x	2x		675 (1350)	900 (1800)	1013 (2026)	1121 (2242)	1350 (2700)		
11001	14x	2x		700 (1400)	933 (1866)	1050 (2100)	1162 (2324)	1400 (2800)		
00011	15x	2x		750 (1500)	1000 (2000)	1125 (2250)	1245 (2490)			
11011	16x	2x		800 (1600)	1066 (2132)	1200 (2400)	1328 (2656)			
00001	17x	2x		850 (1900)	1132 (2264)	1275 (2550)	1411 (2822)			
00101	18x	2x	600 (1200)	900 (1800)	1200 (2400)	1350 (2700)				
00111	20x	2x	667 (1334)	1000 (2000)	1332 (2664)					
01001	21x	2x	700 (1400)	1050 (2100)	1399 (2797)					
01101	24x	2x	800 (1600)	1200 (2400)						
11101	28x	2x	933 (1866)	1400 (2800)						
00110	PLL bypass		PLL off, SYSCLK clocks core circuitry directly							
11110	PLL off		PLL off, no core clocking occurs							

Notes:
1. PLL_CFG[0:4] settings not listed are reserved.
2. The sample bus-to-core frequencies shown are for reference only. Some PLL configurations may select bus, core, or VCO frequencies that are not useful, not supported, or not tested for by the PC7455; see Section "Clock AC Specifications" on page 25 for valid SYSCLK, core, and VCO frequencies.
3. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly and the PLL is disabled. However, the bus interface unit requires a 2x clock to function. Therefore, an additional signal, EXT_QUAL, must be driven at one-half the frequency of SYSCLK and offset in phase to meet the required input setup tIVKH and hold time tIXKH (see Table 9-3 on page 27). The result will be that the processor bus frequency will be one-half SYSCLK while the internal processor is clocked at SYSCLK frequency. This mode is intended for factory use and emulator tool use only.
   Note: The AC timing specifications given in this document do not apply in PLL-bypass mode.
4. In PLL-off mode, no clocking occurs inside the PC7447A regardless of the SYSCLK input.

12.6 Pull-up/Pull-down Resistor Requirements

The PC7447A requires high-resistive (weak: 4.7-KΩ) pull-up resistors on several control pins of the bus interface to maintain the control signals in the negated state after they have been actively negated and released by the PC7447A or other bus masters. These pins are: $\overline{TS}$, $\overline{ARTRY}$, $\overline{SHDO}$, and $\overline{SHD1}$.

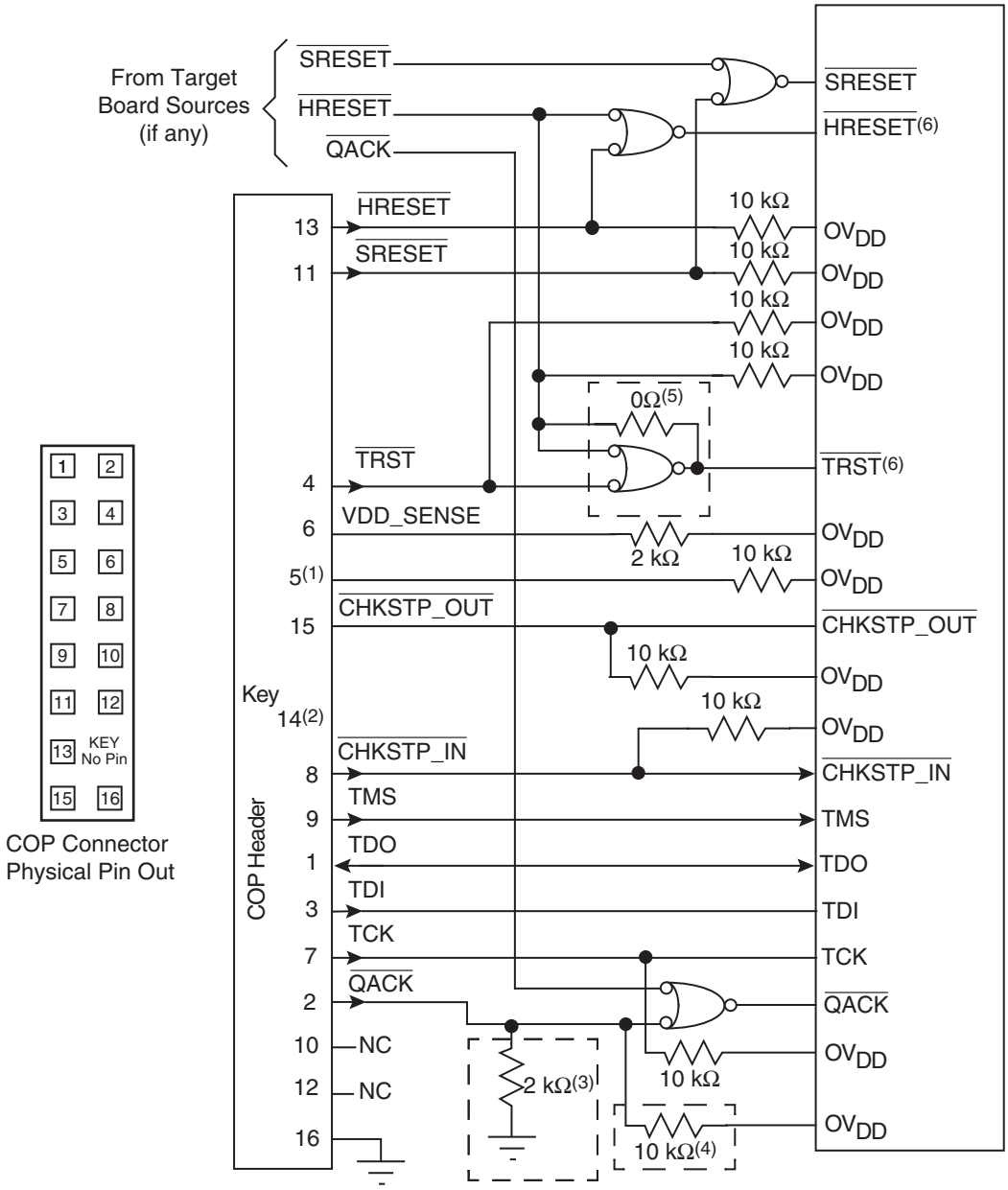
Some pins designated as being factory test pins must be pulled up to OV_{DD} or down to GND to ensure proper device operation. For the PC7447A, 360 BGA, the pins that must be pulled up to OV_{DD} are $\overline{LSSD\_MODE}$ and TEST[0:3]; the pins that must be pulled down to GND are: L1_TSTCLK and TEST[4]. The $\overline{CKSTP\_IN}$ signal should likewise be pulled up through a pull-up resistor (weak or stronger: 4.7–1 KΩ) to prevent erroneous assertions of this signal.
In addition, the PC7447A has one open-drain style output that requires a pull-up resistor (weak or stronger: 4.7–1 KΩ) if it is used by the system. This pin is $\overline{CKSTP\_OUT}$.

If pull-down resistors are used to configure BVSEL, the resistors should be less than 250Ω (see Table 8-1 on page 21). Because PLL_CFG[0:4] must remain stable during normal operation, strong pull-up and pull-down resistors (1 KΩ or less) are recommended to configure these signals in order to protect against erroneous switching due to ground bounce, power supply noise or noise coupling.

During inactive periods on the bus, the address and transfer attributes may not be driven by any master and may, therefore, float in the high-impedance state for relatively long periods of time. Because the PC7447A must continually monitor these signals for snooping, this float condition may cause excessive power draw by the input receivers on the PC7447A or by other receivers in the system. These signals can be pulled up through weak (10-KΩ) pull-up resistors by the system, address bus driven mode enabled (see the *MPC7450 RISC Microprocessor Family Users' Manual* for more information on this mode), or they may be otherwise driven by the system during inactive periods of the bus to avoid this additional power draw. Preliminary studies have shown the additional power draw by the PC7447A input receivers to be negligible and, in any event, none of these measures are necessary for proper device operation. The snooped address and transfer attribute inputs are: A[0:35], AP[0:4], TT[0:4], $\overline{CI}$, $\overline{WT}$, and $\overline{GBL}$.

If address or data parity is not used by the system, and respective parity checking is disabled through HID1, the input receivers for those pins are disabled and do not require pull-up resistors, and may be left unconnected by the system. If extended addressing is not used (HID0[XAEN] = 0), A[0:3] are unused and must be pulled low to GND through weak pull-down resistors; additionally, if address parity checking is enabled (HID1[EBA] = 1) and extended addressing is not used, AP[0] must be pulled up to OV_{DD} through a weak pull-up resistor. If the PC7447A is in 60x bus mode, DTI[0:3] must be pulled low to GND through weak pull-down resistors. The data bus input receivers are normally turned off when no read operation is in progress and, therefore, do not require pull-up resistors on the bus. Other data bus receivers in the system, however, may require pull-ups, or that those signals be otherwise driven by the system during inactive periods by the system. The data bus signals are: D[0:63] and DP[0:7].

Figure 12-3. JTAG Interface Connection



Notes:
1. RUN/$\overline{\text{STOP}}$, normally found on pin 5 of the COP header, is not implemented on the PC7447A. Connect pin 5 of the COP header to OV_{DD} with a 10 kΩ pull-up resistor.
2. Key location; pin 14 is not physically present on the COP header.
3. Component not populated. Populate only if debug tool does not drive $\overline{\text{QACK}}$.
4. Populate only if debug tool uses an open-drain type output and does not actively de-assert $\overline{\text{QACK}}$.
5. If the JTAG interface is implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ from the COP header though an AND gate to $\overline{\text{TRST}}$ of the part. If the JTAG interface is not implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ of the part through a 0Ω isolation resistor.
6. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown above.

15. Document Revision History

Table 15-1 provides a revision history for this hardware specification.

Table 15-1. Document Revision History

Revision Number	Date	Substantive Change(s)
E	01/07	Name change from Atmel to e2v
D	07/06	Page 35: b parameter modification; remove preliminary.
C	12/05	Add RoHS package and LGA package.
B	07/05	Changed die size.
		Table 9-2 on page 25: Modified jitter specifications to conform to JEDEC standards, changed jitter specification to cycle-to-cycle jitter (instead of long- and short-term jitter); changed jitter bandwidth recommendations.
		Added t_{KHTSV}, t_{KHARV}, t_{KHTSX}, and t_{KHARX} to Table 9-3 on page 27; these were previously grouped with t_{KHOV} and t_{KHOX}. Note: Documentation change only; the values for the output valid and output hold AC timing specifications remain unchanged for $\overline{TS}$, $\overline{ARTRY}$, and $\overline{SHD}$[0:1].
A	04/04	Initial revision.