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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.167GHZ
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	1.1V, 1.3V
Operating Temperature	-40°C ~ 110°C (TJ)
Security Features	-
Package / Case	360-BCBGA
Supplier Device Package	360-HiTCE-CBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pcx7447avgh1167nb

- Rename buffers
  - 16 GPR rename buffers
  - 16 FPR rename buffers
  - 16 VR rename buffers
- Dispatch unit
  - Decode/dispatch stage fully decodes each instruction
- Completion unit
  - The completion unit retires an instruction from the 16-entry completion queue (CQ) when all instructions ahead of it have been completed, the instruction has finished execution, and no exceptions are pending
  - Guarantees sequential programming model (precise exception model)
  - Monitors all dispatched instructions and retires them in order
  - Tracks unresolved branches and flushes instructions after a mispredicted branch
  - Retires as many as three instructions per clock cycle
- Separate on-chip L1 instruction and data caches (Harvard Architecture)
  - 32-Kbyte, eight-way set-associative instruction and data caches
  - Pseudo least-recently-used (PLRU) replacement algorithm
  - 32-byte (eight-word) L1 cache block
  - Physically indexed/physical tags
  - Cache write-back or write-through operation programmable on a per-page or per-block basis
  - Instruction cache can provide four instructions per clock cycle; data cache can provide four words per clock cycle
  - Caches can be disabled in software
  - Caches can be locked in software
  - MESI data cache coherency maintained in hardware
  - Separate copy of data cache tags for efficient snooping
  - Parity support on cache and tags
  - No snooping of instruction cache except for icbi instruction
  - Data cache supports AltiVec LRU and transient instructions
  - Critical double- and/or quad-word forwarding is performed as needed. Critical quad-word forwarding is used for AltiVec loads and instruction fetches. Other accesses use critical double-word forwarding.
- Level 2 (L2) cache interface
  - On-chip, 512-Kbyte, eight-way set-associative unified instruction and data cache
  - Fully pipelined to provide 32 bytes per clock cycle to the L1 caches
  - A total nine-cycle load latency for an L1 data cache miss that hits in L2
  - Cache write-back or write-through operation programmable on a per-page or per-block basis 64-byte, two-sectored line size
  - Parity support on cache
- Separate memory management units (MMUs) for instructions and data
  - 52-bit virtual address, 32- or 36-bit physical address

  - Address translation for 4-Kbyte pages, variable-sized blocks, and 256-Mbyte segments
  - Memory programmable as write-back/write-through, caching-inhibited/caching-allowed, and memory coherency enforced/memory coherency not enforced on a page or block basis
  - Separate IBATs and DBATs (eight each) also defined as SPRs
  - Separate instruction and data translation look aside buffers (TLBs)

    Both TLBs are 128-entry, two-way set-associative, and use a LRU replacement algorithm

    TLBs are hardware- or software-reloadable (that is, a page table search is performed in hardware or by system software on a TLB miss).
- Efficient data flow
  - Although the VR/LSU interface is 128 bits, the L1/L2 bus interface allows up to 256 bits
  - The L1 data cache is fully pipelined to provide 128 bits/cycle to or from the VRs
  - L2 cache is fully pipelined to provide 256 bits per processor clock cycle to the L1 cache
  - As many as eight outstanding, out-of-order, cache misses are allowed between the L1 data cache and the L2 bus
  - As many as 16 out-of-order transactions can be present on the MPX bus
  - Store merging for multiple store misses to the same line. Only coherency action taken (address-only) for store misses merged to all 32 bytes of a cache block (no data tenure needed)
  - Three-entry finished store queue and five-entry completed store queue between the LSU and the L1 data cache
  - Separate additional queues for efficient buffering of outbound data (such as castouts and write-through stores) from the L1 data cache and L2 cache
- Multiprocessing support features include the following:
  - Hardware-enforced, MESI cache coherency protocols for data cache
  - Load/store with reservation instruction pair for atomic memory references, semaphores, and other multiprocessor operations
- Power and thermal management
  - A new dynamic frequency switching (DFS) feature allows the processor core frequency to be halved through software to reduce power consumption
  - The following three power-saving modes are available to the system:

    Nap: Instruction fetching is halted. Only the clocks for the time base, decrementer, and JTAG logic remain running. The part goes into the doze state to snoop memory operations on the bus and then back to nap using a QREQ/QACK processor-system handshake protocol.

    Sleep: Power consumption is further reduced by disabling bus snooping, leaving only the PLL in a locked and running state. All internal functional units are disabled.

    Deep sleep: When the part is in the deep Sleep state, the system can disable the PLL. The system can then disable the SYSCLK source for greater system power savings. Power-on reset procedures for restarting and relocking the PLL must be followed upon exiting the deep sleep state.

  - Instruction cache throttling provides control of instruction fetching to limit device temperature
  - A new temperature diode that can determine the temperature of the microprocessor
- Performance monitor can be used to help debug system designs and improve software efficiency
- In-system testability and debugging features through JTAG boundary-scan capability
- Testability
  - LSSD scan design
  - IEEE 1149.1 JTAG interface
  - Array built-in self test (ABIST), factory test only
- Reliability and serviceability
  - Parity checking on system bus
  - Parity checking on the L1 and L2 caches

3. General Parameters

Table 3-1 provides a summary of the general parameters of the PC7447A.

Table 3-1. Device Parameters

Parameter	Description
Technology	0.13 µm CMOS, nine-layer metal
Die size	8.51 mm × 9.86 mm
Transistor count	48.6 million
Logic design	Fully-static
Packages	Surface mount 360 ceramic ball grid array (HITCE)
Core power supply	1.3V ± 50 mV and 1.1V ± 50 mV DC nominal
I/O power supply	1.8V ± 5% DC, or 2.5V ±5% DC

6.3 Recommended Operating Conditions

Table 6-2 provides the recommended operating conditions for the PC7447A.

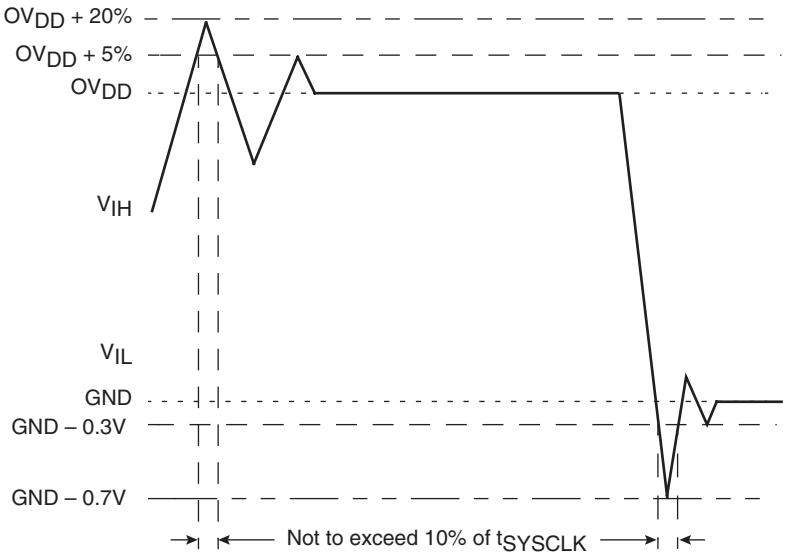
Table 6-2. Recommended Operating Conditions[1]

Symbol	Characteristic		Recommended Value		Unit
			Min	Max	
V_{DD}	Core supply voltage		1.3V ± 50 mV or 1.1V ± 50 mV		V
AV_{DD}[2]	PLL supply voltage		1.3V ± 50 mV or 1.1V ± 50 mV		V
OV_{DD}	Processor bus supply voltage	BVSEL = 0	1.8V ± 5%		V
OV_{DD}		BVSEL = $\overline{\text{HRESET}}$ or OV_{DD}	2.5V ± 5%		
V_{IN}	Input voltage	Processor bus	GND	OV_{DD}	V
V_{IN}		JTAG signals	GND	OV_{DD}	
T_J	Die-junction temperature		-55	125°C	°C

Notes: 1. These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

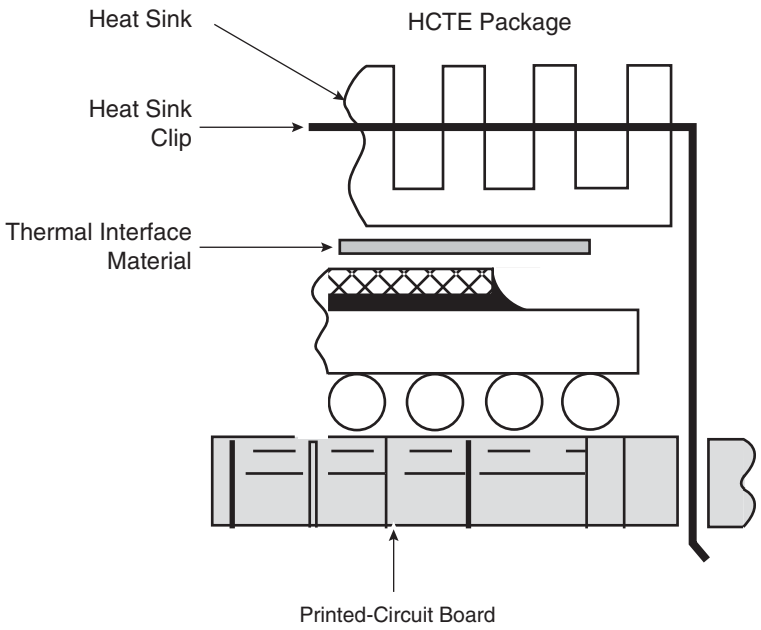
2. This voltage is the input to the filter discussed in Section "PLL Power Supply Filtering" on page 41 and not necessarily the voltage at the AV_{DD} pin, which may be reduced from V_{DD} by the filter.

Figure 6-1. Overshoot/Undershoot Voltage



The PC7447A provides several I/O voltages to support both compatibility with existing systems and migration to future systems. The PC7447A core voltage must always be provided at a nominal 1.3V (see Table 6-2 on page 10 for the actual recommended core voltage). The input voltage threshold for each bus is selected by sampling the state of the voltage select pins at the negation of the signal HRESET. The output voltage will swing from GND to the maximum voltage applied to the OVDD power pins. Table 6-3 on page 11 provides the input threshold voltage settings. Because these settings may change in future products, it is recommended that BVSEL be configured using resistor options, jumpers, or some other flexible means, with the capability to reconfigure the termination of this signal in the future if necessary.

Figure 6-3. Package Exploded Cross-sectional View with Several Heat Sink Options



6.4.4 Thermal Interface Materials

A thermal interface material is recommended at the package lid-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 6-4 on page 14 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure.

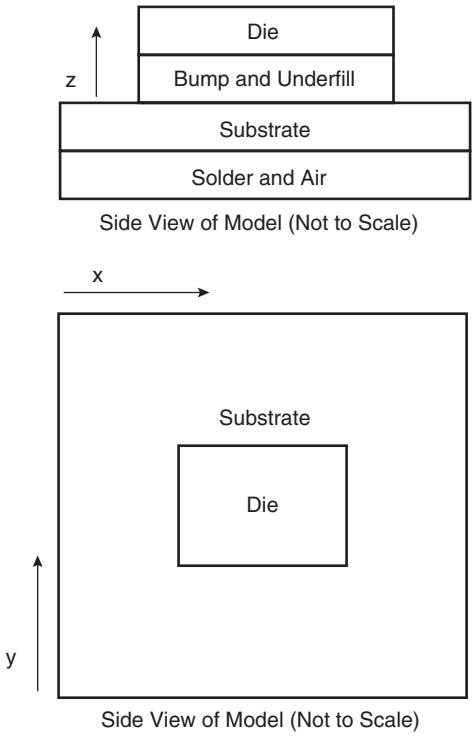
As shown, the performance of these thermal interface materials improves with increasing contact pressure.

The use of thermal grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal resistance approximately seven times greater than the thermal grease joint.

Often, heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 6-3 on page 13). Therefore, synthetic grease offers the best thermal performance, considering the low interface pressure, and is recommended due to the high power dissipation of the PC7447A. Of course, the selection of any thermal interface material depends on many factors – thermal performance requirements, manufacturability, service temperature, dielectric properties, cost, and so on.

Figure 6-5. Recommended Thermal Model of PC7447A

Conductivity	Value	Unit
Bump and Underfill (7.3 x 9.3 x 0.070 mm)		
k_x	0.6	W/(m x K)
k_y	0.6	
k_z	1.9	
Substrate (25 x 25 x 1.2 mm)		
k_x	8.1	
k_y	8.1	
k_z	4.0	
Solder Ball and Air (25 x 25 x 0.6 mm)		
k_x	0.034	
k_y	0.034	
k_z	3.8	



6.4.4.2 Temperature Diode

The PC7447A has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices. These devices use the negative temperature coefficient of a diode operated at a constant current to determine the temperature of the microprocessor and its environment. For proper operation, the monitoring device used should auto-calibrate the device by canceling out the V_{BE} variation of each PC7447A's internal diode.

The following are the specifications of the PC7447A on-board temperature diode:

$V_f > 0.40V$

$V_f < 0.90V$

Operating range 2 - 300 µA

Diode leakage < 10 nA at 125°C

Ideality factor over 5 µA – 150 µA at 60°C: 1 <= n <= TBD

Ideality factor is defined as the deviation from the ideal diode equation:

$$I_{fW} = I_s\left[e^{\frac{qV_f}{nKT}} - 1\right]$$

Another useful equation is:

$$V_H - V_L = n\frac{KT}{q}\left[In\frac{I_H}{I_L}\right]$$

8. Pinout Listings

Table 8-1 provides the pinout listing for the PC7447A, 360 HITCE package. The pinouts of the PC7447A and PC7447 are pin compatible but there have been some changes. A PC7447A may be populated on a board designed for a PC7447 provided all pins defined as 'Not Connected' for the PC7447 are unterminated as required by the PC7457 RISC Microprocessor Specification. The PC7447A uses pins previously marked 'Not Connected' for the temperature diode pins and for additional power and ground connections. Because these 'Not Connected' pins in the PC7447 360 pin package are not driven in functional mode, a PC7447 can be populated in a PC7447A board. See section "Connection Recommendations" on page 41 for additional information.

Note: This pinout is not compatible with the PC750, PC7400, or PC7410 360 BGA package.

Table 8-1. Pinout Listing for the PC7447A, 360 HITCE Package

Signal Name	Pin Number	Active	I/O	I/F Select(1)
A[0:35](2)	E11, H1, C11, G3, F10, L2, D11, D1, C10, G2, D12, L3, G4, T2, F4, V1, J4, R2, K5, W2, J2, K4, N4, J3, M5, P5, N3, T1, V2, U1, N5, W1, B12, C4, G10, B11	High	I/O	BVSEL
$\overline{\text{AACK}}$	R1	Low	Input	BVSEL
AP[0:4](2)	C1, E3, H6, F5, G7	High	I/O	BVSEL
$\overline{\text{ARTRY}}$(3)	N2	Low	I/O	BVSEL
AV_{DD}	A8	–	Input	BVSEL
$\overline{\text{BG}}$	M1	Low	Input	BVSEL
$\overline{\text{BMODE0}}$(4)	G9	Low	Input	BVSEL
$\overline{\text{BMODE1}}$(5)	F8	Low	Input	BVSEL
$\overline{\text{BR}}$	D2	Low	Output	BVSEL
BVSEL(1)(6)	B7	High	Input	BVSEL
$\overline{\text{CI}}$(3)	J1	Low	Output	BVSEL
$\overline{\text{CKSTP\_IN}}$	A3	Low	Input	BVSEL
$\overline{\text{CKSTP\_OUT}}$	B1	Low	Output	BVSEL
CLK_OUT	H2	High	Output	BVSEL
D[0:63]	R15, W15, T14, V16, W16, T15, U15, P14, V13, W13, T13, P13, U14, W14, R12, T12, W12, V12, N11, N10, R11, U11, W11, T11, R10, N9, P10, U10, R9, W10, U9, V9, W5, U6, T5, U5, W7, R6, P7, V6, P17, R19, V18, R18, V19, T19, U19, W19, U18, W17, W18, T16, T18, T17, W3, V17, U4, U8, U7, R7, P6, R8, W8, T8	High	I/O	BVSEL
$\overline{\text{DBG}}$	M2	Low	Input	BVSEL
DP[0:7]	T3, W4, T4, W9, M6, V3, N8, W6	High	I/O	BVSEL
$\overline{\text{DRDY}}$(7)	R3	Low	Output	BVSEL
DTI[0:3](8)	G1, K1, P1, N1	High	Input	BVSEL
EXT_QUAL(9)	A11	High	Input	BVSEL
$\overline{\text{GBL}}$	E2	Low	I/O	BVSEL

Table 8-1. Pinout Listing for the PC7447A, 360 HITCE Package (Continued)

Signal Name	Pin Number	Active	I/O	I/F Select[1]
GND	B5, C3, D6, D13, E17, F3, G17, H4, H7, H9, H11, H13, J6, J8, J10, J12, K7, K3, K9, K11, K13, L6, L8, L10, L12, M4, M7, M9, M11, M13, N7, P3, P9, P12, R5, R14, R17, T7, T10, U3, U13, U17, V5, V8, V11, V15	–	–	N/A
GND[15]	A17, A19, B13, B16, B18, E12, E19, F13, F16, F18, G19, H18, J14, L14, M15, M17, M19, N14, N16, P15, P19	–	–	N/A
GND_SENSE[19]	G12, N13	–	–	N/A
$\overline{\text{HIT}}$[7]	B2	Low	Output	BVSEL
$\overline{\text{HRESET}}$	D8	Low	Input	BVSEL
$\overline{\text{INT}}$	D4	Low	Input	BVSEL
L1_TSTCLK[9]	G8	High	Input	BVSEL
L2_TSTCLK[10]	B3	High	Input	BVSEL
No Connect[11]	A6, A14, A15, B14, B15, C14, C15, C16, C17, C18, C19, D14, D15, D16, D17, D18, D19, E14, E15, F14, F15, G14, G15, H15, H16, J15, J16, J17, J18, J19, K15, K16, K17, K18, K19, L15, L16, L17, L18, L19	–	–	–
$\overline{\text{LSSD\_MODE}}$[6][12]	E8	Low	Input	BVSEL
$\overline{\text{MCP}}$	C9	Low	Input	BVSEL
OV_{DD}	B4, C2, C12, D5, F2, H3, J5, K2, L5, M3, N6, P2, P8, P11, R4, R13, R16, T6, T9, U2, U12, U16, V4, V7, V10, V14	–	–	N/A
OV_{DD}_SENSE[16]	E18, G18	–	–	N/A
PLL_CFG[0:4]	B8, C8, C7, D7, A7	High	Input	BVSEL
$\overline{\text{PMON\_IN}}$[13]	D9	Low	Input	BVSEL
$\overline{\text{PMON\_OUT}}$	A9	Low	Output	BVSEL
$\overline{\text{QACK}}$	G5	Low	Input	BVSEL
$\overline{\text{QREQ}}$	P4	Low	Output	BVSEL
$\overline{\text{SHD}}$[0:1][3]	E4, H5	Low	I/O	BVSEL
$\overline{\text{SMI}}$	F9	Low	Input	BVSEL
$\overline{\text{SRESET}}$	A2	Low	Input	BVSEL
SYSCLK	A10	–	Input	BVSEL
$\overline{\text{TA}}$	K6	Low	Input	BVSEL
TBEN	E1	High	Input	BVSEL
$\overline{\text{TBST}}$	F11	Low	Output	BVSEL
TCK	C6	High	Input	BVSEL
TDI[6]	B9	High	Input	BVSEL
TDO	A4	High	Output	BVSEL
$\overline{\text{TEA}}$	L1	Low	Input	BVSEL
TEMP_ANODE[17]	N18			
TEMP_CATHODE[17]	N19			

18. These pins are internally connected to V_{DD} and are intended to allow an external device to detect the processor core voltage level present inside the device package. If unused, they must be connected directly to V_{DD} or left unconnected.
19. These pins are internally connected to GND and are intended to allow an external device to detect the processor ground voltage level present inside the device package. If unused, they must be connected directly to GND or left unconnected.

Note: Caution must be exercised when performing boundary scan test operations on a board designed for a PC7447A but populated with an PC7447. This is because in the PC7447 it is possible to drive the latches associated with the former 'No Connect' pins in the PC7447, potentially causing contention on those pins. To prevent this, ensure that these pins are not connected on the board or, if they are connected, ensure that the states of internal PC7447 latches do not cause these pins to be driven during board testing.

9. Electrical Characteristics

9.1 Static Characteristics

Table 9-1 provides the DC electrical characteristics for the PC7447A.

Table 9-1. DC Electrical Specifications (see Table 6-2 on page 10 for Recommended Operating Conditions)

Symbol	Characteristic	Nominal Bus Voltage(1)	Min	Max	Unit	Notes
V_{IH}	Input high voltage (all inputs)	1.8	$OV_{DD} \times 0.65$	$OV_{DD} + 0.3$	V	(2)
		2.5	1.7	$OV_{DD} + 0.3$		
V_{IL}	Input low voltage (all inputs)	1.8	-0.3	$OV_{DD} \times 0.35$	V	(2)(6)
		2.5	-0.3	0.7		
I_{IN}	Input leakage current, $V_{IN} = GV_{DD}/O_{DD}$ V_{IN} = GND	–	–	30 -30	µA	(2)(3)
I_{TSI}	High-impedance (off-state) leakage current, $V_{IN} = GV_{DD}/O_{DD}$ V_{IN} = GND	–	–	30 -30	µA	(2)(3)(4)
V_{OH}	Output high voltage at I_{OH} = -5 mA	1.8	OV_{DD} - 0.45	–	V	
		2.5	1.8	–		
V_{OL}	Output low voltage at I_{OL} = 5 mA	1.8	–	0.45	V	
		2.5	–	0.6		
C_{IN}	Capacitance, V_{IN} = 0V f = 1 MHz — All other inputs		–	8	pF	(5)
V_{IH}	Input high voltage (all inputs)	1.8	$OV_{DD} \times 0.65$	$OV_{DD} + 0.3$	V	(2)
		2.5	1.7	$OV_{DD} + 0.3$		
V_{IL}	Input low voltage (all inputs)	1.8	-0.3	$OV_{DD} \times 0.35$	V	(2)(6)
		2.5	-0.3	0.7		
I_{IN}	Input leakge current, $V_{IN} = GV_{DD}/OV_{DD}$ V_{IN} = GND	–	–	30 -30	µA	(2)(3)

Notes: 1. Nominal voltages; see Table 6-2 on page 10 for recommended operating conditions.
2. For processor bus signals, the reference is OV_{DD} while GV_{DD} is the reference for the L3 bus signals.

3. Excludes test signals and IEEE 1149.1 boundary scan (JTAG) signals.
4. The leakage is measured for nominal OV_{DD}/GV_{DD} and V_{DD}, or both OV_{DD}/GV_{DD} and V_{DD} must vary in the same direction (for example, both OV_{DD} and V_{DD} vary by either +5% or -5%).
5. Capacitance is periodically sampled rather than 100% tested.
6. Excludes signals with internal pull ups: BVSEL, $\overline{\text{LSSD\_MODE}}$, TDI, TMS, and $\overline{\text{TRST}}$. Characterization of leakage current for these signals is currently being conducted.

9.2 Dynamic Characteristics

This section provides the AC electrical characteristics for the PC7447A. After fabrication, functional parts are sorted by maximum processor core frequency as shown in Section "Clock AC Specifications" on page 25 and tested for conformance to the AC specifications for that frequency. The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG[0:4] signals, and can be dynamically modified using dynamic frequency switching (DFS). Parts are sold by maximum processor core frequency; See "Ordering Information" on page 46. for information on ordering parts. DFS is described in Section "Dynamic Frequency Switching (DFS)" on page 17.

9.2.1 Clock AC Specifications

Table 9-2 provides the clock AC timing specifications as defined in Figure 9-1 on page 26 and represents the tested operating frequencies of the devices. The maximum system bus frequency, f_{SYSCLK}, given in Table 9-2 on page 25 is considered a practical maximum in a typical single-processor system. The actual maximum SYSCLK frequency for any application of the PC7447A will be a function of the AC timings of the PC7447A, the AC timings for the system controller, bus loading, printed-circuit board topology, trace lengths, and so forth, and may be less than the value given in Table 9-2 on page 25.

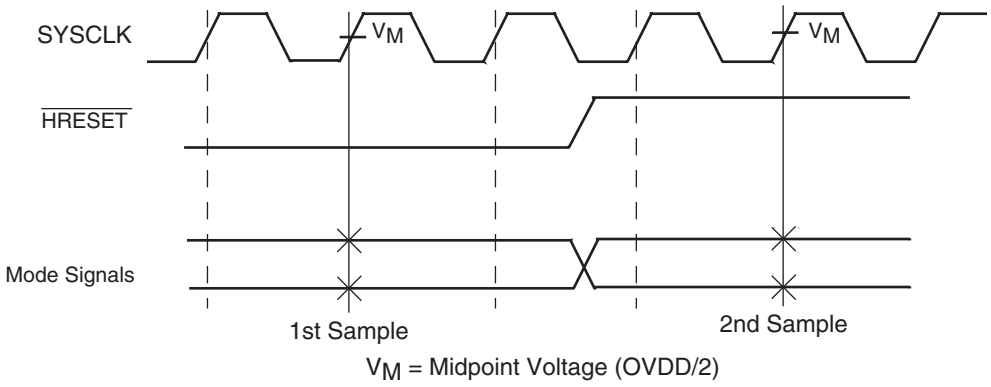
Table 9-2. Clock AC Timing Specifications (See Table 6-2 on page 10 for Recommended Operating Conditions)

		Maximum Processor Core Frequency									
		1000 MHz		1267 MHz		1333 MHz		1420 MHz			
		V_{DD} = 1.3V		V_{DD} = 1.3V		V_{DD} = 1.3		V_{DD} = 1.3			
Symbol	**Characteristic**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
f_{CORE}	Processor core frequency	600	1000	600	1267	600	1333	600	1420	MHz	(1)(8)(9)
f_{VCO}	VCO frequency	1200	2000	1200	2533	1200	2667	1200	2840	MHz	(1)(9)
f_{SYSCLK}	SYSCLK frequency	33	167	33	167	33	167	33	167	MHz	(1)(2)(8)
t_{SYSCLK}	SYSCLK cycle time	6.0	30	6	30	6	30	6	30	ns	(2)
t_{KR}, t_{KF}	SYSCLK rise and fall time	–	1.0	–	1	–	1	–	1	ns	(3)
t_{KHKL}/t_{SYSCLK}	SYSCLK duty cycle measured at $OV_{DD}/2$	40	60	40	60	40	60	40	60	%	(4)
	SYSCLK jitter(5)(6)	–	150	–	150	–	150	–	150	ps	(5)(6)
	Internal PLL relock time(7)	–	100	–	100	–	100	–	100	µs	(7)

2. The symbology used for timing specifications herein follows the pattern of $t_{(signal)(state)(reference)(state)}$ for inputs and $t_{(reference)(state)(signal)(state)}$ for outputs. For example, t_{IVKH} symbolizes the time input signals (I) reach the valid state (V) relative to the SYSCLK reference (K) going to the high (H) state or input setup time. And t_{KHOV} symbolizes the time from SYSCLK (K) going high (H) until outputs (O) are valid (V) or output valid time. Input hold time can be read as the time that the input signal (I) went invalid (X) with respect to the rising clock edge (KH) (note the position of the reference and its state for inputs) and output hold time can be read as the time from the rising edge (KH) until the output went invalid (OX).
3. t_{SYSCLK} is the period of the external clock (SYSCLK) in ns. The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
4. According to the bus protocol, $\overline{TS}$ is driven only by the currently active bus master. It is asserted low and precharged high before returning to high impedance, as shown in Figure 9-3 on page 29. The nominal precharge width for $\overline{TS}$ is $0.5 \times t_{SYSCLK}$, that is, less than the minimum t_{SYSCLK} period, to ensure that another master asserting $\overline{TS}$ on the following clock will not contend with the precharge. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge.The high-impedance behavior is guaranteed by design.
5. Guaranteed by design and not tested.
6. According to the bus protocol, $\overline{ARTRY}$ can be driven by multiple bus masters through the clock period immediately following $\overline{AACK}$. Bus contention is not an issue because any master asserting $\overline{ARTRY}$ will be driving it low. Any master asserting it low in the first clock following $\overline{AACK}$ will then go to high impedance for 1 clock before precharging it high during the second cycle after the assertion of $\overline{AACK}$. The nominal precharge width for $\overline{ARTRY}$ is 1.0 t_{SYSCLK}; that is, it should be high impedance as shown in Figure 9-3 on page 29 before the first opportunity for another master to assert $\overline{ARTRY}$. Output valid and output hold timing is tested for the signal asserted.The high-impedance behavior is guaranteed by design.
7. According to the MPX bus protocol, $\overline{SHD0}$ and $\overline{SHD1}$ can be driven by multiple bus masters beginning the cycle of $\overline{TS}$. Timing is the same as $\overline{ARTRY}$, that is, the signal is high impedance for a fraction of a cycle, then negated for up to an entire cycle (crossing a bus cycle boundary) before being three-stated again. The nominal precharge width for $\overline{SHD0}$ and $\overline{SHD1}$ is 1.0 t_{SYSCLK}. The edges of the precharge vary depending on the programmed ratio of core to bus (PLL configurations).
8. $\overline{BMODE}$[0:1] and BVSEL are mode select inputs and are sampled before and after $\overline{HRESET}$ negation. These parameters represent the input setup and hold times for each sample. These values are guaranteed by design and not tested. These inputs must remain stable after the second sample. See Figure 9-2 on page 28 for sample timing.

Figure 9-2 provides the mode select input timing diagram for the PC7447A. The mode select inputs are sampled twice, once before and once after $\overline{HRESET}$ negation.

Figure 9-2. Mode Input Sample Timing Diagram



9.2.3 IEEE 1149.1 AC Timing Specifications

Table 9-4 provides the IEEE 1149.1 (JTAG) AC timing specifications as defined in Figure 9-5 through Figure 9-8 on page 32.

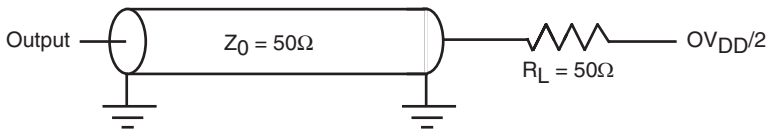
Table 9-4. JTAG AC Timing Specifications (Independent of SYSCLK)(1) at Recommended Operating Conditions (see Table 6-2 on page 10)

Symbol	Parameter	Min	Max	Unit
f_{TCLK}	TCK frequency of operation	0	33.3	MHz
t_{TCLK}	TCK cycle time	30	–	ns
t_{JHJL}	TCK clock pulse width measured at 1.4V	15	–	ns
t_{JR} and t_{JF}	TCK rise and fall times	–	2	ns
t_{TRST}(2)	$\overline{TRST}$ assert time	25	–	ns
t_{DVJH}(3) t_{IVJH}	Input Setup Times: Boundary-scan data TMS, TDI	 4 0	 – –	ns
t_{DXJH}(3) t_{IXJH}	Input Hold Times: Boundary-scan data TMS, TDI	 20 25	 – –	ns
t_{JLDV}(4) t_{JLOV}	Valid Times: Boundary-scan data TDO	 4 4	 20 25	ns
t_{JLDX}(4) t_{JLOX}	Output hold times: Boundary-scan data TDO	 30 30	 – –	
t_{JLDZ}(4)(5) t_{JLOZ}	TCK to output high impedance: Boundary-scan data TDO	 3 3	 19 9	ns

Notes:
1. All outputs are measured from the midpoint voltage of the falling/rising edge of TCLK to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50Ω load (see Figure 9-4). Time-of-flight delays must be added for trace lengths, vias and connectors in the system.
2. $\overline{TRST}$ is an asynchronous level sensitive signal. The time is for test purposes only.
3. Non-JTAG signal input timing with respect to TCK.
4. Non-JTAG signal output timing with respect to TCK.
5. Guaranteed by design and characterization.

Figure 9-4 provides the AC test load for TDO and the boundary-scan outputs of the PC7457.

Figure 9-4. Alternate AC Test Load for the JTAG Interface



11.5 Package Parameters for the PC7447A, 360 HCTE LGA

The package parameters are as provided in the following list. The package type is 25 × 25 mm, 360 high coefficient of thermal expansion ceramic land grid array (HCTE).

Package outline	25 mm × 25 mm
Interconnects	360 (19 × 19 ball array - 1)
Pitch	1.27 mm (50 mil)
Minimum module height	1.92 mm
Maximum module height	2.20 mm
Coefficient of thermal expansion	12.3 ppm/°C

Note that when DFS is enabled the resulting core frequency must meet the minimum core frequency requirements described in Table 9-2 on page 25.

Table 12-1. PC7447A Microprocessor PLL Configuration Example for 1420-MHz Parts

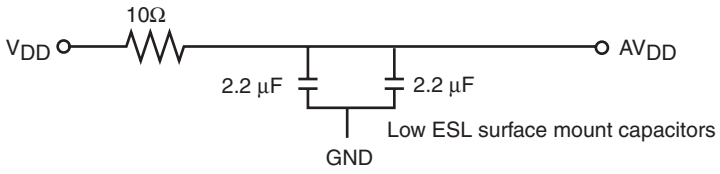
	Example Bus-to-Core Frequency in MHz (VCO Frequency in MHz)									
			Bus (SYSCLK) Frequency							
PLL_CFG[0:4]	Bus-to-Core Multiplier	Core-to-VCO Multiplier	33.33 MHz	50 MHz	66.66 MHz	75 MHz	83 MHz	100 MHz	133.33 MHz	166.66 MHz
01000	2x	2x								
10000	3x	2x								
10100	4x	2x								667 (1333)
10110	5x	2x							667 (1333)	835 (1670)
10010	5.5x	2x							733 (1466)	919 (1837)
11010	6x	2x						600 (1200)	800 (1600)	1002 (2004)
01010	6.5x	2x						650 (1300)	866 (1730)	1086 (2171)
00100	7x	2x						700 (1400)	931 (1862)	1169 (2338)
00010	7.5x	2x					623 (1245)	750 (1500)	1000 (2000)	1253 (2505)
11000	8x	2x				600 (1200)	664 (1328)	800 (1600)	1064 (2128)	1336 (2672)
01100	8.5x	2x				638 (1276)	706 (1412)	850 (1700)	1131 (2261)	1417 (2833)
01111	9x	2x			600 (1200)	675 (1350)	747 (1494)	900 (1800)	1197 (2394)	
01110	9.5x	2x			633 (1266)	712 (1524)	789 (1578)	950 (1900)	1264 (2528)	
10101	10x	2x			667 (1333)	750 (1500)	830 (1660)	1000 (2000)	1333 (2667)	
10001	10.5x	2x			700 (1400)	938 (1876)	872 (1744)	1050 (2100)	1397 (2793)	
10011	11x	2x			733 (1466)	825 (1650)	913 (1826)	1100 (2200)		
00000	11.5x	2x			766 (532)	863 (1726)	955 (1910)	1150 (2300)		
10111	12x	2x		600 (1200)	800 (1600)	900 (1800)	996 (1992)	1200 (2400)		

12.2 PLL Power Supply Filtering

The AV_{DD} power signal is provided on the PC7447A to provide power to the clock generation PLL. To ensure stability of the internal clock, the power supplied to the AV_{DD} input signal should be filtered of any noise in the 500 KHz to 10 MHz resonant frequency range of the PLL. A circuit similar to the one shown in Figure 12-1 using surface mount capacitors with minimum effective series inductance (ESL) is recommended.

The circuit should be placed as close as possible to the AV_{DD} pin to minimize noise coupled from nearby circuits. It is often possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the 360 HITCE footprint.

Figure 12-1. PLL Power Supply Filter Circuit



12.3 Decoupling Recommendations

Due to the PC7447A dynamic power management feature, large address and data buses, and high operating frequencies, the PC7447A can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the PC7447A system, and the PC7447A itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer use sufficient decoupling capacitors, typically one capacitor for every 1-2 V_{DD} pins, and a similar or lesser amount for the OV_{DD} pins, placed as close as possible to the power pins of the PC7447A. It is also recommended that these decoupling capacitors receive their power from separate V_{DD}, OV_{DD}, and GND power planes in the PCB, utilizing short traces to minimize inductance.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic surface mount technology (SMT) capacitors should be used to minimize lead inductance. Orientations where connections are made along the length of the part, such as 0204, are preferable but not mandatory. Consistent with the recommendations of Dr. Howard Johnson in High Speed Digital Design: A Handbook of Black Magic (Prentice Hall, 1993) and contrary to previous recommendations for decoupling Freescale™ microprocessors, multiple small capacitors of equal value are recommended over using multiple values of capacitance.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD} and OV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low equivalent series resistance (ESR) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors are: 100-330 µF (AVX TPS tantalum or Sanyo OSCON).

12.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unless otherwise noted, unused active low inputs should be tied to OV_{DD}, and unused active high inputs should be connected to GND. All NC (no connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, OV_{DD}, and GND pins in the PC7447A.

For backward compatibility with the PC7447 to the PC7447A, the new power and ground signals (formerly NC, see Table 8-1 on page 21) may be left unconnected. There is no performance degradation associated with leaving these pins unconnected. However, future devices may require these additional power and ground signals to be connected to achieve maximum performance, and it is recommended that new designs include the additional connections to facilitate future upgrades. See also section "Pinout Listings" on page 21 for additional information.

12.5 Output Buffer DC Impedance

The PC7447A processor bus drivers are characterized over process, voltage, and temperature. To measure Z_0, an external resistor is connected from the chip pad to OV_{DD} or GND. The value of each resistor is varied until the pad voltage is $OV_{DD}/2$. Figure 12-2 on page 42 shows the driver impedance measurement.

The output impedance is the average of two components–the resistances of the pull-up and pull-down devices. When data is held low, SW2 is closed (SW1 is open), and R_N is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_N then becomes the resistance of the pull-down devices. When data is held high, SW1 is closed (SW2 is open), and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

Figure 12-2. Driver Impedance Measurement

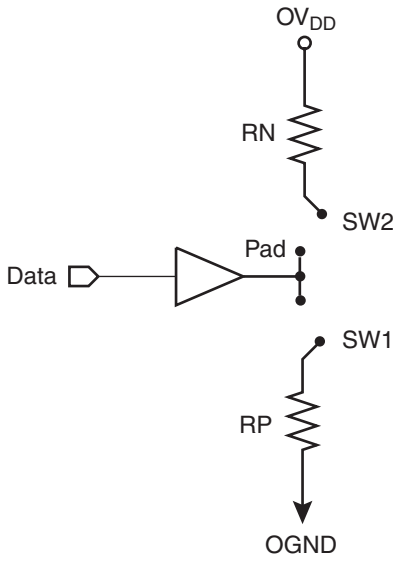


Table 12-2 summarizes the signal impedance results. The impedance increases with junction temperature and is relatively unaffected by bus voltage.

Table 12-2. Impedance Characteristics with V_{DD} = 1.5V, OV_{DD} = 1.8V ±5%, T_j = 5° - 85°C

Impedance		Processor bus	L3 Bus	Unit
Z_0	Typical	33 – 42	34 – 42	Ω
	Maximum	31 – 51	32 – 44	Ω

12.6 Pull-up/Pull-down Resistor Requirements

The PC7447A requires high-resistive (weak: 4.7-KΩ) pull-up resistors on several control pins of the bus interface to maintain the control signals in the negated state after they have been actively negated and released by the PC7447A or other bus masters. These pins are: $\overline{TS}$, $\overline{ARTRY}$, $\overline{SHDO}$, and $\overline{SHD1}$.

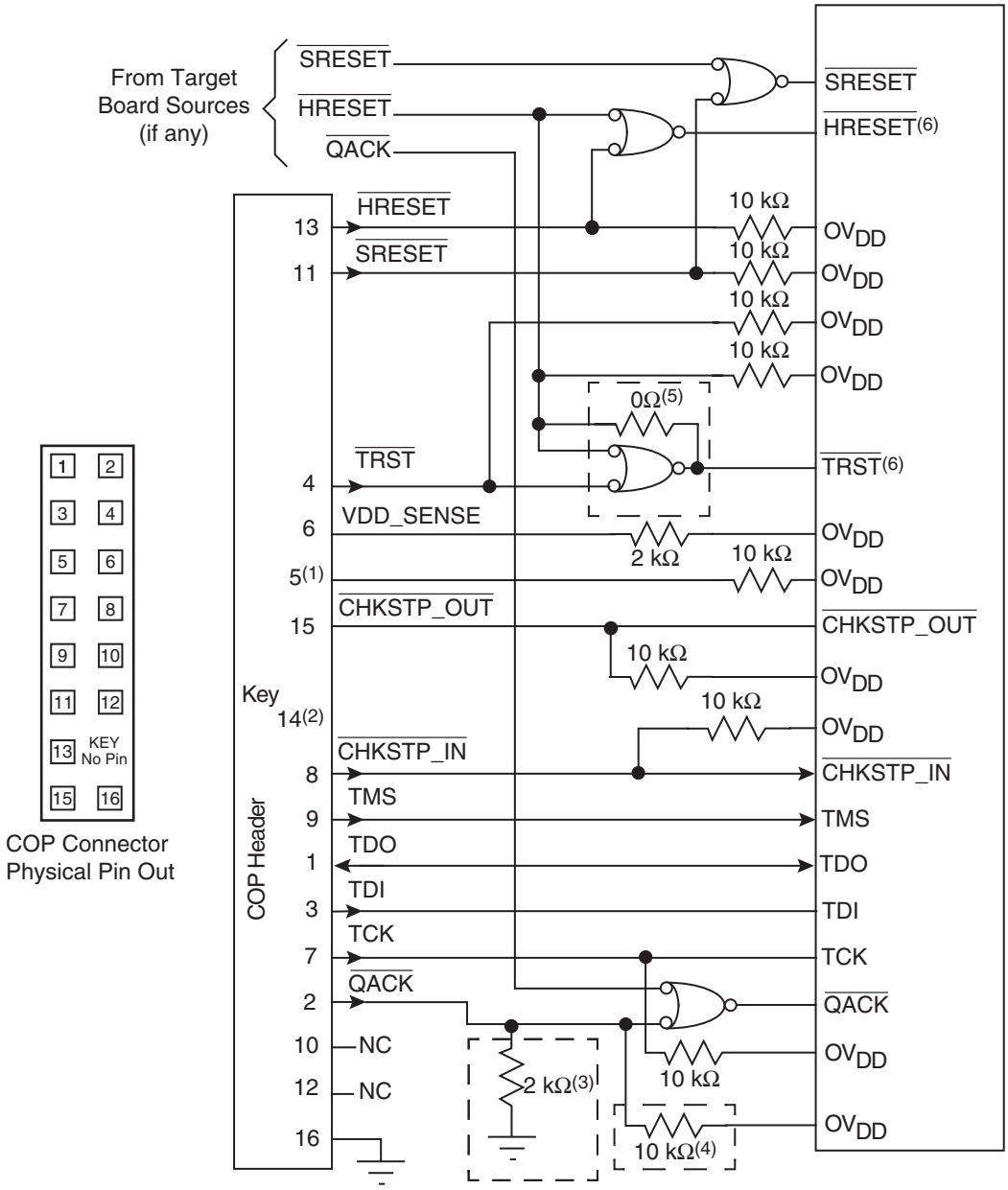
Some pins designated as being factory test pins must be pulled up to OV_{DD} or down to GND to ensure proper device operation. For the PC7447A, 360 BGA, the pins that must be pulled up to OV_{DD} are $\overline{LSSD\_MODE}$ and TEST[0:3]; the pins that must be pulled down to GND are: L1_TSTCLK and TEST[4]. The $\overline{CKSTP\_IN}$ signal should likewise be pulled up through a pull-up resistor (weak or stronger: 4.7–1 KΩ) to prevent erroneous assertions of this signal.
In addition, the PC7447A has one open-drain style output that requires a pull-up resistor (weak or stronger: 4.7–1 KΩ) if it is used by the system. This pin is $\overline{CKSTP\_OUT}$.

If pull-down resistors are used to configure BVSEL, the resistors should be less than 250Ω (see Table 8-1 on page 21). Because PLL_CFG[0:4] must remain stable during normal operation, strong pull-up and pull-down resistors (1 KΩ or less) are recommended to configure these signals in order to protect against erroneous switching due to ground bounce, power supply noise or noise coupling.

During inactive periods on the bus, the address and transfer attributes may not be driven by any master and may, therefore, float in the high-impedance state for relatively long periods of time. Because the PC7447A must continually monitor these signals for snooping, this float condition may cause excessive power draw by the input receivers on the PC7447A or by other receivers in the system. These signals can be pulled up through weak (10-KΩ) pull-up resistors by the system, address bus driven mode enabled (see the *MPC7450 RISC Microprocessor Family Users' Manual* for more information on this mode), or they may be otherwise driven by the system during inactive periods of the bus to avoid this additional power draw. Preliminary studies have shown the additional power draw by the PC7447A input receivers to be negligible and, in any event, none of these measures are necessary for proper device operation. The snooped address and transfer attribute inputs are: A[0:35], AP[0:4], TT[0:4], $\overline{CI}$, $\overline{WT}$, and $\overline{GBL}$.

If address or data parity is not used by the system, and respective parity checking is disabled through HID1, the input receivers for those pins are disabled and do not require pull-up resistors, and may be left unconnected by the system. If extended addressing is not used (HID0[XAEN] = 0), A[0:3] are unused and must be pulled low to GND through weak pull-down resistors; additionally, if address parity checking is enabled (HID1[EBA] = 1) and extended addressing is not used, AP[0] must be pulled up to OV_{DD} through a weak pull-up resistor. If the PC7447A is in 60x bus mode, DTI[0:3] must be pulled low to GND through weak pull-down resistors. The data bus input receivers are normally turned off when no read operation is in progress and, therefore, do not require pull-up resistors on the bus. Other data bus receivers in the system, however, may require pull-ups, or that those signals be otherwise driven by the system during inactive periods by the system. The data bus signals are: D[0:63] and DP[0:7].

Figure 12-3. JTAG Interface Connection



Notes:
1. RUN/$\overline{\text{STOP}}$, normally found on pin 5 of the COP header, is not implemented on the PC7447A. Connect pin 5 of the COP header to OV_{DD} with a 10 kΩ pull-up resistor.
2. Key location; pin 14 is not physically present on the COP header.
3. Component not populated. Populate only if debug tool does not drive $\overline{\text{QACK}}$.
4. Populate only if debug tool uses an open-drain type output and does not actively de-assert $\overline{\text{QACK}}$.
5. If the JTAG interface is implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ from the COP header though an AND gate to $\overline{\text{TRST}}$ of the part. If the JTAG interface is not implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ of the part through a 0Ω isolation resistor.
6. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown above.

15. Document Revision History

Table 15-1 provides a revision history for this hardware specification.

Table 15-1. Document Revision History

Revision Number	Date	Substantive Change(s)
E	01/07	Name change from Atmel to e2v
D	07/06	Page 35: b parameter modification; remove preliminary.
C	12/05	Add RoHS package and LGA package.
B	07/05	Changed die size.
		Table 9-2 on page 25: Modified jitter specifications to conform to JEDEC standards, changed jitter specification to cycle-to-cycle jitter (instead of long- and short-term jitter); changed jitter bandwidth recommendations.
		Added t_{KHTSV}, t_{KHARV}, t_{KHTSX}, and t_{KHARX} to Table 9-3 on page 27; these were previously grouped with t_{KHOV} and t_{KHOX}. Note: Documentation change only; the values for the output valid and output hold AC timing specifications remain unchanged for $\overline{TS}$, $\overline{ARTRY}$, and $\overline{SHD}$[0:1].
A	04/04	Initial revision.

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