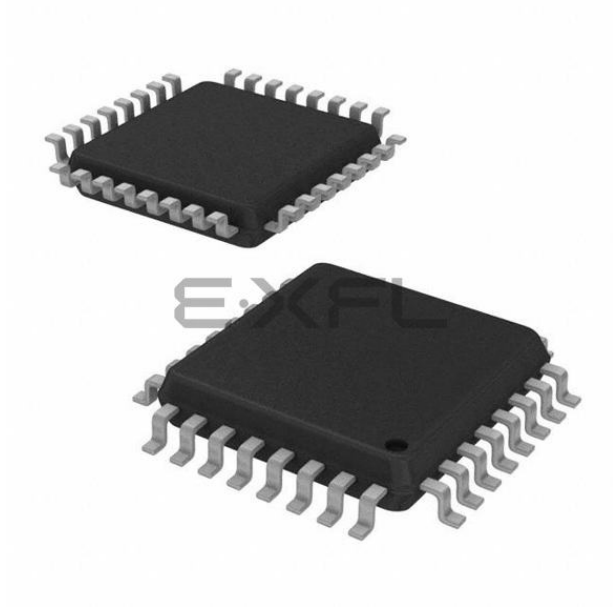

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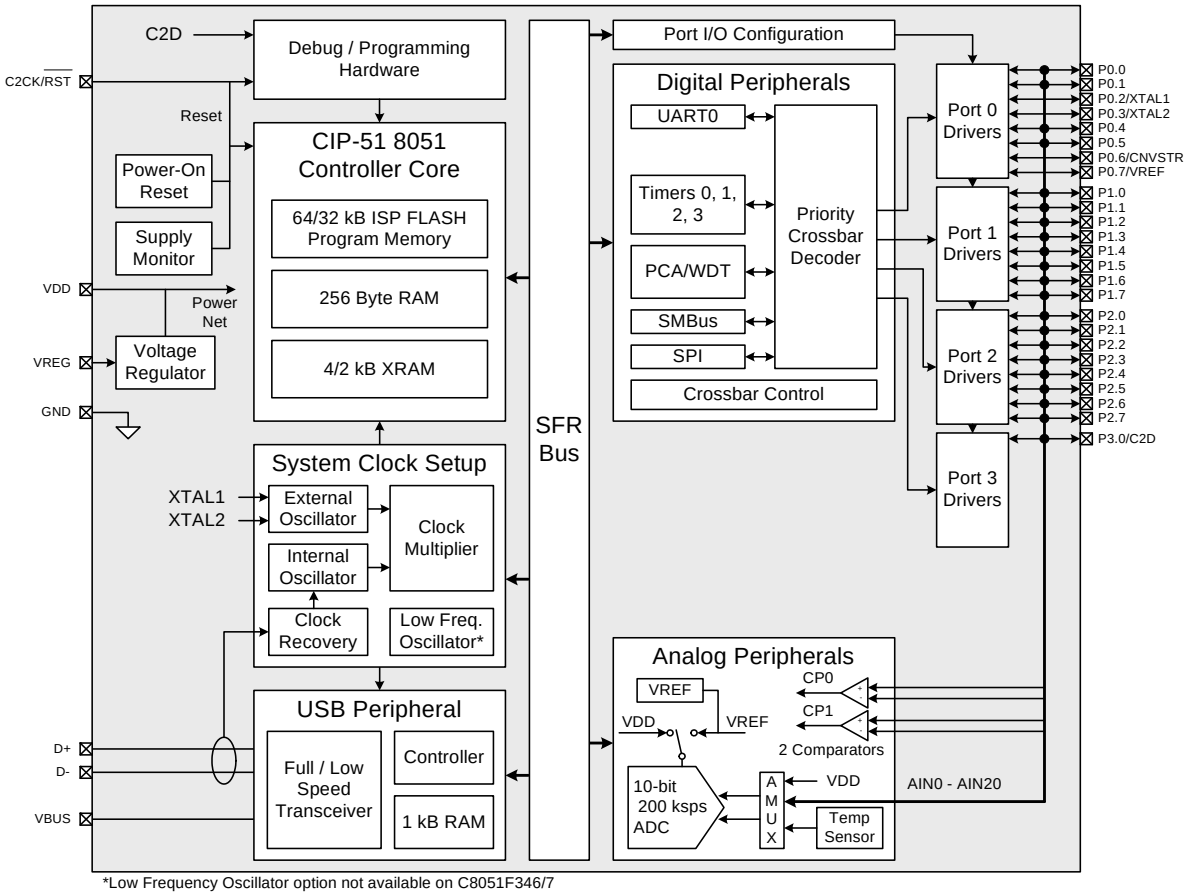
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	8051
Core Size	8-Bit
Speed	48MHz
Connectivity	SMBus (2-Wire/I²C), SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	25
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 21x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f342-gqr



*Low Frequency Oscillator option not available on C8051F346/7

Figure 1.2. C8051F342/3/6/7 Block Diagram

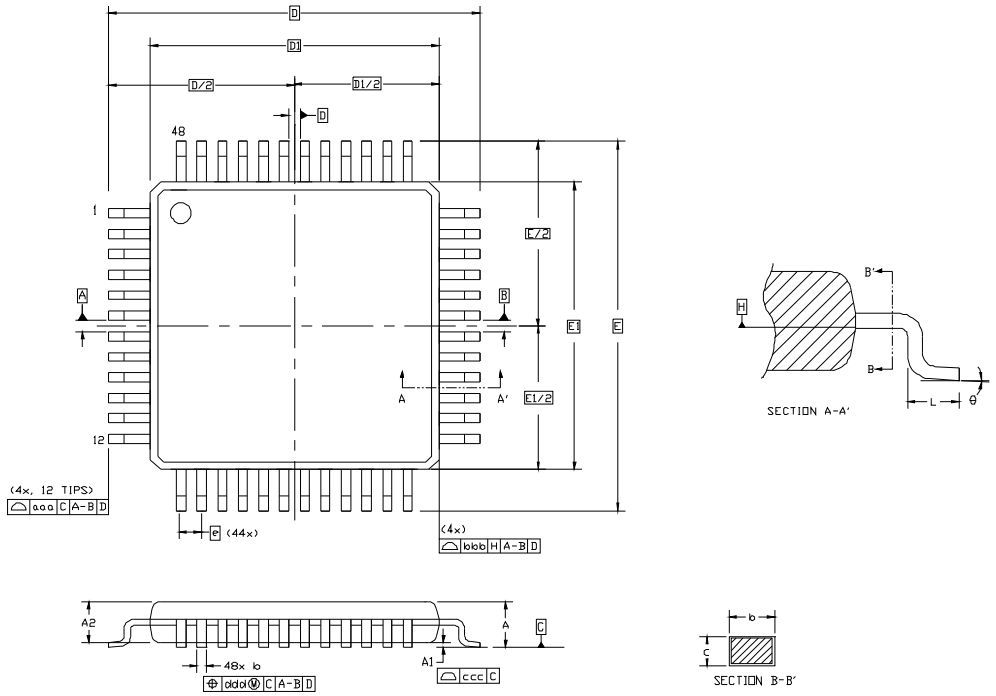


Figure 4.2. TQFP-48 Package Diagram

Table 4.2. TQFP-48 Package Dimensions

Dimension	Min	Nom	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.09	—	0.20
D	9.00 BSC		
D1	7.00 BSC		
e	0.50 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.45	0.60	0.75
aaa	0.20		
bbb	0.20		
ccc	0.08		
ddd	0.08		
θ	0°	3.5°	7°

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MS-026, variation ABC.
4. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

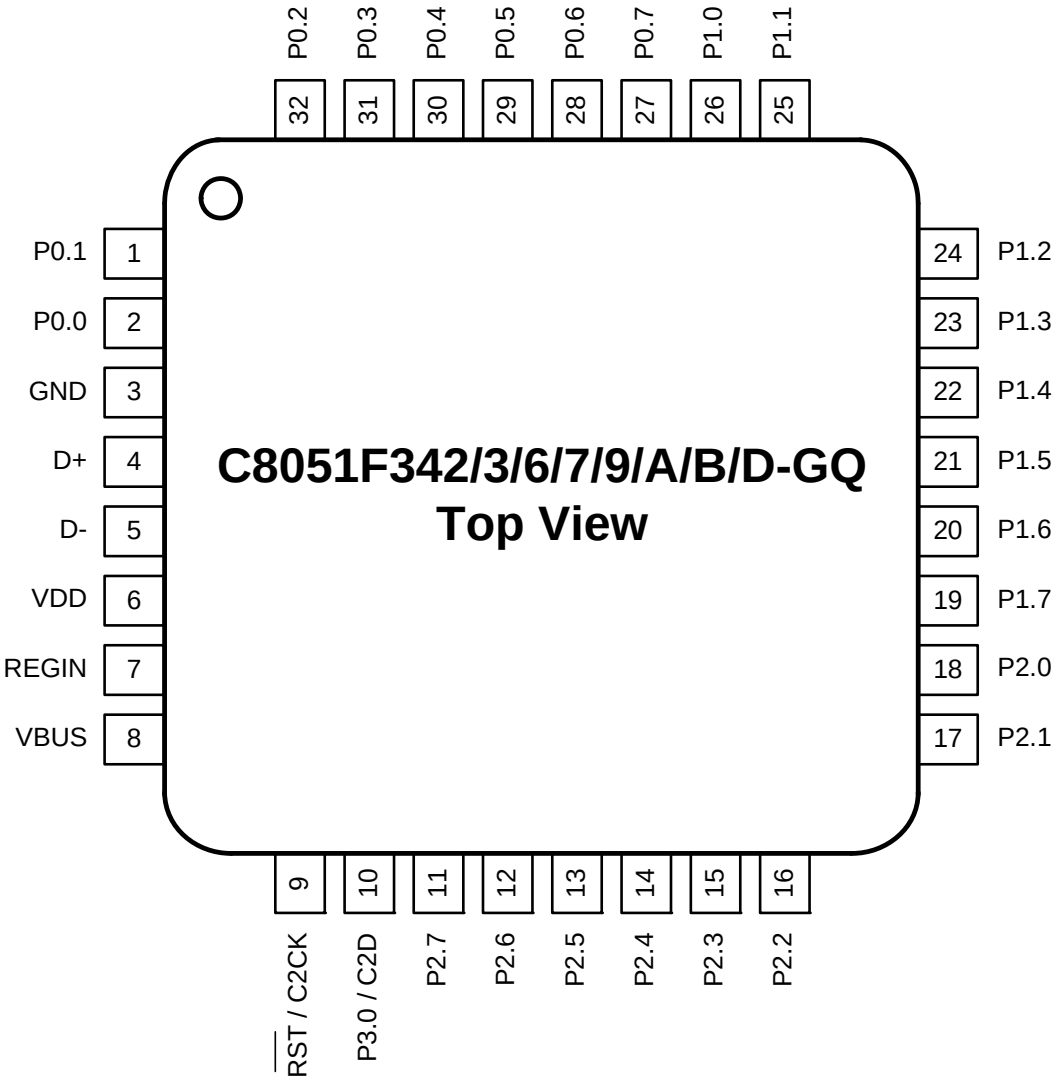


Figure 4.4. LQFP-32 Pinout Diagram (Top View)

5.3.2. Tracking Modes

The AD0TM bit in register ADC0CN controls the ADC0 track-and-hold mode. In its default state, the ADC0 input is continuously tracked, except when a conversion is in progress. When the AD0TM bit is logic 1, ADC0 operates in low-power track-and-hold mode. In this mode, each conversion is preceded by a tracking period of 3 SAR clocks (after the start-of-conversion signal). When the CNVSTR signal is used to initiate conversions in low-power tracking mode, ADC0 tracks only when CNVSTR is low; conversion begins on the rising edge of CNVSTR (see Figure 5.4). Tracking can also be disabled (shutdown) when the device is in low power standby or sleep modes. Low-power track-and-hold mode is also useful when AMUX settings are frequently changed, due to the settling time requirements described in **Section "5.3.3. Settling Time Requirements" on page 47**.

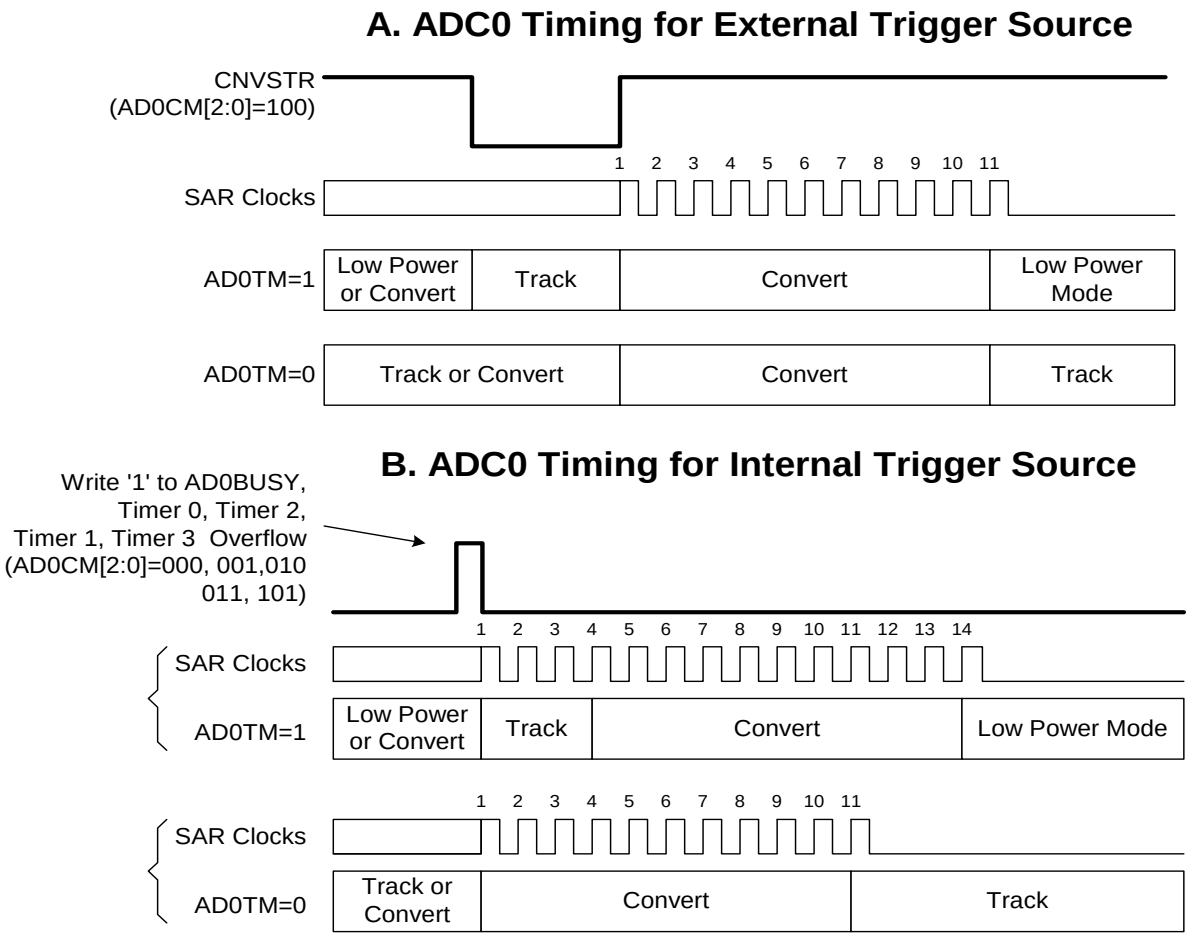


Figure 5.4. 10-Bit ADC Track and Conversion Example Timing

Table 9.3. Special Function Registers

SFRs are listed in alphabetical order. All undefined SFR locations are reserved.

Register	Address	Description	Page
ACC	0xE0	Accumulator	87
ADC0CF	0xBC	ADC0 Configuration	50
ADC0CN	0xE8	ADC0 Control	51
ADC0GTH	0xC4	ADC0 Greater-Than Compare High	52
ADC0GTL	0xC3	ADC0 Greater-Than Compare Low	52
ADC0H	0xBE	ADC0 High	50
ADC0L	0xBD	ADC0 Low	50
ADC0LTH	0xC6	ADC0 Less-Than Compare Word High	53
ADC0LTL	0xC5	ADC0 Less-Than Compare Word Low	53
AMX0N	0xBA	AMUX0 Negative Channel Select	49
AMX0P	0xBB	AMUX0 Positive Channel Select	48
B	0xF0	B Register	88
CKCON	0x8E	Clock Control	241
CLKMUL	0xB9	Clock Multiplier	138
CLKSEL	0xA9	Clock Select	140
CPT0CN	0x9B	Comparator0 Control	62
CPT0MD	0x9D	Comparator0 Mode Selection	64
CPT0MX	0x9F	Comparator0 MUX Selection	63
CPT1CN	0x9A	Comparator1 Control	65
CPT1MD	0x9C	Comparator1 Mode Selection	67
CPT1MX	0x9E	Comparator1 MUX Selection	66
DPH	0x83	Data Pointer High	86
DPL	0x82	Data Pointer Low	86
EIE1	0xE6	Extended Interrupt Enable 1	93
EIE2	0xE7	Extended Interrupt Enable 2	95
EIP1	0xF6	Extended Interrupt Priority 1	94
EIP2	0xF7	Extended Interrupt Priority 2	95
EMI0CN	0xAA	External Memory Interface Control	117
EMI0CF	0x85	External Memory Interface Configuration	118
EMI0TC	0x84	External Memory Interface Timing	123
FLKEY	0xB7	Flash Lock and Key	112
FLSCL	0xB6	Flash Scale	113
IE	0xA8	Interrupt Enable	91
IP	0xB8	Interrupt Priority	92
IT01CF	0xE4	INT0/INT1 Configuration	96
OSCICL	0xB3	Internal Oscillator Calibration	133
OSCICN	0xB2	Internal Oscillator Control	132
OSCLCN	0x86	Internal Low-Frequency Oscillator Control	134
OSCXCN	0xB1	External Oscillator Control	137
P0	0x80	Port 0 Latch	150
P0MDIN	0xF1	Port 0 Input Mode Configuration	150
P0MDOUT	0xA4	Port 0 Output Mode Configuration	151
P0SKIP	0xD4	Port 0 Skip	151
P1	0x90	Port 1 Latch	152

Table 9.3. Special Function Registers (Continued)

SFRs are listed in alphabetical order. All undefined SFR locations are reserved.

Register	Address	Description	Page
SBUF0	0x99	UART0 Data Buffer	211
SCON0	0x98	UART0 Control	210
SMB0CF	0xC1	SMBus Configuration	194
SMB0CN	0xC0	SMBus Control	196
SMB0DAT	0xC2	SMBus Data	198
SMOD1	0xE5	UART1 Mode	219
SP	0x81	Stack Pointer	86
SPI0CFG	0xA1	SPI Configuration	229
SPI0CKR	0xA2	SPI Clock Rate Control	231
SPI0CN	0xF8	SPI Control	230
SPI0DAT	0xA3	SPI Data	231
TCON	0x88	Timer/Counter Control	239
TH0	0x8C	Timer/Counter 0 High	242
TH1	0x8D	Timer/Counter 1 High	242
TL0	0x8A	Timer/Counter 0 Low	242
TL1	0x8B	Timer/Counter 1 Low	242
TMOD	0x89	Timer/Counter Mode	240
TMR2CN	0xC8	Timer/Counter 2 Control	247
TMR2H	0xCD	Timer/Counter 2 High	248
TMR2L	0xCC	Timer/Counter 2 Low	248
TMR2RLH	0xCB	Timer/Counter 2 Reload High	248
TMR2RLL	0xCA	Timer/Counter 2 Reload Low	248
TMR3CN	0x91	Timer/Counter 3Control	253
TMR3H	0x95	Timer/Counter 3 High	254
TMR3L	0x94	Timer/Counter 3Low	254
TMR3RLH	0x93	Timer/Counter 3 Reload High	254
TMR3RLL	0x92	Timer/Counter 3 Reload Low	254
VDM0CN	0xFF	V_{DD} Monitor Control	102
USB0ADR	0x96	USB0 Indirect Address Register	163
USB0DAT	0x97	USB0 Data Register	164
USB0XCN	0xD7	USB0 Transceiver Control	161
XBR0	0xE1	Port I/O Crossbar Control 0	148
XBR1	0xE2	Port I/O Crossbar Control 1	149
XBR2	0xE3	Port I/O Crossbar Control 2	149
All Other Addresses		Reserved	

SFR Definition 9.11. EIE2: Extended Interrupt Enable 2

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	-	-	-	-	ES1	EVBUS	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xE7

Bits7–2: UNUSED. Read = 000000b. Write = don't care.
Bit1: ES1: Enable UART1 Interrupt.
This bit sets the masking of the UART1 interrupt.
0: Disable UART1 interrupt.
1: Enable UART1 interrupt.
Bit0: EVBUS: Enable VBUS Level Interrupt.
This bit sets the masking of the VBUS interrupt.
0: Disable all VBUS interrupts.
1: Enable interrupt requests generated by VBUS level sense.

SFR Definition 9.12. EIP2: Extended Interrupt Priority 2

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	-	-	-	-	PS1	PVBUS	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xF7

Bits7–2: UNUSED. Read = 000000b. Write = don't care.
Bit1: PS1: UART1 Interrupt Priority Control.
This bit sets the priority of the UART1 interrupt.
0: UART1 interrupt set to low priority level.
1: UART1 interrupts set to high priority level.
Bit0: PVBUS: VBUS Level Interrupt Priority Control.
This bit sets the priority of the VBUS interrupt.
0: VBUS interrupt set to low priority level.
1: VBUS interrupt set to high priority level.

SFR Definition 14.2. OSCICL: Internal H-F Oscillator Calibration

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	-	OSCCAL					Variable
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xB3

Bits4–0: OSCCAL: Oscillator Calibration Value
These bits determine the internal H-F oscillator period. When set to 00000b, the oscillator operates at its fastest setting. When set to 11111b, the oscillator operates at is slowest setting. The contents of this register are factory calibrated to produce a 12 MHz internal oscillator frequency.

Note: The contents of this register are undefined when Clock Recovery is enabled. See Section "16.4. USB Clock Configuration" on page 166 for details on Clock Recovery.

14.2. Programmable Internal Low-Frequency (L-F) Oscillator

The C8051F340/1/2/3/4/5/8/9/C/D devices include a programmable internal oscillator which operates at a nominal frequency of 80 kHz. The low-frequency oscillator circuit includes a divider that can be changed to divide the clock by 1, 2, 4, or 8, using the OSCLD bits in the OSCLCN register (see SFR Definition 14.3). Additionally, the OSCLF bits (OSCLCN5:2) can be used to adjust the oscillator's output frequency.

14.2.1. Calibrating the Internal L-F Oscillator

Timers 2 and 3 include capture functions that can be used to capture the oscillator frequency, when running from a known time base. When either Timer 2 or Timer 3 is configured for L-F Oscillator Capture Mode, a falling edge (Timer 2) or rising edge (Timer 3) of the low-frequency oscillator's output will cause a capture event on the corresponding timer. As a capture event occurs, the current timer value (TMRnH:TMRnL) is copied into the timer reload registers (TMRnRLH:TMRnRLL). By recording the difference between two successive timer capture values, the low-frequency oscillator's period can be calculated. The OSCLF bits can then be adjusted to produce the desired oscillator period.

14.5. System and USB Clock Selection

The internal oscillator requires little start-up time and may be selected as the system or USB clock immediately following the OSCICN write that enables the internal oscillator. External crystals and ceramic resonators typically require a start-up time before they are settled and ready for use. The Crystal Valid Flag (XTLVLD in register OSCXCN) is set to '1' by hardware when the external oscillator is settled. **To avoid reading a false XTLVLD, in crystal mode software should delay at least 1 ms between enabling the external oscillator and checking XTLVLD.** RC and C modes typically require no startup time.

14.5.1. System Clock Selection

The CLKSL[1:0] bits in register CLKSEL select which oscillator source is used as the system clock. CLKSL[1:0] must be set to 01b for the system clock to run from the external oscillator; however the external oscillator may still clock certain peripherals (timers, PCA, USB) when the internal oscillator is selected as the system clock. The system clock may be switched on-the-fly between the internal oscillator, external oscillator, and 4x Clock Multiplier so long as the selected oscillator is enabled and has settled. C8051F340/1/2/3 devices can use the 48 MHz Clock Multiplier output as system clock. See Table 3.1, "Global DC Electrical Characteristics," on page 25 for system clock frequency specifications. When operating with a system clock of greater than 25 MHz (up to 48 MHz), the FLRT bit (FLSCL.4) should be set to '1'. See **Section "10. Prefetch Engine" on page 99** for more details.

14.5.2. USB Clock Selection

The USBCLK[2:0] bits in register CLKSEL select which oscillator source is used as the USB clock. The USB clock may be derived from the 4x Clock Multiplier output, a divided version of the internal oscillator, or a divided version of the external oscillator. Note that the USB clock must be 48 MHz when operating USB0 as a Full Speed Function; the USB clock must be 6 MHz when operating USB0 as a Low Speed Function. See SFR Definition 14.6 for USB clock selection options.

Some example USB clock configurations for Full and Low Speed mode are given below:

Internal Oscillator		
Clock Signal	**Input Source Selection**	**Register Bit Settings**
USB Clock	Clock Multiplier	USBCLK = 000b
Clock Multiplier Input	Internal Oscillator*	MULSEL = 00b
Internal Oscillator	Divide by 1	IFCN = 11b
External Oscillator		
Clock Signal	**Input Source Selection**	**Register Bit Settings**
USB Clock	Clock Multiplier	USBCLK = 000b
Clock Multiplier Input	External Oscillator	MULSEL = 01b
External Oscillator	Crystal Oscillator Mode 12 MHz Crystal	XOSCMD = 110b XFCN = 111b

***Note:** Clock Recovery must be enabled for this configuration.

Internal Oscillator		
Clock Signal	**Input Source Selection**	**Register Bit Settings**
USB Clock	Internal Oscillator / 2	USBCLK = 001b
Internal Oscillator	Divide by 1	IFCN = 11b
External Oscillator		
Clock Signal	**Input Source Selection**	**Register Bit Settings**

SFR Definition 15.11. P1SKIP: Port1 Skip

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xD5

Bits7–0: P1SKIP[7:0]: Port1 Crossbar Skip Enable Bits.
These bits select Port pins to be skipped by the Crossbar Decoder. Port pins used as analog inputs (for ADC or Comparator) or used as special functions (VREF input, external oscillator circuit, CNVSTR input) should be skipped by the Crossbar.
0: Corresponding P1.n pin is not skipped by the Crossbar.
1: Corresponding P1.n pin is skipped by the Crossbar.

SFR Definition 15.12. P2: Port2 Latch

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
							(bit addressable)	0xA0

Bits7–0: P2.[7:0]
Write - Output appears on I/O pins per Crossbar Registers (when XBARE = ‘1’).
0: Logic Low Output.
1: Logic High Output (high impedance if corresponding P2MDOUT.n bit = 0).
Read - Always reads ‘0’ if selected as analog input in register P2MDIN. Directly reads Port pin when configured as digital input.
0: P2.n pin is logic low.
1: P2.n pin is logic high.

SFR Definition 15.13. P2MDIN: Port2 Input Mode

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xF3

Bits7-0: Analog Input Configuration Bits for P2.7-P2.0 (respectively).
Port pins configured as analog inputs have their weak pull-up, digital driver, and digital receiver disabled.
0: Corresponding P2.n pin is configured as an analog input.
1: Corresponding P2.n pin is not configured as an analog input.

SFR Definition 16.2. USB0ADR: USB0 Indirect Address

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
BUSY	AUTORD	USBADDR						00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0x96

Bits7: BUSY: USB0 Register Read Busy Flag
This bit is used during indirect USB0 register accesses. Software should write '1' to this bit to initiate a read of the USB0 register targeted by the USBADDR bits (USB0ADR.[5-0]). The target address and BUSY bit may be written in the same write to USB0ADR. After BUSY is set to '1', hardware will clear BUSY when the targeted register data is ready in the USB0DAT register. Software should check BUSY for '0' before writing to USB0DAT.
Write:
0: No effect.
1: A USB0 indirect register read is initiated at the address specified by the USBADDR bits.
Read:
0: USB0DAT register data is valid.
1: USB0 is busy accessing an indirect register; USB0DAT register data is invalid.

Bit6: AUTORD: USB0 Register Auto-read Flag
This bit is used for block FIFO reads.
0: BUSY must be written manually for each USB0 indirect register read.
1: The next indirect register read will automatically be initiated when software reads USB0DAT (USBADDR bits will not be changed).

Bits5–0: USBADDR: USB0 Indirect Register Address
These bits hold a 6-bit address used to indirectly access the USB0 core registers. Table 16.2 lists the USB0 core registers and their indirect addresses. Reads and writes to USB0DAT will target the register indicated by the USBADDR bits.

USB Register Definition 16.20. EINCSRH: USB0 IN Endpoint Control High Byte

R/W	R/W	R/W	R	R/W	R/W	R	R	Reset Value
DBIEN	ISO	DIRSEL	-	FCDT	SPLIT	-	-	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	USB Address: 0x12

Bit7: DBIEN: IN Endpoint Double-buffer Enable.
0: Double-buffering disabled for the selected IN endpoint.
1: Double-buffering enabled for the selected IN endpoint.

Bit6: ISO: Isochronous Transfer Enable.
This bit enables/disables isochronous transfers on the current endpoint.
0: Endpoint configured for bulk/interrupt transfers.
1: Endpoint configured for isochronous transfers.

Bit5: DIRSEL: Endpoint Direction Select.
This bit is valid only when the selected FIFO is not split (SPLIT = ‘0’).
0: Endpoint direction selected as OUT.
1: Endpoint direction selected as IN.

Bit4: Unused. Read = ‘0’. Write = don’t care.

Bit3: FCDT: Force Data Toggle.
0: Endpoint data toggle switches only when an ACK is received following a data packet transmission.
1: Endpoint data toggle forced to switch after every data packet is transmitted, regardless of ACK reception.

Bit2: SPLIT: FIFO Split Enable.
When SPLIT = ‘1’, the selected endpoint FIFO is split. The upper half of the selected FIFO is used by the IN endpoint; the lower half of the selected FIFO is used by the OUT endpoint.

Bits1–0: Unused. Read = 00b; Write = don’t care.

16.13. Controlling Endpoints1-3 OUT

Endpoints1-3 OUT are managed via USB registers EOUTCSRL and EOUTCSRH. All OUT endpoints can be used for Interrupt, Bulk, or Isochronous transfers. Isochronous (ISO) mode is enabled by writing ‘1’ to the ISO bit in register EOUTCSRH. Bulk and Interrupt transfers are handled identically by hardware.

An Endpoint1-3 OUT interrupt may be generated by the following:

1. Hardware sets the OPRDY bit (EINCSRL.0) to ‘1’.
2. Hardware generates a STALL condition.

16.13.1.Endpoints1-3 OUT Interrupt or Bulk Mode

When the ISO bit (EOUTCSRH.6) = ‘0’ the target endpoint operates in Bulk or Interrupt mode. Once an endpoint has been configured to operate in Bulk/Interrupt OUT mode (typically following an Endpoint0 SET_INTERFACE command), hardware will set the OPRDY bit (EOUTCSRL.0) to ‘1’ and generate an interrupt upon reception of an OUT token and data packet. The number of bytes in the current OUT data packet (the packet ready to be unloaded from the FIFO) is given in the EOUTCNTH and EOUTCNTL registers. In response to this interrupt, firmware should unload the data packet from the OUT FIFO and reset the OPRDY bit to ‘0’.

Table 17.4. SMBus Status Decoding

Mode	Values Read				Current SMbus State	Typical Response Options	Values Written		
	Status Vector	ACKRQ	ARBLOST	ACK			STA	STo	ACK
Master Transmitter	1110	0	0	X	A master START was generated.	Load slave address + R/W into SMB0DAT.	0	0	X
	1100	0	0	0	A master data or address byte was transmitted; NACK received.	Set STA to restart transfer.	1	0	X
						Abort transfer.	0	1	X
		0	0	1	A master data or address byte was transmitted; ACK received.	Load next data byte into SMB0DAT.	0	0	X
						End transfer with STOP.	0	1	X
						End transfer with STOP and start another transfer.	1	1	X
						Send repeated START.	1	0	X
						Switch to Master Receiver Mode (clear SI without writing new data to SMB0DAT).	0	0	X
Master Receiver	1000	1	0	X	A master data byte was received; ACK requested.	Acknowledge received byte; Read SMB0DAT.	0	0	1
						Send NACK to indicate last byte, and send STOP.	0	1	0
						Send NACK to indicate last byte, and send STOP followed by START.	1	1	0
						Send ACK followed by repeated START.	1	0	1
						Send NACK to indicate last byte, and send repeated START.	1	0	0
						Send ACK and switch to Master Transmitter Mode (write to SMB0DAT before clearing SI).	0	0	1
						Send NACK and switch to Master Transmitter Mode (write to SMB0DAT before clearing SI).	0	0	0

18. UART0

UART0 is an asynchronous, full duplex serial port offering modes 1 and 3 of the standard 8051 UART. Enhanced baud rate support allows a wide range of clock sources to generate standard baud rates (details in **Section "18.1. Enhanced Baud Rate Generation" on page 206**). Received data buffering allows UART0 to start reception of a second incoming data byte before software has finished reading the previous data byte.

UART0 has two associated SFRs: Serial Control Register 0 (SCON0) and Serial Data Buffer 0 (SBUF0). The single SBUF0 location provides access to both transmit and receive registers. **Writes to SBUF0 always access the Transmit register. Reads of SBUF0 always access the buffered Receive register; it is not possible to read data from the Transmit register.**

With UART0 interrupts enabled, an interrupt is generated each time a transmit is completed (TI0 is set in SCON0), or a data byte has been received (RI0 is set in SCON0). The UART0 interrupt flags are not cleared by hardware when the CPU vectors to the interrupt service routine. They must be cleared manually by software, allowing software to determine the cause of the UART0 interrupt (transmit complete or receive complete).

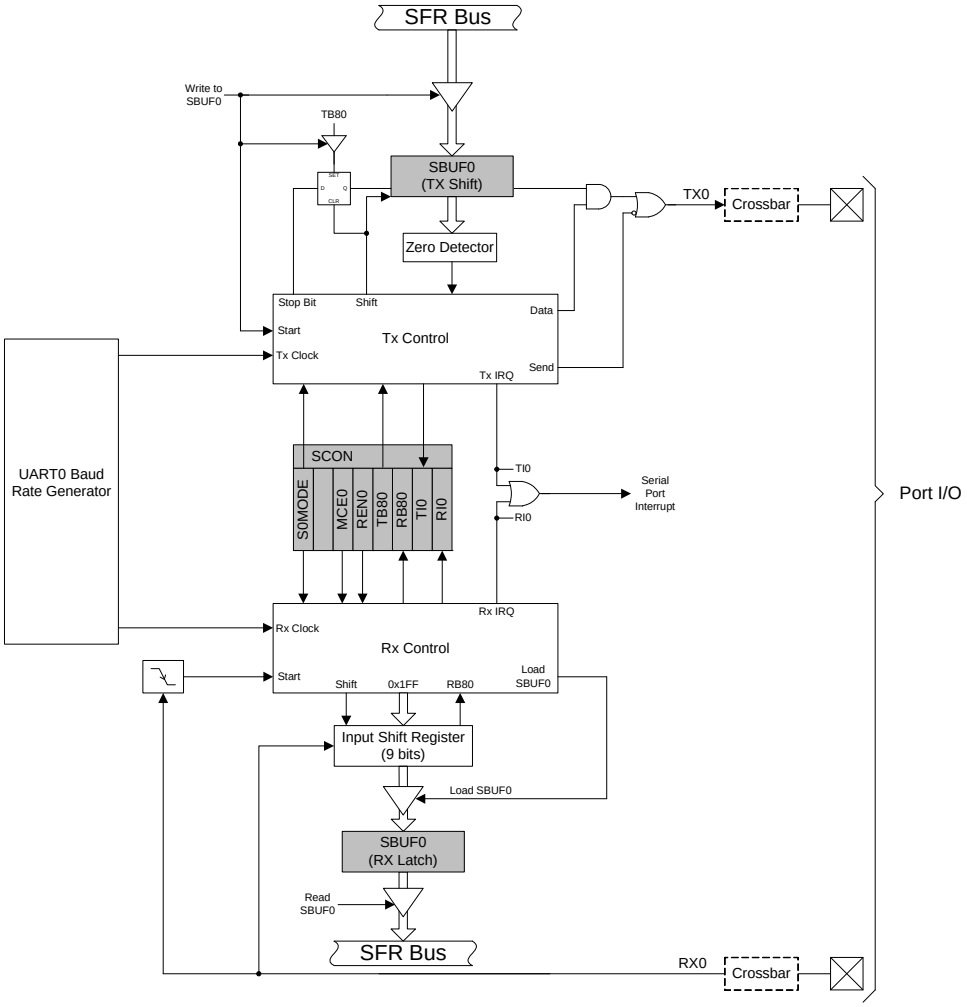


Figure 18.1. UART0 Block Diagram

SFR Definition 21.9. TMR2RLL: Timer 2 Reload Register Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xCA

Bits 7–0: TMR2RLL: Timer 2 Reload Register Low Byte.
TMR2RLL holds the low byte of the reload value for Timer 2 when operating in auto-reload mode, or the captured value of the TMR2L register in capture mode.

SFR Definition 21.10. TMR2RLH: Timer 2 Reload Register High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xCB

Bits 7–0: TMR2RLH: Timer 2 Reload Register High Byte.
The TMR2RLH holds the high byte of the reload value for Timer 2 when operating in auto-reload mode, or the captured value of the TMR2H register in capture mode.

SFR Definition 21.11. TMR2L: Timer 2 Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xCC

Bits 7–0: TMR2L: Timer 2 Low Byte.
In 16-bit mode, the TMR2L register contains the low byte of the 16-bit Timer 2. In 8-bit mode, TMR2L contains the 8-bit low byte timer value.

SFR Definition 21.12. TMR2H Timer 2 High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xCD

Bits 7–0: TMR2H: Timer 2 High Byte.
In 16-bit mode, the TMR2H register contains the high byte of the 16-bit Timer 2. In 8-bit mode, TMR2H contains the 8-bit high byte timer value.

SFR Definition 21.14. TMR3RLL: Timer 3 Reload Register Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0x92

Bits 7–0: TMR3RLL: Timer 3 Reload Register Low Byte.
TMR3RLL holds the low byte of the reload value for Timer 3 when operating in auto-reload mode, or the captured value of the TMR3L register when operating in capture mode.

SFR Definition 21.15. TMR3RLH: Timer 3 Reload Register High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0x93

Bits 7–0: TMR3RLH: Timer 3 Reload Register High Byte.
The TMR3RLH holds the high byte of the reload value for Timer 3 when operating in auto-reload mode, or the captured value of the TMR3H register when operating in capture mode.

SFR Definition 21.16. TMR3L: Timer 3 Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0x94

Bits 7–0: TMR3L: Timer 3 Low Byte.
In 16-bit mode, the TMR3L register contains the low byte of the 16-bit Timer 3. In 8-bit mode, TMR3L contains the 8-bit low byte timer value.

SFR Definition 21.17. TMR3H Timer 3 High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0x95

Bits 7–0: TMR3H: Timer 3 High Byte.
In 16-bit mode, the TMR3H register contains the high byte of the 16-bit Timer 3. In 8-bit mode, TMR3H contains the 8-bit high byte timer value.

SFR Definition 22.3. PCA0CPMn: PCA Capture/Compare Mode

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
PWM16n	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xDA, 0xDB, 0xDC, 0xDD, 0xDE

PCA0CPMn Address: PCA0CPM0 = 0xDA (n = 0), PCA0CPM1 = 0xDB (n = 1),
PCA0CPM2 = 0xDC (n = 2), PCA0CPM3 = 0xDD (n = 3),
PCA0CPM4 = 0xDE (n = 4)

Bit7: PWM16n: 16-bit Pulse Width Modulation Enable.
This bit selects 16-bit mode when Pulse Width Modulation mode is enabled (PWMn = 1).
0: 8-bit PWM selected.
1: 16-bit PWM selected.

Bit6: ECOMn: Comparator Function Enable.
This bit enables/disables the comparator function for PCA module n.
0: Disabled.
1: Enabled.

Bit5: CAPPn: Capture Positive Function Enable.
This bit enables/disables the positive edge capture for PCA module n.
0: Disabled.
1: Enabled.

Bit4: CAPNn: Capture Negative Function Enable.
This bit enables/disables the negative edge capture for PCA module n.
0: Disabled.
1: Enabled.

Bit3: MATn: Match Function Enable.
This bit enables/disables the match function for PCA module n. When enabled, matches of the PCA counter with a module's capture/compare register cause the CCFn bit in PCA0MD register to be set to logic 1.
0: Disabled.
1: Enabled.

Bit2: TOGn: Toggle Function Enable.
This bit enables/disables the toggle function for PCA module n. When enabled, matches of the PCA counter with a module's capture/compare register cause the logic level on the CEXn pin to toggle. If the PWMn bit is also set to logic 1, the module operates in Frequency Output Mode.
0: Disabled.
1: Enabled.

Bit1: PWMn: Pulse Width Modulation Mode Enable.
This bit enables/disables the PWM function for PCA module n. When enabled, a pulse width modulated signal is output on the CEXn pin. 8-bit PWM is used if PWM16n is cleared; 16-bit mode is used if PWM16n is set to logic 1. If the TOGn bit is also set, the module operates in Frequency Output Mode.
0: Disabled.
1: Enabled.

Bit0: ECCFn: Capture/Compare Flag Interrupt Enable.
This bit sets the masking of the Capture/Compare Flag (CCFn) interrupt.
0: Disable CCFn interrupts.
1: Enable a Capture/Compare Flag interrupt request when CCFn is set.

23.2. C2 Pin Sharing

The C2 protocol allows the C2 pins to be shared with user functions so that in-system debugging and Flash programming functions may be performed. This is possible because C2 communication is typically performed when the device is in the halt state, where all on-chip peripherals and user software are stalled. In this halted state, the C2 interface can safely ‘borrow’ the C2CK (RST) and C2D (P3.0) pins. Note that the C2D pin is shared on the 32-pin packages only (C8051F342/3/6/7/9/A/B). In most applications, external resistors are required to isolate C2 interface traffic from the user application. A typical isolation configuration is shown in Figure 23.1.

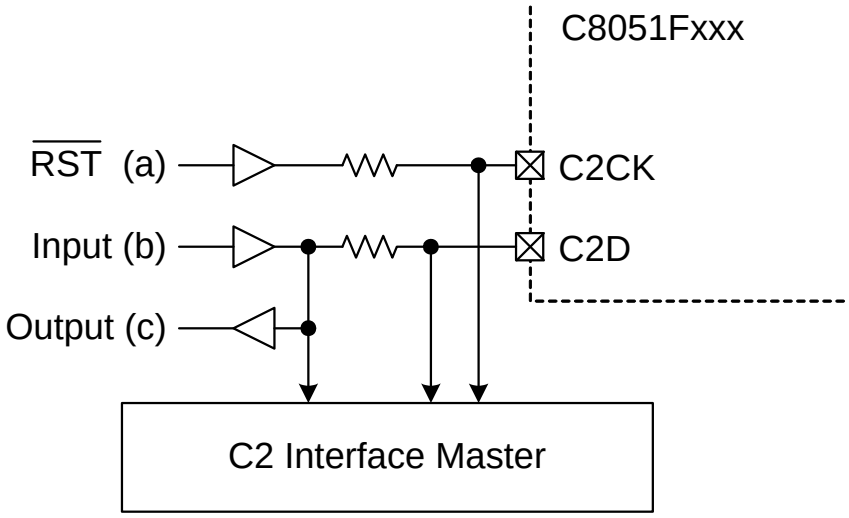


Figure 23.1. Typical C2 Pin Sharing

The configuration in Figure 23.1 assumes the following:

1. The user input (b) cannot change state while the target device is halted.
2. The RST pin on the target device is used as an input only.

Additional resistors may be necessary depending on the specific application.