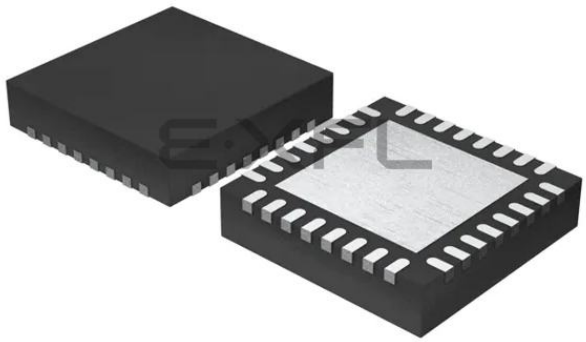

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SMBus (2-Wire/I²C), SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f349-gmr

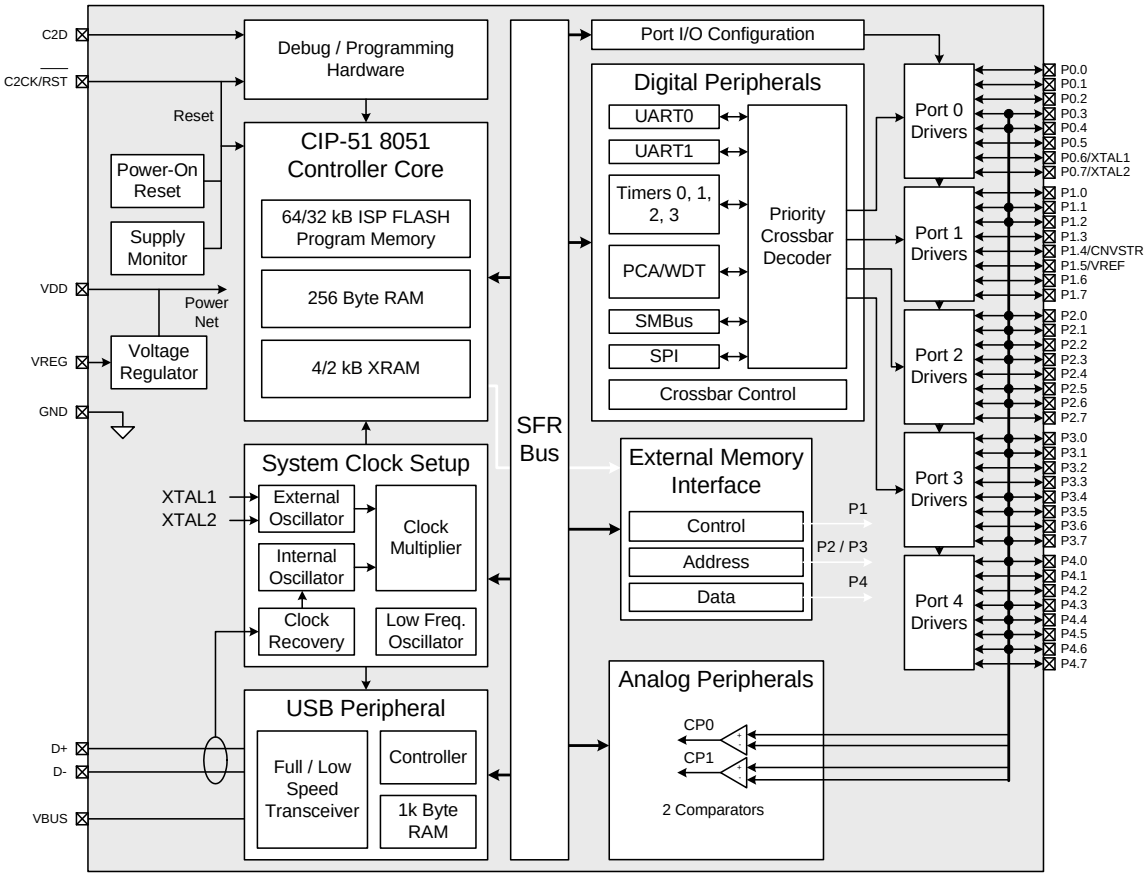

Figure 1.3. C8051F348/C Block Diagram

Table 3.2. Index to Electrical Characteristics Tables

Table Title	Page No.
ADC0 Electrical Characteristics	56
Voltage Reference Electrical Characteristics	58
Comparator Electrical Characteristics	68
Voltage Regulator Electrical Specifications	69
Reset Electrical Characteristics	106
Flash Electrical Characteristics	109
AC Parameters for External Memory Interface	130
Oscillator Electrical Characteristics	141
Port I/O DC Electrical Characteristics	158
USB Transceiver Electrical Characteristics	187

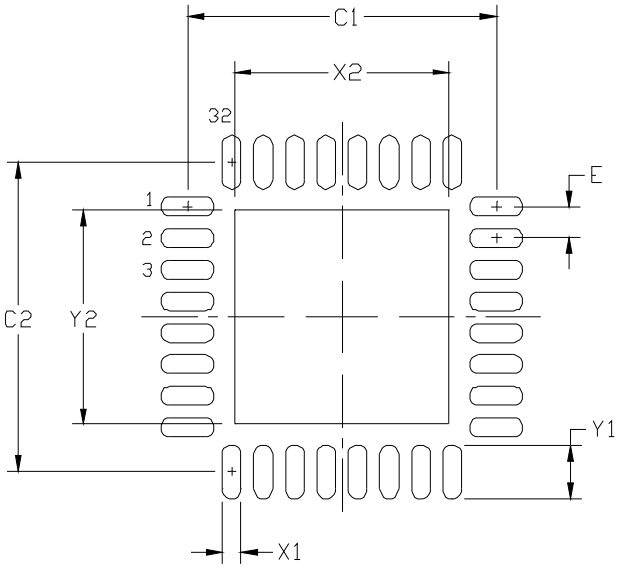

Figure 4.9. QFN-32 Recommended PCB Land Pattern

Table 4.7. QFN-32 PCB Land Pattern Dimesions

Dimension	Min	Max
C1	4.80	4.90
C2	4.80	4.90
E	0.50 BSC	
X1	0.20	0.30

Dimension	Min	Max
X2	3.20	3.40
Y1	0.75	0.85
Y2	3.20	3.40

Notes:

General:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design:

3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60µm minimum, all the way around the pad.

Stencil Design:

4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pins.
7. A 3x3 array of 1.0 mm openings on a 1.2mm pitch should be used for the center pad to assure the proper paste volume.

Card Assembly:

8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

5. 10-Bit ADC (ADC0, C8051F340/1/2/3/4/5/6/7/A/B Only)

The ADC0 subsystem for the C8051F34x devices consists of two analog multiplexers (referred to collectively as AMUX0), and a 200 ksps, 10-bit successive-approximation-register ADC with integrated track-and-hold and programmable window detector. The AMUX0, data conversion modes, and window detector are all configured under software control via the Special Function Registers shown in Figure 5.1. ADC0 operates in both Single-ended and Differential modes, and may be configured to measure voltages at port pins, the Temperature Sensor output, or V_{DD} with respect to a port pin, VREF, or GND. The connection options for AMUX0 are detailed in SFR Definition 5.1 and SFR Definition 5.2. The ADC0 subsystem is enabled only when the AD0EN bit in the ADC0 Control register (ADC0CN) is set to logic 1. The ADC0 subsystem is in low power shutdown when this bit is logic 0.

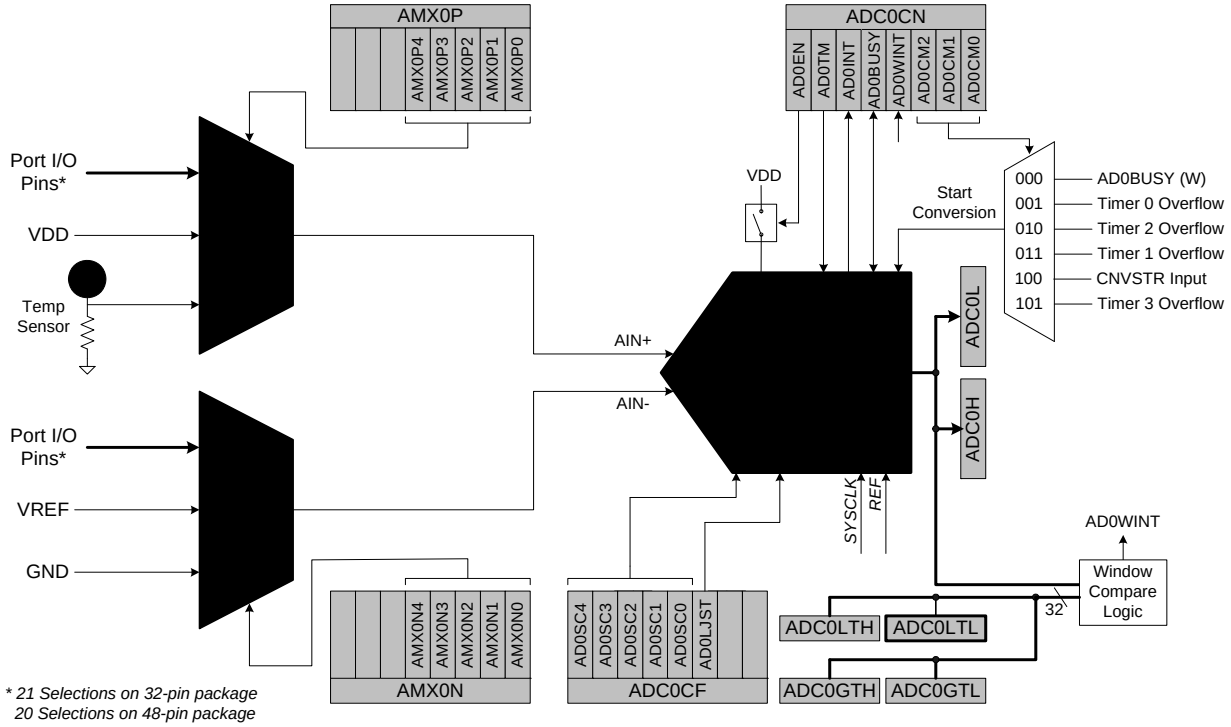

Figure 5.1. ADC0 Functional Block Diagram

SFR Definition 5.2. AMX0N: AMUX0 Negative Channel Select

R	R	R	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	-	AMX0N4	AMX0N3	AMX0N2	AMX0N1	AMX0N0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xBA

Bits7–5: UNUSED. Read = 000b; Write = don't care.
Bits4–0: AMX0N4–0: AMUX0 Negative Input Selection.
Note that when GND is selected as the Negative Input, ADC0 operates in Single-ended mode. For all other Negative Input selections, ADC0 operates in Differential mode.

AMX0N4-0	ADC0 Negative Input (32-pin Package)	ADC0 Negative Input (48-pin Package)
00000	P1.0	P2.0
00001	P1.1	P2.1
00010	P1.2	P2.2
00011	P1.3	P2.3
00100	P1.4	P2.5
00101	P1.5	P2.6
00110	P1.6	P3.0
00111	P1.7	P3.1
01000	P2.0	P3.4
01001	P2.1	P3.5
01010	P2.2	P3.7
01011	P2.3	P4.0
01100	P2.4	P4.3
01101	P2.5	P4.4
01110	P2.6	P4.5
01111	P2.7	P4.6
10000	P3.0	RESERVED
10001	P0.0	P0.3
10010	P0.1	P0.4
10011	P0.4	P1.1
10100	P0.5	P1.2
10101 - 11101	RESERVED	RESERVED
11110	VREF	VREF
11111	GND (Single-Ended Mode)	GND (Single-Ended Mode)

9.2. Memory Organization

The memory organization of the CIP-51 System Controller is similar to that of a standard 8051. There are two separate memory spaces: program memory and data memory. Program and data memory share the same address space but are accessed via different instruction types. The CIP-51 memory organization is shown in Figure 9.2 and Figure 9.3.

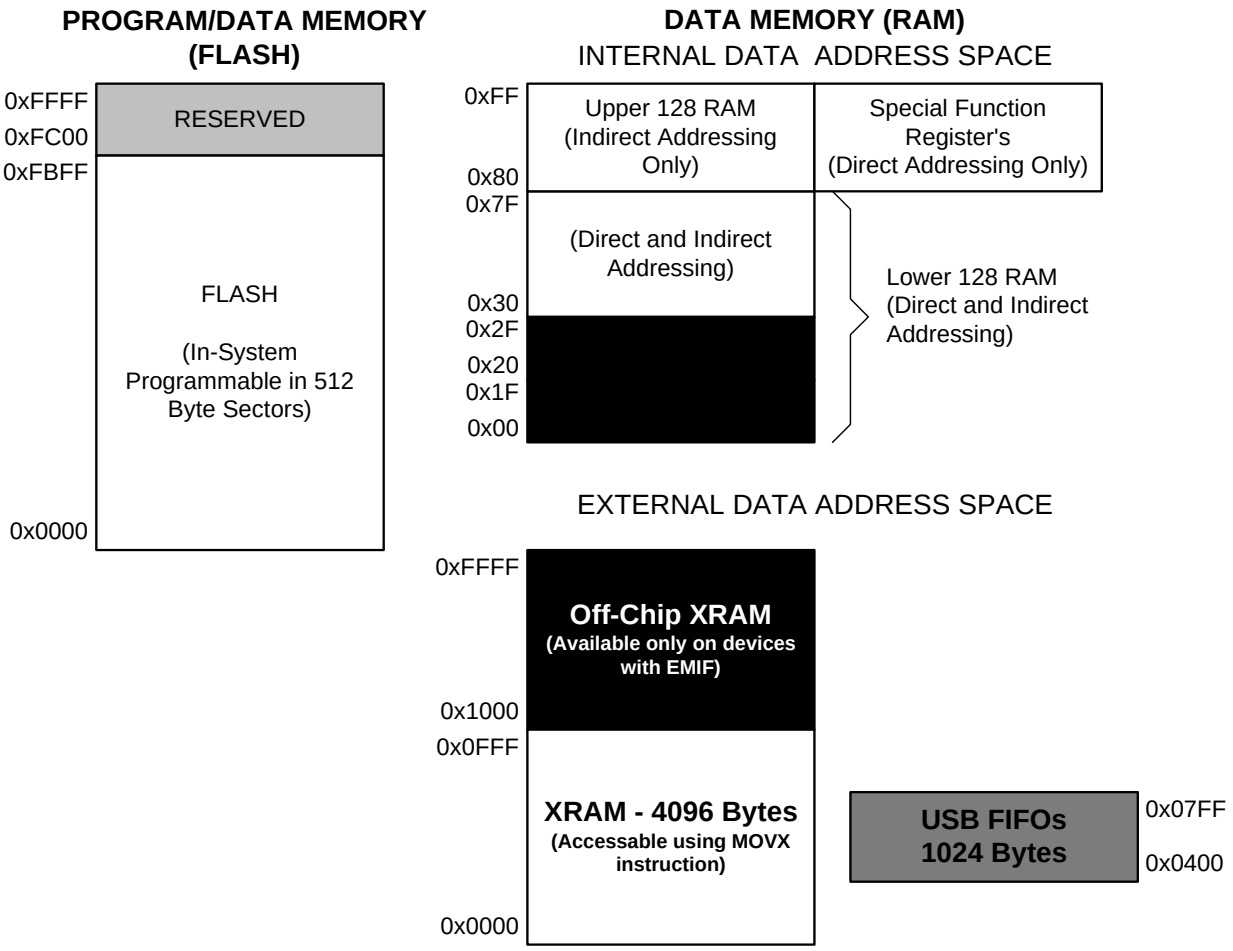

Figure 9.2. On-Chip Memory Map for 64 kB Devices

SFR Definition 9.11. EIE2: Extended Interrupt Enable 2

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	-	-	-	-	ES1	EVBUS	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xE7

Bits7–2: UNUSED. Read = 000000b. Write = don't care.
Bit1: ES1: Enable UART1 Interrupt.
This bit sets the masking of the UART1 interrupt.
0: Disable UART1 interrupt.
1: Enable UART1 interrupt.
Bit0: EVBUS: Enable VBUS Level Interrupt.
This bit sets the masking of the VBUS interrupt.
0: Disable all VBUS interrupts.
1: Enable interrupt requests generated by VBUS level sense.

SFR Definition 9.12. EIP2: Extended Interrupt Priority 2

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	-	-	-	-	PS1	PVBUS	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xF7

Bits7–2: UNUSED. Read = 000000b. Write = don't care.
Bit1: PS1: UART1 Interrupt Priority Control.
This bit sets the priority of the UART1 interrupt.
0: UART1 interrupt set to low priority level.
1: UART1 interrupts set to high priority level.
Bit0: PVBUS: VBUS Level Interrupt Priority Control.
This bit sets the priority of the VBUS interrupt.
0: VBUS interrupt set to low priority level.
1: VBUS interrupt set to high priority level.

11.8. Software Reset

Software may force a reset by writing a ‘1’ to the SWRSF bit (RSTSRC.4). The SWRSF bit will read ‘1’ following a software forced reset. The state of the $\overline{\text{RST}}$ pin is unaffected by this reset.

11.9. USB Reset

Writing ‘1’ to the USBRSF bit in register RSTSRC selects USB0 as a reset source. With USB0 selected as a reset source, a system reset will be generated when either of the following occur:

1. RESET signaling is detected on the USB network. The USB Function Controller (USB0) must be enabled for RESET signaling to be detected. See **Section “16. Universal Serial Bus Controller (USB0)” on page 159** for information on the USB Function Controller.
2. The voltage on the VBUS pin matches the polarity selected by the VBPOL bit in register REG0CN. See **Section “8. Voltage Regulator (REG0)” on page 69** for details on the VBUS detection circuit.

The USBRSF bit will read ‘1’ following a USB reset. The state of the $\overline{\text{RST}}$ pin is unaffected by this reset.

SFR Definition 12.3. FLSCL: Flash Scale

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
FOSE	Reserved	Reserved	FLRT	Reserved	Reserved	Reserved	Reserved	10000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xB6

Bits7: FOSE: Flash One-shot Enable
This bit enables the Flash read one-shot. When the Flash one-shot disabled, the Flash sense amps are enabled for a full clock cycle during Flash reads. At system clock frequencies below 10 MHz, disabling the Flash one-shot will increase system power consumption.
0: Flash one-shot disabled.
1: Flash one-shot enabled.

Bits6–5: RESERVED. Read = 00b. Must Write 00b.

Bit 4: FLRT: FLASH Read Time.
This bit should be programmed to the smallest allowed value, according to the system clock speed.
0: SYSCLK <= 25 MHz.
1: SYSCLK <= 48 MHz.

Bits3–0: RESERVED. Read = 0000b. Must Write 0000b.

13.2. Accessing USB FIFO Space

The C8051F34x devices include 1k of RAM which functions as USB FIFO space. Figure 13.1 shows an expanded view of the FIFO space and user XRAM. FIFO space is normally accessed via USB FIFO registers; see **Section "16.5. FIFO Management" on page 167** for more information on accessing these FIFOs. The MOVX instruction should not be used to load or modify USB data in the FIFO space.

Unused areas of the USB FIFO space may be used as general purpose XRAM if necessary. The FIFO block operates on the USB clock domain; thus the USB clock must be active when accessing FIFO space. Note that the number of SYSCLK cycles required by the MOVX instruction is increased when accessing USB FIFO space.

To access the FIFO RAM directly using MOVX instructions, the following conditions must be met: (1) the USBFAE bit in register EMI0CF must be set to '1', and (2) the USB clock must be greater than or equal to twice the SYSCLK (USBCLK $\geq$ 2 x SYSCLK). When this bit is set, the USB FIFO space is mapped into XRAM space at addresses 0x0400 to 0x07FF. The normal XRAM (on-chip or external) at the same addresses cannot be accessed when the USBFAE bit is set to '1'.

Important Note: The USB clock must be active when accessing FIFO space.

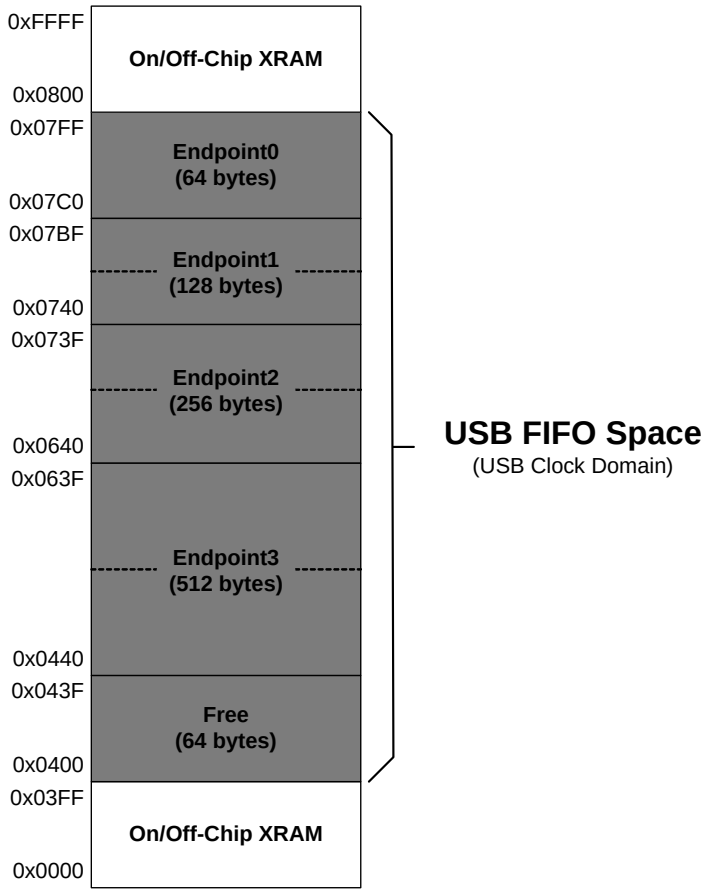

Figure 13.1. USB FIFO Space and XRAM Memory Map with USBFAE set to '1'

13.7.2. Multiplexed Mode

13.7.2.1.16-bit MOVX: EMI0CF[4:2] = ‘001’, ‘010’, or ‘011’.

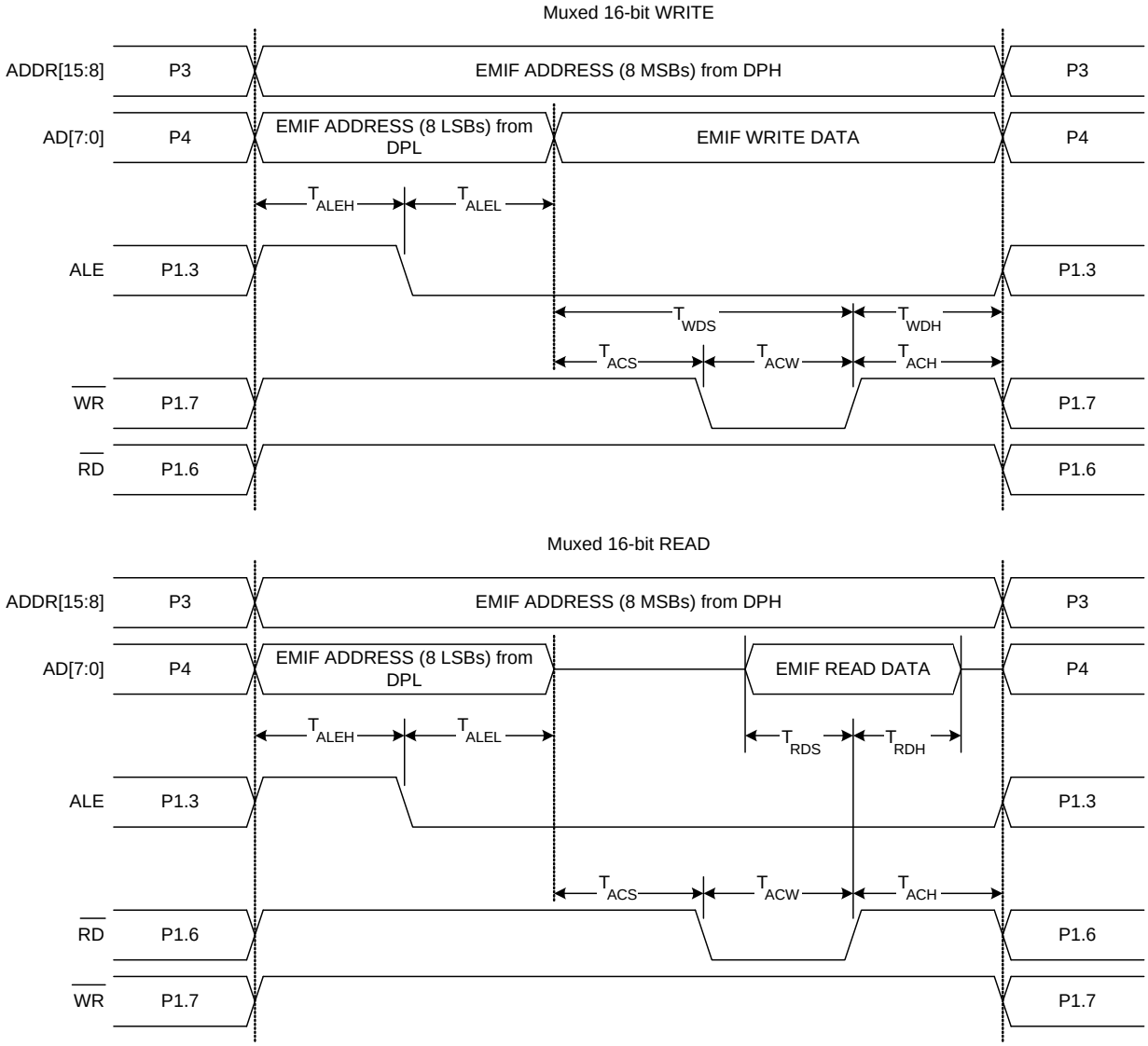

Figure 13.8. Multiplexed 16-bit MOVX Timing

13.7.2.3.8-bit MOVX with Bank Select: EMI0CF[4:2] = ‘010’.

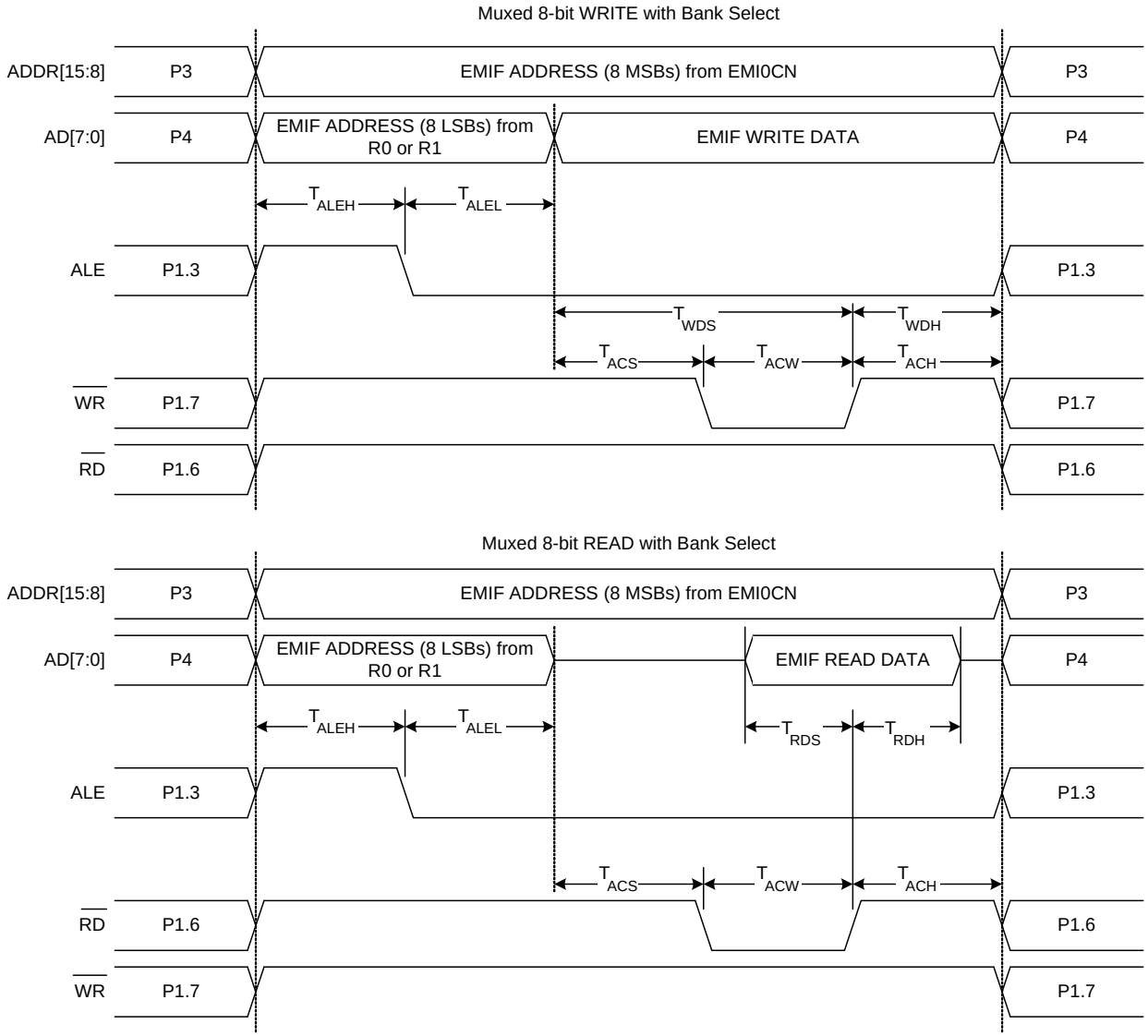

Figure 13.10. Multiplexed 8-bit MOVX with Bank Select Timing

Table 16.2. USB0 Controller Registers

USB Register Name	USB Register Address	Description	Page Number
Interrupt Registers			
IN1INT	0x02	Endpoint0 and Endpoints1-3 IN Interrupt Flags	173
OUT1INT	0x04	Endpoints1-3 OUT Interrupt Flags	173
CMINT	0x06	Common USB Interrupt Flags	174
IN1IE	0x07	Endpoint0 and Endpoints1-3 IN Interrupt Enables	175
OUT1IE	0x09	Endpoints1-3 OUT Interrupt Enables	175
CMIE	0x0B	Common USB Interrupt Enables	176
Common Registers			
FADDR	0x00	Function Address	169
POWER	0x01	Power Management	171
FRAMEL	0x0C	Frame Number Low Byte	172
FRAMEH	0x0D	Frame Number High Byte	172
INDEX	0x0E	Endpoint Index Selection	165
CLKREC	0x0F	Clock Recovery Control	166
FIFOn	0x20–0x23	Endpoints0-3 FIFOs	168
Indexed Registers			
E0CSR	0x11	Endpoint0 Control / Status	179
EINCSRL		Endpoint IN Control / Status Low Byte	182
EINCSRH	0x12	Endpoint IN Control / Status High Byte	183
EOUTCSRL	0x14	Endpoint OUT Control / Status Low Byte	185
EOUTCSRH	0x15	Endpoint OUT Control / Status High Byte	186
E0CNT	0x16	Number of Received Bytes in Endpoint0 FIFO	180
EOUTCNTL		Endpoint OUT Packet Count Low Byte	186
EOUTCNTH	0x17	Endpoint OUT Packet Count High Byte	186

USB Register Definition 16.4. INDEX: USB0 Endpoint Index

R	R	R	R	R/W	R/W	R/W	R/W	Reset Value
-	-	-	-	EPSEL				00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	USB Address: 0x0E

Bits7–4: Unused. Read = 0000b; Write = don't care.
Bits3–0: EPSEL: Endpoint Select
These bits select which endpoint is targeted when indexed USB0 registers are accessed.

INDEX	Target Endpoint
0x0	0
0x1	1
0x2	2
0x3	3
0x4–0xF	Reserved

mode feature of the internal oscillator.

USB0 exits Suspend mode when any of the following occur: (1) Resume signaling is detected or generated, (2) Reset signaling is detected, or (3) a device or USB reset occurs. If suspended, the internal oscillator will exit Suspend mode upon any of the above listed events.

Resume Signaling: USB0 will exit Suspend mode if Resume signaling is detected on the bus. A Resume interrupt will be generated upon detection if enabled (RESINTE = ‘1’). Software may force a Remote Wakeup by writing ‘1’ to the RESUME bit (POWER.2). When forcing a Remote Wakeup, software should write RESUME = ‘0’ to end Resume signaling 10-15 ms after the Remote Wakeup is initiated (RESUME = ‘1’).

ISO Update: When software writes ‘1’ to the ISOUP bit (POWER.7), the ISO Update function is enabled. With ISO Update enabled, new packets written to an ISO IN endpoint will not be transmitted until a new Start-Of-Frame (SOF) is received. If the ISO IN endpoint receives an IN token before a SOF, USB0 will transmit a zero-length packet. When ISOUP = ‘1’, ISO Update is enabled for all ISO endpoints.

USB Enable: USB0 is disabled following a Power-On-Reset (POR). USB0 is enabled by clearing the USBINH bit (POWER.4). Once written to ‘0’, the USBINH can only be set to ‘1’ by one of the following: (1) a Power-On-Reset (POR), or (2) an asynchronous USB0 reset generated by writing ‘1’ to the USBRST bit (POWER.3).

Software should perform all USB0 configuration before enabling USB0. The configuration sequence should be performed as follows:

Step 1. Select and enable the USB clock source.
Step 2. Reset USB0 by writing USBRST= ‘1’.
Step 3. Configure and enable the USB Transceiver.
Step 4. Perform any USB0 function configuration (interrupts, Suspend detect).
Step 5. Enable USB0 by writing USBINH = ‘0’.

20.2. SPI0 Master Mode Operation

A SPI master device initiates all data transfers on a SPI bus. SPI0 is placed in master mode by setting the Master Enable flag (MSTEN, SPI0CFG.6). Writing a byte of data to the SPI0 data register (SPI0DAT) when in master mode writes to the transmit buffer. If the SPI shift register is empty, the byte in the transmit buffer is moved to the shift register, and a data transfer begins. The SPI0 master immediately shifts out the data serially on the MOSI line while providing the serial clock on SCK. The SPIF (SPI0CN.7) flag is set to logic 1 at the end of the transfer. If interrupts are enabled, an interrupt request is generated when the SPIF flag is set. While the SPI0 master transfers data to a slave on the MOSI line, the addressed SPI slave device simultaneously transfers the contents of its shift register to the SPI master on the MISO line in a full-duplex operation. Therefore, the SPIF flag serves as both a transmit-complete and receive-data-ready flag. The data byte received from the slave is transferred MSB-first into the master's shift register. When a byte is fully shifted into the register, it is moved to the receive buffer where it can be read by the processor by reading SPI0DAT.

When configured as a master, SPI0 can operate in one of three different modes: multi-master mode, 3-wire single-master mode, and 4-wire single-master mode. The default, multi-master mode is active when NSSMD1 (SPI0CN.3) = 0 and NSSMD0 (SPI0CN.2) = 1. In this mode, NSS is an input to the device, and is used to disable the master SPI0 when another master is accessing the bus. When NSS is pulled low in this mode, MSTEN (SPI0CFG.6) and SPIEN (SPI0CN.0) are set to 0 to disable the SPI master device, and a Mode Fault is generated (MODF, SPI0CN.5 = 1). Mode Fault will generate an interrupt if enabled. SPI0 must be manually re-enabled in software under these circumstances. In multi-master systems, devices will typically default to being slave devices while they are not acting as the system master device. In multi-master mode, slave devices can be addressed individually (if needed) using general-purpose I/O pins. Figure 20.2 shows a connection diagram between two master devices in multiple-master mode.

3-wire single-master mode is active when NSSMD1 (SPI0CN.3) = 0 and NSSMD0 (SPI0CN.2) = 0. In this mode, NSS is not used, and is not mapped to an external port pin through the crossbar. Any slave devices that must be addressed in this mode should be selected using general-purpose I/O pins. Figure 20.3 shows a connection diagram between a master device in 3-wire master mode and a slave device.

4-wire single-master mode is active when NSSMD1 (SPI0CN.3) = 1. In this mode, NSS is configured as an output pin, and can be used as a slave-select signal for a single SPI device. In this mode, the output value of NSS is controlled (in software) with the bit NSSMD0 (SPI0CN.2). Additional slave devices can be addressed using general-purpose I/O pins. Figure 20.4 shows a connection diagram for a master device in 4-wire master mode and two slave devices.

22.3. Watchdog Timer Mode

A programmable watchdog timer (WDT) function is available through the PCA Module 4. The WDT is used to generate a reset if the time between writes to the WDT update register (PCA0CPH4) exceed a specified limit. The WDT can be configured and enabled/disabled as needed by software.

With the WDTE and/or WDLCK bits set to '1' in the PCA0MD register, Module 4 operates as a watchdog timer (WDT). The Module 4 high byte is compared to the PCA counter high byte; the Module 4 low byte holds the offset to be used when WDT updates are performed. **The Watchdog Timer is enabled on reset. Writes to some PCA registers are restricted while the Watchdog Timer is enabled.**

22.3.1. Watchdog Timer Operation

While the WDT is enabled:

- PCA counter is forced on.
- Writes to PCA0L and PCA0H are not allowed.
- PCA clock source bits (CPS2-CPS0) are frozen.
- PCA Idle control bit (CIDL) is frozen.
- Module 4 is forced into Watchdog Timer mode.
- Writes to the Module 4 mode register (PCA0CPM4) are disabled.

While the WDT is enabled, writes to the CR bit will not change the PCA counter state; the counter will run until the WDT is disabled. The PCA counter run control (CR) will read zero if the WDT is enabled but user software has not enabled the PCA counter. If a match occurs between PCA0CPH4 and PCA0H while the WDT is enabled, a reset will be generated. To prevent a WDT reset, the WDT may be updated with a write of any value to PCA0CPH4. Upon a PCA0CPH4 write, PCA0H plus the offset held in PCA0CPL4 is loaded into PCA0CPH4 (See Figure 22.10).

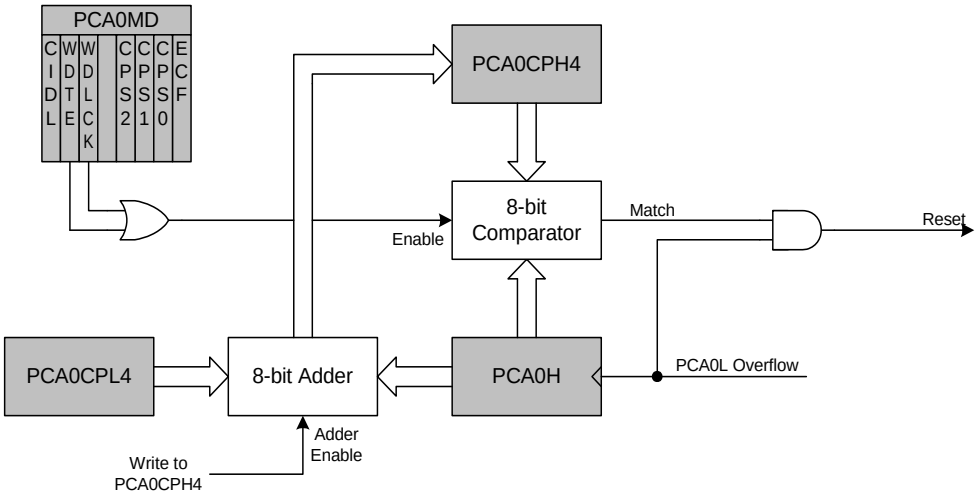

Figure 22.10. PCA Module 4 with Watchdog Timer Enabled

Note that the 8-bit offset held in PCA0CPH4 is compared to the upper byte of the 16-bit PCA counter. This offset value is the number of PCA0L overflows before a reset. Up to 256 PCA clocks may pass before the first PCA0L overflow occurs, depending on the value of the PCA0L when the update is performed. The total offset is then given (in PCA clocks) by Equation 22.4, where PCA0L is the value of the PCA0L register at the time of the update.

C2 Register Definition 23.3. REVID: C2 Revision ID

Reset Value: Variable

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

This read-only register returns the 8-bit revision ID.

C2 Register Definition 23.4. FPCTL: C2 Flash Programming Control

Reset Value: 00000000

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

Bits7–0 FPCTL: Flash Programming Control Register.
This register is used to enable Flash programming via the C2 interface. To enable C2 Flash programming, the following codes must be written in order: 0x02, 0x01. Note that once C2 Flash programming is enabled, a system reset must be issued to resume normal operation.

C2 Register Definition 23.5. FPDAT: C2 Flash Programming Data

Reset Value: 00000000

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

Bits7–0: FPDAT: C2 Flash Programming Data Register.
This register is used to pass Flash commands, addresses, and data during C2 Flash accesses. Valid commands are listed below.

Code	Command
0x06	Flash Block Read
0x07	Flash Block Write
0x08	Flash Page Erase
0x03	Device Erase