Silicon Labs - C8051F34C-GQ Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	8051
Core Size	8-Bit
Speed	48MHz
Connectivity	EBI/EMI, SMBus (2-Wire/I²C), SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	40
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.25V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f34c-gq

8. Voltage Regulator (REG0)

C8051F34x devices include a voltage regulator (REG0). When enabled, the REG0 output appears on the V_{DD} pin and can be used to power external devices. REG0 can be enabled/disabled by software using bit REGEN in register REG0CN. See Table 8.1 for REG0 electrical characteristics.

Note that the VBUS signal must be connected to the VBUS pin when using the device in a USB network. The VBUS signal should only be connected to the REGIN pin when operating the device as a bus-powered function. REG0 configuration options are shown in Figure 8.1–Figure 8.4.

8.1. Regulator Mode Selection

REG0 offers a low power mode intended for use when the device is in suspend mode. In this low power mode, the REG0 output remains as specified; however the REG0 dynamic performance (response time) is degraded. See Table 8.1 for normal and low power mode supply current specifications. The REG0 mode selection is controlled via the REGMOD bit in register REG0CN.

8.2. VBUS Detection

When the USB Function Controller is used (see section **Section “16. Universal Serial Bus Controller (USB0)” on page 159**), the VBUS signal should be connected to the VBUS pin. The VBSTAT bit (register REG0CN) indicates the current logic level of the VBUS signal. If enabled, a VBUS interrupt will be generated when the VBUS signal matches the polarity selected by the VBPOL bit in register REG0CN. The VBUS interrupt is level-sensitive, and has no associated interrupt pending flag. The VBUS interrupt will be active as long as the VBUS signal matches the polarity selected by VBPOL. See Table 8.1 for VBUS input parameters.

Important Note: When USB is selected as a reset source, a system reset will be generated when the VBUS signal matches the polarity selected by the VBPOL bit. See **Section “11. Reset Sources” on page 100** for details on selecting USB as a reset source

Table 8.1. Voltage Regulator Electrical Specifications

–40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Input Voltage Range[1]		2.7		5.25	V
Output Voltage (V_{DD})[2]	Output Current = 1 to 100 mA	3.0	3.3	3.6	V
Output Current[2]				100	mA
VBUS Detection Input Low Voltage				1.0	V
VBUS Detection Input High Voltage		3.0			V
Bias Current	Normal Mode (REGMOD = ‘0’) Low Power Mode (REGMOD = ‘1’)		65 35	111 61	µA
Dropout Voltage (V_{DO})[3]			1		mV/mA

Notes:
1. Input range specified for regulation. When an external regulator is used, should be tied to V_{DD}.
2. Output current is total regulator output, including any current required by the C8051F34x.
3. The minimum input voltage is 2.70 V or VDD + V_{DO} (max load), whichever is greater.

SFR Definition 8.1. REG0CN: Voltage Regulator Control

R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
REGDIS	VBSTAT	VBPOL	REGMOD	Reserved	Reserved	Reserved	Reserved	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xC9

Bit7: REGDIS: Voltage Regulator Disable.
0: Voltage Regulator Enabled.
1: Voltage Regulator Disabled.

Bit6: VBSTAT: VBUS Signal Status.
0: VBUS signal currently absent (device not attached to USB network).
1: VBUS signal currently present (device attached to USB network).

Bit5: VBPOL: VBUS Interrupt Polarity Select.
This bit selects the VBUS interrupt polarity.
0: VBUS interrupt active when VBUS is low.
1: VBUS interrupt active when VBUS is high.

Bit4: REGMOD: Voltage Regulator Mode Select.
This bit selects the Voltage Regulator mode. When REGMOD is set to ‘1’, the voltage regulator operates in low power (suspend) mode.
0: USB0 Voltage Regulator in normal mode.
1: USB0 Voltage Regulator in low power mode.

Bits3–0: Reserved. Read = 0000b. Must Write = 0000b.

Table 9.1. CIP-51 Instruction Set Summary (Continued)

Mnemonic	Description	Bytes	Clock Cycles
ORL A, #data	OR immediate to A	2	2
ORL direct, A	OR A to direct byte	2	2
ORL direct, #data	OR immediate to direct byte	3	3
XRL A, Rn	Exclusive-OR Register to A	1	1
XRL A, direct	Exclusive-OR direct byte to A	2	2
XRL A, @Ri	Exclusive-OR indirect RAM to A	1	2
XRL A, #data	Exclusive-OR immediate to A	2	2
XRL direct, A	Exclusive-OR A to direct byte	2	2
XRL direct, #data	Exclusive-OR immediate to direct byte	3	3
CLR A	Clear A	1	1
CPL A	Complement A	1	1
RL A	Rotate A left	1	1
RLC A	Rotate A left through Carry	1	1
RR A	Rotate A right	1	1
RRC A	Rotate A right through Carry	1	1
SWAP A	Swap nibbles of A	1	1
Data Transfer			
MOV A, Rn	Move Register to A	1	1
MOV A, direct	Move direct byte to A	2	2
MOV A, @Ri	Move indirect RAM to A	1	2
MOV A, #data	Move immediate to A	2	2
MOV Rn, A	Move A to Register	1	1
MOV Rn, direct	Move direct byte to Register	2	2
MOV Rn, #data	Move immediate to Register	2	2
MOV direct, A	Move A to direct byte	2	2
MOV direct, Rn	Move Register to direct byte	2	2
MOV direct, direct	Move direct byte to direct byte	3	3
MOV direct, @Ri	Move indirect RAM to direct byte	2	2
MOV direct, #data	Move immediate to direct byte	3	3
MOV @Ri, A	Move A to indirect RAM	1	2
MOV @Ri, direct	Move direct byte to indirect RAM	2	2
MOV @Ri, #data	Move immediate to indirect RAM	2	2
MOV DPTR, #data16	Load DPTR with 16-bit constant	3	3
MOVC A, @A+DPTR	Move code byte relative DPTR to A	1	3
MOVC A, @A+PC	Move code byte relative PC to A	1	3
MOVX A, @Ri	Move external data (8-bit address) to A	1	3
MOVX @Ri, A	Move A to external data (8-bit address)	1	3
MOVX A, @DPTR	Move external data (16-bit address) to A	1	3
MOVX @DPTR, A	Move A to external data (16-bit address)	1	3
PUSH direct	Push direct byte onto stack	2	2
POP direct	Pop direct byte from stack	2	2
XCH A, Rn	Exchange Register with A	1	1
XCH A, direct	Exchange direct byte with A	2	2
XCH A, @Ri	Exchange indirect RAM with A	1	2
XCHD A, @Ri	Exchange low nibble of indirect RAM with A	1	2

Table 9.3. Special Function Registers

SFRs are listed in alphabetical order. All undefined SFR locations are reserved.

Register	Address	Description	Page
ACC	0xE0	Accumulator	87
ADC0CF	0xBC	ADC0 Configuration	50
ADC0CN	0xE8	ADC0 Control	51
ADC0GTH	0xC4	ADC0 Greater-Than Compare High	52
ADC0GTL	0xC3	ADC0 Greater-Than Compare Low	52
ADC0H	0xBE	ADC0 High	50
ADC0L	0xBD	ADC0 Low	50
ADC0LTH	0xC6	ADC0 Less-Than Compare Word High	53
ADC0LTL	0xC5	ADC0 Less-Than Compare Word Low	53
AMX0N	0xBA	AMUX0 Negative Channel Select	49
AMX0P	0xBB	AMUX0 Positive Channel Select	48
B	0xF0	B Register	88
CKCON	0x8E	Clock Control	241
CLKMUL	0xB9	Clock Multiplier	138
CLKSEL	0xA9	Clock Select	140
CPT0CN	0x9B	Comparator0 Control	62
CPT0MD	0x9D	Comparator0 Mode Selection	64
CPT0MX	0x9F	Comparator0 MUX Selection	63
CPT1CN	0x9A	Comparator1 Control	65
CPT1MD	0x9C	Comparator1 Mode Selection	67
CPT1MX	0x9E	Comparator1 MUX Selection	66
DPH	0x83	Data Pointer High	86
DPL	0x82	Data Pointer Low	86
EIE1	0xE6	Extended Interrupt Enable 1	93
EIE2	0xE7	Extended Interrupt Enable 2	95
EIP1	0xF6	Extended Interrupt Priority 1	94
EIP2	0xF7	Extended Interrupt Priority 2	95
EMI0CN	0xAA	External Memory Interface Control	117
EMI0CF	0x85	External Memory Interface Configuration	118
EMI0TC	0x84	External Memory Interface Timing	123
FLKEY	0xB7	Flash Lock and Key	112
FLSCL	0xB6	Flash Scale	113
IE	0xA8	Interrupt Enable	91
IP	0xB8	Interrupt Priority	92
IT01CF	0xE4	INT0/INT1 Configuration	96
OSCICL	0xB3	Internal Oscillator Calibration	133
OSCICN	0xB2	Internal Oscillator Control	132
OSCLCN	0x86	Internal Low-Frequency Oscillator Control	134
OSCXCN	0xB1	External Oscillator Control	137
P0	0x80	Port 0 Latch	150
P0MDIN	0xF1	Port 0 Input Mode Configuration	150
P0MDOUT	0xA4	Port 0 Output Mode Configuration	151
P0SKIP	0xD4	Port 0 Skip	151
P1	0x90	Port 1 Latch	152

11. Reset Sources

Reset circuitry allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the following occur:

- CIP-51 halts program execution
- Special Function Registers (SFRs) are initialized to their defined reset values
- External Port pins are forced to a known state
- Interrupts and timers are disabled.

All SFRs are reset to the predefined values noted in the SFR detailed descriptions. The contents of internal data memory are unaffected during a reset; any previously stored data is preserved. However, since the stack pointer SFR is reset, the stack is effectively lost even though the data on the stack is not altered.

The Port I/O latches are reset to 0xFF (all logic ones) in open-drain mode. Weak pull-ups are enabled during and after the reset. For V_{DD} Monitor and Power-On Resets, the $\overline{RST}$ pin is driven low until the device exits the reset state.

On exit from the reset state, the program counter (PC) is reset, and the system clock defaults to the internal oscillator. Refer to **Section “14. Oscillators” on page 131** for information on selecting and configuring the system clock source. The Watchdog Timer is enabled with the system clock divided by 12 as its clock source (**Section “22.3. Watchdog Timer Mode” on page 264** details the use of the Watchdog Timer). Program execution begins at location 0x0000.

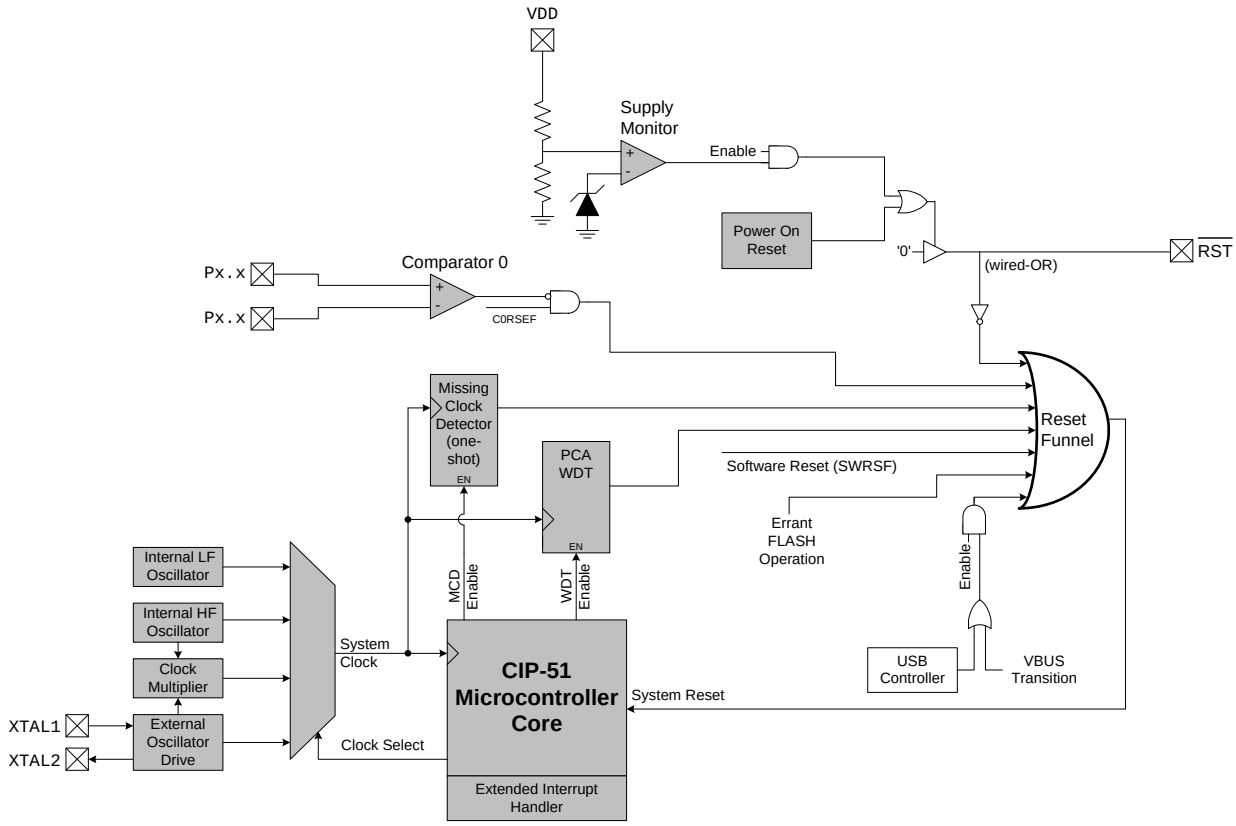

Figure 11.1. Reset Sources

Table 12.1. Flash Electrical Characteristics

Parameter	Conditions	Min	Typ	Max	Units
Flash Size	C8051F340/2/4/6/A/C/D*	65536*			Bytes
	C8051F341/3/5/7/8/9/B	32768			Bytes
Endurance		20k	100k		Erase/Write
Erase Cycle Time	25 MHz System Clock	10	15	20	ms
Write Cycle Time	25 MHz System Clock	40	55	70	µs

***Note:** 1024 bytes at location 0xFC00 to 0xFFFF are reserved.

12.2. Non-Volatile Data Storage

The Flash memory can be used for non-volatile data storage as well as program code. This allows data such as calibration coefficients to be calculated and stored at run time. Data is written using the MOVX write instruction and read using the MOVC instruction. Note: MOVX read instructions always target XRAM.

12.3. Security Options

The CIP-51 provides security options to protect the Flash memory from inadvertent modification by software as well as to prevent the viewing of proprietary program code and constants. The Program Store Write Enable (bit PSWE in register PSCTL) and the Program Store Erase Enable (bit PSEE in register PSCTL) bits protect the Flash memory from accidental modification by software. PSWE must be explicitly set to ‘1’ before software can modify the Flash memory; both PSWE and PSEE must be set to ‘1’ before software can erase Flash memory. Additional security features prevent proprietary program code and data constants from being read or altered across the C2 interface.

A Security Lock Byte located at the last byte of Flash user space offers protection of the Flash program memory from access (reads, writes, or erases) by unprotected code or the C2 interface. The Flash security mechanism allows the user to lock *n* 512-byte Flash pages, starting at page 0 (addresses 0x0000 to 0x01FF), where *n* is the 1’s complement number represented by the Security Lock Byte. Note that the page containing the Flash Security Lock Byte is also locked when any other Flash pages are locked. See example below.

Security Lock Byte:	11111101b
1’s Complement:	00000010b
Flash pages locked:	3 (2 + Flash Lock Byte Page)
Addresses locked:	First two pages of Flash: 0x0000 to 0x03FF Flash Lock Byte Page: (0xFA00 to 0xFBFF for 64k devices; 0x7E00 to 0x7FFF for 32k devices)

SFR Definition 12.1. PSCTL: Program Store R/W Control

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	-	-	-	Reserved	PSEE	PSWE	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0x8F

Bits7–3: Unused: Read = 00000b. Write = don't care.
Bit2: Reserved. Read = 0b. Must Write = 0b.
Bit1: PSEE: Program Store Erase Enable
Setting this bit (in combination with PSWE) allows an entire page of Flash program memory to be erased. If this bit is logic 1 and Flash writes are enabled (PSWE is logic 1), a write to Flash memory using the MOVX instruction will erase the entire page that contains the location addressed by the MOVX instruction. The value of the data byte written does not matter.
0: Flash program memory erasure disabled.
1: Flash program memory erasure enabled.
Bit0: PSWE: Program Store Write Enable
Setting this bit allows writing a byte of data to the Flash program memory using the MOVX write instruction. The Flash location should be erased before writing data.
0: Writes to Flash program memory disabled.
1: Writes to Flash program memory enabled; the MOVX write instruction targets Flash memory.

SFR Definition 12.2. FLKEY: Flash Lock and Key

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xB7

Bits–0: FLKEY: Flash Lock and Key Register
Write:
This register must be written to before Flash writes or erases can be performed. Flash remains locked until this register is written to with the following key codes: 0xA5, 0xF1. The timing of the writes does not matter, as long as the codes are written in order. The key codes must be written for each Flash write or erase operation. Flash will be locked until the next system reset if the wrong codes are written or if a Flash operation is attempted before the codes have been written correctly.
Read:
When read, bits 1-0 indicate the current Flash lock state.
00: Flash is write/erase locked.
01: The first key code has been written (0xA5).
10: Flash is unlocked (writes/erases allowed).
11: Flash writes/erases disabled until the next reset.

SFR Definition 13.3. EMI0TC: External Memory Timing Control

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
EAS1	EAS0	EWR3	EWR2	EWR1	EWR0	EAH1	EAH0	11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x84

Bits7–6: EAS1–0: EMIF Address Setup Time Bits.
00: Address setup time = 0 SYSCLK cycles.
01: Address setup time = 1 SYSCLK cycle.
10: Address setup time = 2 SYSCLK cycles.
11: Address setup time = 3 SYSCLK cycles.

Bits5–2: EWR3–0: EMIF $\overline{WR}$ and $\overline{RD}$ Pulse-Width Control Bits.
0000: $\overline{WR}$ and $\overline{RD}$ pulse width = 1 SYSCLK cycle.
0001: $\overline{WR}$ and $\overline{RD}$ pulse width = 2 SYSCLK cycles.
0010: $\overline{WR}$ and $\overline{RD}$ pulse width = 3 SYSCLK cycles.
0011: $\overline{WR}$ and $\overline{RD}$ pulse width = 4 SYSCLK cycles.
0100: $\overline{WR}$ and $\overline{RD}$ pulse width = 5 SYSCLK cycles.
0101: $\overline{WR}$ and $\overline{RD}$ pulse width = 6 SYSCLK cycles.
0110: $\overline{WR}$ and $\overline{RD}$ pulse width = 7 SYSCLK cycles.
0111: $\overline{WR}$ and $\overline{RD}$ pulse width = 8 SYSCLK cycles.
1000: $\overline{WR}$ and $\overline{RD}$ pulse width = 9 SYSCLK cycles.
1001: $\overline{WR}$ and $\overline{RD}$ pulse width = 10 SYSCLK cycles.
1010: $\overline{WR}$ and $\overline{RD}$ pulse width = 11 SYSCLK cycles.
1011: $\overline{WR}$ and $\overline{RD}$ pulse width = 12 SYSCLK cycles.
1100: $\overline{WR}$ and $\overline{RD}$ pulse width = 13 SYSCLK cycles.
1101: $\overline{WR}$ and $\overline{RD}$ pulse width = 14 SYSCLK cycles.
1110: $\overline{WR}$ and $\overline{RD}$ pulse width = 15 SYSCLK cycles.
1111:$\overline{WR}$ and $\overline{RD}$ pulse width = 16 SYSCLK cycles.

Bits1–0: EAH1–0: EMIF Address Hold Time Bits.
00: Address hold time = 0 SYSCLK cycles.
01: Address hold time = 1 SYSCLK cycle.
10: Address hold time = 2 SYSCLK cycles.
11: Address hold time = 3 SYSCLK cycles.

13.7.2. Multiplexed Mode

13.7.2.1.16-bit MOVX: EMI0CF[4:2] = ‘001’, ‘010’, or ‘011’.

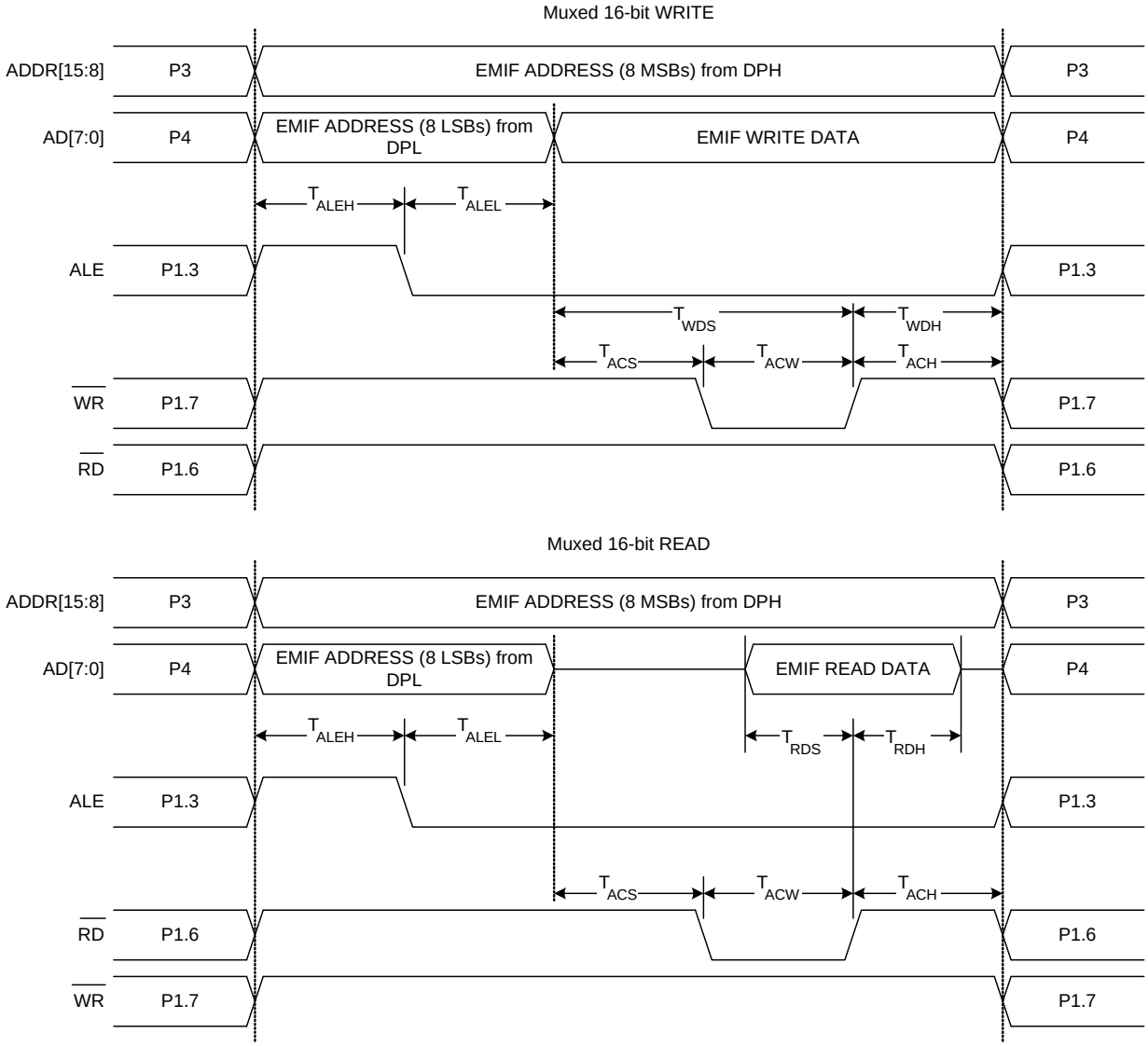

Figure 13.8. Multiplexed 16-bit MOVX Timing

14.4. 4x Clock Multiplier

The 4x Clock Multiplier allows a 12 MHz oscillator to generate the 48 MHz clock required for Full Speed USB communication (see **Section “16.4. USB Clock Configuration” on page 166**). A divided version of the Multiplier output can also be used as the system clock. C8051F340/1/2/3 devices can use the 48 MHz Clock Multiplier output as system clock. See Table 3.1, “Global DC Electrical Characteristics,” on page 25 for system clock frequency specifications. See **Section 14.5** for details on system clock and USB clock source selection.

The 4x Clock Multiplier is configured via the CLKMUL register. The procedure for configuring and enabling the 4x Clock Multiplier is as follows:

1. Reset the Multiplier by writing 0x00 to register CLKMUL.
2. Select the Multiplier input source via the MULSEL bits.
3. Enable the Multiplier with the MULEN bit (CLKMUL | = 0x80).
4. Delay for >5 µs.
5. Initialize the Multiplier with the MULINIT bit (CLKMUL | = 0xC0).
6. Poll for MULRDY => ‘1’.

Important Note: When using an external oscillator as the input to the 4x Clock Multiplier, the external source must be enabled and stable before the Multiplier is initialized. See Section 14.5 for details on selecting an external oscillator source.

SFR Definition 14.5. CLKMUL: Clock Multiplier Control

R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	Reset Value
MULEN	MULINIT	MULRDY	-	-	-	MULSEL		00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address
								0xB9

Bit7: MULEN: Clock Multiplier Enable
0: Clock Multiplier disabled.
1: Clock Multiplier enabled.

Bit6: MULINIT: Clock Multiplier Initialize
This bit should be a ‘0’ when the Clock Multiplier is enabled. Once enabled, writing a ‘1’ to this bit will initialize the Clock Multiplier. The MULRDY bit reads ‘1’ when the Clock Multiplier is stabilized.

Bit5: MULRDY: Clock Multiplier Ready
This read-only bit indicates the status of the Clock Multiplier.
0: Clock Multiplier not ready.
1: Clock Multiplier ready (locked).

Bits4–2: Unused. Read = 000b; Write = don’t care.

Bits1–0: MULSEL: Clock Multiplier Input Select
These bits select the clock supplied to the Clock Multiplier.

MULSEL	Selected Clock
00	Internal Oscillator
01	External Oscillator
10	External Oscillator / 2
11	RESERVED

SFR Definition 15.21. P4MDIN: Port4 Input Mode

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xF5

Bits7–0: Analog Input Configuration Bits for P4.7–P4.0 (respectively).
Port pins configured as analog inputs have their weak pull-up, digital driver, and digital receiver disabled.
0: Corresponding P4.n pin is configured as an analog input.
1: Corresponding P4.n pin is not configured as an analog input.

Note: P4 is only available on 48-pin devices.

SFR Definition 15.22. P4MDOUT: Port4 Output Mode

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xAE

Bits7–0: Output Configuration Bits for P4.7–P4.0 (respectively); ignored if corresponding bit in register P4MDIN is logic 0.
0: Corresponding P4.n Output is open-drain.
1: Corresponding P4.n Output is push-pull.

Note: P4 is only available on 48-pin devices.

Table 16.2. USB0 Controller Registers

USB Register Name	USB Register Address	Description	Page Number
Interrupt Registers			
IN1INT	0x02	Endpoint0 and Endpoints1-3 IN Interrupt Flags	173
OUT1INT	0x04	Endpoints1-3 OUT Interrupt Flags	173
CMINT	0x06	Common USB Interrupt Flags	174
IN1IE	0x07	Endpoint0 and Endpoints1-3 IN Interrupt Enables	175
OUT1IE	0x09	Endpoints1-3 OUT Interrupt Enables	175
CMIE	0x0B	Common USB Interrupt Enables	176
Common Registers			
FADDR	0x00	Function Address	169
POWER	0x01	Power Management	171
FRAMEL	0x0C	Frame Number Low Byte	172
FRAMEH	0x0D	Frame Number High Byte	172
INDEX	0x0E	Endpoint Index Selection	165
CLKREC	0x0F	Clock Recovery Control	166
FIFOn	0x20–0x23	Endpoints0-3 FIFOs	168
Indexed Registers			
E0CSR	0x11	Endpoint0 Control / Status	179
EINCSRL		Endpoint IN Control / Status Low Byte	182
EINCSRH	0x12	Endpoint IN Control / Status High Byte	183
EOUTCSRL	0x14	Endpoint OUT Control / Status Low Byte	185
EOUTCSRH	0x15	Endpoint OUT Control / Status High Byte	186
E0CNT	0x16	Number of Received Bytes in Endpoint0 FIFO	180
EOUTCNTL		Endpoint OUT Packet Count Low Byte	186
EOUTCNTH	0x17	Endpoint OUT Packet Count High Byte	186

USB Register Definition 16.4. INDEX: USB0 Endpoint Index

R	R	R	R	R/W	R/W	R/W	R/W	Reset Value
-	-	-	-	EPSEL				00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	USB Address: 0x0E

Bits7–4: Unused. Read = 0000b; Write = don't care.
Bits3–0: EPSEL: Endpoint Select
These bits select which endpoint is targeted when indexed USB0 registers are accessed.

INDEX	Target Endpoint
0x0	0
0x1	1
0x2	2
0x3	3
0x4–0xF	Reserved

SFR Definition 17.2. SMB0CN: SMBus Control

R	R	R/W	R/W	R	R	R/W	R/W	Reset Value
MASTER	TXMODE	STA	STO	ACKRQ	ARBLOST	ACK	SI	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable

SFR Address: 0xC0

Bit7: MASTER: SMBus Master/Slave Indicator.
This read-only bit indicates when the SMBus is operating as a master.
0: SMBus operating in Slave Mode.
1: SMBus operating in Master Mode.

Bit6: TXMODE: SMBus Transmit Mode Indicator.
This read-only bit indicates when the SMBus is operating as a transmitter.
0: SMBus in Receiver Mode.
1: SMBus in Transmitter Mode.

Bit5: STA: SMBus Start Flag.
Write:
0: No Start generated.
1: When operating as a master, a START condition is transmitted if the bus is free (If the bus is not free, the START is transmitted after a STOP is received or a timeout is detected). If STA is set by software as an active Master, a repeated START will be generated after the next ACK cycle.
Read:
0: No Start or repeated Start detected.
1: Start or repeated Start detected.

Bit4: STO: SMBus Stop Flag.
Write:
0: No STOP condition is transmitted.
1: Setting STO to logic 1 causes a STOP condition to be transmitted after the next ACK cycle. When the STOP condition is generated, hardware clears STO to logic 0. If both STA and STO are set, a STOP condition is transmitted followed by a START condition.
Read:
0: No Stop condition detected.
1: Stop condition detected (if in Slave Mode) or pending (if in Master Mode).

Bit3: ACKRQ: SMBus Acknowledge Request
This read-only bit is set to logic 1 when the SMBus has received a byte and needs the ACK bit to be written with the correct ACK response value.

Bit2: ARBLOST: SMBus Arbitration Lost Indicator.
This read-only bit is set to logic 1 when the SMBus loses arbitration while operating as a transmitter. A lost arbitration while a slave indicates a bus error condition.

Bit1: ACK: SMBus Acknowledge Flag.
This bit defines the out-going ACK level and records incoming ACK levels. It should be written each time a byte is received (when ACKRQ=1), or read after each byte is transmitted.
0: A "not acknowledge" has been received (if in Transmitter Mode) OR will be transmitted (if in Receiver Mode).
1: An "acknowledge" has been received (if in Transmitter Mode) OR will be transmitted (if in Receiver Mode).

Bit0: SI: SMBus Interrupt Flag.
This bit is set by hardware under the conditions listed in Table 17.3. SI must be cleared by software. While SI is set, SCL is held low and the SMBus is stalled.

17.5.4. Slave Transmitter Mode

Serial data is transmitted on SDA and the clock is received on SCL. When slave events are enabled (INH = 0), the interface enters Slave Receiver Mode (to receive the slave address) when a START followed by a slave address and direction bit (READ in this case) is received. Upon entering Slave Transmitter Mode, an interrupt is generated and the ACKRQ bit is set. Software responds to the received slave address with an ACK, or ignores the received slave address with a NACK. If the received slave address is ignored, slave interrupts will be inhibited until a START is detected. If the received slave address is acknowledged, data should be written to SMB0DAT to be transmitted. The interface enters Slave Transmitter Mode, and transmits one or more bytes of data. After each byte is transmitted, the master sends an acknowledge bit; if the acknowledge bit is an ACK, SMB0DAT should be written with the next data byte. If the acknowledge bit is a NACK, SMB0DAT should not be written to before SI is cleared (Note: an error condition may be generated if SMB0DAT is written following a received NACK while in Slave Transmitter Mode). The interface exits Slave Transmitter Mode after receiving a STOP. Note that the interface will switch to Slave Receiver Mode if SMB0DAT is not written following a Slave Transmitter interrupt. Figure 17.8 shows a typical Slave Transmitter sequence. Two transmitted data bytes are shown, though any number of bytes may be transmitted. Notice that the 'data byte transferred' interrupts occur **after** the ACK cycle in this mode.

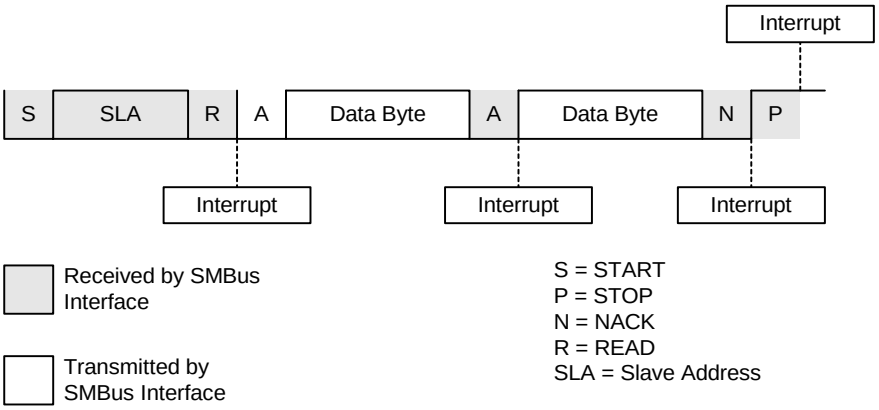

Figure 17.8. Typical Slave Transmitter Sequence

17.6. SMBus Status Decoding

The current SMBus status can be easily decoded using the SMB0CN register. In the table below, STATUS VECTOR refers to the four upper bits of SMB0CN: MASTER, TXMODE, STA, and STO. Note that the shown response options are only the typical responses; application-specific procedures are allowed as long as they conform to the SMBus specification. Highlighted responses are allowed but do not conform to the SMBus specification.

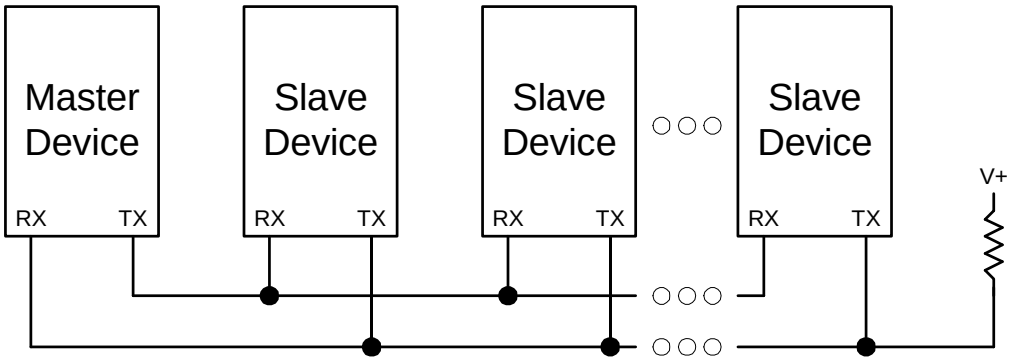

Figure 18.6. UART Multi-Processor Mode Interconnect Diagram

SFR Definition 18.1. SCON0: Serial Port 0 Control

R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
S0MODE	-	MCE0	REN0	TB80	RB80	TI0	RI0	01000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable

SFR Address: 0x98

Bit7: S0MODE: Serial Port 0 Operation Mode.
This bit selects the UART0 Operation Mode.
0: 8-bit UART with Variable Baud Rate.
1: 9-bit UART with Variable Baud Rate.

Bit6: UNUSED. Read = 1b. Write = don't care.

Bit5: MCE0: Multiprocessor Communication Enable.
The function of this bit is dependent on the Serial Port 0 Operation Mode.
S0MODE = 0: Checks for valid stop bit.
0: Logic level of stop bit is ignored.
1: RI0 will only be activated if stop bit is logic level 1.
S0MODE = 1: Multiprocessor Communications Enable.
0: Logic level of ninth bit is ignored.
1: RI0 is set and an interrupt is generated only when the ninth bit is logic 1.

Bit4: REN0: Receive Enable.
This bit enables/disables the UART receiver.
0: UART0 reception disabled.
1: UART0 reception enabled.

Bit3: TB80: Ninth Transmission Bit.
The logic level of this bit will be assigned to the ninth transmission bit in 9-bit UART Mode. It is not used in 8-bit UART Mode. Set or cleared by software as required.

Bit2: RB80: Ninth Receive Bit.
RB80 is assigned the value of the STOP bit in Mode 0; it is assigned the value of the 9th data bit in Mode 1.

Bit1: TI0: Transmit Interrupt Flag.
Set by hardware when a byte of data has been transmitted by UART0 (after the 8th bit in 8-bit UART Mode, or at the beginning of the STOP bit in 9-bit UART Mode). When the UART0 interrupt is enabled, setting this bit causes the CPU to vector to the UART0 interrupt service routine. This bit must be cleared manually by software.

Bit0: RI0: Receive Interrupt Flag.
Set to '1' by hardware when a byte of data has been received by UART0 (set at the STOP bit sampling time). When the UART0 interrupt is enabled, setting this bit to '1' causes the CPU to vector to the UART0 interrupt service routine. This bit must be cleared manually by software.

21.1.3. Mode 2: 8-bit Counter/Timer with Auto-Reload

Mode 2 configures Timer 0 and Timer 1 to operate as 8-bit counter/timers with automatic reload of the start value. TL0 holds the count and TH0 holds the reload value. When the counter in TL0 overflows from all ones to 0x00, the timer overflow flag TF0 (TCON.5) is set and the counter in TL0 is reloaded from TH0. If Timer 0 interrupts are enabled, an interrupt will occur when the TF0 flag is set. The reload value in TH0 is not changed. TL0 must be initialized to the desired value before enabling the timer for the first count to be correct. When in Mode 2, Timer 1 operates identically to Timer 0.

Both counter/timers are enabled and configured in Mode 2 in the same manner as Mode 0. Setting the TR0 bit (TCON.4) enables the timer when either GATE0 (TMOD.3) is logic 0 or when the input signal INT0 is active as defined by bit IN0PL in register INT01CF (see **Section "9.3.2. External Interrupts" on page 88** for details on the external input signals INT0 and INT1).

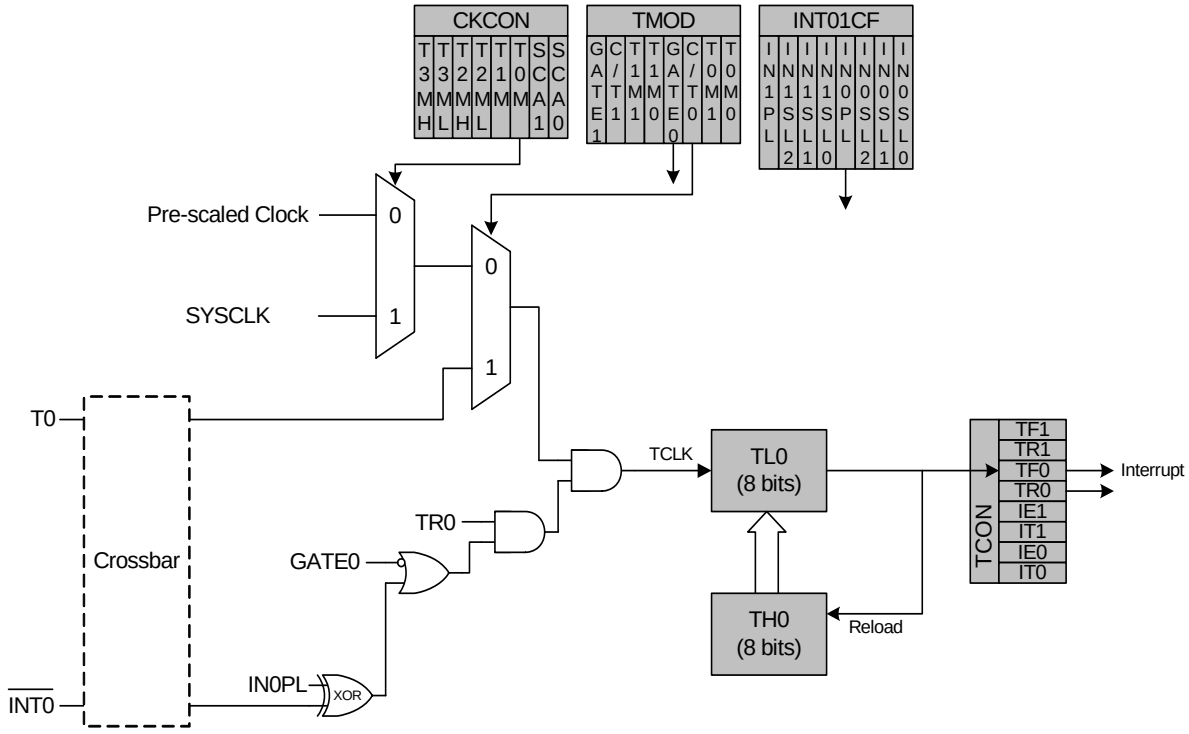

Figure 21.2. T0 Mode 2 Block Diagram

21.2. Timer 2

Timer 2 is a 16-bit timer formed by two 8-bit SFRs: TMR2L (low byte) and TMR2H (high byte). Timer 2 may operate in 16-bit auto-reload mode, (split) 8-bit auto-reload mode, USB Start-of-Frame (SOF) capture mode, or Low-Frequency Oscillator (LFO) Falling Edge capture mode. The Timer 2 operation mode is defined by the T2SPLIT (TMR2CN.3), T2CE (TMR2CN.4) bits, and T2CSS (TMR2CN.1) bits.

Timer 2 may be clocked by the system clock, the system clock divided by 12, or the external oscillator source divided by 8. The external clock mode is ideal for real-time clock (RTC) functionality, where the internal oscillator drives the system clock while Timer 2 (and/or the PCA) is clocked by an external precision oscillator. Note that the external oscillator source divided by 8 is synchronized with the system clock.

21.2.1. 16-bit Timer with Auto-Reload

When T2SPLIT = ‘0’ and T2CE = ‘0’, Timer 2 operates as a 16-bit timer with auto-reload. Timer 2 can be clocked by SYSCLK, SYSCLK divided by 12, or the external oscillator clock source divided by 8. As the 16-bit timer register increments and overflows from 0xFFFF to 0x0000, the 16-bit value in the Timer 2 reload registers (TMR2RLH and TMR2RLL) is loaded into the Timer 2 register as shown in Figure 21.4, and the Timer 2 High Byte Overflow Flag (TMR2CN.7) is set. If Timer 2 interrupts are enabled, an interrupt will be generated on each Timer 2 overflow. Additionally, if Timer 2 interrupts are enabled and the TF2LEN bit is set (TMR2CN.5), an interrupt will be generated each time the lower 8 bits (TMR2L) overflow from 0xFF to 0x00.

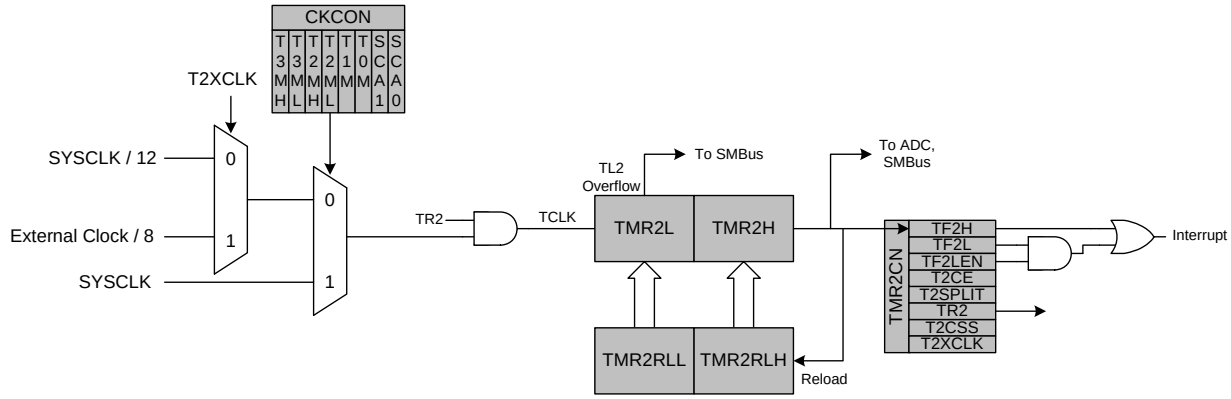

Figure 21.4. Timer 2 16-Bit Mode Block Diagram

22.2.2. Software Timer (Compare) Mode

In Software Timer mode, the PCA counter/timer value is compared to the module's 16-bit capture/compare register (PCA0CPHn and PCA0CPLn). When a match occurs, the Capture/Compare Flag (CCFn) in PCA0CN is set to logic 1 and an interrupt request is generated if CCF interrupts are enabled. The CCFn bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software. Setting the ECOMn and MATn bits in the PCA0CPMn register enables Software Timer mode.

Important Note About Capture/Compare Registers: When writing a 16-bit value to the PCA0 Capture/Compare registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to '0'; writing to PCA0CPHn sets ECOMn to '1'.

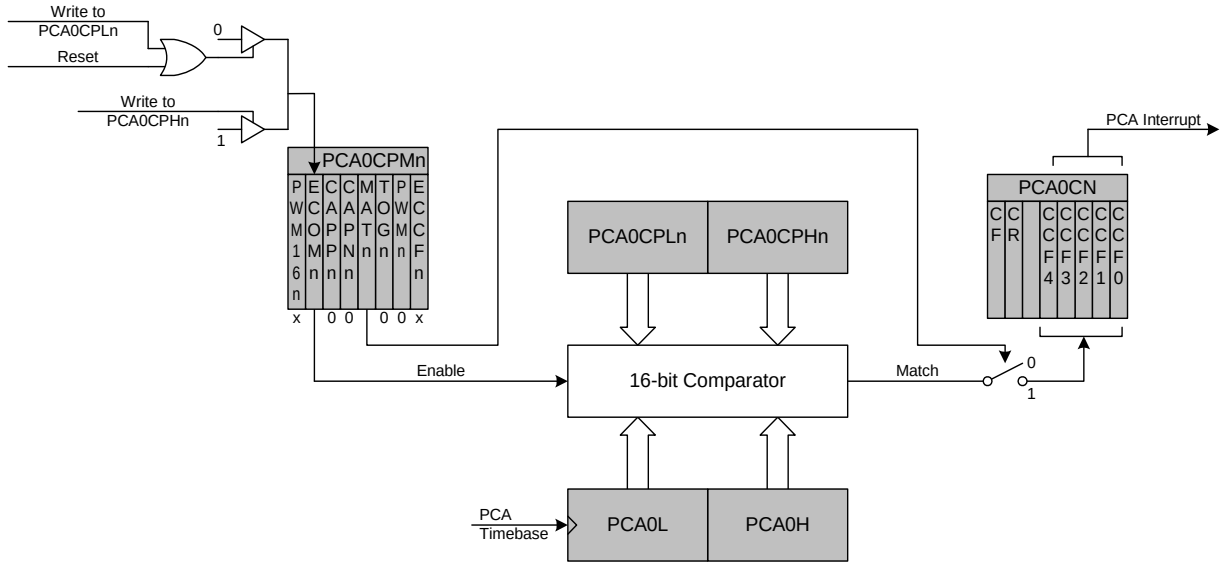

Figure 22.5. PCA Software Timer Mode Diagram

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